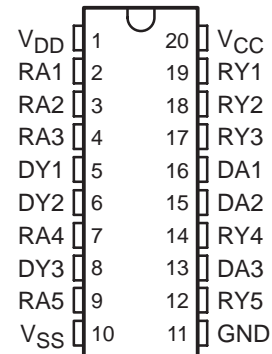


GD65232, GD75232 MULTIPLE RS-232 DRIVERS AND RECEIVERS

SLLS206J – MAY 1995 – REVISED NOVEMBER 2004

- **Single Chip With Easy Interface Between UART and Serial-Port Connector of IBM™ PC/AT and Compatibles**
- **Meet or Exceed the Requirements of TIA/EIA-232-F and ITU v.28 Standards**
- **Designed to Support Data Rates up to 120 kbit/s**
- **Pinout Compatible With SN75C185 and SN75185**

GD65232, GD75232 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



description/ordering information

The GD65232 and GD75232 combine three drivers and five receivers from the Texas Instruments trade-standard SN75188 and SN75189 bipolar quadruple drivers and receivers, respectively. The pinout matches the flow-through design of the SN75C185 to decrease the part count, reduce the board space required, and allow easy interconnection of the UART and serial-port connector of an IBM™ PC/AT and compatibles. The bipolar circuits and processing of the GD65232 and GD75232 provide a rugged, low-cost solution for this function at the expense of quiescent power and external passive components relative to the SN75C185.

The GD65232 and GD75232 comply with the requirements of the TIA/EIA-232-F and ITU (formerly CCITT) V.28 standards. These standards are for data interchange between a host computer and a peripheral at signaling rates up to 20 kbit/s. The switching speeds of these devices are fast enough to support rates up to 120 kbit/s with lower capacitive loads (shorter cables). Interoperability at the higher signaling rates cannot be expected unless the designer has design control of the cable and the interface circuits at both ends. For interoperability at signaling rates up to 120 kbit/s, use of TIA/EIA-423-B (ITU V.10) and TIA/EIA-422-B (ITU V.11) standards is recommended.

ORDERING INFORMATION

| T _A | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|--------------|--------------|-----------------------|------------------|
| –40°C to 85°C | PDIP (N) | Tube of 20 | GD65232N | GD65232N |
| | SOIC (DW) | Tube of 25 | GD65232DW | GD65232 |
| | | Reel of 2000 | GD65232DWR | |
| | SSOP (DB) | Reel of 2000 | GD65232DBR | GD65232 |
| TSSOP (PW) | Tube of 70 | GD65232PW | GD65232 | |
| | Reel of 2000 | GD65232PWR | | |
| 0°C to 70°C | PDIP (N) | Tube of 20 | GD75232N | GD75232N |
| | SOIC (DW) | Tube of 25 | GD75232DW | GD75232 |
| | | Reel of 2000 | GD75232DWR | |
| | SSOP (DB) | Reel of 2000 | GD75232DBR | GD75232 |
| TSSOP (PW) | Tube of 70 | GD75232PW | GD75232 | |
| | Reel of 2000 | GD75232PWR | | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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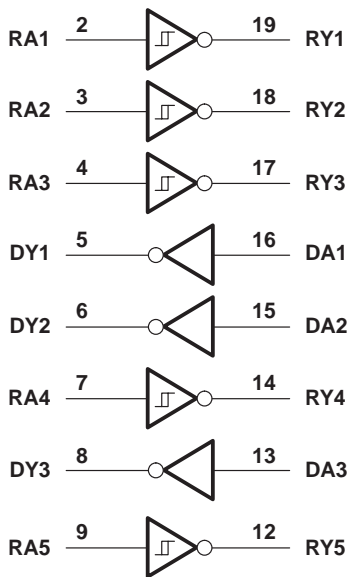


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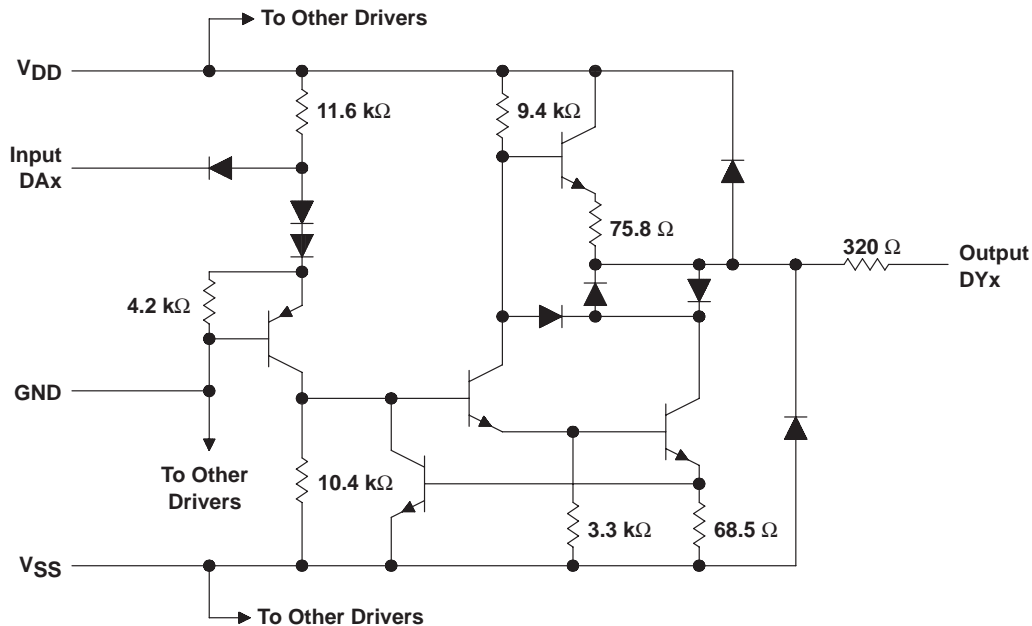
GD65232, GD75232 MULTIPLE RS-232 DRIVERS AND RECEIVERS

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logic diagram (positive logic)

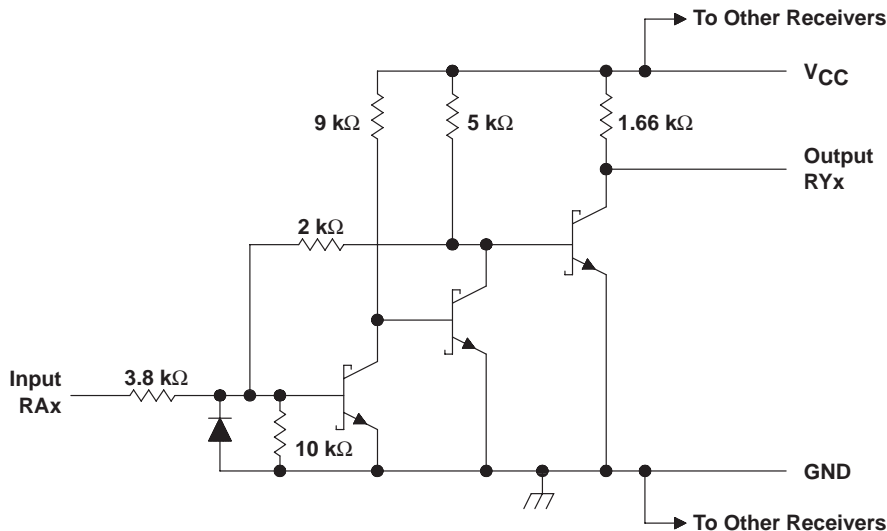


schematic (each driver)



Resistor values shown are nominal.

schematic (each receiver)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|--|----------------|
| Supply voltage (see Note 1): V_{CC} | 10 V |
| V_{DD} | 15 V |
| V_{SS} | -15 V |
| Input voltage range, V_I : Driver | -15 V to 7 V |
| Receiver | -30 V to 30 V |
| Driver output voltage range, V_O | -15 V to 15 V |
| Receiver low-level output current, I_{OL} | 20 mA |
| Package thermal impedance, θ_{JA} (see Notes 2 and 3): DB package | 70°C/W |
| DW package | 58°C/W |
| N package | 69°C/W |
| PW package | 83°C/W |
| Operating virtual junction temperature, T_J | 150°C |
| Storage temperature range, T_{Stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltages are with respect to the network ground terminal.
 2. Maximum power dissipation is a function of $T_J(max)$, θ_{JA} , and T_A . The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
 3. The package thermal impedance is calculated in accordance with JESD 51-7.

GD65232, GD75232 MULTIPLE RS-232 DRIVERS AND RECEIVERS

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recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|-----------------|--|----------|-----|------|------|
| V _{DD} | Supply voltage (see Note 4) | 7.5 | 9 | 15 | V |
| V _{SS} | Supply voltage (see Note 4) | -7.5 | -9 | -15 | V |
| V _{CC} | Supply voltage (see Note 4) | 4.5 | 5 | 5.5 | V |
| V _{IH} | High-level input voltage (driver only) | 1.9 | | | V |
| V _{IL} | Low-level input voltage (driver only) | | | 0.8 | V |
| I _{OH} | High-level output current | Driver | | -6 | mA |
| | | Receiver | | -0.5 | |
| I _{OL} | Low-level output current | Driver | | 6 | mA |
| | | Receiver | | 16 | |
| T _A | Operating free-air temperature | GD65232 | -40 | 85 | °C |
| | | GD75232 | 0 | 70 | |

NOTE 4: When powering up the GD65232 and GD75232, the following sequence should be used:

1. V_{SS}
2. V_{DD}
3. V_{CC}
4. I/Os

Applying V_{CC} before V_{DD} may allow large currents to flow, causing damage to the device. When powering down the GD65232 and GD75232, the reverse sequence should be used.

supply currents over recommended operating free-air temperature range

| PARAMETER | | TEST CONDITIONS | | MIN | MAX | UNIT |
|-----------------|-------------------------------------|---|---|-----|------|------|
| I _{DD} | Supply current from V _{DD} | All inputs at 1.9 V, No load | V _{DD} = 9 V, V _{SS} = -9 V | | 15 | mA |
| | | | V _{DD} = 12 V, V _{SS} = -12 V | | 19 | |
| | | | V _{DD} = 15 V, V _{SS} = -15 V | | 25 | |
| | | All inputs at 0.8 V, No load | V _{DD} = 9 V, V _{SS} = -9 V | | 4.5 | |
| | | | V _{DD} = 12 V, V _{SS} = -12 V | | 5.5 | |
| | | | V _{DD} = 15 V, V _{SS} = -15 V | | 9 | |
| I _{SS} | Supply current from V _{SS} | All inputs at 1.9 V, No load | V _{DD} = 9 V, V _{SS} = -9 V | | -15 | mA |
| | | | V _{DD} = 12 V, V _{SS} = -12 V | | -19 | |
| | | | V _{DD} = 15 V, V _{SS} = -15 V | | -25 | |
| | | All inputs at 0.8 V, No load | V _{DD} = 9 V, V _{SS} = -9 V | | -3.2 | |
| | | | V _{DD} = 12 V, V _{SS} = -12 V | | -3.2 | |
| | | | V _{DD} = 15 V, V _{SS} = -15 V | | -3.2 | |
| I _{CC} | Supply current from V _{CC} | All inputs at 5 V, No load, V _{CC} = 5 V | GD65232 | | 38 | mA |
| | | | GD75232 | | 30 | |



DRIVER SECTION

electrical characteristics over recommended operating free-air temperature range, $V_{DD} = 9\text{ V}$, $V_{SS} = -9\text{ V}$, $V_{CC} = 5\text{ V}$ (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|-------------|--|----------------------------------|----------------------------|------------------------------------|------|------|-------|---------------|
| V_{OH} | High-level output voltage | $V_{IL} = 0.8\text{ V}$, | $R_L = 3\text{ k}\Omega$, | See Figure 1 | 6 | 7.5 | | V |
| V_{OL} | Low-level output voltage (see Note 5) | $V_{IH} = 1.9\text{ V}$, | $R_L = 3\text{ k}\Omega$, | See Figure 1 | | -7.5 | -6 | V |
| I_{IH} | High-level input current | $V_I = 5\text{ V}$, | See Figure 2 | | | | 10 | μA |
| I_{IL} | Low-level input current | $V_I = 0$, | See Figure 2 | | | | -1.6 | mA |
| $I_{OS(H)}$ | High-level short-circuit output current (see Note 6) | $V_{IL} = 0.8\text{ V}$, | $V_O = 0$, | See Figure 1 | -4.5 | -12 | -19.5 | mA |
| $I_{OS(L)}$ | Low-level short-circuit output current | $V_{IH} = 2\text{ V}$, | $V_O = 0$, | See Figure 1 | 4.5 | 12 | 19.5 | mA |
| r_o | Output resistance (see Note 7) | $V_{CC} = V_{DD} = V_{SS} = 0$, | | $V_O = -2\text{ V to } 2\text{ V}$ | 300 | | | Ω |

- NOTES: 5. The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only (e.g., if -10 V is maximum, the typical value is a more negative voltage).
6. Output short-circuit conditions must maintain the total power dissipation below absolute maximum ratings.
7. Test conditions are those specified by TIA/EIA-232-F and as listed above.

switching characteristics, $V_{CC} = 5\text{ V}$, $V_{DD} = 12\text{ V}$, $V_{SS} = -12\text{ V}$, $T_A = 25^\circ\text{C}$

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|-----------|---|--|--------------------------|-------------------------|-----|-----|-----|---------------|
| t_{PLH} | Propagation delay time, low- to high-level output | $R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$, | $C_L = 15\text{ pF}$, | See Figure 3 | | 315 | 500 | ns |
| t_{PHL} | Propagation delay time, high- to low-level output | $R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$, | $C_L = 15\text{ pF}$, | See Figure 3 | | 75 | 175 | ns |
| t_{TLH} | Transition time, low- to high-level output | $R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$ | $C_L = 15\text{ pF}$, | See Figure 3 | | 60 | 100 | ns |
| | | | $C_L = 2500\text{ pF}$, | See Figure 3 and Note 8 | | 1.7 | 2.5 | μs |
| t_{THL} | Transition time, high- to low-level output | $R_L = 3\text{ k}\Omega$ to $7\text{ k}\Omega$ | $C_L = 15\text{ pF}$, | See Figure 3 | | 40 | 75 | ns |
| | | | $C_L = 2500\text{ pF}$, | See Figure 3 and Note 8 | | 1.5 | 2.5 | μs |

NOTE 8: Measured between $\pm 3\text{-V}$ and $\pm 3\text{-V}$ points of the output waveform (TIA/EIA-232-F conditions); all unused inputs are tied either high or low.

GD65232, GD75232

MULTIPLE RS-232 DRIVERS AND RECEIVERS

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RECEIVER SECTION

electrical characteristics over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|------------------|---|-------------------------------|--------------------------|---------|-------|------|------|
| V _{IT+} | Positive-going input threshold voltage | T _A = 25°C, | See Figure 5 | 1.75 | 1.9 | 2.3 | V |
| | | T _A = 0°C to 70°C, | See Figure 5 | 1.55 | | 2.3 | |
| V _{IT-} | Negative-going input threshold voltage | | | 0.75 | 0.97 | 1.25 | V |
| V _{hys} | Input hysteresis voltage (V _{IT+} - V _{IT-}) | | | 0.5 | | | V |
| V _{OH} | High-level output voltage | I _{OH} = -0.5 mA | V _{IH} = 0.75 V | 2.6 | 4 | 5 | V |
| | | | Inputs open | 2.6 | | | |
| V _{OL} | Low-level output voltage | I _{OL} = 10 mA, | V _I = 3 V | | 0.2 | 0.45 | V |
| I _{IH} | High-level input current | V _I = 25 V, | See Figure 5 | GD65232 | 3.6 | 11 | mA |
| | | | | GD75232 | 3.6 | 8.3 | |
| | | V _I = 3 V, | See Figure 5 | | 0.43 | | |
| I _{IL} | Low-level input current | V _I = -25 V, | See Figure 5 | GD65232 | -3.6 | -11 | mA |
| | | | | GD75232 | -3.6 | -8.3 | |
| | | V _I = -3 V, | See Figure 5 | | -0.43 | | |
| I _{OS} | Short-circuit output current | See Figure 4 | | | -3.4 | -12 | mA |

† All typical values are at T_A = 25°C, V_{CC} = 5 V, V_{DD} = 9 V, and V_{SS} = -9 V.

switching characteristics, V_{CC} = 5 V, V_{DD} = 12 V, V_{SS} = -12 V, T_A = 25°C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|------------------|---|---|--|-----|-----|-----|------|
| t _{PLH} | Propagation delay time, low- to high-level output | C _L = 50 pF, R _L = 5 kΩ, See Figure 6 | | | 107 | 250 | ns |
| t _{PHL} | Propagation delay time, high- to low-level output | | | | 42 | 150 | ns |
| t _{TLH} | Transition time, low- to high-level output | | | | 175 | 350 | ns |
| t _{THL} | Transition time, high- to low-level output | | | | 16 | 60 | ns |
| t _{PLH} | Propagation delay time, low- to high-level output | C _L = 15 pF, R _L = 1.5 kΩ, See Figure 6 | | | 100 | 160 | ns |
| t _{PHL} | Propagation delay time, high- to low-level output | | | | 60 | 100 | ns |
| t _{TLH} | Transition time, low- to high-level output | | | | 90 | 175 | ns |
| t _{THL} | Transition time, high- to low-level output | | | | 15 | 50 | ns |



PARAMETER MEASUREMENT INFORMATION

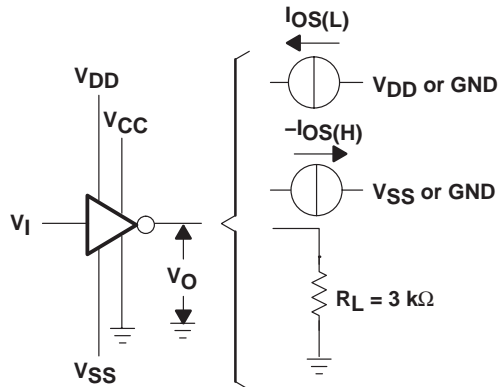


Figure 1. Driver Test Circuit for V_{OH} , V_{OL} , $I_{OS(H)}$, and $I_{OS(L)}$

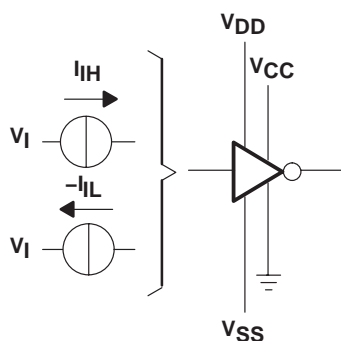
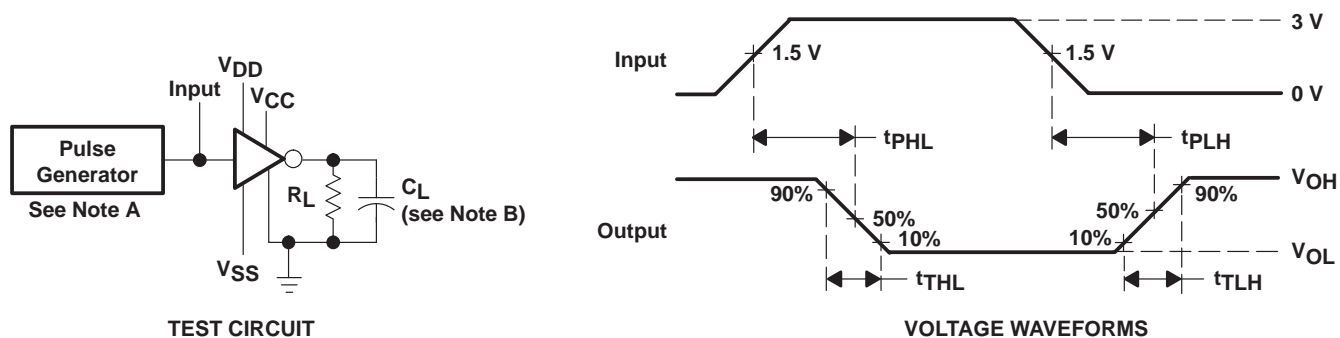


Figure 2. Driver Test Circuit for I_{IH} and I_{IL}



NOTES: A. The pulse generator has the following characteristics: $t_w = 25\ \mu\text{s}$, PRR = 20 kHz, $Z_O = 50\ \Omega$, $t_r = t_f < 50\ \text{ns}$.
 B. C_L includes probe and jig capacitance.

Figure 3. Driver Test Circuit and Voltage Waveforms

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PARAMETER MEASUREMENT INFORMATION

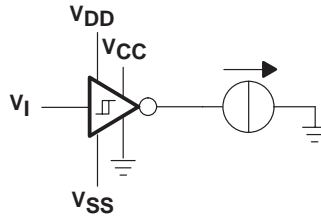


Figure 4. Receiver Test Circuit for I_{0S}

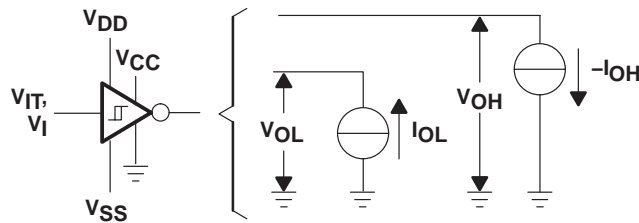
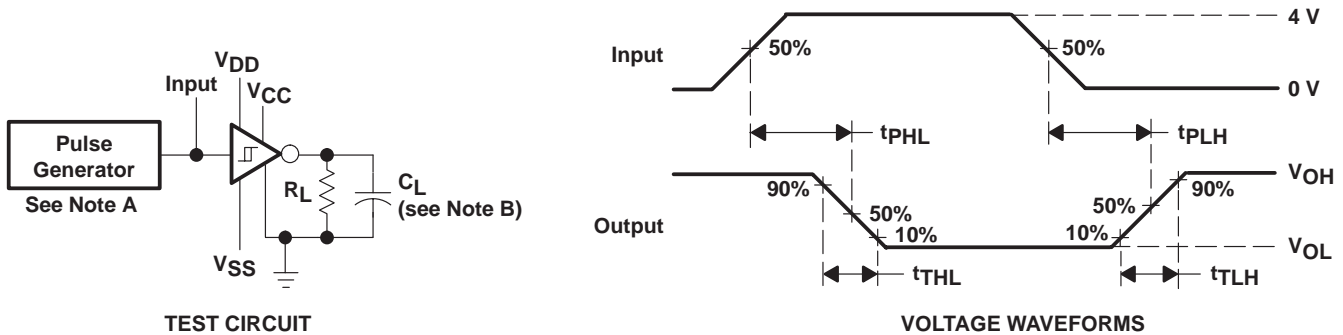


Figure 5. Receiver Test Circuit for V_{IT} , V_{OH} , and V_{OL}



NOTES: A. The pulse generator has the following characteristics: $t_w = 25 \mu s$, $PRR = 20 \text{ kHz}$, $Z_O = 50 \Omega$, $t_r = t_f < 50 \text{ ns}$.
B. C_L includes probe and jig capacitance.

Figure 6. Receiver Propagation and Transition Times

TYPICAL CHARACTERISTICS

DRIVER SECTION

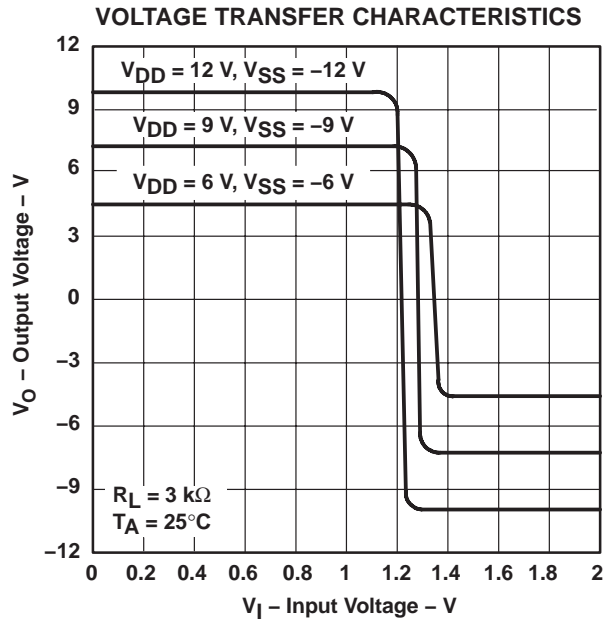


Figure 7

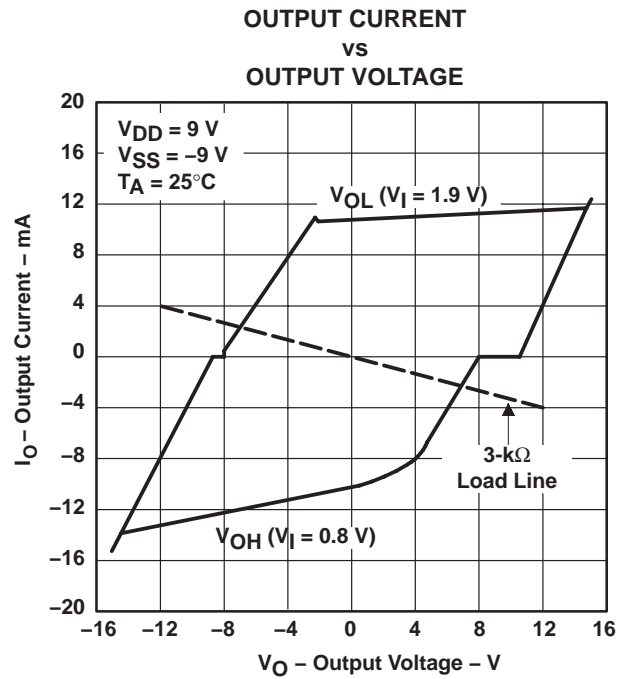


Figure 8

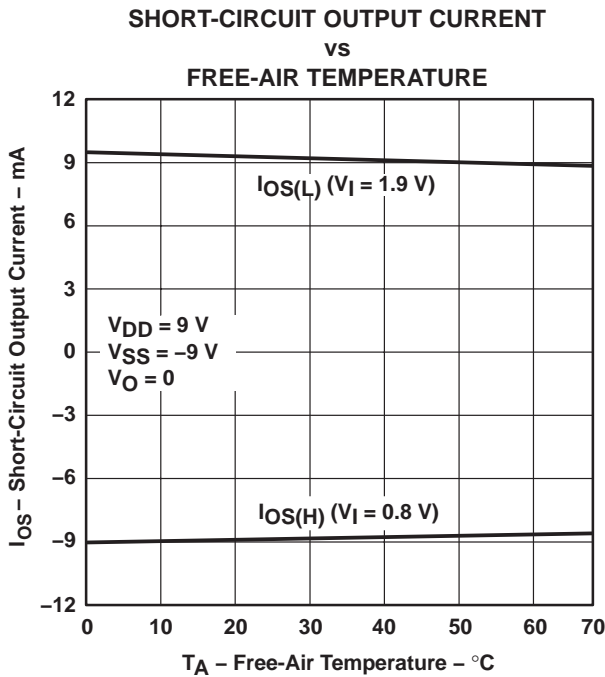


Figure 9

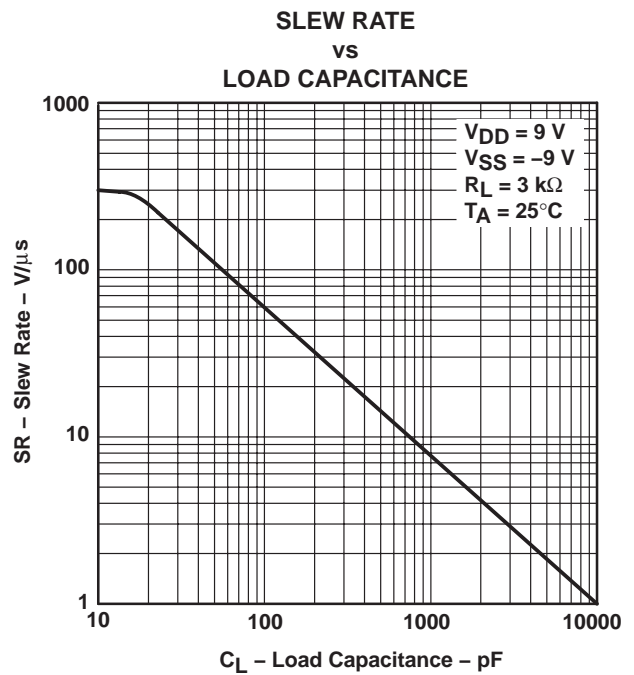


Figure 10

TYPICAL CHARACTERISTICS

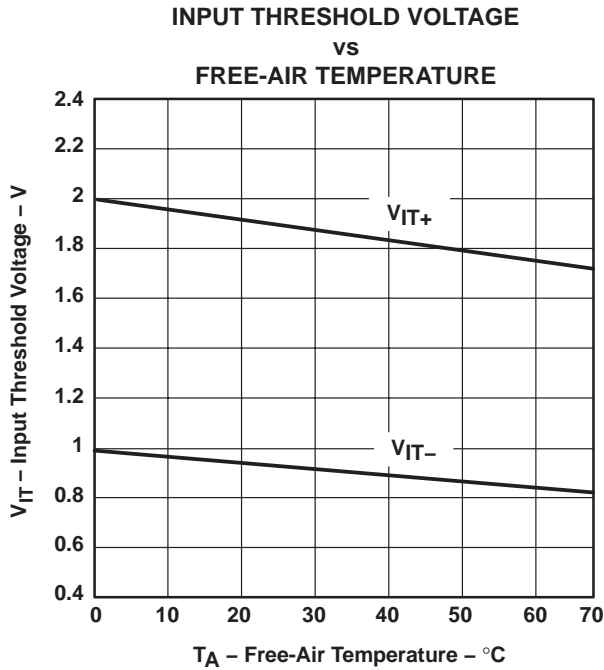


Figure 11

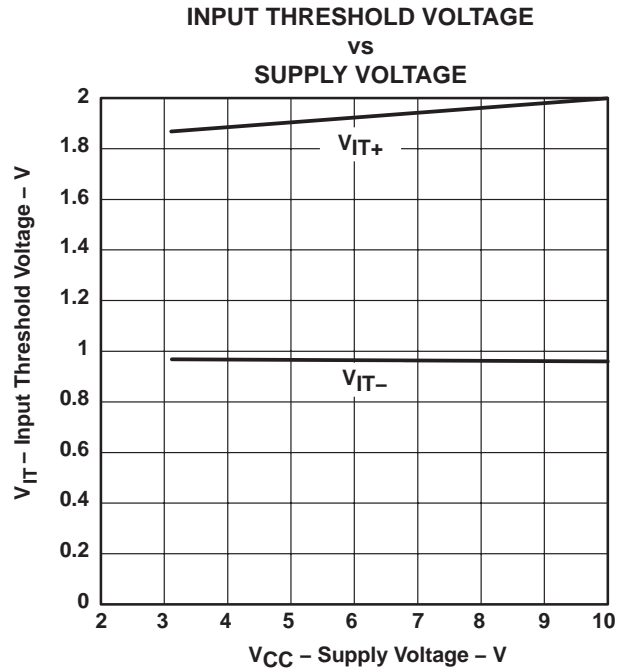
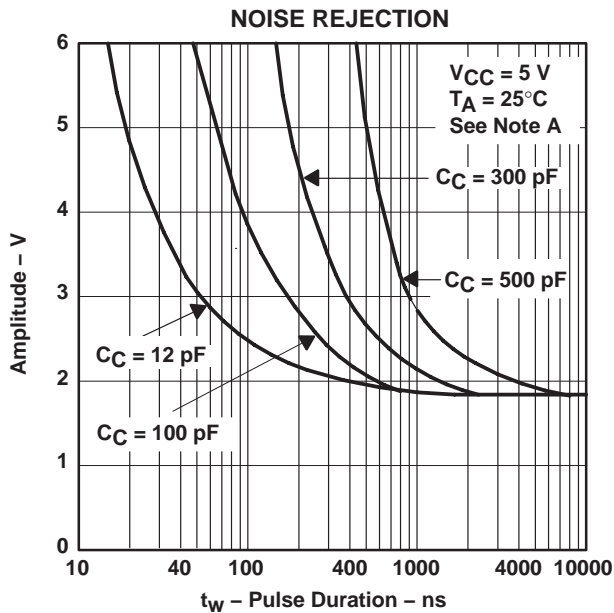


Figure 12



NOTE A: This figure shows the maximum amplitude of a positive-going pulse that, starting from 0 V, does not cause a change of the output level.

Figure 13

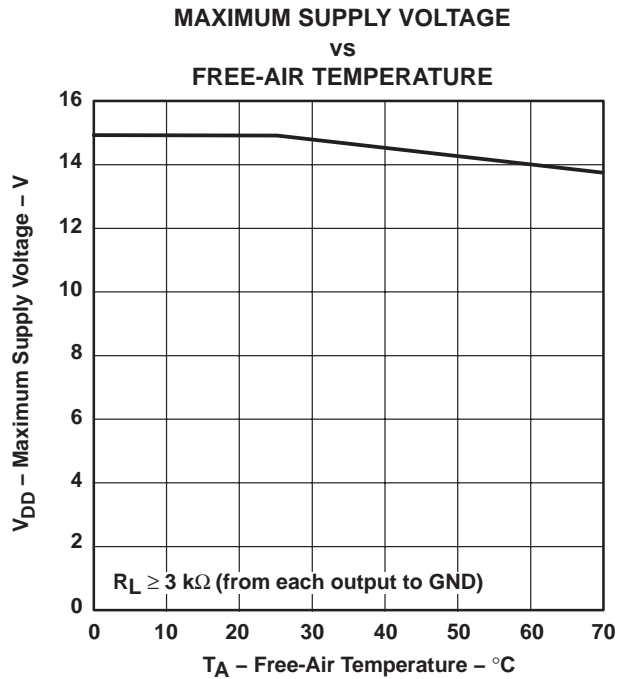


Figure 14

APPLICATION INFORMATION

Diodes placed in series with the V_{DD} and V_{SS} leads protect the GD65232 and GD75232 in the fault condition in which the device outputs are shorted to ± 15 V and the power supplies are at low and provide low-impedance paths to ground (see Figure 15).

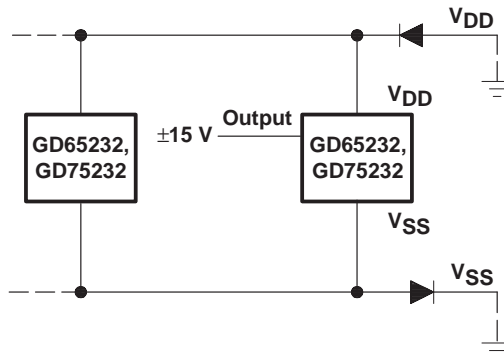


Figure 15. Power-Supply Protection to Meet Power-Off Fault Conditions of TIA/EIA-232-F

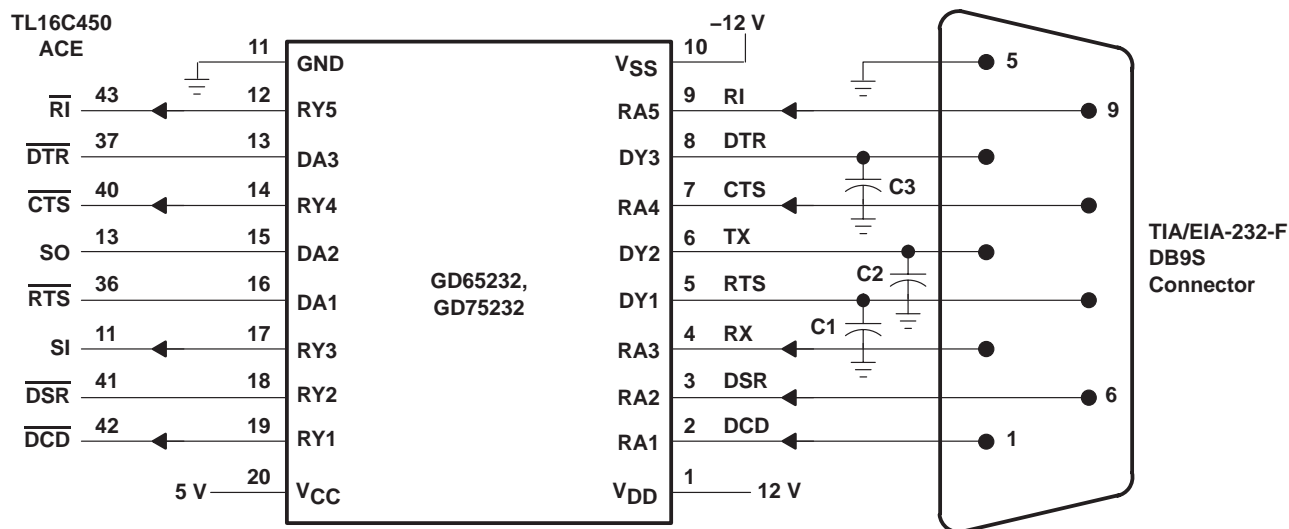


Figure 16. Typical Connection

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|---------------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| GD65232DW | LIFEBUY | SOIC | DW | 20 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | GD65232 | |
| GD65232DWR | LIFEBUY | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | GD65232 | |
| GD65232PWR | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | GD65232 | Samples |
| GD75232DBR | ACTIVE | SSOP | DB | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | GD75232 | Samples |
| GD75232DW | LIFEBUY | SOIC | DW | 20 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | GD75232 | |
| GD75232DWR | LIFEBUY | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | GD75232 | |
| GD75232DWRG4 | LIFEBUY | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | GD75232 | |
| GD75232N | LIFEBUY | PDIP | N | 20 | 20 | RoHS & Non-Green | NIPDAU | N / A for Pkg Type | 0 to 70 | GD75232N | |
| GD75232PW | LIFEBUY | TSSOP | PW | 20 | 70 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | GD75232 | |
| GD75232PWR | ACTIVE | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU SN | Level-1-260C-UNLIM | 0 to 70 | GD75232 | Samples |
| GD75232PWRG4 | LIFEBUY | TSSOP | PW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | GD75232 | |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| GD65232DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| GD65232PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| GD75232DBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| GD75232DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| GD75232PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |
| GD75232PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |
| GD75232PWGR4 | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.0 | 1.4 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| GD65232DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| GD65232PWR | TSSOP | PW | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| GD75232DBR | SSOP | DB | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| GD75232DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| GD75232PWR | TSSOP | PW | 20 | 2000 | 364.0 | 364.0 | 27.0 |
| GD75232PWR | TSSOP | PW | 20 | 2000 | 356.0 | 356.0 | 35.0 |
| GD75232PWRG4 | TSSOP | PW | 20 | 2000 | 356.0 | 356.0 | 35.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-----------|--------------|--------------|------|-----|--------|--------|--------|--------|
| GD65232DW | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| GD75232DW | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| GD75232DW | DW | SOIC | 20 | 25 | 506.98 | 12.7 | 4826 | 6.6 |
| GD75232N | N | PDIP | 20 | 20 | 506 | 13.97 | 11230 | 4.32 |
| GD75232PW | PW | TSSOP | 20 | 70 | 530 | 10.2 | 3600 | 3.5 |

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

- 8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 9. Board assembly site may have different recommendations for stencil design.

DB0020A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW0020A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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