LM3630A 高效双灯串白光发光二级管 (LED) 驱动器

查询样品: LM3630A

特性

- 驱动多达 **2** 灯串 **LED**（每个灯串有 **10** 个串联的 **LED**）
- 效率高达 **87%**
- **8** 位 **I²C** 兼容可编程指数或线性亮度控制
- 针对内容自适应亮度控制 **(CABC)** 操作的脉宽调制 **(PWM)** 亮度控制
- 每个灯串的单独电流控制
- 针对 **LED** 的真正关断隔离
- 内部软启动限制了浪涌电流
- **2.3V** 至 **5.5V** 的宽输入电压范围
- 自适应净空
- 可编程 **16V/24V/32V/40V** 过压保护
- 具有可选额外偏移的 **500kHz** 或 **1MHz** 的可选升压频率
- 半高 **12** 焊锡凸点芯片级球栅阵列 **(DSBGA)** 封装
- 解决方案尺寸 **32mm²**

应用范围

- 智能手机 **LCD** 背光
- **LCD +** 键盘照明

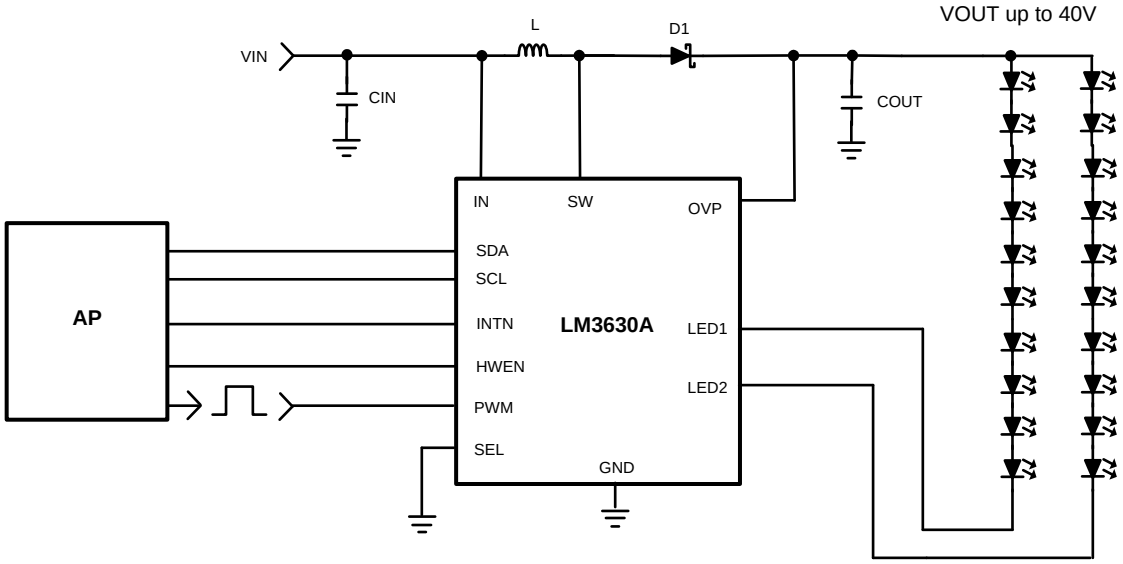
说明

LM3630A 是一款电流模式升压转换器，此转换器为每串具有 10 个 LED 的两个灯串供电并控制其中的电流。 可通过一个 I²C 兼容接口完成设定。 最大 LED 电流可在 5mA 至 28.5mA 的范围内调节。 在任一指定的最大 LED 电流情况下，可使用 256 个指数或线性调光步长来进一步调节 LED 亮度。 此外，可启用脉宽调制 ("PWM") 亮度控制，以实现通过一个逻辑电平 PWM 信号来调整 LED 电流。

可在 500kHz 时设定升压开关频率以实现低开关损耗性能，或者在 1MHz 时使用微型半高电感器。 可将这些频率的偏移设定为 10%。 在 16V，24V，32V 或 40V 时可设定过压保护以适应多种 LED 配置以及肖特基二极管/输出电容器组合的需要。

此器件在 2.3V 至 5.5V 的运行电压范围和 -40°C 至 +85°C 的温度范围内运转。 LM3630A 采用超小型 12 焊锡凸点 DSBGA 封装。

TYPICAL APPLICATION CIRCUIT



TYPICAL PCB LAYOUT

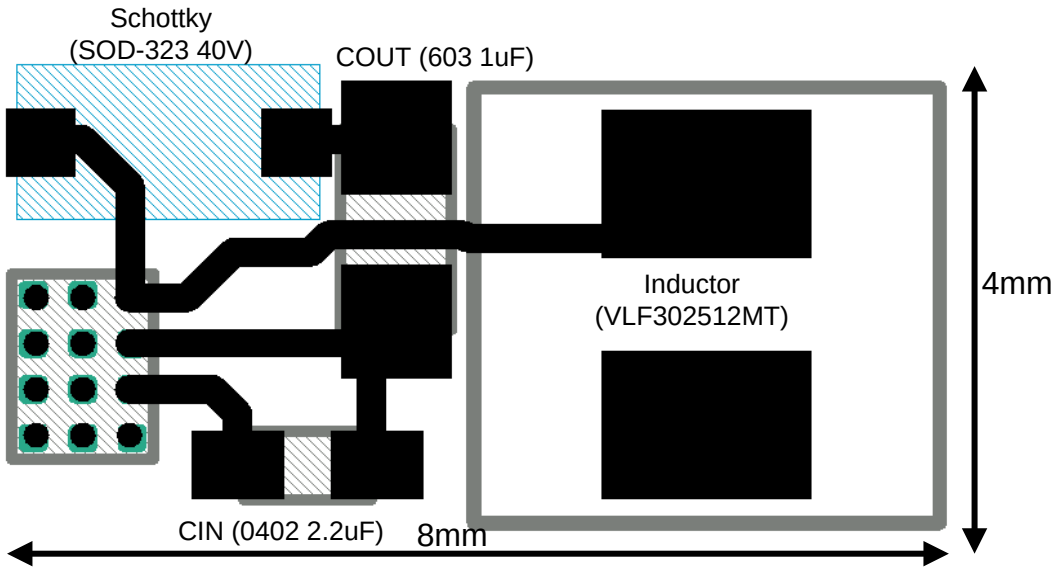


Figure 1. Typical PCB Layout (2 x 10 LED Application)

CONNECTION DIAGRAM

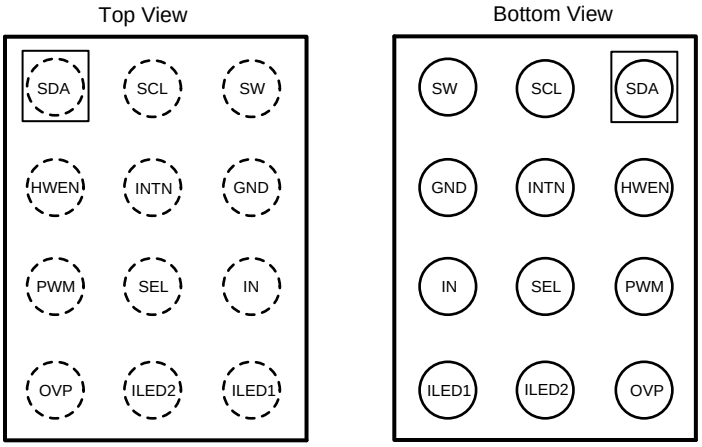


Figure 2. Package Number YFQ12HNA

AVAILABLE OPTIONS

PART NUMBER	PACKAGE MARKING (1)	PACKAGE	SUPPLIED AS
LM3630ATME	YM	YFQ12HNA	250 Units, Tape & Reel
LM3630ATMX	D6		3000 Units, Tape & Reel

(1) YM = Date Code.

PIN DESCRIPTIONS

Ball	Name	Description
A1	SDA	Serial Data Connection for I^2C-Compatible Interface
A2	SCL	Serial Clock Connection for I^2C-Compatible Interface
A3	SW	Inductor Connection, Diode Anode Connection, and Drain Connection for Internal NFET. Connect the inductor and diode as close as possible to SW to reduce inductance and capacitive coupling to nearby traces.
B1	HWEN	Logic High Hardware Enable
B2	INTN	Interrupt output for fault status change. Open drain active low signal.
B3	GND	Ground
C1	PWM	External PWM Brightness Control Input
C2	SEL	Selects I^2C-compatible address. Ground selects 7-bit address 36h. VIN selects address 38h.
C3	IN	Input Voltage Connection. Connect a 2.3V to 5.5V supply to IN and bypass to GND with a 2.2 µF or greater ceramic capacitor.
D1	OVP	Output Voltage Sense Connection for Over Voltage Sensing. Connect OVP to the positive terminal of the output capacitor.
D2	ILED2	Input Terminal to Internal Current Sink #2.
D3	ILED1	Input Terminal to Internal Current Sink #1.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS (1) (2)

		VALUE	UNIT
IN, HWEN, PWM, SCL, SDA, INTN, SEL to GND		−0.3 to 6.0	V
SW, OVP, ILED1, ILED2 to GND		−0.3 to 45	
$T_{(J\text{-}MAX)}$	Continuous Power Dissipation (3)	Internally Limited	
	Maximum Junction Temperature	150	°C
	Storage Temperature Range	−45 to +150	
	Maximum Lead Temperature (Soldering) (4) Vapor Phase (60 sec.)	215	
	Maximum Lead Temperature (Soldering) (4) Infrared (15 sec.)	220	
ESD Rating (5)	Human Body Model	2	kV
	Charged Device Mod	500	V
Operating Ratings (1) (2)			
V_{IN}	Input Voltage Range	2.3 to 5.5	V
T_A	Operating Ambient Temperature Range (6)	−40 to +85	°C
Thermal Properties			
θ_{JA}	Junction-to-Ambient Thermal Resistance, YFQ12 package (7)	78.1	°C/W

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pin.
(3) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 140°C (typ.) and disengages at T_J = 125°C (typ.).
(4) For detailed soldering specifications and information, please refer to Texas Instruments Application Note 1112: DSBGA Wafer Level Chip Scale Package (AN-1112)
(5) The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. (MIL-STD-883 3015.7) .
(6) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature ($T_{A\text{-}MAX}$) is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125ºC), the maximum power dissipation of the device in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A\text{-}MAX} = T_{J\text{-}MAX\text{-}OP} – (\theta_{JA} \times P_{D\text{-}MAX})$.
(7) Junction-to-ambient thermal resistance is highly dependent on application and board layout. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design. For more information, please refer to Texas Instruments Application Note 1112: DSBGA Wafer Level Chip Scale Package.

ELECTRICAL CHARACTERISTICS (1)

Limits in standard typeface are for T_A = 25°C, and limits **in boldface** type apply over the full operating ambient temperature range (−40°C ≤ T_A ≤ +85°C). Unless otherwise specified, V_{IN} = 3.6V.

Symbol	Parameter	Condition		Min	Typ	Max	Units
ILED1, ILED2	Output Current Regulation	2.5V ≤ V_{IN} ≤ 5.5V, Full Scale Current = 20 mA		**19**	20	**21**	mA
I_{MATCH}	ILED1 to ILED2 Current Matching (2)	2.5V ≤ V_{IN} ≤ 5.5V, ILED = 10 mA, TA = +25°C	ILED1 on A ILED2 on B	-1	0.5	1	%
		2.5V ≤ V_{IN} ≤ 5.5V, ILED = 10 mA, 0°C ≤ T_A ≤ +70°C		**-2.5**	0.5	**2.5**	
V_{REG_CS}	Regulated Current Sink Headroom Voltage	ILED = 5 mA			250		mV
V_{HR}	Current Sink Minimum Headroom Voltage	ILED = 95% of nominal, ILED = 20 mA			160	**240**	
R_{DSON}	NMOS Switch On Resistance	I_{SW} = 100 mA			0.25		Ω
I_{CL}	NMOS Switch Current Limit	2.5V ≤ V_{IN} ≤ 5.5V		**480**	600	**720**	mA
				640	800	**960**	
				800	1000	**1200**	
				960	1200	**1440**	
V_{OVP}	Output Over-Voltage Protection	ON Threshold, 2.3V ≤ V_{IN} ≤ 5.5V, 24V option		**23**	24	**25**	V
		ON Threshold, 2.3V ≤ V_{IN} ≤ 5.5V, 40V option		**39**	41	**44**	
		Hysteresis			1		
f_{SW}	Switching Frequency	2.5V ≤ V_{IN} ≤ 5.5V	560 kHz shift = 1	**538**	560	**582**	kHz
			500 kHz shift = 0	**481**	500	**518**	
			1.12 MHz shift = 1	**1077**	1120	**1163**	
			1MHz shift = 0	**962**	1000	**1038**	
D_{MAX}	Maximum Duty Cycle				94		%
I_Q	Quiescent Current into Device, Not Switching.	V_{IN} = 3.6V	ILED1 = ILED2 = 20mA, Feedback disabled.		350		µA
I_{SHDN}	Shutdown Current	2.3V ≤ V_{IN} ≤ 5.5V	HWEN = VIN, I^2C Shutdown		1	**4**	µA
			HWEN = GND		1	**4**	
I_{LED_MIN}	Minimum LED Current in ILED1 or ILED2	Full Scale Current = 20 mA, BRT = 0x01, Exponential Mapping Mode			13		
T_{SD}	Thermal Shutdown				+140		°C
	Hysteresis				15		
t_{WAIT}	Initialization Timing	Time period to wait from the assertion of HWEN or after Software Reset, before an I^2C transaction will be ACK'ed. During this time period an I^2C transaction will be NAK'ed		1			ms
Logic Inputs (PWM, HWEN, SEL, SCL, SDA)							
V_{IL}	Input Logic Low	2.3V ≤ V_{IN} ≤ 5.5V		**0**		**0.4**	V
V_{IH}	Input Logic High			**1.2**		**V_{IN}**	
V_{OL}	Output Logic Low (SDA, INTN)					**400**	mV
f_{PWM}	PWM Input Frequency			**10**		**80**	kHz
C_{IN}	Input Capacitance	SDA			4.5		pF
		SCL			5.0		

(1) Min and Max limits are specified by design, test, or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm. Unless otherwise specified, conditions for typical specifications are: V_{IN} = 3.6V and T_A = +25ºC.

(2) LED current sink matching between LED1 and LED2 is given by taking the difference between I_{LED1} and I_{LED2} and dividing by the average. This simplifies to $(I_{LED1} - I_{LED2})/(I_{LED1} + I_{LED2})$ x 2 at I_{LED} = 10 mA. I_{LED1} is driven by Bank A and I_{LED2} is driven by Bank B.

ELECTRICAL CHARACTERISTICS (1) (continued)

Limits in standard typeface are for T_A = 25°C, and limits **in boldface** type apply over the full operating ambient temperature range (−40°C ≤ T_A ≤ +85°C). Unless otherwise specified, V_{IN} = 3.6V.

Symbol	Parameter	Condition		Min	Typ	Max	Units
I^2C-Compatible Timing Specifications (SCL, SDA) (3)							
t_1	SCL (Clock Period)			**2.5**			µs
t_2	Data in Setup Time to SCL High			**100**			ns
t_3	Data in Setup Time to SCL Low			**0**			
t_4	SDA Low Setup Time to SCL Low (Start)			**100**			
t_5	SDA High Hold Time to SCL High (Stop)			**100**			

(3) SCL and SDA must be glitch-free in order for proper brightness to be realized.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25°C, ILED Full Scale = 20.0mA unless specified otherwise.

Boost and LED Efficiency at VIN = 2.5V, 2p6s, Freq=500kHz, L=22uH

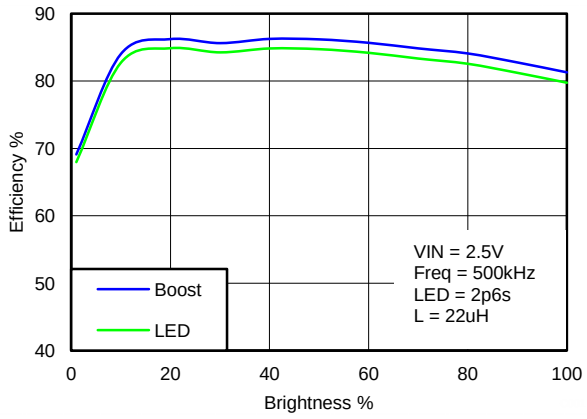


Figure 3.

Boost and LED Efficiency at VIN = 2.7V, 2p6s, Freq=500kHz, L=22uH

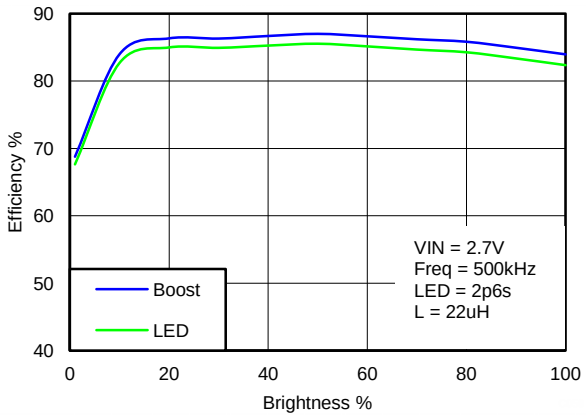


Figure 4.

Boost and LED Efficiency at VIN = 3.6V, 2p6s, Freq=500kHz, L=22µH

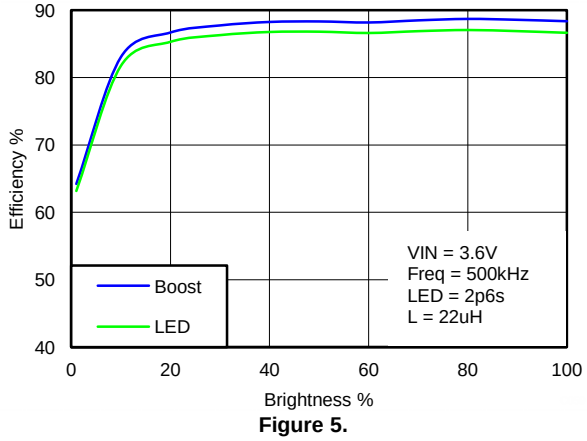


Figure 5.

Boost and LED Efficiency at VIN = 4.2V, 2p6s, Freq=500kHz, L=22uH

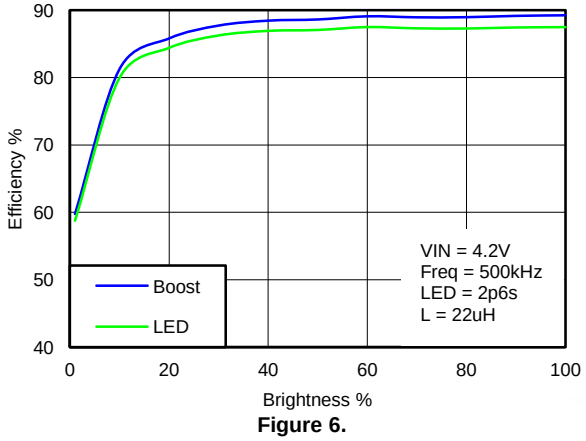


Figure 6.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25°C, ILED Full Scale = 20.0mA unless specified otherwise.

Boost and LED Efficiency at VIN = 5.5V, 2p6s, Freq=500kHz, L=22uH

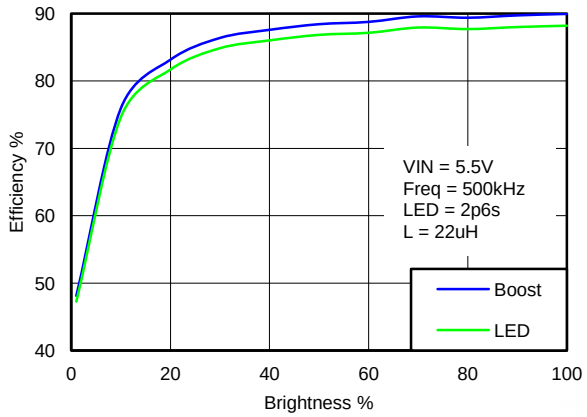


Figure 7.

Boost and LED Efficiency at VIN = 2.5V, 2p6s, Freq=500kHz, L=10uH

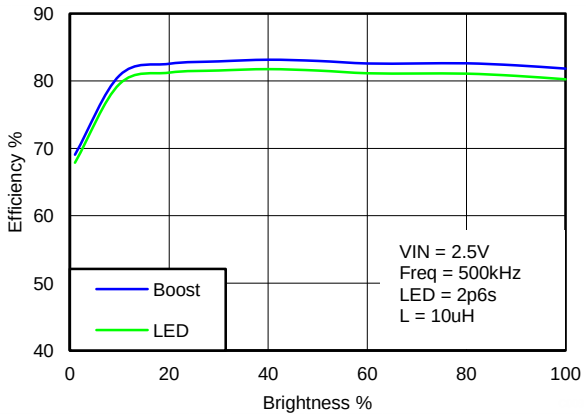


Figure 8.

Boost and LED Efficiency at VIN = 2.7V, 2p6s, Freq=500kHz, L=10uH

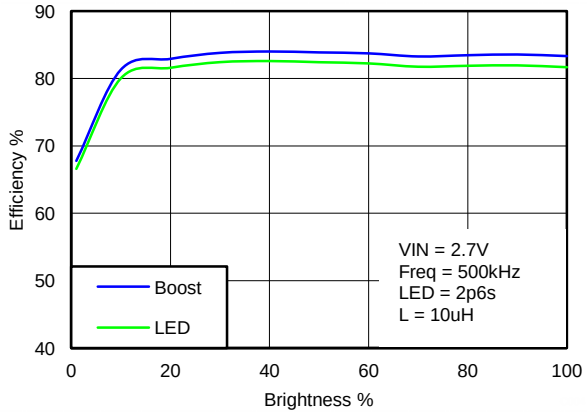


Figure 9.

Boost and LED Efficiency at VIN = 3.6V, 2p6s, Freq=500kHz, L=10uH

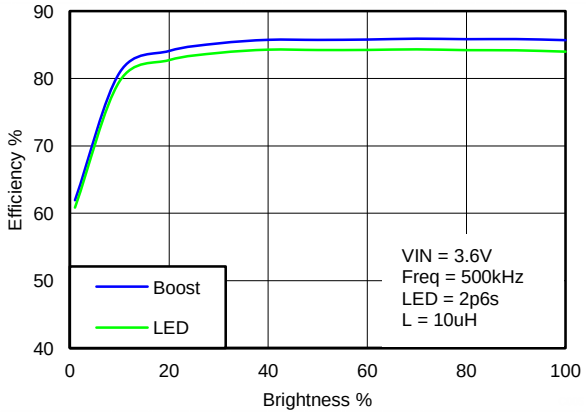


Figure 10.

Boost and LED Efficiency at VIN = 4.2V, 2p6s, Freq=500kHz, L=10uH

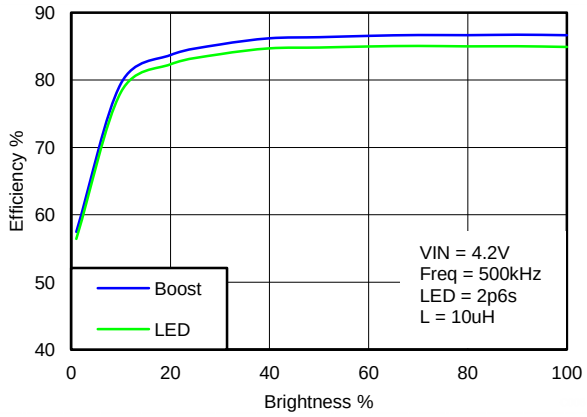


Figure 11.

Boost and LED Efficiency at VIN = 5.5V, 2p6s, Freq=500kHz, L=10uH

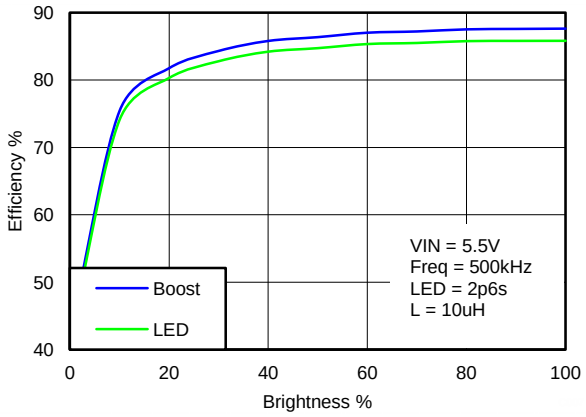


Figure 12.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25°C, ILED Full Scale = 20.0mA unless specified otherwise.

Boost and LED Efficiency at VIN = 2.5V, 1p10s, Freq=500kHz, L=22uH

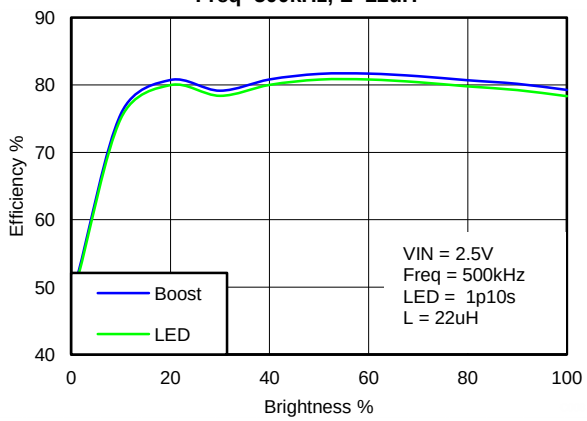


Figure 13.

Boost and LED Efficiency at VIN = 2.7V, 1p10s, Freq=500kHz, L=22uH

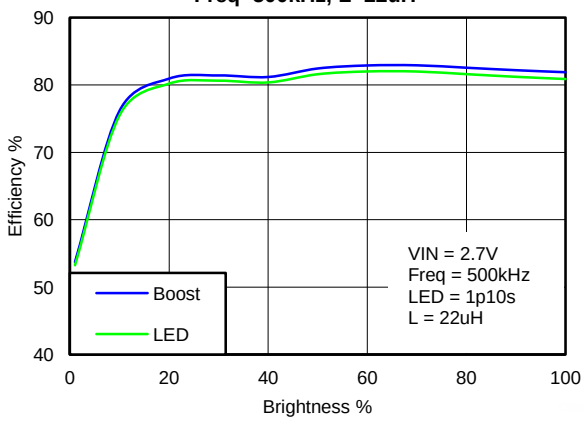


Figure 14.

Boost and LED Efficiency at VIN = 3.6V, 1p10s, Freq=500kHz, L=22uH

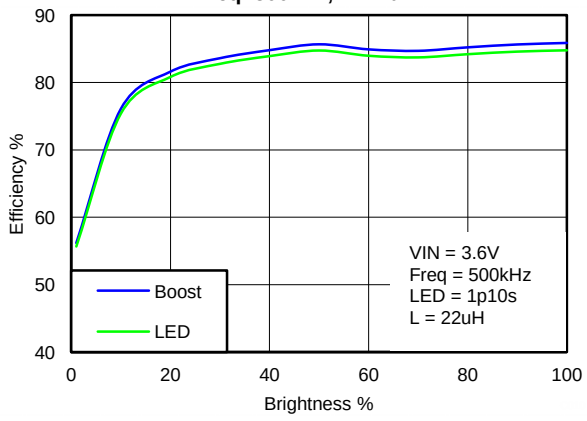


Figure 15.

Boost and LED Efficiency at VIN = 4.2V, 1p10s, Freq=500kHz, L=22uH

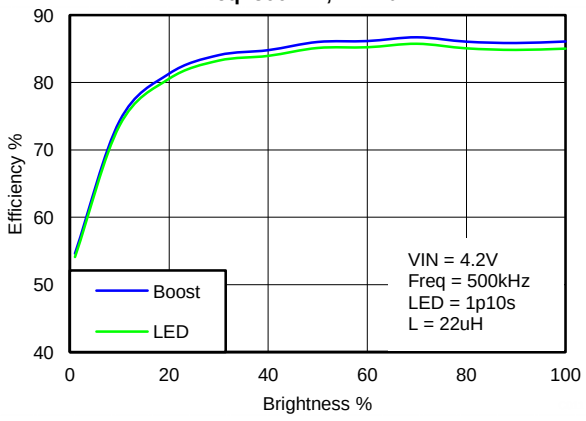


Figure 16.

Boost and LED Efficiency at VIN = 5.5V, 1p10s, Freq=500kHz, L=22uH

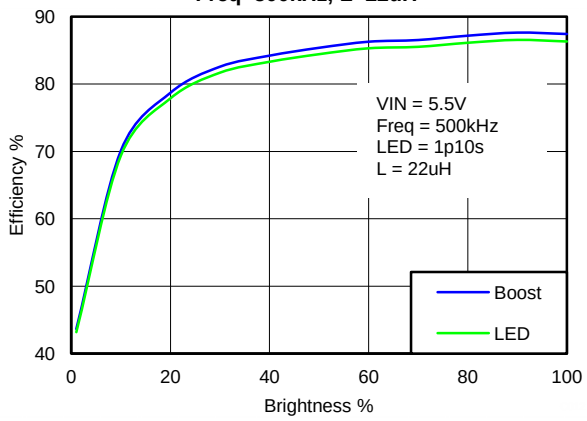


Figure 17.

Boost and LED Efficiency at VIN = 2.5V, 1p10s, Freq=500kHz, L=10uH

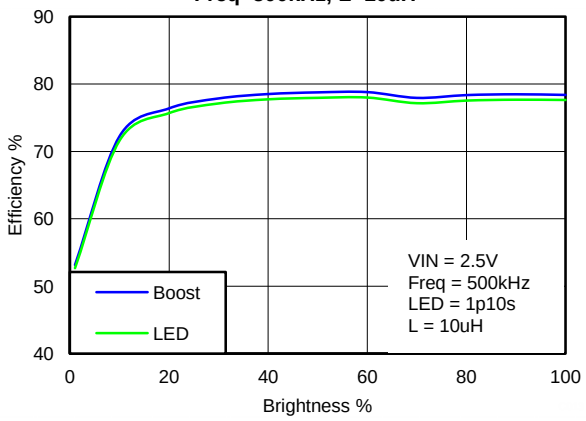


Figure 18.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25°C, ILED Full Scale = 20.0mA unless specified otherwise.

Boost and LED Efficiency at VIN = 2.7V, 1p10s, Freq=500kHz, L=10uH

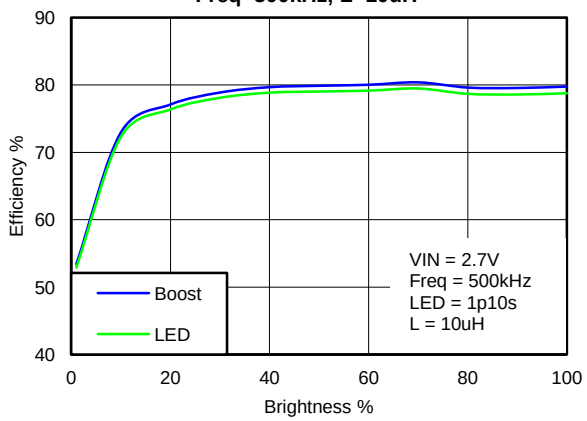


Figure 19.

Boost and LED Efficiency at VIN = 3.6V, 1p10s, Freq=500kHz, L=10uH

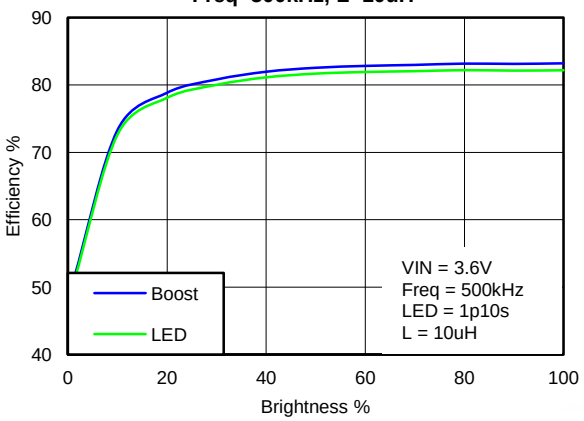


Figure 20.

Boost and LED Efficiency at VIN = 4.2V, 1p10s, Freq=500kHz, L=10uH

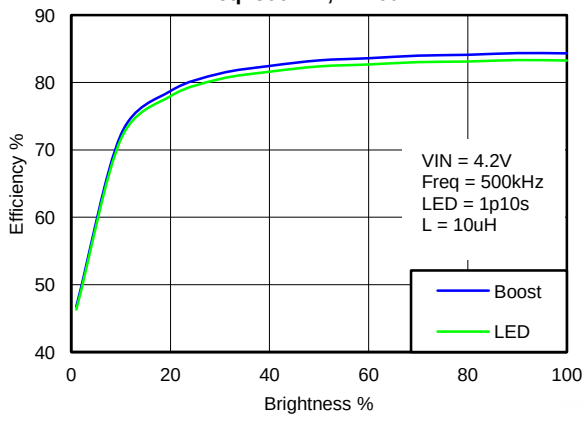


Figure 21.

Boost and LED Efficiency at VIN = 5.5V, 1p10s, Freq=500kHz, L=10uH

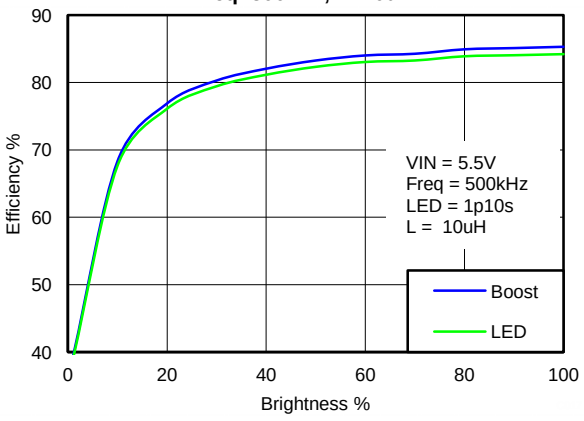


Figure 22.

Boost and LED Efficiency at VIN = 2.5V, 2p10s, Freq=1MHz, L=10uH

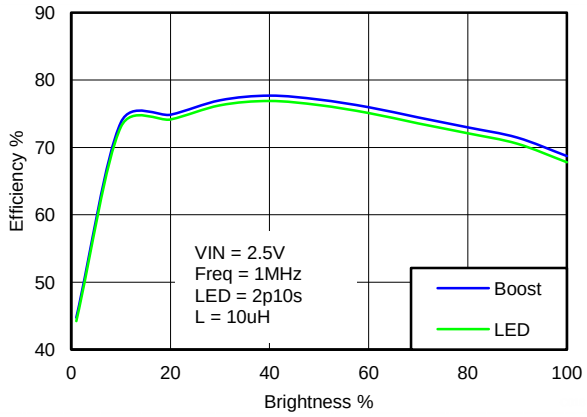


Figure 23.

Boost and LED Efficiency at VIN = 2.7V, 2p10s, Freq=1MHz, L=10uH

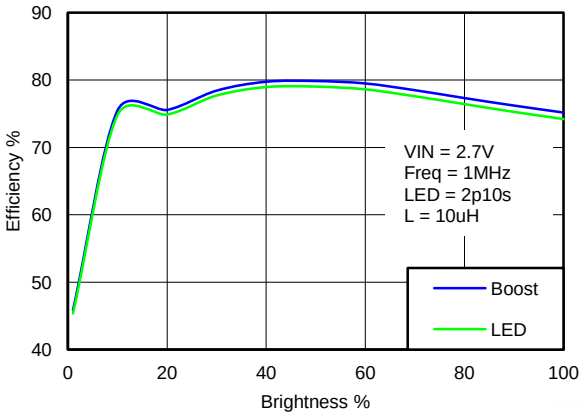


Figure 24.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25°C, ILED Full Scale = 20.0mA unless specified otherwise.

Boost and LED Efficiency at VIN = 3.6V, 2p10s, Freq=1MHz, L=10uH

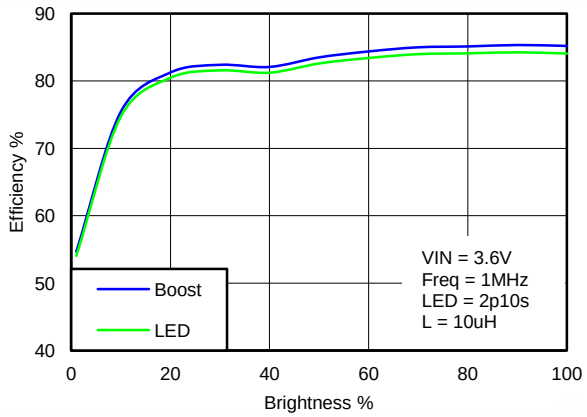


Figure 25.

Boost and LED Efficiency at VIN = 4.2V, 2p10s, Freq=1MHz, L=10uH

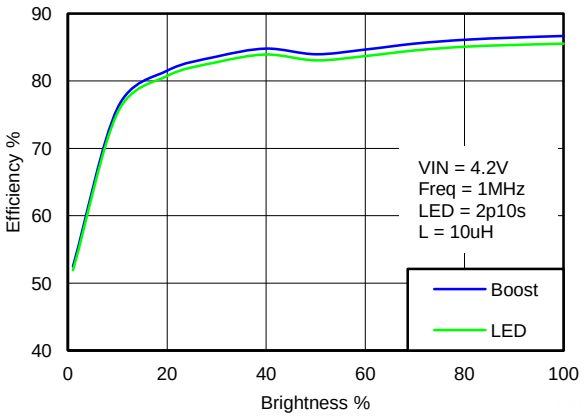


Figure 26.

Boost and LED Efficiency at VIN = 5.5V, 2p10s, Freq=1MHz, L=10uH

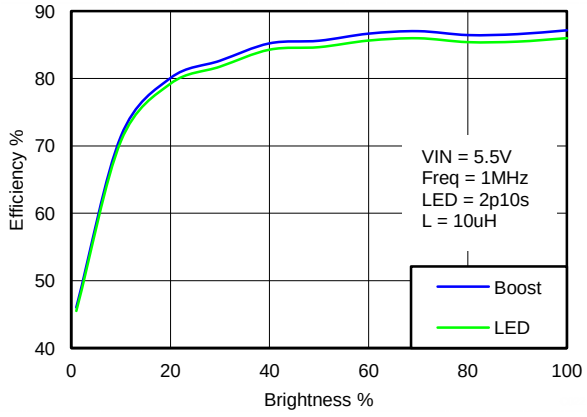


Figure 27.

Boost and LED Efficiency at VIN = 2.7V, 2p10s, Freq=500kHz, L=10uH

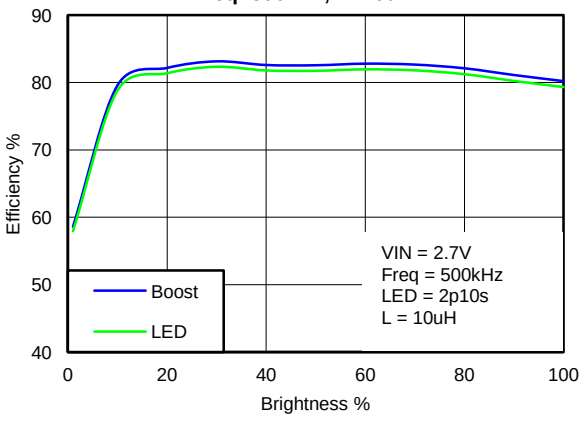


Figure 28.

Boost and LED Efficiency at VIN = 3.6V, 2p10s, Freq=500kHz, L=10uH

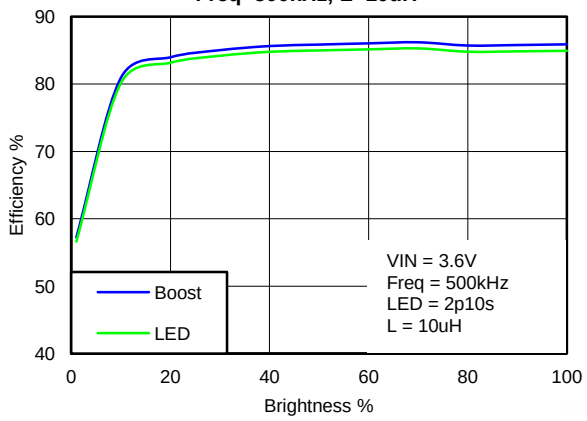


Figure 29.

Boost and LED Efficiency at VIN = 4.2V, 2p10s, Freq=500kHz, L=10uH

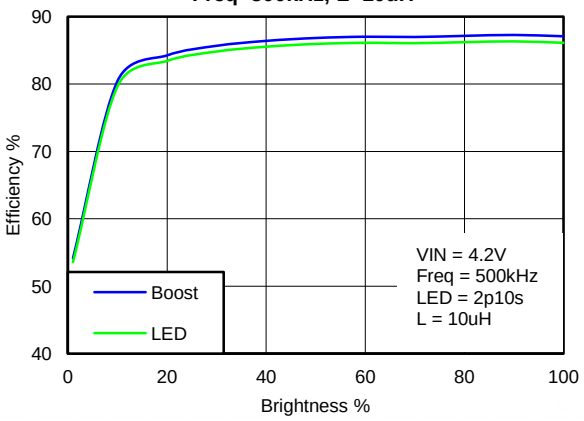


Figure 30.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25°C, ILED Full Scale = 20.0mA unless specified otherwise.

Boost and LED Efficiency at VIN = 5.5V, 2p10s, Freq=500kHz, L=10uH

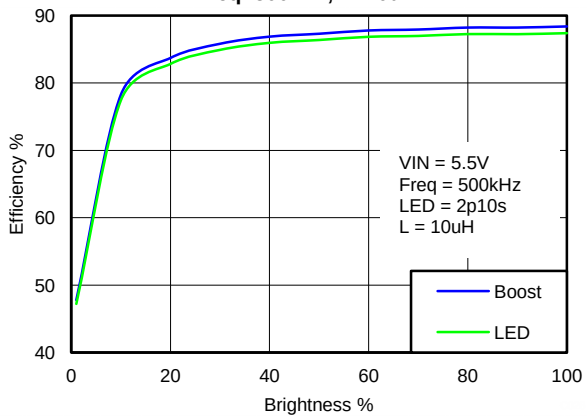


Figure 31.

IIN across VIN, 2p6s, Freq=500kHz, L=10uH, LED1 & 2 on DACA, ILED Full Scale=28.5mA

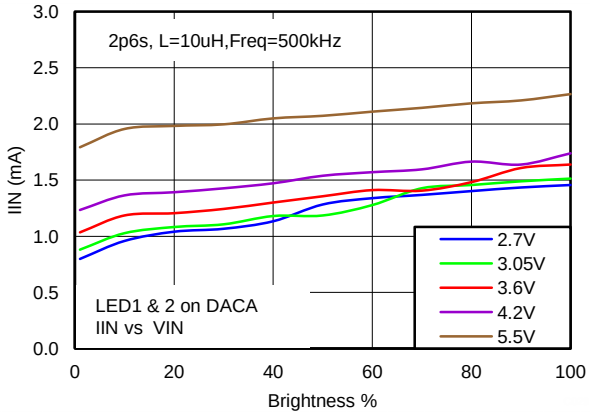


Figure 32.

PWR_IN across VIN, 2p6s, Freq=500kHz, L=10uH, LED1 & 2 on DACA, ILED Full Scale=28.5mA

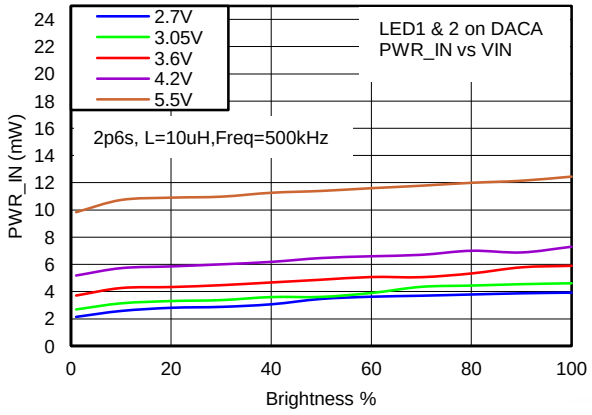


Figure 33.

VOUT across VIN, 2p6s, Freq=500kHz, L=10uH, LED1 & 2 on DACA, ILED Full Scale=28.5mA

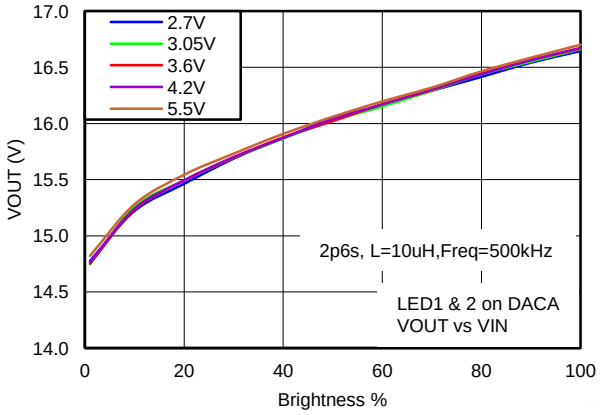


Figure 34.

IOUT across VIN, 2p6s, Freq=500kHz, L=10uH, LED1 & 2 on DACA, ILED Full Scale=28.5mA

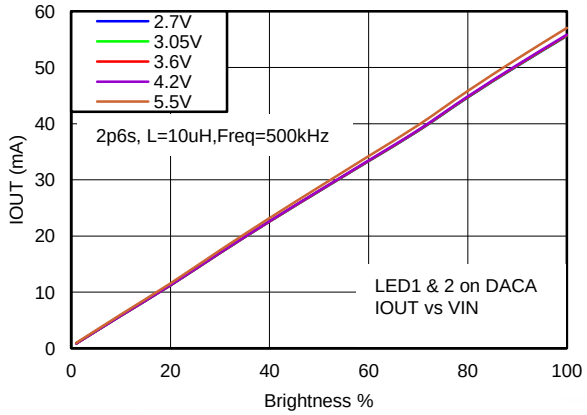


Figure 35.

PWR_OUT across VIN, 2p6s, Freq=500kHz, L=10uH, LED1 & 2 on DACA, ILED Full Scale=28.5mA

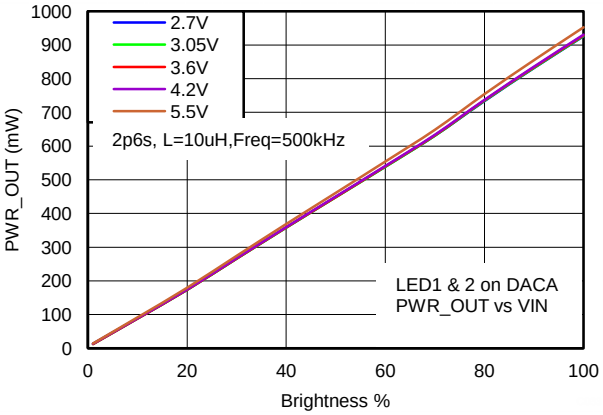


Figure 36.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25°C, ILED Full Scale = 20.0mA unless specified otherwise.

ILED across VIN, 2p6s, Freq=500kHz, L=10uH, LED1 & 2 on DACA, ILED Full Scale=28.5mA

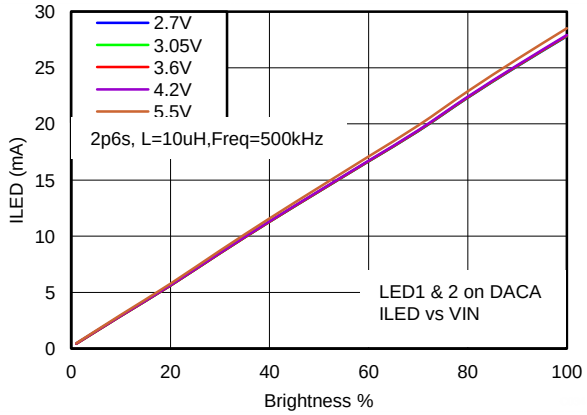


Figure 37.

I_Inductor across VIN, 2p6s, Freq=500kHz, L=10uH, LED1 & 2 on DACA, ILED Full Scale=28.5mA

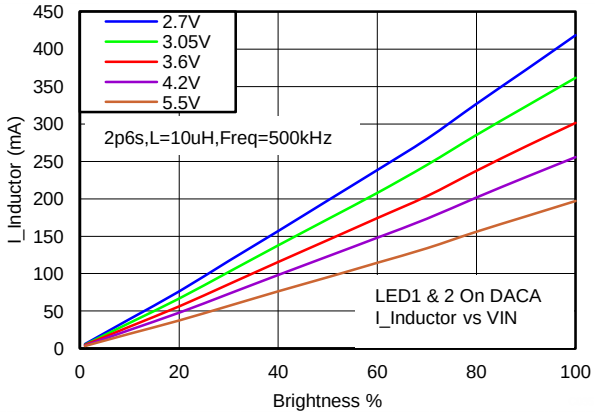


Figure 38.

IIN across VIN, 2p6s, Freq=500kHz, L=10uH, LED1 on DACA, LED2 on DACB, ILED Full Scale=28.5mA

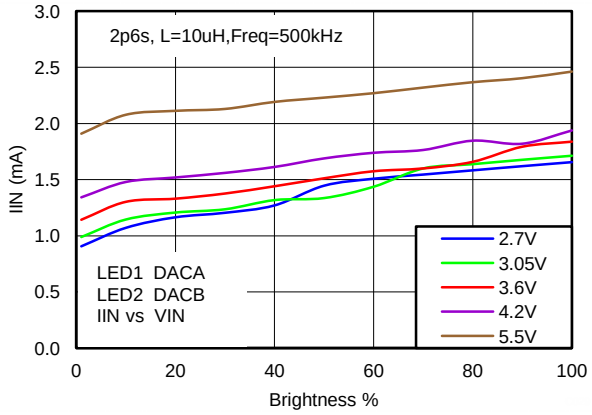


Figure 39.

PWR_IN across VIN, 2p6s, Freq=500kHz, L=10uH, LED1 on DACA, LED2 on DACB, ILED Full Scale=28.5mA

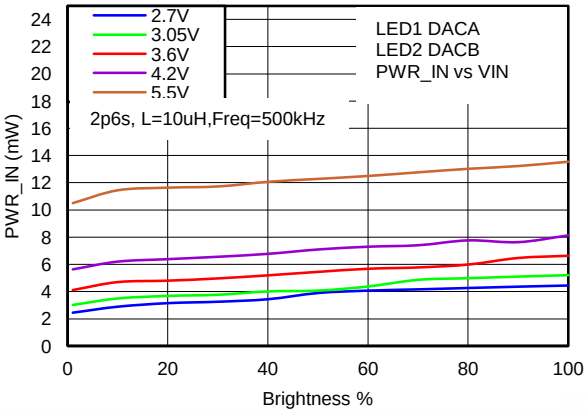


Figure 40.

VOUT across VIN, 2p6s, Freq=500kHz, L=10uH, LED1 on DACA, LED2 on DACB, ILED Full Scale=28.5mA

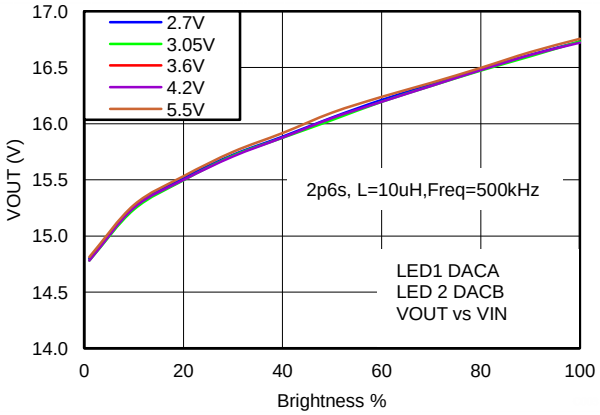


Figure 41.

IOUT across VIN, 2p6s, Freq=500kHz, L=10uH, LED1 on DACA, LED2 on DACB, ILED Full Scale=28.5mA

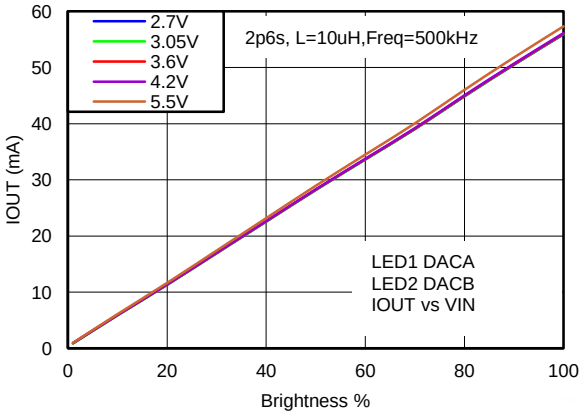


Figure 42.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25°C, ILED Full Scale = 20.0mA unless specified otherwise.

PWR_OUT across VIN, 2p6s, Freq=500kHz, L=10uH, LED1 on DACA, LED2 on DACB, ILED Full Scale=28.5mA

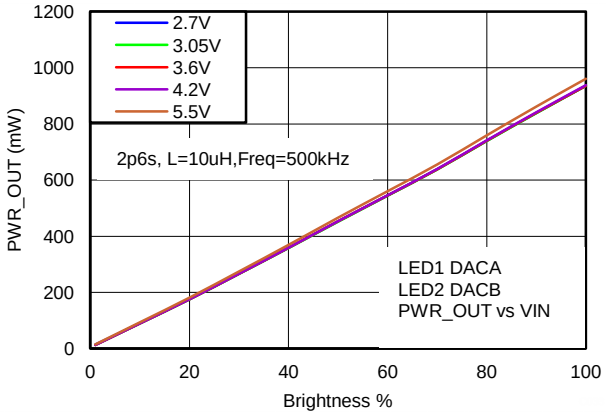


Figure 43.

ILED across VIN, 2p6s, Freq=500kHz, L=10uH, LED1 on DACA, LED2 on DACB, ILED Full Scale=28.5mA

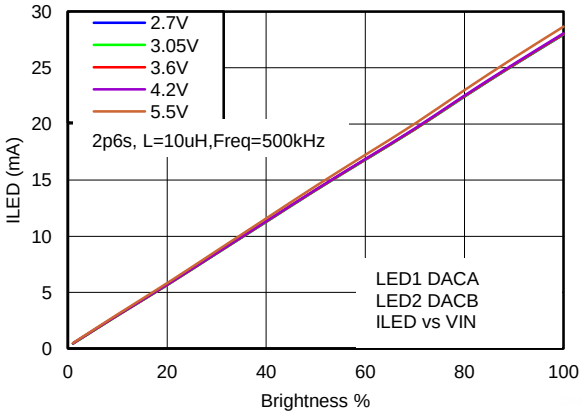


Figure 44.

I_Inductor across VIN, 2p6s, Freq=500kHz, L=10uH, LED1 on DACA, LED2 on DACB, ILED Full Scale=28.5mA

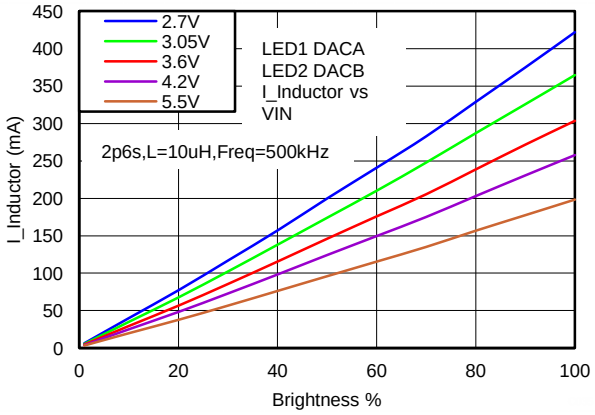


Figure 45.

IIN across VIN, 2p10s, Freq=1MHz, L=10uH, LED1 & 2 on DACA, ILED Full Scale=28.5mA

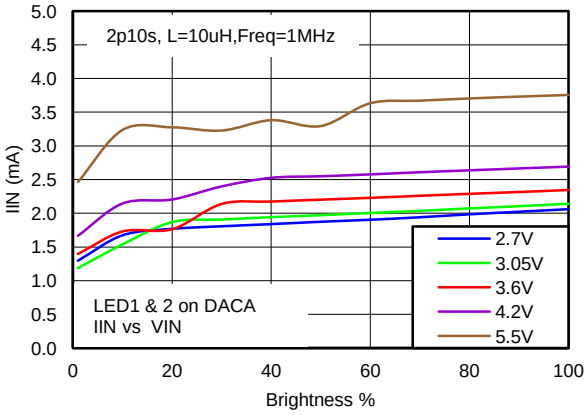


Figure 46.

PWR_IN across VIN, 2p10s, Freq=1MHz, L=10uH, LED1 & 2 on DACA, ILED Full Scale=28.5mA

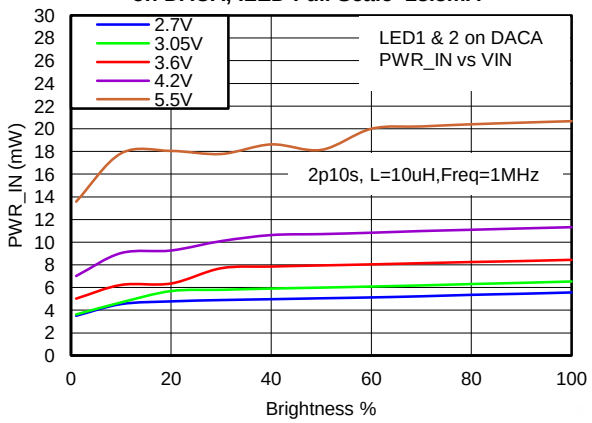


Figure 47.

VOUT across VIN, 2p10s, Freq=1MHz, L=10uH, LED1 & 2 on DACA, ILED Full Scale=28.5mA

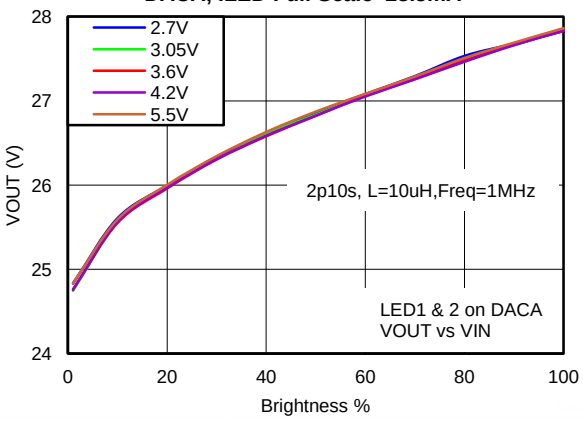


Figure 48.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25°C, ILED Full Scale = 20.0mA unless specified otherwise.

IOUT across VIN, 2p10s, Freq=1MHz, L=10uH, LED1 & 2 on DACA, ILED Full Scale=28.5mA

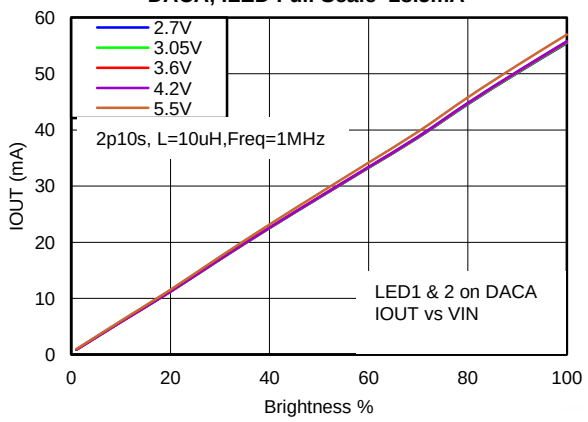


Figure 49.

PWR_OUT across VIN, 2p10s, Freq=1MHz, L=10uH, LED1 & 2 on DACA, ILED Full Scale=28.5mA

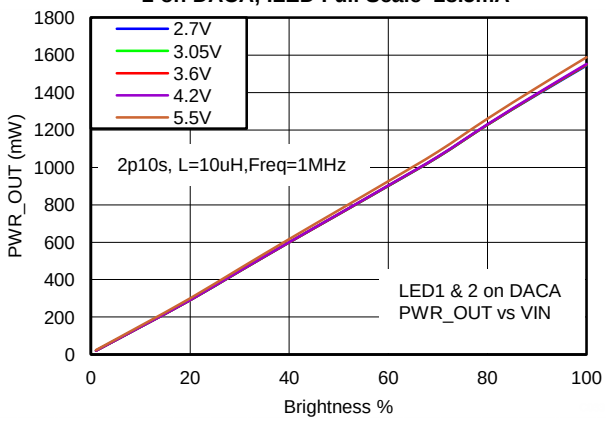


Figure 50.

ILED across VIN, 2p10s, Freq=1MHz, L=10uH, LED1 & 2 on DACA, ILED Full Scale=28.5mA

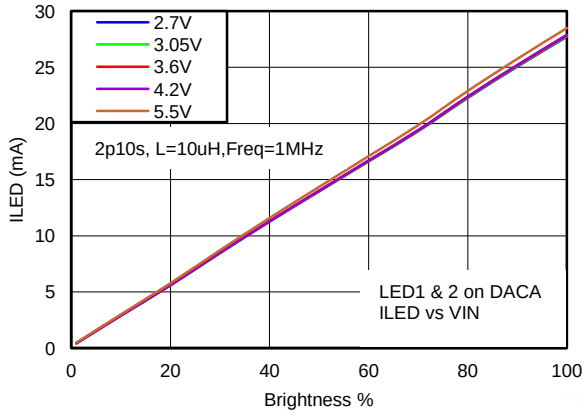


Figure 51.

I_Inductor across VIN, 2p10s, Freq=1MHz, L=10uH, LED1 & 2 on DACA, ILED Full Scale=28.5mA

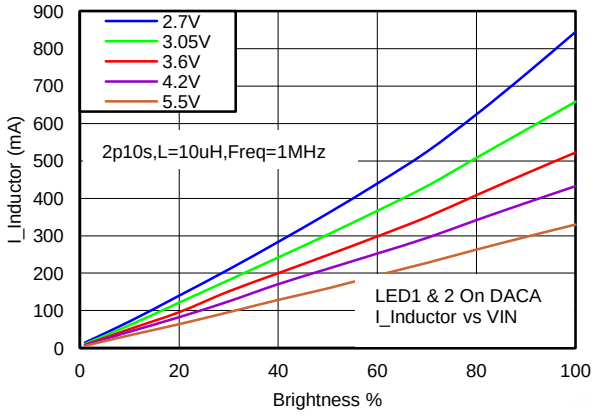


Figure 52.

IIN across VIN, 2p10s, Freq=1MHz, L=10uH, LED1 on DACA, LED2 on DACB, ILED Full Scale=28.5mA

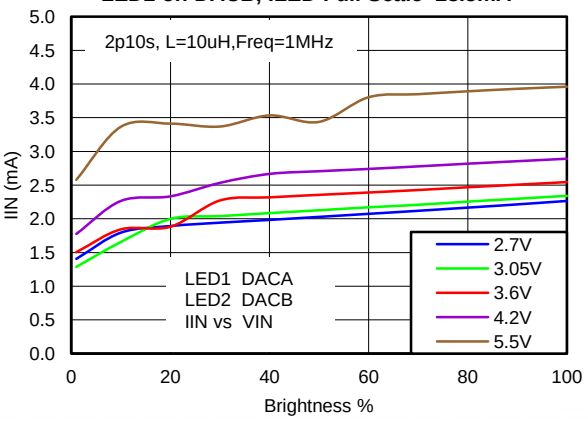


Figure 53.

PWR_IN across VIN, 2p10s, Freq=1MHz, L=10uH, LED1 on DACA, LED2 on DACB, ILED Full Scale=28.5mA

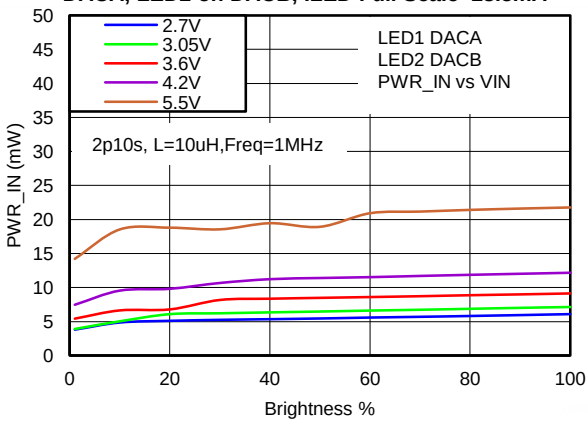


Figure 54.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25°C, ILED Full Scale = 20.0mA unless specified otherwise.

VOUT across VIN, 2p10s, Freq=1MHz, L=10uH, LED1 on DACA, LED2 on DACB, ILED Full Scale=28.5mA

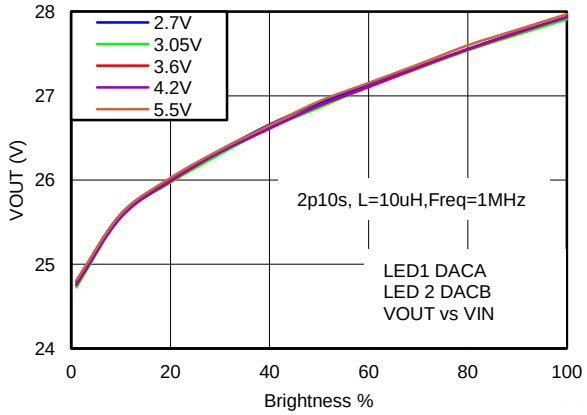


Figure 55.

IOUT across VIN, 2p10s, Freq=1MHz, L=10uH, LED1 on DACA, LED2 on DACB, ILED Full Scale=28.5mA

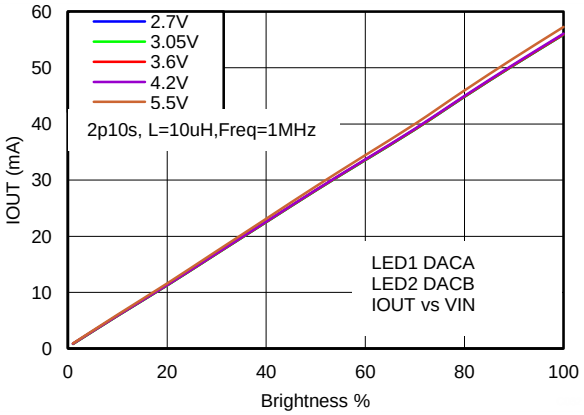


Figure 56.

PWR_OUT across VIN, 2p10s, Freq=1MHz, L=10uH, LED1 on DACA, LED2 on DACB, ILED Full Scale=28.5mA

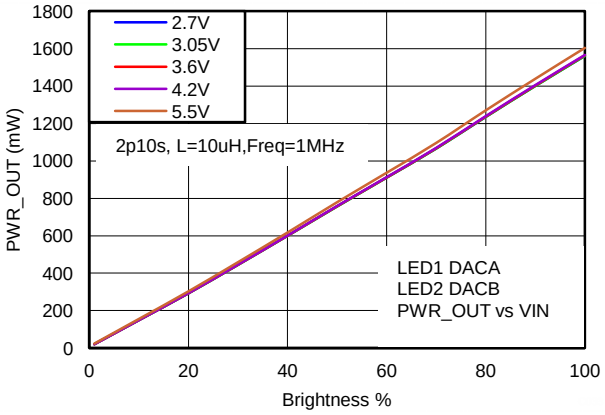


Figure 57.

ILED across VIN, 2p10s, Freq=1MHz, L=10uH, LED1 on DACA, LED2 on DACB, ILED Full Scale=28.5mA

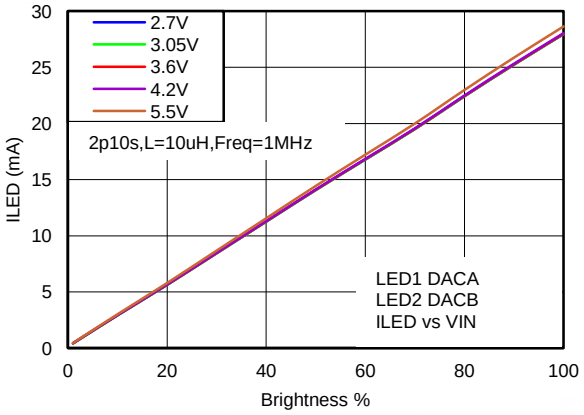


Figure 58.

I_Inductor across VIN, 2p10s, Freq=1MHz, L = 10uH, LED1 on DACA, LED2 on DACB, ILED Full Scale=28.5mA

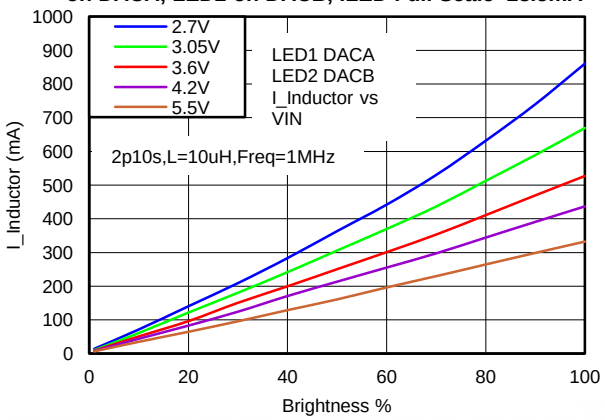


Figure 59.

IIN across VIN, 2p6s, Freq=500kHz, L=22uH, LED1 & 2 on DACA, ILED Full Scale=28.5mA

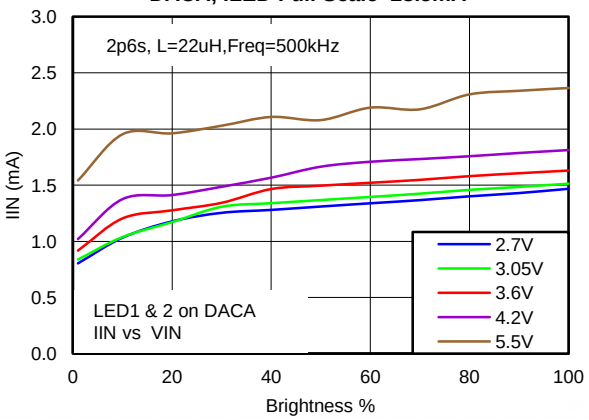


Figure 60.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25°C, ILED Full Scale = 20.0mA unless specified otherwise.

PWR_IIN across VIN, 2p6s, Freq=500kHz, L=22uH, LED1 & 2 on DACA, ILED Full Scale=28.5mA

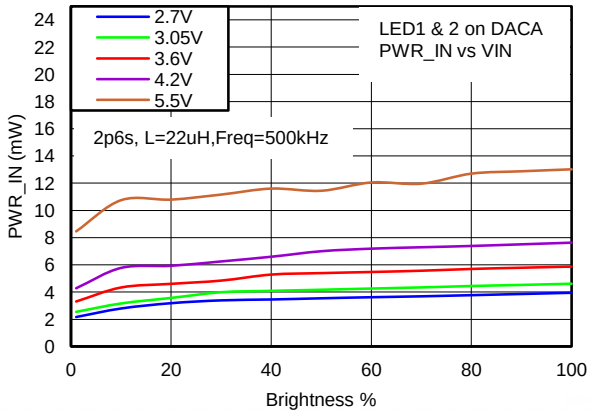


Figure 61.

VOUT across VIN, 2p6s, Freq=500kHz, L=22uH, LED1 & 2 on DACA, ILED Full Scale=28.5mA

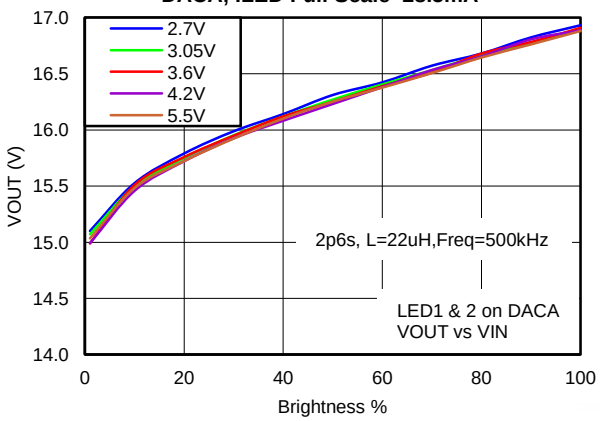


Figure 62.

IOUT across VIN, 2p6s, Freq=500kHz, L=22uH, LED1 & 2 on DACA, ILED Full Scale=28.5mA

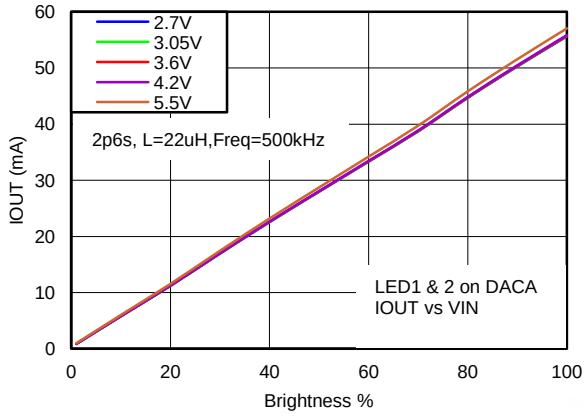


Figure 63.

PWR_IOUT across VIN, 2p6s, Freq=500kHz, L=22uH, LED1 & 2 on DACA, ILED Full Scale=28.5mA

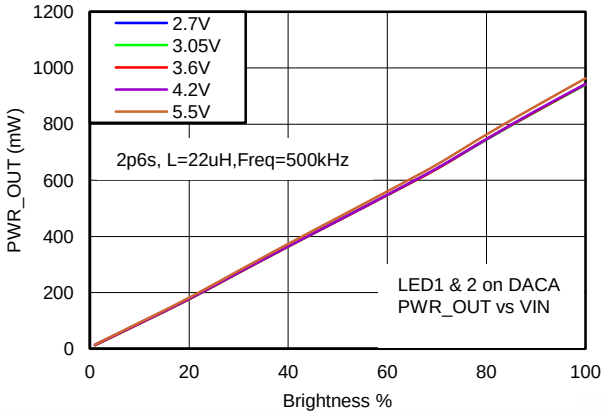


Figure 64.

ILED across VIN, 2p6s, Freq=500kHz, L=22uH, LED1 & 2 on DACA, ILED Full Scale=28.5mA

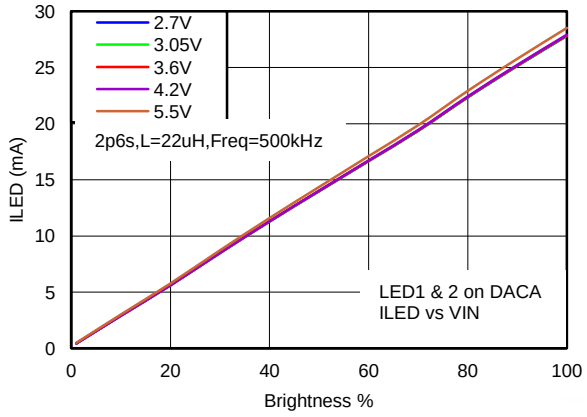


Figure 65.

I_Inductor across VIN, 2p6s, Freq=500kHz, L=22uH, LED1 & 2 on DACA, ILED Full Scale=28.5mA

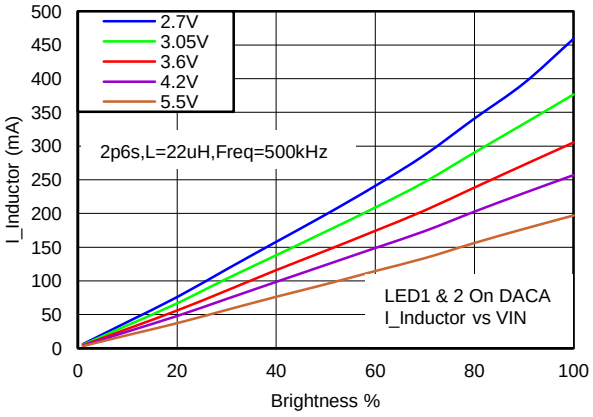


Figure 66.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25°C, ILED Full Scale = 20.0mA unless specified otherwise.

IIN across VIN, 2p6s, Freq=500kHz, L=22uH, LED1 on DACA, LED2 on DACB, ILED Full Scale=28.5mA

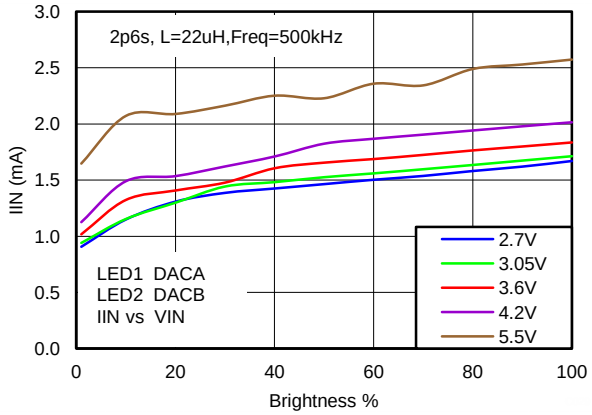


Figure 67.

PWR_IIN across VIN, 2p6s, Freq=500kHz, L=22uH, LED1 on DACA, LED2 on DACB, ILED Full Scale=28.5mA

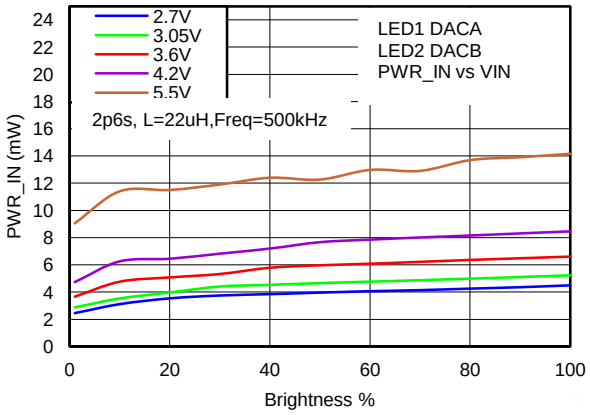


Figure 68.

VOUT across VIN, 2p6s, Freq=500kHz, L=22uH, LED1 on DACA, LED2 on DACB, ILED Full Scale=28.5mA

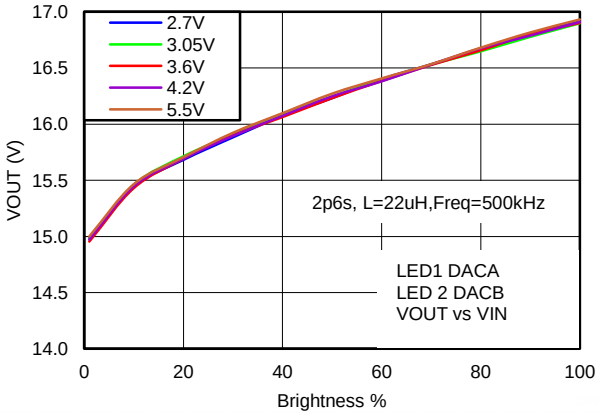


Figure 69.

IOUT across VIN, 2p6s, Freq=500kHz, L=22uH, LED1 on DACA, LED2 on DACB, ILED Full Scale=28.5mA

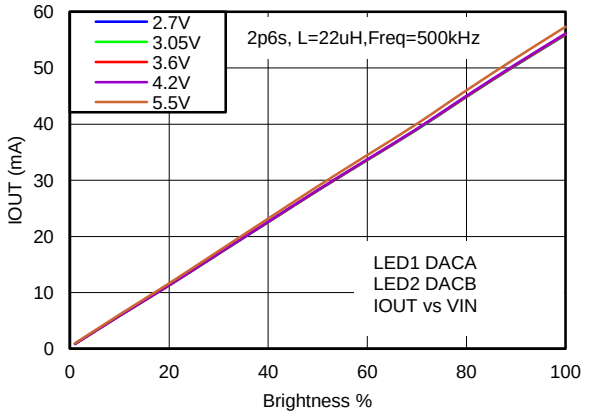


Figure 70.

PWR_OUT across VIN, 2p6s, Freq=500kHz, L=22uH, LED1 on DACA, LED2 on DACB, ILED Full Scale=28.5mA

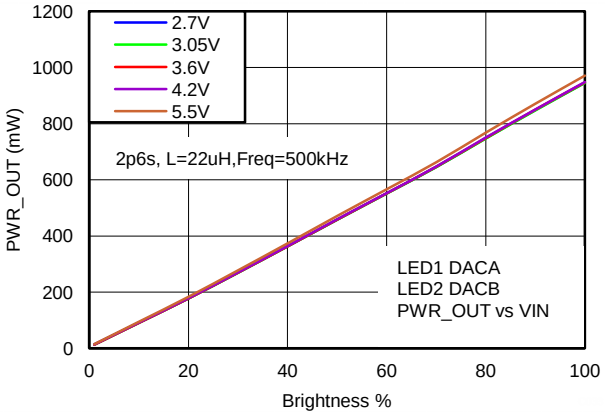


Figure 71.

ILED across VIN, 2p6s, Freq=500kHz, L=22uH, LED1 on DACA, LED2 on DACB, ILED Full Scale=28.5mA

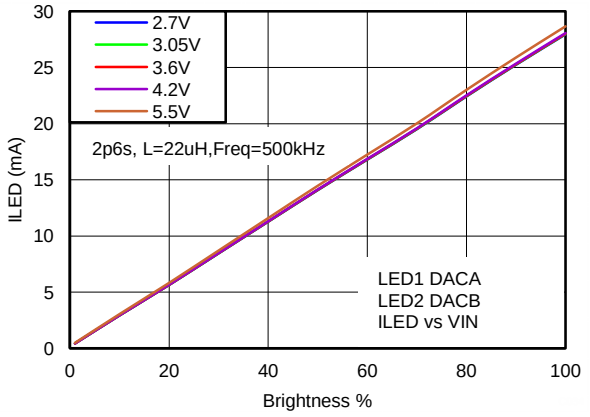


Figure 72.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25°C, ILED Full Scale = 20.0mA unless specified otherwise.

I_Inductor across VIN, 2p6s, Freq=500kHz, L=22uH, LED1 on DACA, LED2 on DACB, ILED Full Scale=28.5mA

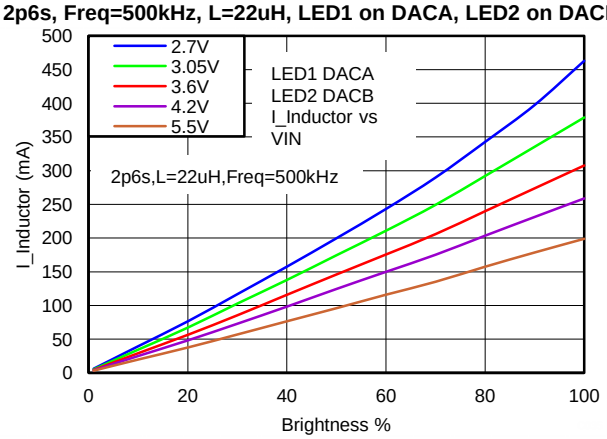
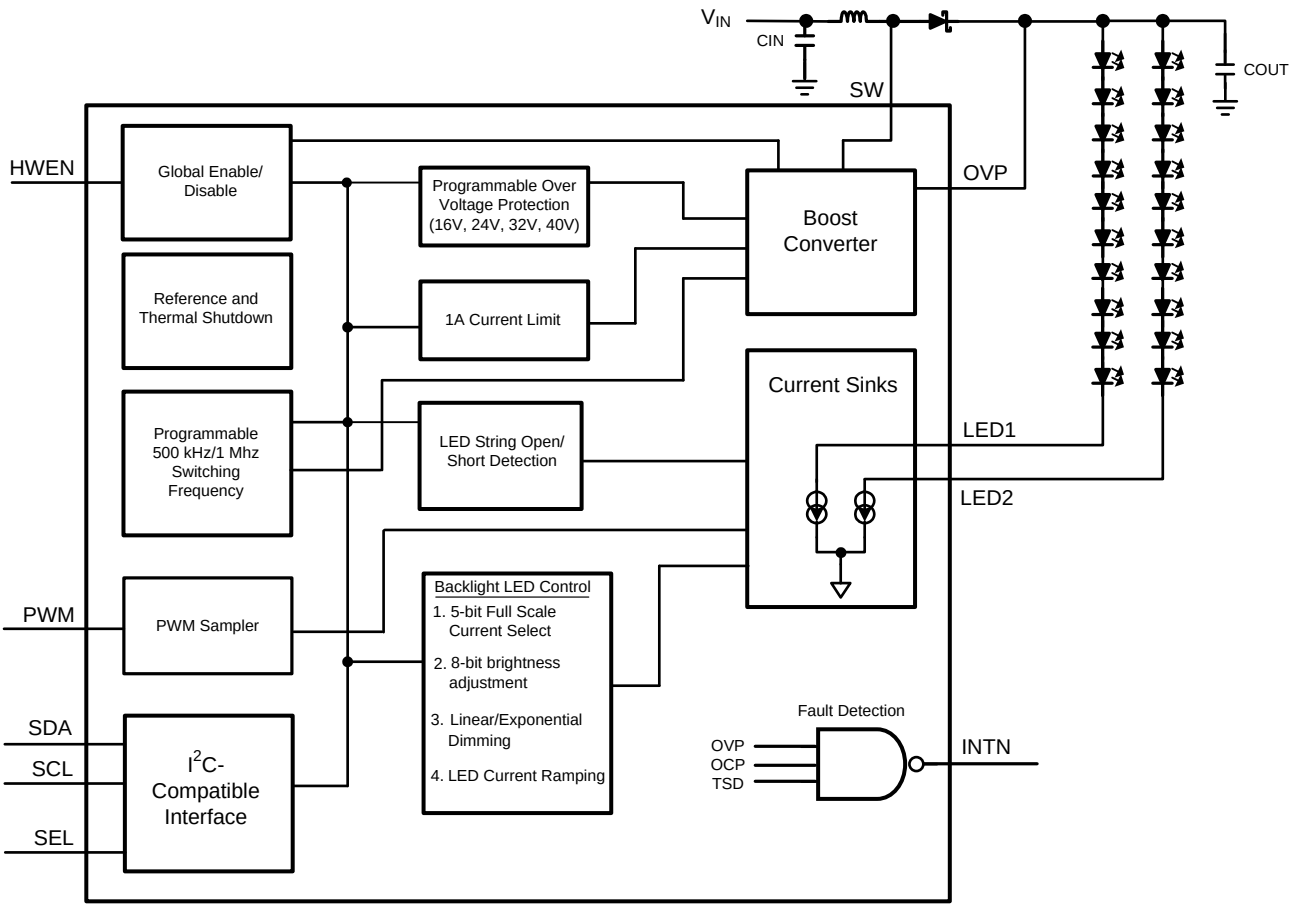


Figure 73.

FUNCTIONAL DESCRIPTION



Operation

The LM3630A provides the power for two high-voltage LED strings (up to 40V at 28.5 mA each). The two high-voltage LED strings are powered from an integrated asynchronous boost converter. The device is programmable over an I^2C-compatible interface. Additional features include a PWM input for content adjustable brightness control, programmable switching frequency, and programmable over voltage protection (OVP).

Control Bank Mapping

Control of the LM3630A's current sinks is not done directly, but through the programming of Control Banks. The current sinks are then assigned to the programmed Control Bank (see Figure 74). Both current sinks can be assigned to Control Bank A or LED1 can use Control Bank A while LED2 uses Control Bank B. Assigning LED1 to Control Bank A and LED2 to Control Bank B allows for better LED current matching. Assigning each current sink to different control banks allows for each current sink to be programmed with a different current or have the PWM input control a specific current sink.

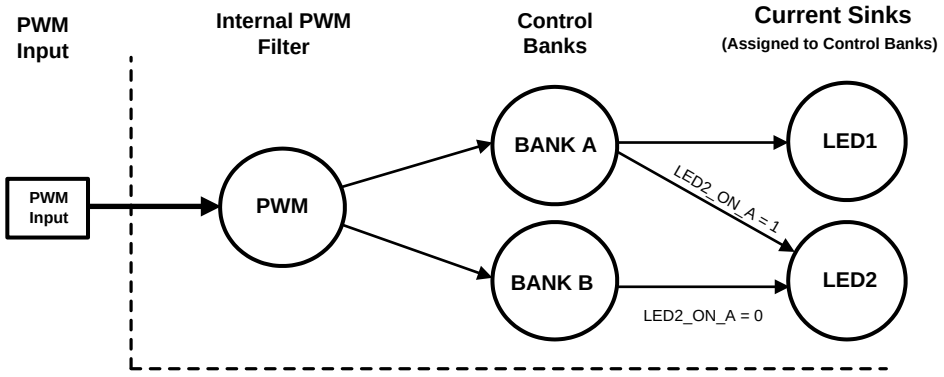


Figure 74. Control Diagram

Table 1. Bank Configuration Examples-Register Values

Registers to Program	ILED1 on A, ILED2 on B with PWM Dimming(1)	ILED1 and ILED2 on A with PWM Dimming	ILED1 on A with PWM ILED2 on B no PWM
Control	1EH linear or 06h exp	15h linear or 05h exp	1EH linear or 06h exp
Configuration	1Bh	09h	19h
Brightness A	used for A	used for both	used for A
Brightness B	used for B	not used	used for B (A and B do not have to be equal)

(1) LED current matching is specified using this configuration.

PWM Input Polaritiy

The PWM Input can be set for active high (default) or active low polarity. With active low polarity the LED current is a function of the negative duty cycle at PWM.

HWEN Input

HWEN is the global hardware enable to the LM3630A. HWEN must be pulled high to enable the device. HWEN is a high-impedance input so it cannot be left floating. When HWEN is pulled low the LM3630A is placed in shutdown and all the registers are reset to their default state.

SEL Input

SEL is the select pin for the serial bus device address. When this pin is connected to ground, the seven-bit device address is 36H. When this pin is tied to the VIN power rail, the device address is 38H.

INTN Output

The INTN pin is an open drain active low output signal which will indicate detected faults. The signal will assert low when either OCP, OVP, or TSD is detected by the LED driver. The Interrupt Enable register must be set to connect these faults to the INTN pin.

Boost Converter

The high-voltage boost converter provides power for the two current sinks (ILED1 and ILED2). The boost circuit operates using a 10 µH to 22 µH inductor and a 1µF output capacitor. The selectable 500 kHz or 1MHz switching frequency allows for the use of small external components and provides for high boost converter efficiency. Both LED1 and LED2 feature an adaptive voltage regulation scheme where the feedback point (LED1 or LED2) is regulated to a minimum of 300 mV. When there are different voltage requirements in both high-voltage LED strings, because of different programmed voltages or string mismatch, the LM3630A will regulate the feedback point of the highest voltage string to 300 mV and drop the excess voltage of the lower voltage string across the lower strings current sink.

Boost Switching Frequency Select

The LM3630A's boost converter can have a 1MHz or 500 kHz switching frequency. For a 500 kHz switching frequency the inductor must be between 10 µH and 22 µH. For the 1MHz switching frequency the inductor can be between 10 µH and 22 µH. Additionally there is a Frequency Shift bit which will offset the frequency approximately 10%. For the 500 kHz setting, Shift = 0. The boost frequency is shifted to 560 kHz when Shift = 1. For the 1MHz setting, Shift = 0. The boost frequency is shifted to 1120 kHz when Shift = 1.

Adaptive Headroom

Reference Figure 75 and Figure 76 for the following description.

The adaptive headroom circuit controls the Boost output voltage to provide the minimal headroom voltage necessary for the current sinks to provide the specified ILED current. The headroom voltage is fed back to the Error Amplifier to dynamically adjust the Boost output voltage. The Error Amplifier's reference voltage is adjusted as the brightness level is changed, since the currents sinks require less headroom at lower ILED currents than at higher ILED currents. Note that the VHR Min block dynamically selects the LED string that requires the higher Boost voltage to maintain the ILED current, this string will have the lower headroom voltage. In Figure 76 this is LED string 2. The headroom voltage on LED string 1 is higher, but this is due to LED string 2 have an overall higher forward voltage than LED string 1. LED strings that have closely matched forward voltages will have closely matched headroom voltages and better overall efficiency.

In a single string LED configuration the Feedback enable must be enabled for only that string (LED1 or LED2). The adaptive headroom circuit is control by that single string. In a two string LED configuration the Feedback enable must be enabled for both strings (LED1 and LED2). The VHR Min block then dynamically selects the LED string to control the adaptive headroom circuit.

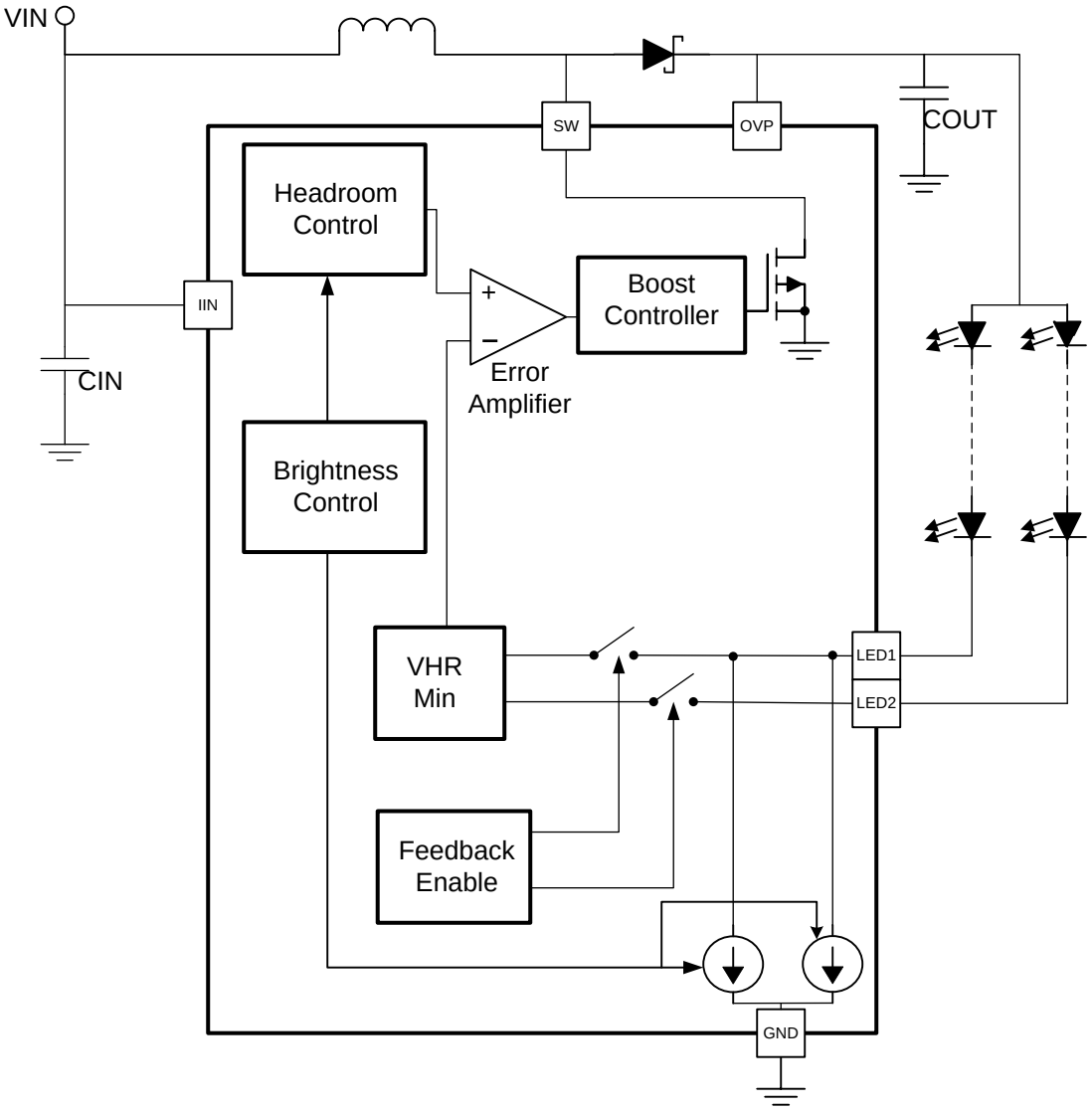


Figure 75. Adaptive Headroom Block Diagram

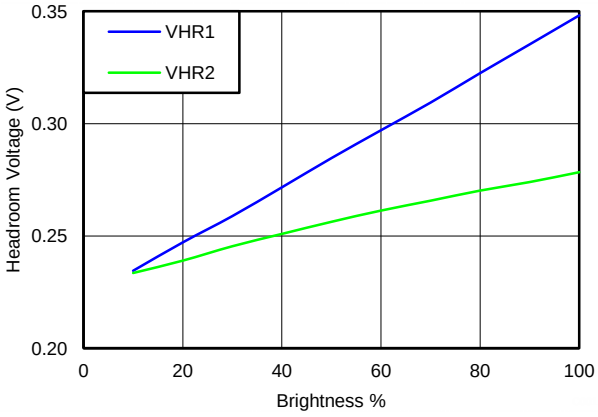


Figure 76. Typical Headroom Voltage Curves

Current Sinks

LED1 and LED2 control the current up to a 40V LED string voltage. Each current sink has 5-bit full-scale current programmability and 8-bit brightness control. Either current sink has its current set through a dedicated brightness register and can additionally be controlled via the PWM input.

Current String Biasing

Each current string can be powered from the LM3630A's boost or from an external source. When powered from an external source the feedback input for either current sink can be disabled in the Configuration register so it no longer controls the boost output voltage.

Full-Scale LED Current

The LM3630A's full-scale current is programmable with 32 different full scale levels. The full-scale current is the LED current in the control bank when the brightness code is at max code (0xFF). The 5 bit full-scale current vs code is given by the following equation:

$$ILED\ FULLSCALE = 5\ mA + Code \times 0.75\ mA \quad (1)$$

With a maximum full-scale current of 28.5 mA.

Brightness Register

Each control bank has its own 8-bit brightness register. The brightness register code and the full-scale current setting determine the LED current depending on the programmed mapping mode.

Exponential Mapping

In exponential mapping mode the brightness code to backlight current transfer function is given by the equation:

$$I_{LED} = I_{LED\_FULLSCALE} \times 0.85^{\left[44 - \left(\frac{(Code+1)}{5.81818}\right)\right]} \times D_{PWM} \quad (2)$$

Where $I_{LED\_FULLSCALE}$ is the full-scale LED current setting, Code is the backlight code in the brightness register, and DPWM is the PWM input duty cycle. Figure 77 and Figure 78 show the approximate backlight code to LED current response using exponential mapping mode. Figure 77 shows the response with a linear Y axis, and Figure 78 shows the response with a logarithmic Y axis. In exponential mapping mode the current ramp (either up or down) appears to the human eye as a more uniform transition then the linear ramp. This is due to the logarithmic response of the eye.

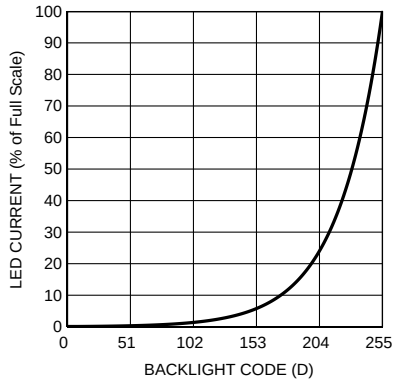


Figure 77. Exponential Mapping Mode (Linear Scale)

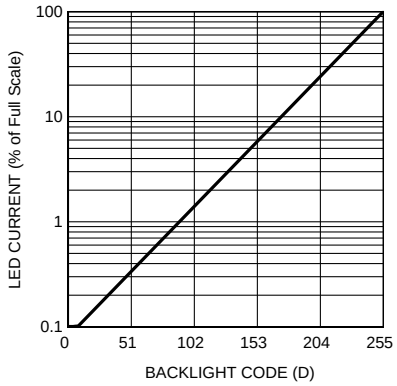


Figure 78. Exponential Mapping Mode (Log Scale)

Linear Mapping

In linear mapping mode the brightness code to backlight current has a linear relationship and follows the equation:

$$I_{LED} = I_{LED\_FULLSCALE} \times \frac{1}{255} \times Code \times D_{PWM} \quad (3)$$

Where $I_{LED\_FULLSCALE}$ is the full scale LED current setting, Code is the backlight code in the brightness register, and DPWM is the PWM input duty cycle. Figure 79 shows the backlight code to LED current response using linear mapping mode. The Configuration register must be set to enable linear mapping.

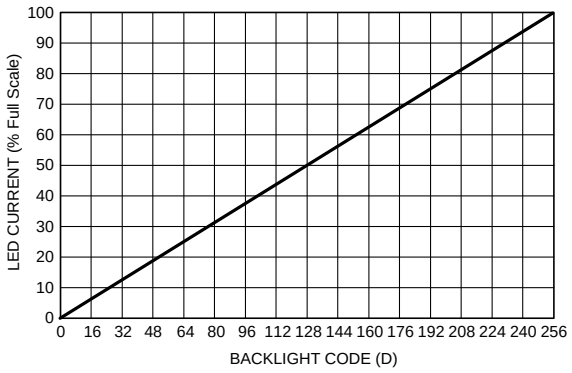


Figure 79. Linear Mapping Mode

LED Current Ramping

Startup/Shutdown Ramp

The LED current turn on time from 0 to the initial LED current set-point is programmable. Similarly, the LED current shutdown time to 0 is programmable. Both the startup and shutdown times are independently programmable with 8 different levels. The Startup times are independently programmable from the Shutdown times, but not independently programmable for each Control bank. For example, programming a Start-up or Shutdown time, programs the same ramp time for each Control Bank. The Startup time is used when the device is first enabled to a non-zero brightness value. The Shutdown time is used when the brightness value is programmed to zero. If HWEN is used to disable the device, the action is immediate and the Shutdown time is not used. The zero code does take a small amount of time which is approximately 0.5 ms.

Table 2. Startup/Shutdown Times

Code	Startup Time	Shutdown Time
000	4 ms	0

Table 2. Startup/Shutdown Times (continued)

Code	Startup Time	Shutdown Time
001	261 ms	261 ms
010	522 ms	522 ms
011	1.045s	1.045s
100	2.091s	2.091s
101	4.182s	4.182s
110	8.364s	8.364s
111	16.73s	16.73s

Run-Time Ramp

Current ramping from one brightness level to the next is programmable. There are 8 different ramp up times and 8 different ramp down times. The ramp up time is independently programmable from the ramp down time, but not independently programmable for each Control Bank. For example, programming a ramp up time or a ramp down time will program the same ramp time for each control bank. The run time ramps are used whenever the device is enabled with a non-zero brightness value and a new non-zero brightness value is written.

Table 3. LED Current Run Ramp Times

Code	Ramp-Up Time	Ramp-Down Time
000	0	0
001	261 ms	261 ms
010	522 ms	522 ms
011	1.045s	1.045s
100	2.091s	2.091s
101	4.182s	4.182s
110	8.364s	8.364s
111	16.73s	16.73s

Test Features

The LM3630A contains an LED open, an LED short, and Over Voltage manufacturing fault detection. This fault detection is designed to be used during the manufacturing process only and not normal operation. These faults do not set the INTN pin.

Open LED String (LED1 and LED2)

An open LED string is detected when the voltage at the input to either LED1 or LED2 has fallen below 200 mV **and** the boost output voltage has hit the OVP threshold. This test assumes that the LED string that is being detected for an open is being powered from the boost output (Feedback Enabled). For an LED string not connected to the boost output, and connected to another voltage source, the boost output would not trigger the OVP flag. In this case an open LED string would not be detected.

Shorted LED String

The LM3630A features an LED short fault flag indicating if either of the LED strings have experienced a short. There are two methods that can trigger a short in the LED strings

1. An LED current sink with feedback enabled and the difference between OVP input and the LED current sink input voltage goes below 1V.
2. An LED current sink is configured with feedback disabled (not powered from the boost output) and the difference between VIN and the LED current sink input voltage goes below 1V.

Over-Voltage Protection (Manufacturing Fault Detection and Shutdown)

The LM3630A provides an Over-Voltage Protection (OVP) mechanism specifically for manufacturing test where a display may not be connected to the device. The over voltage protection threshold (OVP) on the LM3630A has 4 different programmable options (16V, 24V, 32V, and 40V). The manufacturing protection is enabled in the Fault Status register bit 0. When enabled, this feature will cause the boost converter to shutdown anytime the selected OVP threshold is exceeded. The OVP_fault bit in the Fault Status register will be set to one. The boost converter will not resume operation until the LM3630A is reset with either a write to the Software Reset bit in the Software Reset register or a cycling of the HWEN pin. The reset will clear the fault.

Fault Flags/Protection Features

The Interrupt Status register contains the status of the protection circuits of the LM3630A. The corresponding bits will be set to one if an OVP, OCP, or TSD event occurs. These faults do set the INTN pin when the corresponding bit is set in the Interrupt Enable register.

Over-Voltage Protection (Inductive Boost Operation)

The over-voltage protection threshold (OVP) on the LM3630A has 4 different programmable options (16V, 24V, 32V, and 40V). Over voltage protection protects the device and associated circuitry from high voltages in the event the feedback enabled LED string becomes open. During normal operation, the LM3630A's inductive boost converter will boost the output up so as to maintain at least 300 mV at the active current sink inputs. When a high-voltage LED string becomes open the feedback mechanism is broken, and the boost converter will inadvertently over boost the output. When the output voltage reaches the over voltage protection (OVP) threshold the boost converter will stop switching, thus allowing the output node to discharge. When the output discharges to VOVP – 1V the boost converter will begin switching again. The OVP sense is at the OVP pin, so this pin must be connected directly to the inductive boost output capacitor's positive terminal.

For current sinks that have feedback disabled the over voltage sense mechanism is not in place to protect from potential over-voltage conditions. In this situation the application must ensure that the voltage at LED1 or LED2 doesn't exceed 40V.

The default setting for OVP is set at 24V. For applications that require higher than 24V at the boost output the OVP threshold will have to be programmed to a higher level at power up.

Current Limit

The switch current limit for the LM3630A's inductive boost is set at 1A. When the current through the NFET switch hits this over current protection threshold (OCP) the device turns the NFET off and the inductor's energy is discharged into the output capacitor. Switching is then resumed at the next cycle. The current limit protection circuitry can operate continuously each switch cycle. The result is that during high output power conditions the device can continuously run in current limit. Under these conditions the LM3630A's inductive boost converter stops regulating the headroom voltage across the high voltage current sinks. This results in a drop in the LED current.

Thermal Shutdown

The LM3630A contains thermal shutdown protection. In the event the die temperature reaches +140°C, the boost power supply and current sinks will shut down until the die temperature drops to typically +125°C.

Initialization Timing

Initialization Timing with HWEN tied to VIN

If the HWEN input is tied to VIN, then the t_{WAIT} time starts when VIN crosses 2.5V as shown below. The initial I^2C transaction can occur after the t_{WAIT} time expires. Any I^2C transaction during the t_{WAIT} period will be NAK'ed.

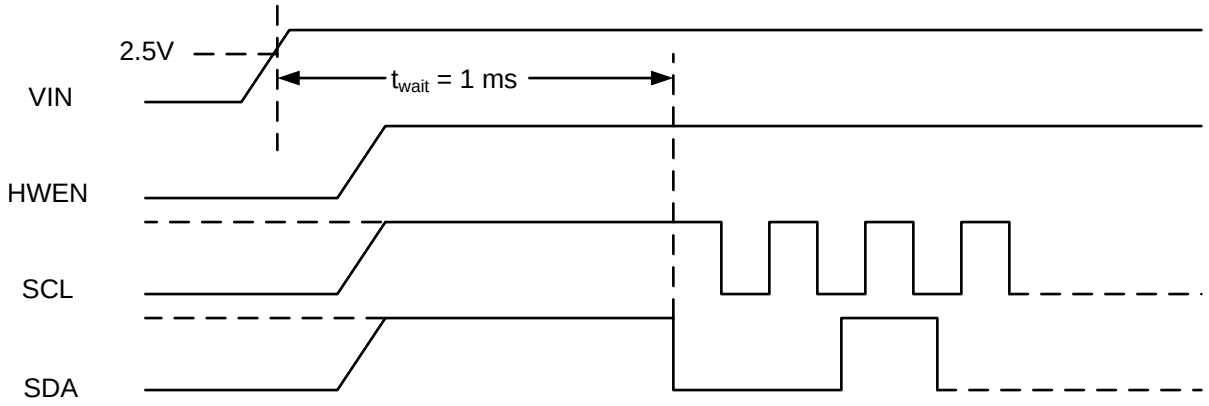


Figure 80. Initialization Timing with HWEN is tied to VIN

Initialization Timing with HWEN driven by GPIO

If the HWEN input is driven by a GPIO then the t_{WAIT}time starts when HWEW crosses 1.2V as shown below. The initial I^2C transaction can occur after the t_{WAIT} time expires. Any I^2C transaction during the t_{WAIT} period will be NAK'ed

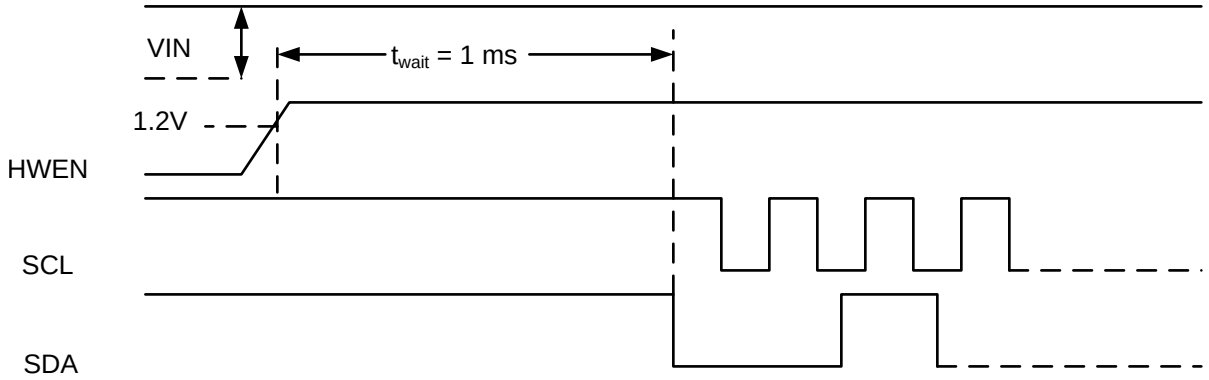


Figure 81. Initialization Timing with HWEN driven by a GPIO

Initialization after Software Reset

The time between the I^2C transaction that issues the software reset, and the subsequent I^2C transaction (ie to configure the LM3630A) must be at greater or equal to the t_{WAIT} period of 1ms. Any I^2C transaction during the t_{WAIT} period will be NAK'ed

I²C-COMPATIBLE INTERFACE

Data Validity

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when SCL is LOW.

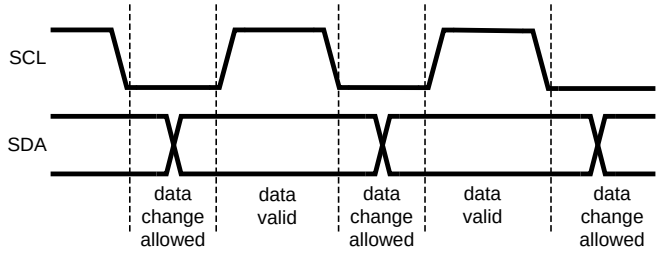


Figure 82. Data Validity Diagram

A pull-up resistor between the controller's VIO line, and SDA must be greater than [**(VIO-V_{OL}) / 3mA**] to meet the V_{OL} requirement on SDA. Using a larger pull-up resistor results in lower switching current with slower edges, while using a smaller pull-up results in higher switching currents with faster edges.

Start And Stop Conditions

START and STOP conditions classify the beginning and the end of the I²C session. A START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. A STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP conditions. The I²C bus is considered to be busy after a START condition and free after a STOP condition. During data transmission, the I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.

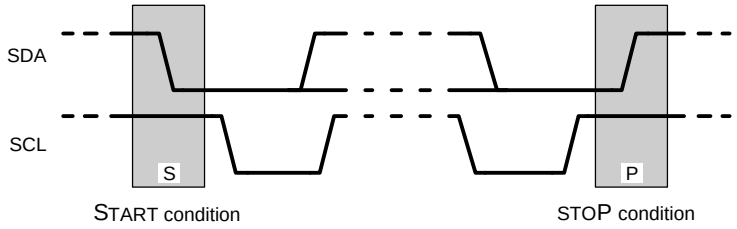


Figure 83. Start and Stop Conditions

Transfering Data

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) transferred first. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the acknowledge clock pulse. The LM3630A pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The LM3630A generates an acknowledge after each byte is received.

After the START condition, the I²C master sends a chip address. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LM3630A address is 36h. For the eighth bit, a “0” indicates a WRITE and a “1” indicates a READ. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

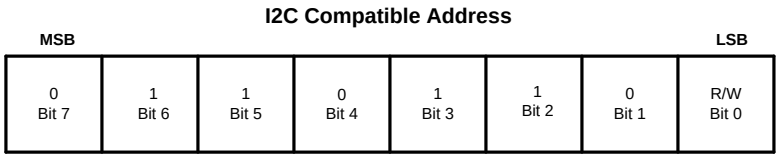


Figure 84. I²C-Compatible Chip Address (0x36), SEL = 0

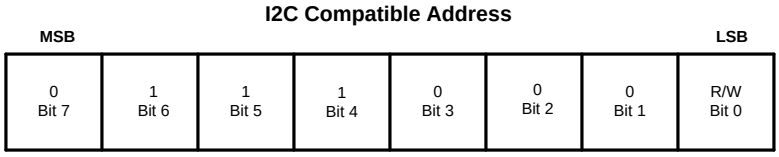


Figure 85. I^2C-Compatible Chip Address (0x38), SEL = 1

LM3630A I²C Register Map

This table summarizes LM3630A I²C-compatible register usage and shows default register bit values after reset, as programmed by the factory. The following sub-sections provide additional details on the use of individual registers. Register bits which are blank in the following tables are considered undefined. Undefined bits should be ignored on reads and written as zero.

Slave Address [0x36h for SEL = 0, 0x38h for SEL = 1]			
Base Registers			
Register Name	**Address**	**Type**	**Default Reset Values**
Control	0x00	R/W	0xC0
Configuration	0x01	R/W	0x18
Boost Control	0x02	R/W	0x38
Brightness A	0x03	R/W	0x00
Brightness B	0x04	R/W	0x00
Current A	0x05	R/W	0x1F
Current B	0x06	R/W	0x1F
On/Off Ramp	0x07	R/W	0x00
Run Ramp	0x08	R/W	0x00
Interrupt Status	0x09	R/W	0x00
Interrupt Enable	0x0A	R/W	0x00
Fault Status	0x0B	R/W	0x00
Software Reset	0x0F	R/W	0x00
PWM Out Low	0x12	Read	0x00
PWM Out High	0x13	Read	0x00
Revision	0x1F	Read	0x02
Filter Strength	0x50	R/W	0x00

Register Descriptions

Control (Offset = 0x00, Default = 0xC0)

Register Bits							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SLEEP_CMD	SLEEP_ STATUS		LINEAR_A	LINEAR_B	LED_A_EN	LED_B_EN	LED2_ON_A

Name	Bit	Access	Description
SLEEP_CMD	7	R/W	The device is put into sleep mode when set to '1'
SLEEP_STATUS	6	Read	Reflects the sleep mode status. A '1' indicates the part is in sleep mode.
			Used to determine when part has entered or exited sleep mode after writing the SLEEP_CMD bit.
	5	Read	
LINEAR_A	4	R/W	Enables the linear output mode for Bank A when set to '1'.
LINEAR_B	3	R/W	Enables the linear output mode for Bank B when set to '1'.
LED_EN_A	2	R/W	Enables the LED A output
LED_EN_B	1	R/W	Enables the LED B output
LED2_ON_A	0	R/W	Connect the LED2 output to Bank A Control

Configuration (Offset = 0x01, Default = 0x18)

Register Bits							
7	6	5	4	3	2	1	0
			FB_EN_B	FB_EN_A	PWM_LOW	PWM_EN-B	PWM_EN_A

Name	Bit	Access	Description
	7	Read	
	6	Read	
	5	Read	
FB_EN_B	4	R/W	Enable Feedback on Bank B
FB_EN_A	3	R/W	Enable Feedback on Bank A
PWM_LOW	2	R/W	Sets the PWM to active low
PWM_EN_B	1	R/W	Enables the PWM for Bank B
PWM_EN_A	0	R/W	Enables the PWM for Bank A

Boost Control (Offset = 0x02, Default = 0x38)

Register Bits							
7	6	5	4	3	2	1	0
	BOOST_OVP[1]	BOOST_OVP[0]	BOOST_OCP[1]	BOOST_OCP[0]	SLOW_START	SHIFT	FMODE

Name	Bit	Access	Description
	7	Read	
BOOST_OVP	6:5	R/W	Selects the voltage limit for over-voltage protection: 00 = 16V 01 = 24V 10 = 32V 11 = 40V
BOOST_OCP	4:3	R/W	Selects the current limit for over-current protection: 00 = 600 mA 01 = 800 mA 10 = 1.0A 11 = 1.2A
SLOW_START	2	R/W	Slows the boost output transition
SHIFT	1	R/W	Enables the alternate oscillator frequencies: For FMODE = 0: SHIFT = 0F = 500 kHz; SHIFT 1F = 560 kHz For FMODE = 1: SHIFT = 0F = 1 MHz; SHIFT 1F = 1120 MHz
FMODE	0	R/W	Selects the boost frequency: 0 = 500 kHz, 1 = 1MHz

Brightness A (Offset = 0x03, Default = 0x00)(1)

Register Bits							
7	6	5	4	3	2	1	0
A[7]	A[6]	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]

Name	Bit	Access	Description
A	[7:0]	R/W	Sets the 8-bit brightness value for outputs connected to Bank A. Minimum brightness setting is code 04h.

(1) These registers will not update if the device is in Sleep Mode (Control: SLEEP_STATUS = 1).

Brightness B (Offset = 0x04, Default = 0x00)(1)

Register Bits							
7	6	5	4	3	2	1	0
B[7]	B[6]	B[5]	B[4]	B[3]	B[2]	B[1]	B[0]

Name	Bit	Access	Description
B	[7:0]	R/W	Sets the 8-bit brightness value for outputs connected to Bank B. Minimum brightness setting is code 04h.

(1) These registers will not update if the device is in Sleep Mode (Control: SLEEP_STATUS = 1).

Current A (Offset = 0x05, Default 0x1F)

Register Bits							
7	6	5	4	3	2	1	0
Hysteresis	Lower Bound		A[4]	A[3]	A[2]	A[1]	A[0]

Name	Bit	Access	Description
Hysteresis	7	R/W	Determines the hysteresis of the PWM Sampler. Clearing this bit, the PWM sampler changes its output upon detecting at least 3 equivalent code changes on the PWM input. Setting this bit, the PWM sampler changes its output upon detecting 2 equivalent code changes on the PWM input.
Lower Bound	6	R/W	Determines the lower bound of the PWM Sampler. Clearing this bit, the PWM sampler outputs code 6 when it detects equivalent codes 2 thru 6; and code 0 when it detects equivalent codes 0 thru 1. Setting this bit, the PWM sampler can output codes below 6, based upon the Hysteresis setting and equivalent code sampled from the input PWM.
	5	Read	
A	[4:0]	R/W	Sets the 5-bit full-scale current for outputs connected to Bank A.

Current B (Offset = 0x06, Default = 0x1F)

Register Bits							
7	6	5	4	3	2	1	0
			B[4]	B[3]	B[2]	B[1]	B[0]

Name	Bit	Access	Description
B	[4:0]	R/W	Sets the 5-bit full-scale current for outputs connected to Bank B

On/Off Ramp (Offset = 0x07, Default 0x00)

Register Bits							
7	6	5	4	3	2	1	0
		T_START[2]	T_START[1]	T_START[0]	T_SHUT[2]	T_SHUT[1]	T_SHUT[0]

Name	Bit	Access	Description
	7	Read	
	6	Read	
T_START	[5:3]	R/W	Ramp time for startup events.
T_SHUT	[2:0]	R/W	Ramp time for shutdown events.

Code	Start-Up Time	Shutdown Time
000	4 ms	0*
001	261 ms	261 ms
010	522 ms	522 ms
011	1.045s	1.045s
100	2.091s	2.091s
101	4.182s	4.182s
110	8.364s	8.364s
111	16.73s	16.73s

*Code 0 results in approximately 0.5 ms ramp time.

Run Ramp (Offset = 0x08, Default = 0x00)

Register Bits							
7	6	5	4	3	2	1	0
		T_UP[2]	T_UP[1]	T_UP[0]	T_DOWN[2]	T_DOWN[1]	T_DOWN[0]

Name	Bit	Access	Description
	7	Read	
	6	Read	
T_UP	[5:3]	R/W	Time for ramp-up events
T_DOWN	[2:0]	R/W	Time for ramp-down events

Code	Ramp-Up Time	Ramp-down Time
000	0*	0*
001	261 ms	261 ms
010	522 ms	522 ms
011	1.045s	1.045s
100	2.091s	2.091s
101	4.182s	4.182s
110	8.364s	8.364s
111	16.73s	16.73s

*Code 0 results in approximately 0.5 ms ramp time.

Interrupt Status (Offset = 0x09, Default = 0x00)

Register Bits							
7	6	5	4	3	2	1	0
					OCP	OVP	TSD

Name	Bit	Access	Description
	7	Read	
	6	Read	
	5	Read	
	4	Read	
	3	Read	
OCP	2	R/W	An over-current condition occurred.
OVP	1	R/W	An over-voltage condition occurred.
TSD	0	R/W	A thermal shutdown event occurred.

The interrupt status register is cleared upon a read of the register. If the condition that caused the interrupt is still present, then the bit will be set to one again and another interrupt is signaled on the INTN output pin. The interrupt status register is not cleared if the device is in sleep mode (Control: SLEEP_STATUS = 1). To disconnect the interrupt condition from the INTN pin during sleep mode, disable the fault connection in the Interrupt Enable register. An interrupt condition will set the status bit and cause an event on the INTN pin only if the corresponding bit in the Interrupt Enable register is one and the Global Enable bit is also one.

Interrupt Enable (Offset = 0x0A, Default = 0x00)

Register Bits							
7	6	5	4	3	2	1	0
					OCP	OVP	TSD

Name	Bit	Access	Description
GLOBAL	7	R/W	Set to '1' to enable interrupts to drive the INTN pin.
	6	Read	
	5	Read	
	4	Read	
	3	Read	
OCP	2	R/W	Set to '1' to enable the over-current condition interrupt.
OVP	1	R/W	Set to '1' to enable the over-voltage condition interrupt.
TSD	0	R/W	Set to '1' to enable the thermal shutdown interrupt.

Fault Status (Offset = 0x0B, Default = 0x00)

Register Bits							
7	6	5	4	3	2	1	0
		OPEN	LED2_SHORT	LED1_SHORT	SHORT_EN	OVP_FAULT	OVP_F_EN

Name	Bit	Access	Description
	7	Read	.
	6	Read	
OPEN	5	R/W	An open circuit was detected on one of the LED strings.
LED2_SHORT	4	R/W	A short was detected on LED string 2.
LED1_SHORT	3	R/W	A short was detected on LED string 1.
SHORT_EN	2	R/W	Set to '1' to enable short test.
OVP_FAULT	1	R/W	An OVP occurred in manufacturing test.
OVP_F_EN	0	R/W	Set to '1' to enable OVP manufacturing test.

Software Reset (Offset = 0x0F, Default = 0x00)

Register Bits							
7	6	5	4	3	2	1	0
							SW_RESET

Name	Bit	Access	Description
	7	Read	.
	6	Read	
	5	Read	
	4	Read	
	3	Read	
	2	Read	
	1	Read	
SW_RESET	0	R/W	Set to '1' to reset the device. This is a full reset which clears the registers, executes a power-on reset, and reads the EPROM configuration.

PWM Out Low (Offset = 0x12, Default 0x00)

Register Bits							
7	6	5	4	3	2	1	0
PWM_OUT[7]	PWM_OUT[6]	PWM_OUT[5]	PWM_OUT[4]	PWM_OUT[3]	PWM_OUT[2]	PWM_OUT[1]	PWM_OUT[0]

PWM Out High (Offset = 0x13, Default 0x00)

Register Bits							
7	6	5	4	3	2	1	0
							PWM_OUT[8]

Name	Bit	Access	Description
PWM_OUT	[7:0]	R/W	The value of the PWM detector. Maximum value is 256 or 100h. If PWM_OUT[7:0] is non-zero PWM_OUT[8] will be zero.

Revision (Offset = 0x1F, Default = 0x02)

Register Bits							
7	6	5	4	3	2	1	0
REV[7]	REV[6]	REV[5]	REV[4]	REV[3]	REV[2]	REV[1]	REV[0]

Name	Bit	Access	Description
REV	[7:0]	R/W	Revision value

Filter Strength (Offset = 0x50, Default = 0x00)

Register Bits							
7	6	5	4	3	2	1	0
						FLTR_STR[1]	FLTR_STR[0]

Name	Bit	Access	Description
FLTR_STR	[1:0]	R/W	Filter Strength

APPLICATION INFORMATION

Recommended Initialization Sequence

The recommended initialization sequence for the device registers is listed below.

1. Set Filter Strength register (offset=50h) to 03h.
2. Set Configuration register (offset=01h) to enable the PWM and the feedback for Bank A, For example writing 09h to the Configuration register, enables PWM and feedback for Bank A. Note the Bank B PWM and feedback need to be configured if Bank B is used, otherwise disable the Bank B feedback by clearing bit 4 and disable the Bank B PWM by clearing bit 1.
3. Configure the Boost Control register (offset=02h) to select the OVP, OCP and FMODE. For example writing 78h to the Boost Control register sets OVP to 40V, OCP to 1.2A and FMODE to 500 kHz.
4. Set the full scale LED current for Bank A and Bank B(if used), by writing to the Current A (offset=05h), and Current B(offset=06) registers. For example writing 14h to the Current A register selects a full scale LED current of 20 mA for Bank A.
5. Set the PWM Sampler Hysteresis to 2 codes by setting Bit 7 of the Current A register. Set the PWM Sampler Lower Bound code to 6 by clearing Bit 6 of the Current A register. Note these settings apply to both Bank A and Bank B. If only Bank B is used, these setting are still necessary when PWM is enabled.
6. Select the current control and enable or disable the LED Bank A and/or B by writing to Control register(offset=00h). For example writing 14h to the Control register select linear current control and enables Bank A.
7. Set the LED brightness by writing to Brightness A (Offset=03h) and Brightness B(Offset=04h) registers. For example writing FFh to Brightness A will set the LED current to 20 mA, with the Current A register set to 14h and the PWM input is high.

PWM Operation

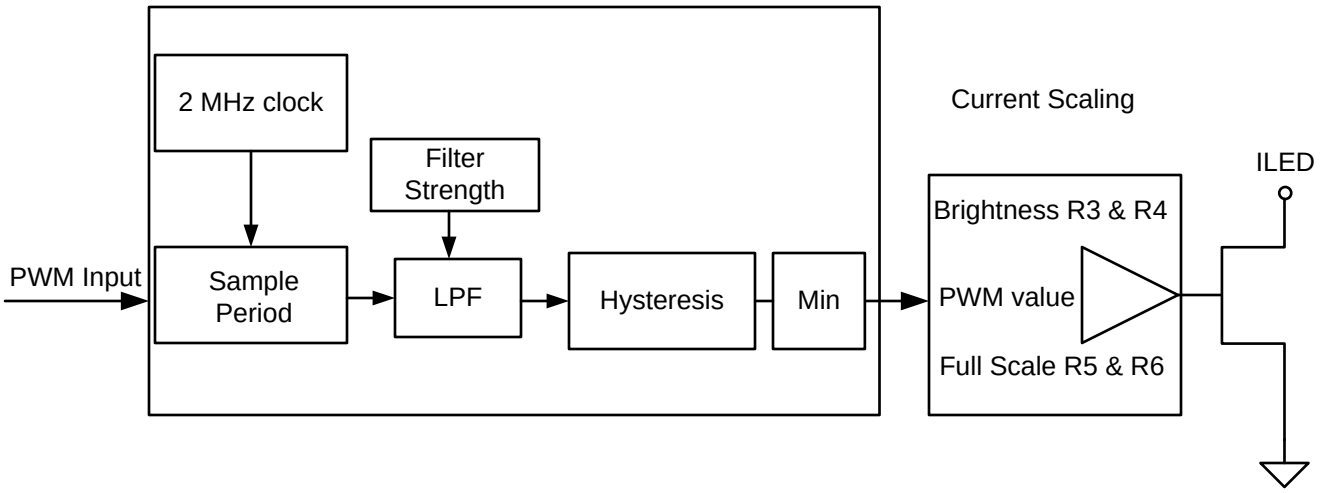


Figure 86. PWM Sampler

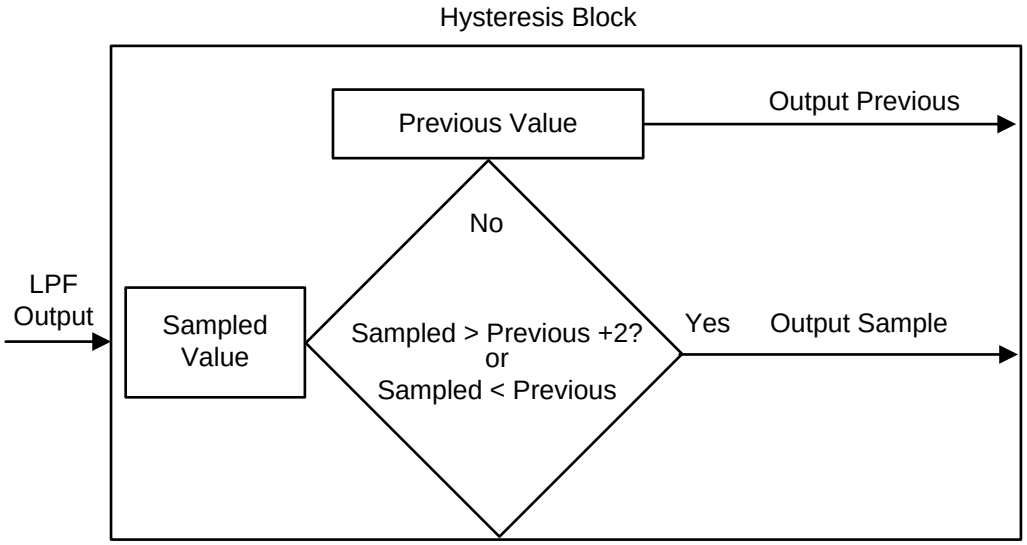


Figure 87. Hysteresis Block (Details)

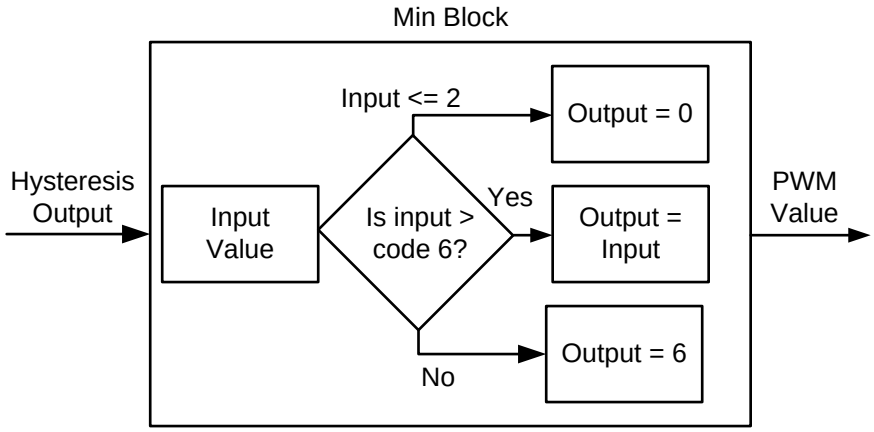


Figure 88. Min Block (Details)

PWM Input

The PWM input can be assigned to any control bank. When assigned to a control bank, the programmed current in the control bank also becomes a function of the duty cycle at the PWM input. The PWM input is sampled by a digital circuit which outputs a brightness code that is equivalent to the PWM input duty cycle. The resultant brightness value is a combination of the maximum current setting, the brightness registers, and the equivalent PWM brightness code.

PWM input Frequency

The specified input frequency of the PWM signal is 10 kHz to 80 kHz. The recommended frequency is 30 kHz or greater. The PWM input sampler will operate beyond those frequency limits. Performance will change based on the input frequency used. It is not recommended to use frequencies outside the specified range. Lower PWM input frequency increases the likelihood that the output of the sampler may change and that a single brightness step may be visible on the screen. This may be visible at low brightness because the step change is large relative to the output level.

Recommended Settings

For best performance of the PWM sampler it is recommended to have a PWM input frequency of at least 30 kHz. The Filter Strength (register 50h) should be set to 03h. The Hysteresis 1 bit should be set in register 05h to 1 when setting the maximum current for bank A. For example if max current is 20 mA, register 05h is set to 14h, change that to 94h for 1 bit hysteresis and a smooth min-to-max brightness transition.

Adjustments to PWM sampler

The digital sampler has controls for hysteresis and minimum output brightness which allow the optimization of sampler output. The default hysteresis mode of the PWM sampler requires detecting a two code change in the input to increase brightness. Reducing the hysteresis to change on 1 code will allow a smoother brightness transition when the brightness control is swept across the screen in a system. The filter strength bits affect the speed of the output transitions from the PWM sampler. A lower bound to the brightness is enabled by default which will limit the minimum output of the PWM sampler to an equivalent code of 6 when the LEDs are turned on. A detected code of 1 will be forced to off. A minimum 2% PWM input duty cycle is recommended. Input duty cycles of 1% or less will cause delayed off to on transitions.

Filter Strength, Register 50h Bits [1:0]

- o Filter Strength controls the amount of sampling cycles that are fed back to the PWM input sampler. A filter strength of 00b allows the output of the PWM sampler to change on every Sample Period. A filter strength of 01b allows the output of the PWM sampler to change every two Sample Periods. A filter strength of 10b allows the output of the PWM sampler to change every four Sample Periods. A filter strength of 11b allows the output of the PWM sampler to change every eight Sample Periods.
- o The effect of setting this value to 11b forces the output of the PWM sampler to change less frequently then lower values. The benefit is this will reduce the appearance of flicker because the output is slower to change. The negative is that the output is slower to change.

Hysteresis 1 bit, Register 05h, Bit 7

- o The default setting for the LM3630A has Bit 7 of register 05h is 0b. This requires the detection of a PWM input change that is at least 3 equivalent codes higher than the present code. If this bit is set to 1b, the hysteresis is turned off and the PWM sampler output is allowed to change by 2 code.
- o Setting this bit to 1b will turn off the 2 code requirement for the PWM sampler output to change. The benefit is the output change will be smoother. The negative is that there may be some PWM input value where the output could change by one code and it might appear as flicker.

Lower Bound Disable, Register 05h, Bit 6

- o The default setting for the LM3630A has Bit 6 of register 05h is 0b. This turns on the lower bound where the minimum output value of the PWM sampler is an equivalent code of 6. If the PWM sampler detects an equivalent code of 0 or 1, the output will be 0 and the LEDs will be off. If the PWM sampler detects an equivalent code of 2 through 6, a current equal to code 6 will be output. Detection of any higher code will output that code conforming to the rules of Hysteresis above.
- o Setting Bit 6 of register 05h to 1b can be used to allow the output to be below an equivalent code 6. The output of the PWM sampler will match the input pulse width conforming to the rules of Hysteresis and equivalent codes 1, 2, 3, 4, and 5 are also allowed. The benefit is the output is allowed to go dimmer than in the default mode. The negative is at the low codes of 1 and 2, the LEDs may not turn on or the LEDs may appear to flicker.
- o Disabling the Lower Bound (05h Bit 6 = 1b) allows the minimum duty cycle to be detected at 0.35% PWM input duty cycle. At 30kHz PWM input frequency, the minimum pulse width required to turn on the LEDs is 0.39% X 33 µS = 129 ns. There is no specified tolerance to this value.

Minimum T_{ON} Pulse Width

The minimum T_{ON} pulse width required to produce a non-zero output is dependent upon the LM3630A settings. The default setting of the LM3630A requires a minimum of 0.78% duty cycle for the output to be turned on. Because the lower bound feature is enabled, a value of 0.78% (equivalent brightness code 2) up to 2.35% (equivalent brightness code 6) will all produce an output equivalent to brightness code 6. At 30 kHz PWM input frequency, the minimum pulse width required to turn on the LEDs is 0.78% X 33uS = 260ns.

Because of the hysteresis on the PWM input, this pulse width may not be sufficient to turn on the LEDs. It is recommended that a minimum pulse width of 2% be used. 2% X 33 µS = 660 ns at 30 kHz input frequency.

Disabling the Lower Bound as described will allow a smaller minimum pulse width.

Maximum Power Output

The LM3630A's maximum output power is governed by two factors: the peak current limit (I_{CL} = 1.2A max.), and the maximum output voltage (V_{OVP} = 40V min.). When the application causes either of these limits to be reached it is possible that the proper current regulation and matching between LED current strings will not be met.

In the case of a peak current limited situation, when the peak of the inductor current hits the LM3630A's current limit the NFET switch turns off for the remainder of the switching period. If this happens, each switching cycle the LM3630A begins to regulate the peak of the inductor current instead of the headroom across the current sinks. This can result in the dropout of the feedback-enabled current sinks and the current dropping below its programmed level.

The peak current in a boost converter is dependent on the value of the inductor, total LED current (IOUT), the output voltage (VOUT) (which is the highest voltage LED string + 0.3V regulated headroom voltage), the input voltage VIN, and the efficiency (Output Power/Input Power). Additionally, the peak current is different depending on whether the inductor current is continuous during the entire switching period (CCM) or discontinuous (DCM) where it goes to 0 before the switching period ends.

For Continuous Conduction Mode the peak inductor current is given by:

$$IPEAK = \frac{IOUT \times VOUT}{VIN \times efficiency} + \left[\frac{VIN}{2 \times fsw \times L} \times \left(1 - \frac{VIN \times efficiency}{VOUT}\right)\right] \quad (4)$$

For Discontinuous Conduction Mode the peak inductor current is given by:

$$IPEAK = \sqrt{\frac{2 \times IOUT}{fsw \times L \times efficiency} \times \left(VOUT - VIN \times efficiency\right)} \quad (5)$$

To determine which mode the circuit is operating in (CCM or DCM) it is necessary to perform a calculation to test whether the inductor current ripple is less than the anticipated input current (IIN). If ΔIL is < then IIN then the device will be operating in CCM. If ΔIL is > IIN then the device is operating in DCM.

$$\frac{IOUT \times VOUT}{VIN \times efficiency} > \frac{VIN}{fsw \times L} \times \left(1 - \frac{VIN \times efficiency}{VOUT}\right) \quad (6)$$

Typically at currents high enough to reach the LM3630A's peak current limit, the device will be operating in CCM.

The following figures show the output current and output voltage derating for a 10 µH and a 22 µH inductor, at switch frequencies of 500 kHz and 1 MHz. A 10 µH will typically be a smaller device with lower on resistance, but the peak currents will be higher. A 22 µH provides for lower peak currents, but to match the DC resistance of a 10 µH requires a larger sized device.

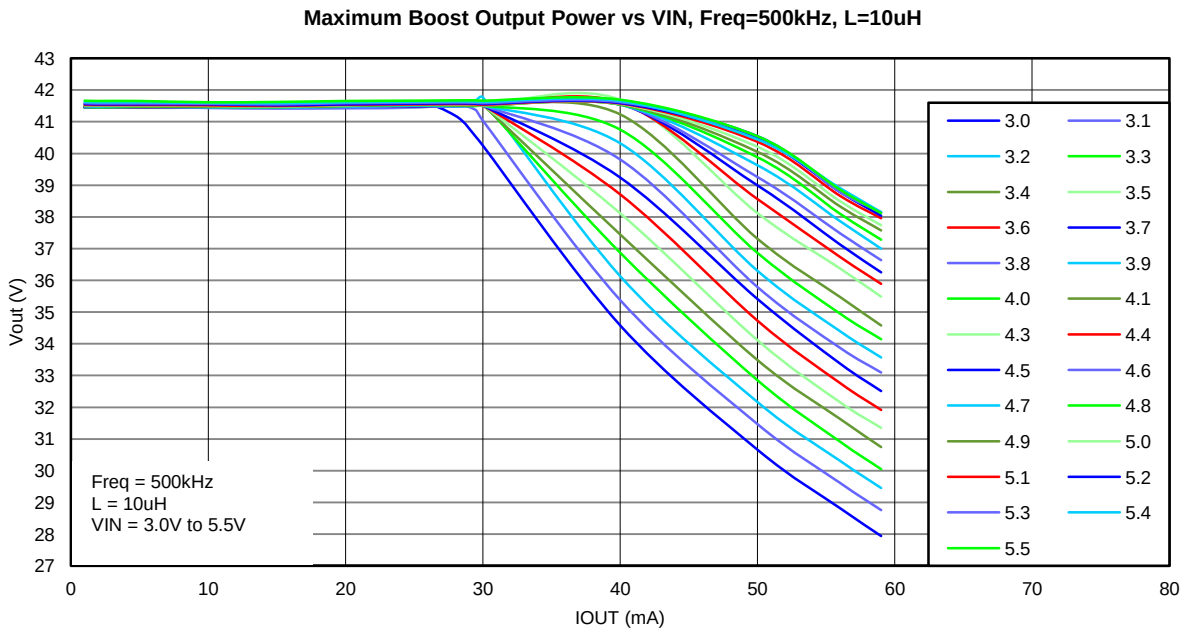


Figure 89.

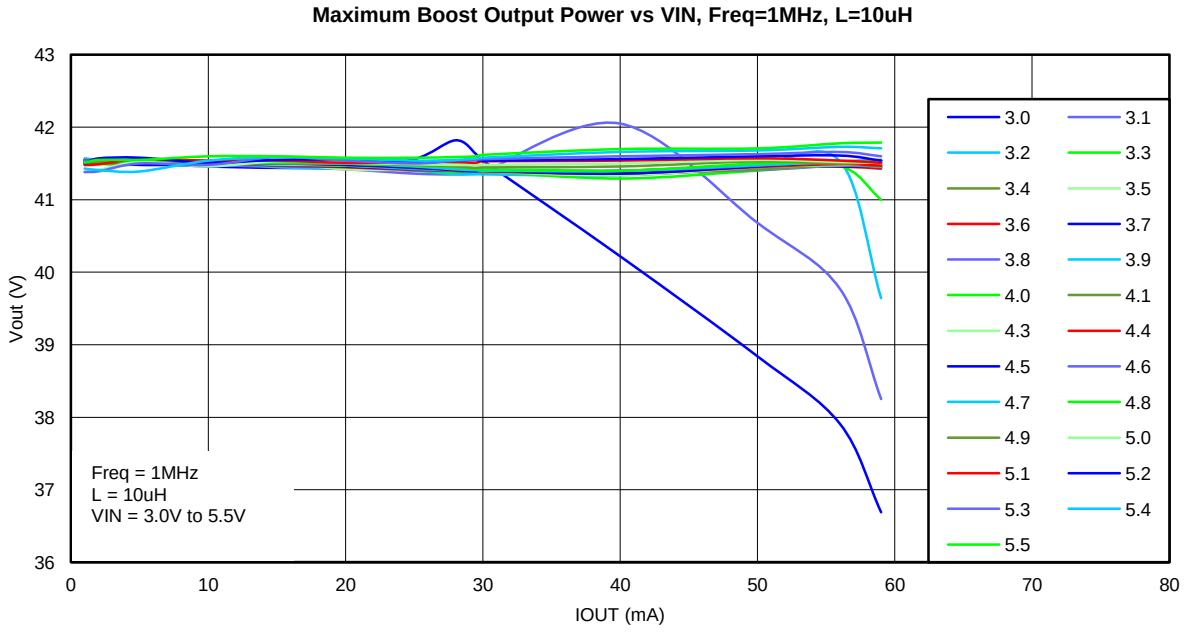


Figure 90.

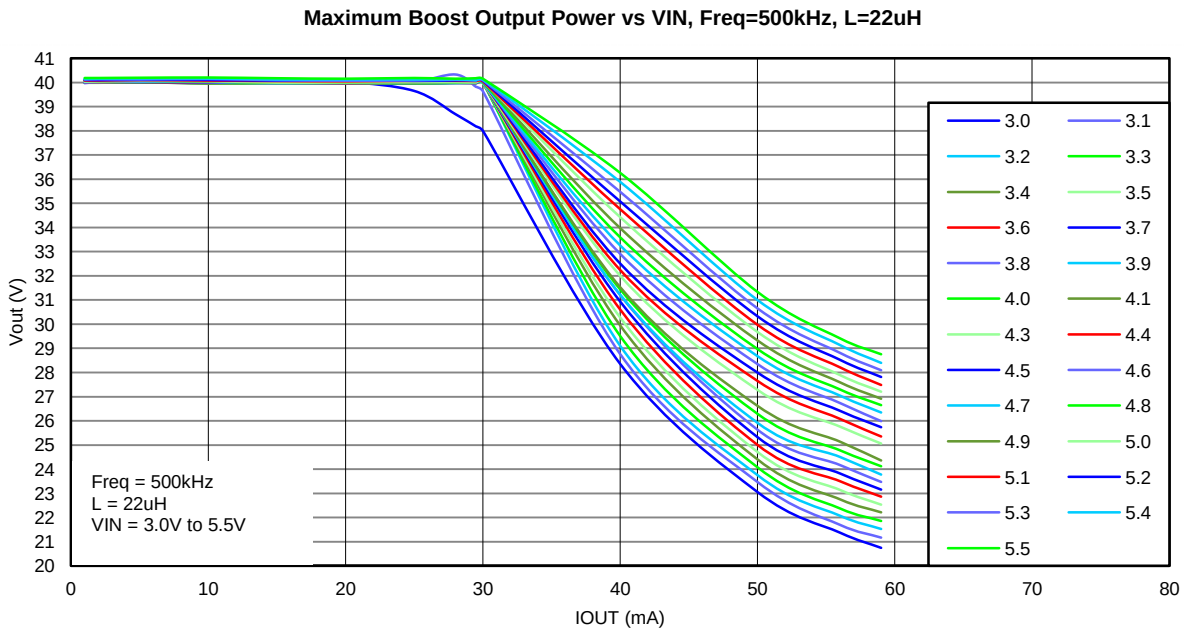


Figure 91.

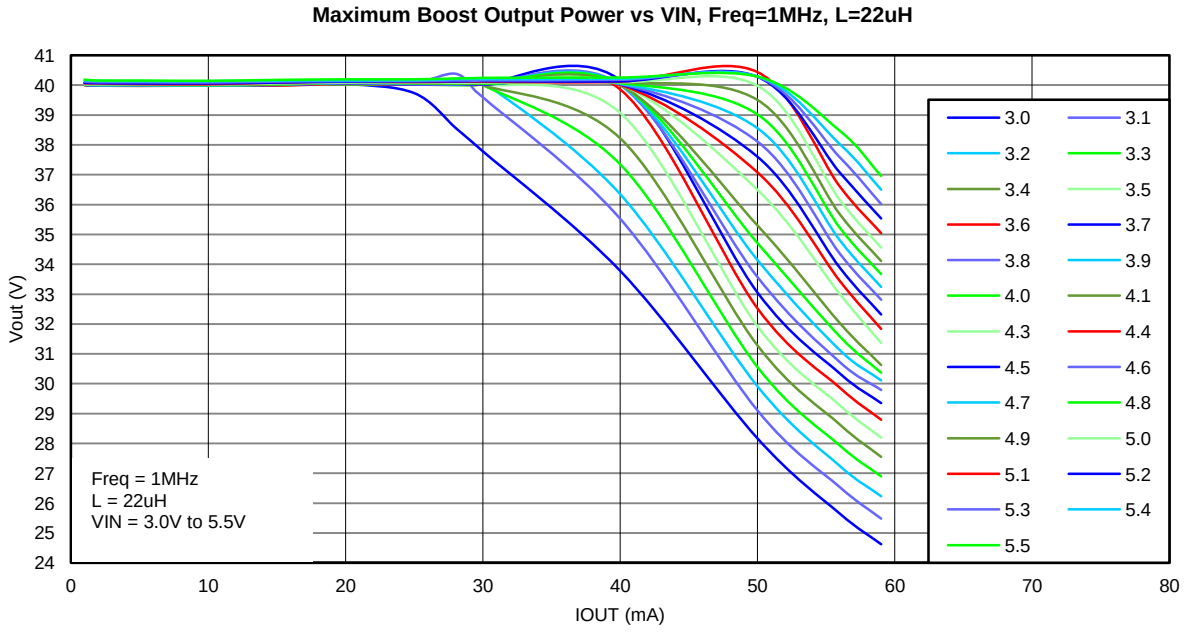


Figure 92.

Inductor Selection

The LM3630A is designed to work with a 10 µH to 22 µH inductor. When selecting the inductor, ensure that the saturation rating for the inductor is high enough to accommodate the peak inductor current . The following equation calculates the peak inductor current based upon LED current, V_{IN}, V_{OUT}, and Efficiency.

$$I_{PEAK} = \frac{I_{LED}}{\eta} \times \frac{V_{OUT}}{V_{IN}} + \Delta I_L \quad (7)$$

where:

$$\Delta I_L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}} \quad (8)$$

When choosing L, the inductance value must also be large enough so that the peak inductor current is kept below the LM3630A's switch current limit. This forces a lower limit on L given by the following equation.

$$L > \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times f_{SW} \times V_{OUT} \times \left(I_{SW\_MAX} - \frac{I_{LED\_MAX} \times V_{OUT}}{\eta \times V_{IN}} \right)} \quad (9)$$

I_{SW_MAX} is given in the Electrical Table, efficiency (η) is shown in theTYPICAL PERFORMANCE CHARACTERISTICS , and f_{SW} is typically 500 kHz or 1 MHz.

Table 4. Inductors

Manufacturer	Part Number	Value	Size	Current Rating	DC Resistance
TDK	VLF4014ST-100M1R0	10 µH	3.8 mm x 3.6 mm x 1.4 mm	1A	0.22 Ω
TDK	VLF302512MT-220M	22 µH	3 mm x 2.5 mm x 1.2 mm	0.43A	0.583 Ω

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3630ATME	ACTIVE	DSBGA	YFQ	12	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	D6	Samples
LM3630ATMX	ACTIVE	DSBGA	YFQ	12	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	D6	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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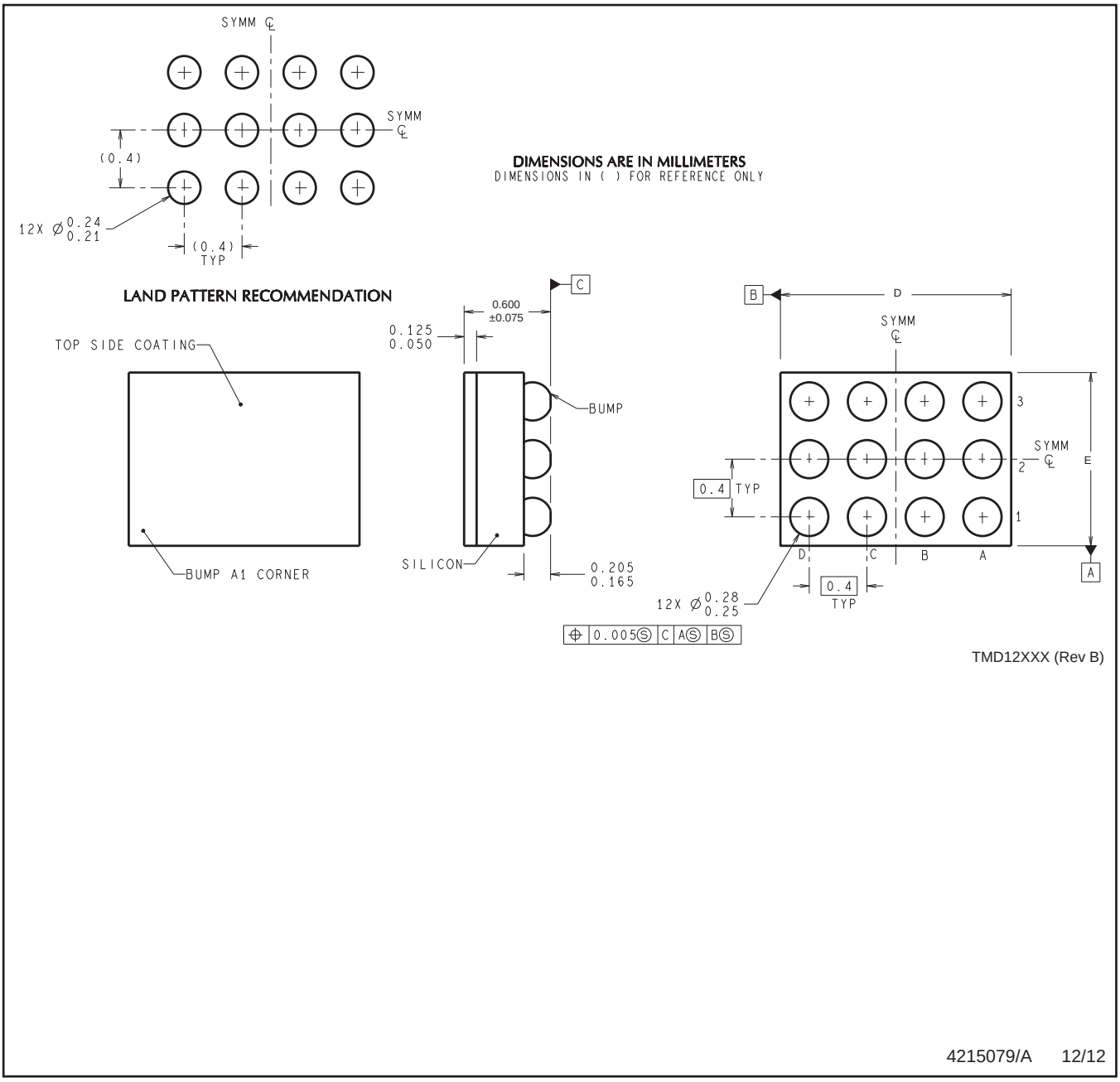

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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