LM3697 高效三灯串白光 LED 驱动器

1 特性

- 可驱动三个并联高压 LED 灯串，用于显示屏和键盘照明
- 高压灯串的输入电压高达 40V，效率高达 90%
- 灌电流高达 30mA
- 11 位可配置调光分辨率
- 用于内容可调亮度控制 (CABC) 的 PWM 输入
- 完全可配置的 LED 分组和控制
- 集成 1A/40V MOSFET
- 自适应升压输出至 LED 电压
- 可选 500kHz 和 1MHz 开关频率
- 四种可配置过压保护阈值（16V、24V、32V 和 40V）
- 过流保护
- 热关断保护
- 总解决方案尺寸为 $29mm^2$

2 应用

- 用于智能手机照明的电源
- 显示屏、键盘和指示灯照明

3 说明

LM3697 11 位 LED 驱动器以高达 90% 的传送效率为 1，2 或 3 串联 LED 灯串提供高性能背光调光功能。具有集成 1A，40V MOSFET 的升压转换器自动调节至 LED 正向电压，以最大限度地减少净空电压并有效提升 LED 效率。

LM3697 是一款针对智能手机内背光或键区 LED 的高效三灯串电源。高压电感升压转换器为三个串联 LED 灯串提供电源，用于实现显示屏背光和键盘功能（HVLED1、HVLED2 和 HVLED3）。

附加功能包括用于内容可调背光控制的脉宽调制 (PWM) 控制输入，该功能可控制所有高电压电流阱。

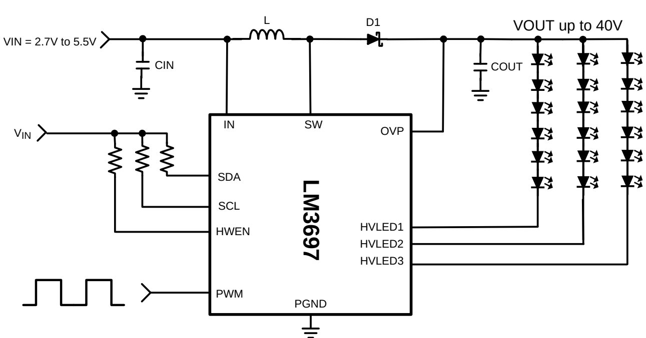
LM3697 可通过兼容 I^2C 的接口实现完全可配置。该器件的工作输入电压范围为
2.7V 至 5.5V，温度范围为 −40°C 至 +85°C。

器件信息(1)

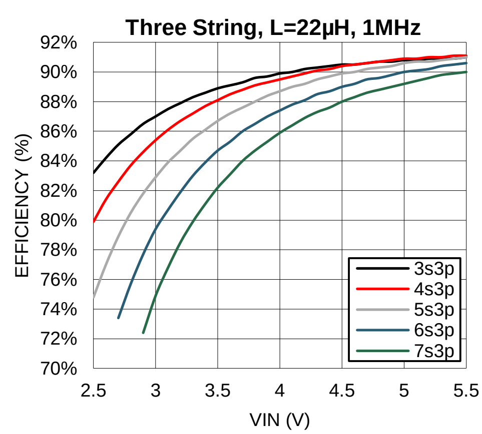
订货编号	封装	封装尺寸（最大值）
LM3697	DSBGA (12)	1.64mm × 1.29mm

(1) 如需了解所有可用封装，请参阅产品说明书书末尾的可订购产品附录。

简化原理图



升压效率



English Data Sheet: SNOSCS2

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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (October 2015) to Revision D	Page
• Changed Table 2 revision register POWER-ON RESET value from 0x00 to 0x01, change silicon revision value in Table 3 from 0000 to 0001	17

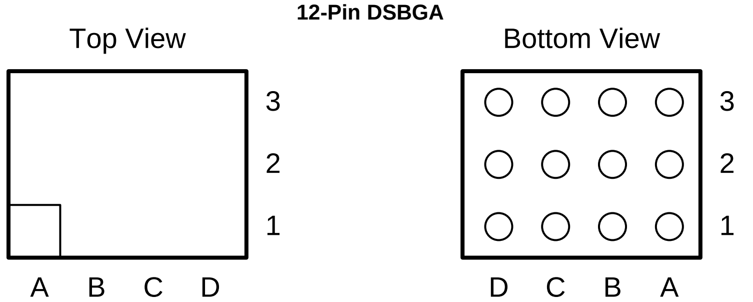
Changes from Revision B (April 2014) to Revision C	Page
• 已更改 *器件信息*的格式；已添加脚注和“MAX”	1
• Changed *Handling Ratings* table to *ESD Ratings* table format; move storage temp to *Abs Max* table	5
• Added additional *Thermal Information*	5
• Added subsection *High-Speed Mode*	16

Changes from Revision A (December 2013) to Revision B	Page
• 已更改 为全新 TI 数据表标准；已添加处理额定值表；分别为 I_{HVLED} 和 I_{MATCH_HV} 新增了 2 项和 1 项环境温度规范	1
• Changed title from Pin Configurations to Terminal Functions and all references from "pins" to "terminals"	4
• Changed change "terminal" back to "pin" per latest documentation standard; add "Type" column to Pin Functions table	4
• Changed Timing information from Elec Char table Timing Requirements	7
• Changed Functional Description section to Detailed Description section	9
• Changed Applications Information section to Application and Implementation	22
• Changed Typical Characteristics from own section into subsection of Specifications	24
• Added new Power Supply Recommendations section	32
• Changed Layout section to include separate Layout Example	33
• 已添加 全新的器件和文档支持部分，以及机械封装和可订购信息段落	37

Changes from Original (November 2013) to Revision A **Page**

5 Pin Configuration and Functions

YFQ Package
12-Pin DSBGA



Pin Functions

PIN		TYPE	DESCRIPTION
NUMBER	NAME		
A1	PWM	Input	PWM brightness control input for CABC operation. PWM is a high-impedance input and cannot be left floating, if not used connect to GND.
A2	SDA	I/O	Serial data connection for I^2C-compatible interface.
A3	HWEN	Input	Hardware enable input. Drive this pinl high to enable the device. Drive this pin low to force the device into a low power shutdown. HWEN is a high-impedance input and cannot be left floating.
B1	HVLED1	Input	Input pin to high-voltage current sink 1 (40 V maximum). The boost converter regulates the minimum of HVLED1, HVLED2 and HVLED3 to V_{HR}.
B2	SCL	Input	Serial clock connection for I^2C-compatible interface.
B3	IN	Input	Input voltage connection. Bypass IN to GND with a minimum 2.2-µF ceramic capacitor.
C1	HVLED2	Input	Input pin to high-voltage current sink 2 (40 V maximum). The boost converter regulates the minimum of HVLED1, HVLED2 and HVLED3 to V_{HR}.
C2	GND	GND	Ground
C3	GND	GND	Ground
D1	HVLED3	Input	Input pin to high-voltage current sink 3 (40 V maximum). The boost converter regulates the minimum of HVLED1, HVLED2 and HVLED3 to V_{HR}.
D2	OVP	Input	Overvoltage sense input. Connect OVP to the positive terminal of the inductive boost's output capacitor (COUT).
D3	SW	Output	Drain connection for the internal NFET. Connect SW to the junction of the inductor and the Schottky diode anode.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
V_{IN} to GND	−0.3	6	V
V_{SW}, V_{OVP}, V_{HVLED1}, V_{HVLED2}, V_{HVLED3} to GND	−0.3	45	V
V_{SCL}, V_{SDA}, V_{PWM} to GND	−0.3	6	V
V_{HWEN} to GND	−0.3	6	V
Continuous power dissipation	Internally Limited		
Junction temperature (T_{J-MAX})		150	°C
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
V_{IN} to GND	2.7	5.5	V
V_{SW}, V_{OVP}, V_{HVLED1}, V_{VHLED2}, V_{HVLED3} to GND	0	40	V
Junction temperature, T_J(1)(2)	−40	125	°C

(1) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J= 140°C (typical) and disengages at T_J= 125°C (typical).
(2) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (R_{\theta JA} \times PD\text{-}MAX)$.

6.4 Thermal Information

THERMAL METRIC(1)		LM3697 YFQ (DSBGA) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	92.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics*.

6.5 Electrical Characteristics

Limits apply over the full operating ambient temperature range (−40°C ≤ T_A ≤ 85°C) and V_{IN} = 3.6 V, unless otherwise specified.(1)(2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{SHDN}	Shutdown current	2.7 V ≤ V_{IN} ≤ 5.5 V, HWEN = GND				3	µA
		T_A = 25°C			1		
I_{LED_MIN}	Minimum LED current	Full-scale current = 20.2 mA Exponential mapping, T_A = 25°C			6		µA
T_{SD}	Thermal shutdown				140		°C
	Hysteresis				15		
BOOST CONVERTER							
$I_{HVLED(1/2/3)}$	Output current regulation (HVLED1, HVLED2, HVLED3)	Full-scale current= 20.2 mA, Exponential mapping, Brightness Code = maximum	2.7 V ≤ V_{IN} ≤ 5.5 V	18.38	20.2	22.02	mA
		Full-scale current= 20.2 mA, Exponential mapping, Brightness Code = maximum HVLED1 Bank A, HVLED2/3 Bank B	T_A = 25°C	–3.4%	±2 %	3.2%	
			T_A = 25°C 3 V ≤ V_{IN} ≤ 4.5 V	–3.6%		3.4%	
			T_A = 25°C		±2 %		
I_{MATCH_HV}	HVLED1 to HVLED2 or HVLED3 matching (3)	Exponential mapping, auto headroom off, PWM Off, HVLED1/2/3 Bank A	2.7 V ≤ V_{IN} ≤ 5.5 V I_{LED} = 20.2 mA	−2.5%		2.5%	
			T_A = 25°C I_{LED} = 20.2 mA	–2%		1.7%	
			2.7 V ≤ V_{IN} ≤ 5.5 V I_{LED} = 500 µA	–8.5%		8.5%	
V_{REG_CS}	Regulated current sink headroom voltage	Auto-headroom off, T_A = 25°C			400		mV
V_{HR_MIN}	Minimum current sink headroom voltage for HVLED current sinks	I_{LED} = 95% of nominal, Full-scale current = 20.2 mA				275	mV
		I_{LED} = 95% of nominal, Full-scale current = 20.2 mA , T_A = 25°C			190		
R_{DSON}	NMOS switch on resistance	I_{SW} = 500 mA, T_A = 25°C			0.3		Ω
I_{CL_BOOST}	NMOS switch current limit			880		1120	mA
		T_A = 25°C			1000		
V_{OVP}	Output overvoltage protection	ON Threshold OVP select bits = 11	2.7 V ≤ V_{IN} ≤ 5.5 V	38.75		41.1	V
			T_A = 25°C		40		
		Hysteresis	T_A = 25°C		1		
f_{SW}	Switching frequency	Boost frequency select bit = 0	2.7 V ≤ V_{IN} ≤ 5.5 V	450		550	kHz
			T_A = 25°C		500		
		Boost frequency select bit = 1	2.7 V ≤ V_{IN} ≤ 5.5 V	900		1100	
			T_A = 25°C		1000		
D_{MAX}	Maximum duty cycle	T_A = 25°C			94%		
HWEN INPUT							
V_{HWEN_L}	Logic low	2.7 V ≤ V_{IN} ≤ 5.5 V		0		0.4	V
V_{HWEN_H}	Logic high	2.7 V ≤ V_{IN} ≤ 5.5 V		1.2		V_{IN}	

(1) All voltages are with respect to the potential at the GND pin.
(2) Minimum and Maximum limits are verified by design, test, or statistical analysis. Typical numbers are not verified, but do represent the most likely norm. Unless otherwise specified, conditions for typical specifications are: V_{IN} = 3.6 V and T_A = 25°C.
(3) LED current sink matching in the high-voltage current sinks (HVLED1 through HVLED3) is given as the maximum matching value between any two current sinks, where the matching between any two high voltage current sinks (X and Y) is given as (I_{HVLEDX} (or I_{HVLEDY}) × $I_{AVE(X-Y)}$)/($I_{AVE(X-Y)}$) × 100. In this test all three HVLED current sinks are assigned to Bank A.

Electrical Characteristics (continued)

Limits apply over the full operating ambient temperature range (−40°C ≤ T_A ≤ 85°C) and V_{IN} = 3.6 V, unless otherwise specified.(1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM INPUT						
V_{PWM_L}	Input logic low	2.7 V ≤ V_{IN} ≤ 5.5 V	0		0.4	V
V_{PWM_H}	Input logic high	2.7V ≤ V_{IN} ≤ 5.5 V	1.31		V_{IN}	V
t_{PWM}	Minimum PWM input pulse	2.7 V ≤ V_{IN} ≤ 5.5 V, PWM zero detect enabled			0.75	µs
I^2C-COMPATIBLE VOLTAGE SPECIFICATIONS (SCL, SDA)						
V_{IL}	Input logic low	2.7 V ≤ V_{IN} ≤ 5.5 V	0		0.4	V
V_{IH}	Input logic high	2.7 V ≤ V_{IN} ≤ 5.5 V	1.29		V_{IN}	V
V_{OL}	Output logic low (SDA)	2.7 V ≤ V_{IN} ≤ 5.5 V, I_{LOAD} = 3 mA			400	mV

6.6 Timing Requirements

			MIN	NOM	MAX	UNIT
I^2C-COMPATIBLE TIMING SPECIFICATIONS (SCL, SDA)(1)						
t_1	SCL (clock period)	2.7 V ≤ V_{IN} ≤ 5.5 V	2.5			µs
t_2	Data In set-up time to SCL high	2.7 V ≤ V_{IN} ≤ 5.5 V	100			ns
t_3	Data out stable after SCL low	2.7 V ≤ V_{IN} ≤ 5.5 V	0			ns
t_4	SDA low set-up time to SCL low (start)	2.7 V ≤ V_{IN} ≤ 5.5 V	100			ns
t_5	SDA high hold time after SCL high (stop)	2.7 V ≤ V_{IN} ≤ 5.5 V	100			ns
INTERNAL POR THRESHOLD AND HWEN TIMING SPECIFICATION						
V_{POR}	POR reset release voltage threshold	V_{IN} ramp time = 100 µs	1.7		2.1	V
		V_{IN} ramp time = 100 µs, T_A = 25°C		1.9		V
t_{HWEN}	First I^2C start pulse after HWEN high	2.7 V ≤ V_{IN} ≤ 5.5 V, POR reset complete			20	µs
		POR reset complete, T_A = 25°C		5.0		µs

(1) SCL and SDA must be glitch-free in order for proper brightness control to be realized.

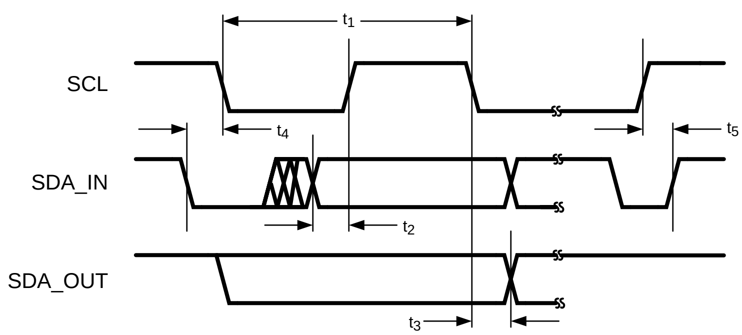


Figure 1. I^2C-Compatible Interface Timing

6.7 Typical Characteristics

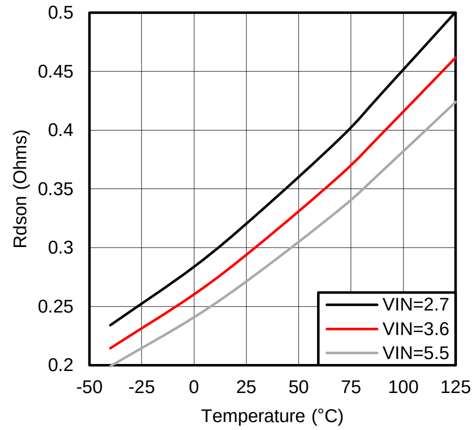


Figure 2. R_{DSON} vs Temperature

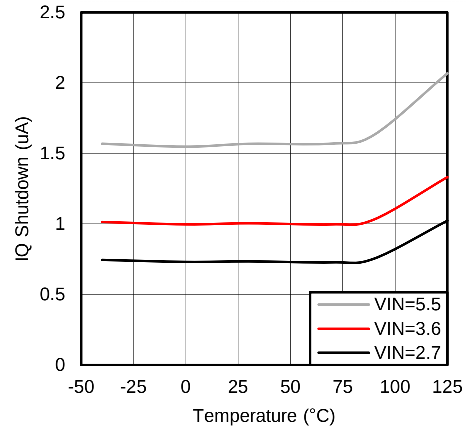


Figure 3. I_Q Shutdown vs Temperature

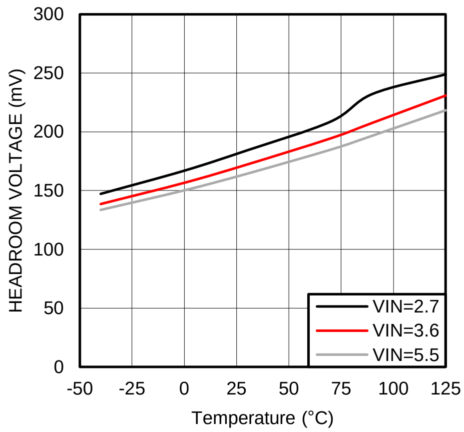


Figure 4. V_{HR_MIN} vs Temperature

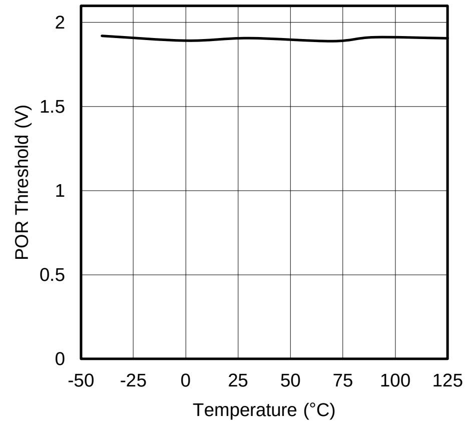


Figure 5. POR Threshold vs Temperature

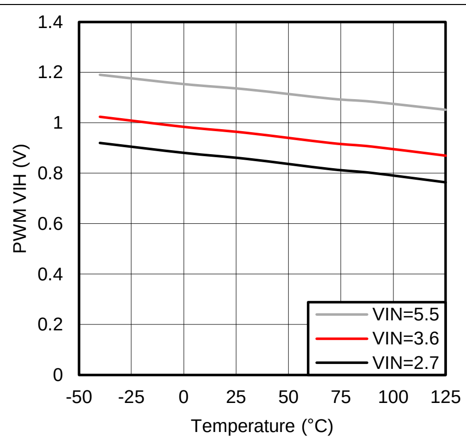


Figure 6. PWM V_{IH} vs Temperature

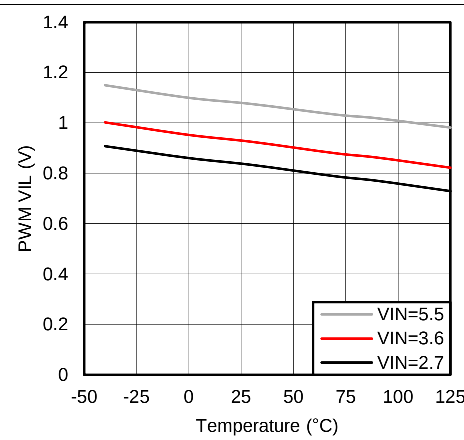


Figure 7. PWM V_{IL} vs Temperature

7 Detailed Description

7.1 Overview

The LM3697 provides the power for three high-voltage LED strings. The three high-voltage LED strings are powered from an integrated boost converter. The device is configured over an I^2C-compatible interface. The LM3697 provides a Pulse Width Modulation (PWM) input for content adjustable brightness control.

7.1.1 PWM Input

The PWM input can be assigned to either of the high-voltage control banks. When assigned to a control bank, the programmed current in the control bank becomes a function of the duty cycle (D_{PWM}) at the PWM input and the control bank brightness setting. When PWM is disabled, D_{PWM} is equal to one.

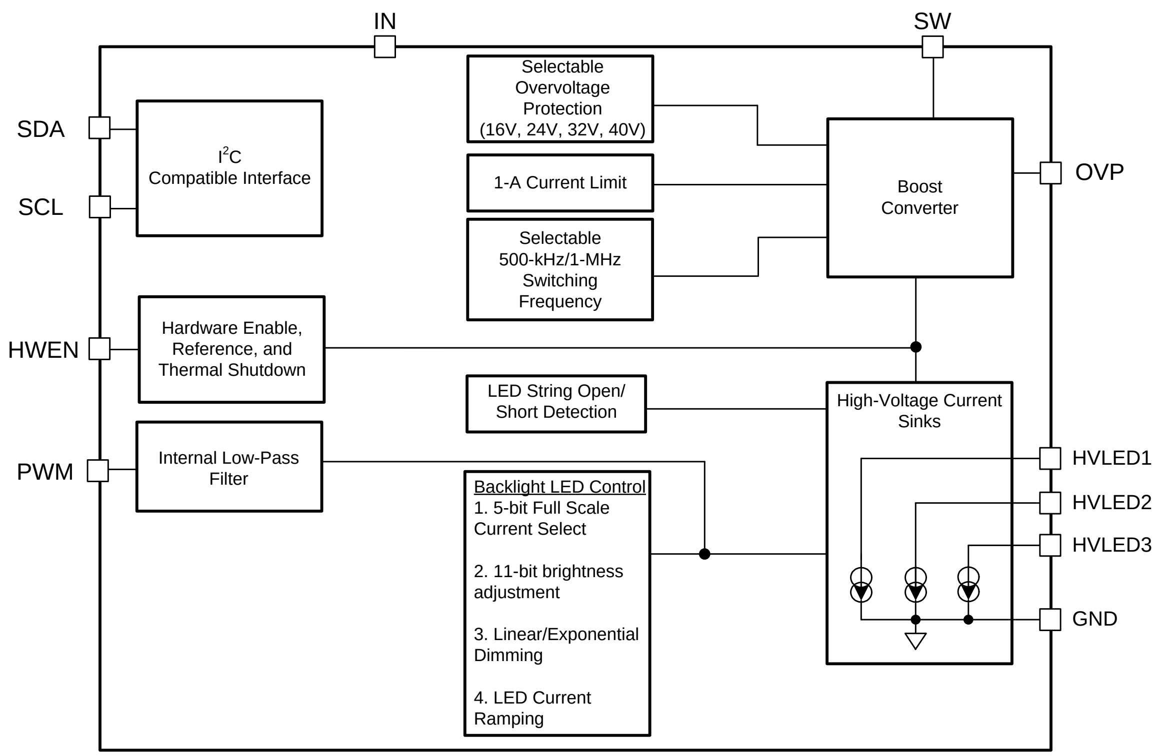
7.1.2 HWEN Input

HWEN is the global hardware enable to the LM3697. HWEN must be pulled high to enable the device. HWEN is a high-impedance input so it cannot be left floating. When HWEN is pulled low the LM3697 is placed in shutdown, and all the registers are reset to their default state.

7.1.3 Thermal Shutdown

The LM3697 contains a thermal shutdown protection. In the event the die temperature reaches 140°C (typical), the boost and current sink outputs shut down until the die temperature drops to typically 125°C (typical).

7.2 Functional Block Diagram



7.3 Feature Descriptions

7.3.1 High-Voltage LED Control

7.3.1.1 High-Voltage Boost Converter

The high-voltage boost converter provides power for the three high-voltage current sinks (HVLED1, HVLED2, and HVLED3). The boost circuit operates using a 4.7-µH to 22-µH inductor and a 1-µF output capacitor. The selectable 500-kHz or 1-MHz switching frequency allows for use of small external components and provides for high boost-converter efficiency. HVLED1, HVLED2, and HVLED3 feature an adaptive current regulation scheme where the feedback point (HVLED1, HVLED2, and HVLED3) regulates the LED headroom voltage V_{HR_MIN}. When there are different voltage requirements in the high-voltage LED strings (string mismatch), the LM3697 regulates the feedback point of the highest voltage string to V_{HR_MIN} and drop the excess voltage of the lower voltage string across the lower strings current sink.

7.3.1.2 High-Voltage Current Sinks (HVLED1, HVLED2 and HVLED3)

HVLED1, HVLED2, and HVLED3 control the current in the high-voltage LED strings as configured by Control Bank A or B. Each Control Bank has 5-bit full-scale current programmability and 11-bit brightness control. Assignment of the high-voltage current sinks to control bank is done through the HVLED Current Sink Output Configuration register (see Table 5).

7.3.1.3 High-Voltage Current String Biasing

Each high-voltage current string can be powered from the LM3697's boost output (COUT) or from an external source. The feedback enable bits (HVLED Current Sink Feedback Enables register bits [2:0]) determine where the high-voltage current string anodes connect. When set to '1' (default) the high-voltage current sink inputs are included in the boost feedback loop. This allows the boost converter to adjust its output voltage in order to maintain the LED headroom voltage V_{HR_MIN} at the current sink input.

When powered from alternate sources the feedback enable bits must be set to '0'. This removes the particular current sink from the boost feedback loop. In these configurations the application must ensure that the headroom voltage across the high-voltage current sink is high enough to prevent the current sink from going into dropout (see the *Typical Characteristics* for data on the high-voltage LED current vs V_{HR_MIN}).

Setting the HVLED Current Sink Feedback Enables register bits also determines triggering of the shorted high-voltage LED String Fault flag (see the *Fault Flags/Protection Features* section).

7.3.2 Boost Switching-Frequency Select

The LM3697's boost converter has two switching frequency settings. The switching frequency setting is controlled via the Boost Frequency Select bit (bit 0 in the Boost Control register). Operating at the 500-kHz switching frequency results in better efficiency under lighter load conditions due to the decreased switching losses. In this mode the inductor must be between 10 µH and 22 µH. Operating at the 1-MHz switching frequency results in better efficiency under higher load conditions resulting in lower conduction losses in the MOSFETs and inductor. In this mode the inductor can be between 4.7 µH and 22 µH.

7.3.3 Automatic Switching Frequency Shift

The LM3697 has an automatic frequency select mode (bit 3 in the Boost Control register) to optimize the frequency vs load dependent losses. In Auto-Frequency mode the boost converter switching frequency is changed based on the high-voltage LED current. The threshold (Control A/B brightness code) at which the frequency switchover occurs is configurable via the Auto-Frequency Threshold register. The Auto-Frequency Threshold register contains an 8-bit code which is compared to the 8 MSB's of the brightness code. When the brightness code is greater than the Auto-Frequency Threshold value the boost converter switching frequency is 1 MHz. When the brightness code is less than or equal to the Auto-Frequency Threshold register the boost converter switching frequency is 500 kHz.

Figure 8 illustrates the LED efficiency improvement (3p5s LED configuration with a 4.7-µH inductor) when the Auto-Frequency feature is enabled. When the LED brightness is less than or equal to 0x6C, the switching frequency is 500 kHz, and it improves the LED efficiency by up to 6%. When the LED brightness is greater than 0x6C, the switching frequency is 1 MHz, and it improves LED efficiency by up to 2.2%.

Feature Descriptions (continued)

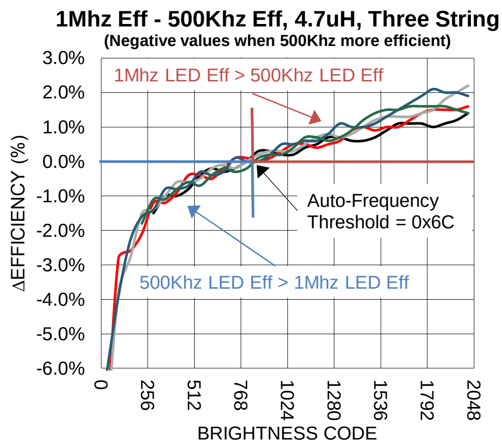


Figure 8. Auto-Frequency Boost Efficiency Improvement Illustration

Table 1 summarizes the general recommendations for Auto-Frequency Threshold setting vs Inductance values and LED string configurations. These are general recommendations — the optimum Auto-Frequency Threshold setting must be evaluated for each application.

Table 1. Auto-Frequency Threshold Settings

	THREE STRING			TWO STRING		
INDUCTOR	AUTO-FREQUENCY THRESHOLD	PEAK EFFICIENCY IMPROVEMENT	PEAK CONFIGURATION	AUTO-FREQUENCY THRESHOLD	PEAK EFFICIENCY IMPROVEMENT	PEAK CONFIGURATION
4.7 µH	6C	2.2%	3p5s	AC	1.1%	2p6s
10 µH	74	1.7%	3p4s	B4	1.3%	2p5s
22 µH	7C	0.7%	3p3s	BC	0.7%	2p4s

7.3.4 Brightness Register Current Control

The LM3697 features Brightness Register Current Control for simple user-adjustable current control set by writing directly to the appropriate Control Bank Brightness Registers. The current for Control Banks A and B is a function of the full-scale LED current, the 11-bit code in the respective brightness register, and the PWM input duty cycle (if PWM is enabled). The Control A/B brightness must always be written with LSB's first and MSB's last.

7.3.4.1 8-Bit Control (Preferred)

The preferred operating mode is to control the high-voltage LED brightness by setting the Control Bank LSB register (3 LSB's) to zero and using only the Control Bank MSB register (8 MSB's). In this mode the LM3697 controls the 3 LSB's to ramp the high-voltage LED current using all 11-bits.

7.3.4.2 11-Bit Control

In this mode of operation, both Control Bank LSB and MSB registers must be written whenever a change in Brightness is required. The high-voltage LED current will not change until the Control Bank MSB register is written. If the brightness change affects only the 3 LSB's, the Control Bank MSB register (8 MSB's) must be re-written to change the high-voltage LED current.

7.3.5 PWM Control

The LM3697's PWM input can be enabled for Control Banks A or B (see Table 14). Once enabled, the LED current becomes a function of the code in the Control Bank Brightness Configuration Register and the PWM input-duty cycle.

The PWM input accepts a logic level voltage and internally filters it to an analog control voltage. This results in a linear response of duty cycle to current, where 100% duty cycle corresponds to the programmed brightness code multiplied by the Full-Scale Current setting.

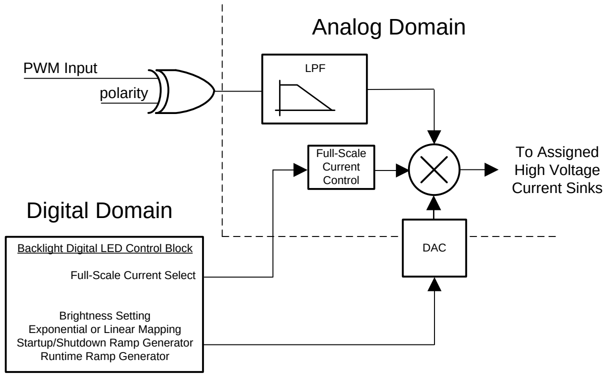


Figure 9. PWM Input Architecture

7.3.5.1 PWM Input Frequency Range

The usable input frequency range for the PWM input is governed on the low end by the cutoff frequency of the internal low-pass filter (540 Hz, Q = 0.33) and on the high end by the propagation delays through the internal logic. For frequencies below 2 kHz the current ripple begins to become a larger portion of the DC LED current. Additionally, at lower PWM frequencies the boost output voltage ripple increases, causing a non-linear response from the PWM duty cycle to the average LED current due to the response time of the boost. For the best response of current vs. duty cycle, the PWM input frequency must be kept between 2 kHz and 100 kHz.

7.3.5.2 PWM Input Polarity

The PWM Input can be set for active low polarity, where the LED current is a function of the negative duty cycle. This is set via the PWM Configuration register (see Table 14).

7.3.5.3 PWM Zero Detection

The LM3697 incorporates a feature to detect when the PWM input is near zero. After the near zero pulse width has been detected the PWM pulse must be greater than t_{PWM} to affect the HVLED output current (see *Electrical Characteristics*). Bit 3 in the PWM Configuration register is used to disable this feature.

7.3.6 Start-up/Shutdown Ramp

The high-voltage LED start-up and shutdown ramp times are independently configurable in the start-up/shutdown transition time Register (see Table 6). There are 16 different start-up and 16 different shutdown times. The start-up times can be programmed independently from the shutdown times, but each Control bank is not independently configurable.

The start-up ramp time is from when the Control Bank is enabled to when the LED current reaches its initial set point. The shutdown ramp time is from when the Control Bank is disabled to when the LED current reaches 0.

7.3.7 Run-Time Ramp

Current ramping from one brightness level to the next is programmed via the Control A and B Run-Time Ramp Time Register (see Table 7). There are 16 different ramp-up times and 16 different ramp-down times. The ramp-up time can be programmed independently from the ramp-down time, but each Control Bank cannot be independently programmed. For example, programming a ramp-up or ramp-down time is a global setting for all high-voltage LED Control Banks.

7.3.8 High-Voltage Control A and B Ramp Select

The LM3697 provides three options for Control A and B ramp times (see Table 8). When the Run-time Ramp Select bits are set to 00, the control bank uses both the Start-up/Shutdown and Run-time ramp times. When the Run-time Ramp Select bits are set to 01, the control bank uses the Start-up/Shutdown ramp times for both start-up/shutdown and run-time. When the Run-time Ramp Select bits are set to 1x the control bank uses a zero µsec run-time ramp.

7.4 Device Functional Modes

7.4.1 LED Current Mapping Modes

All control banks can be programmed for either exponential or linear mapping modes (see Figure 10 and Figure 11). These modes determine the transfer characteristic of backlight code to LED current. Independent mapping of Control Banks A and B is not allowed: both banks uses the same mapping mode.

7.4.1.1 Exponential Mapping

In Exponential Mapping Mode the current ramp (either up or down) appears to the human eye as a more uniform transition then the linear ramp. This is due to the logarithmic response of the eye.

7.4.1.1.1 8-Bit Code Calculation

In Exponential Mapping Mode the brightness code to backlight current transfer function is given by the equation:

$$I_{LED} = I_{LED\_FULLSCALE} \times 0.85^{\left(44 - \frac{Code + 1}{5.8181818}\right)} \times D_{PWM} \quad (1)$$

Where $I_{LED\_FULLSCALE}$ is the full-scale LED current setting (see Table 10), Code is the 8-bit backlight code in the Control Brightness MSB register and D_{PWM} is the PWM Duty Cycle.

7.4.1.1.2 11-Bit Code Calculation

In Exponential Mapping Mode the brightness code to backlight current transfer function is given by the equation:

$$I_{LED} = I_{LED\_FULLSCALE} \times 0.85^{\left(44 - \frac{\frac{Code}{8} + 1}{5.8181818}\right)} \times D_{PWM} \quad (2)$$

Where $I_{LED\_FULLSCALE}$ is the full-scale LED current setting (see Table 10), Code is the 11-bit backlight code in the Control Brightness MSB and LSB registers and D_{PWM} is the PWM Duty Cycle.

7.4.1.2 Linear Mapping

In Linear Mapping Mode the brightness code to backlight current has a linear relationship.

7.4.1.2.1 8-Bit Code Calculation

The 8-bit linear mapping follows the equation:

$$I_{LED} = I_{LED\_FULLSCALE} \times \frac{1}{255} \times Code \times D_{PWM} \quad (3)$$

Where $I_{LED\_FULLSCALE}$ is the full-scale LED current setting, Code is the 8-bit backlight code in the Control Brightness MSB register and D_{PWM} is the PWM Duty Cycle.

7.4.1.2.2 11-Bit Code Calculation

The 11-bit linear mapping follows the equation:

$$I_{LED} = I_{LED\_FULLSCALE} \times \frac{1}{2047} \times Code \times D_{PWM} \quad (4)$$

Where $I_{LED\_FULLSCALE}$ is the full-scale LED current setting, Code is the 11-bit backlight code in the Control Brightness MSB and LSB registers and D_{PWM} is the PWM Duty Cycle.

Device Functional Modes (continued)

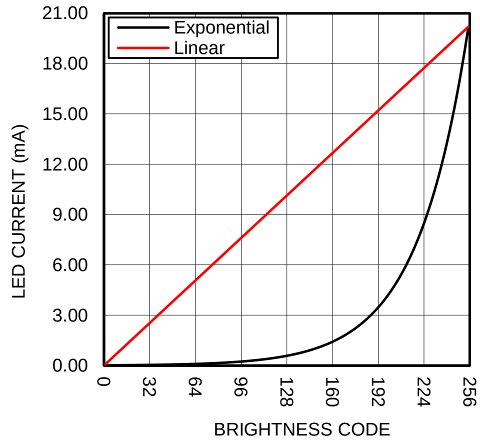


Figure 10. LED Current Mapping Modes (8-Bit)

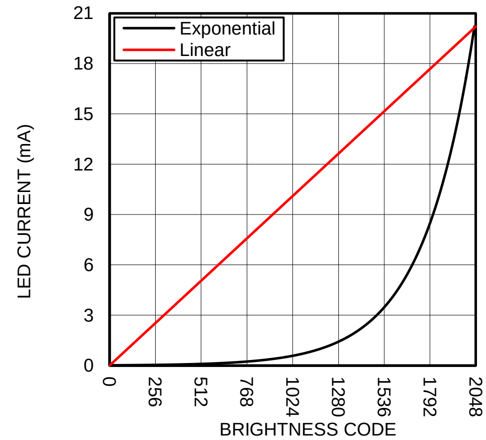


Figure 11. LED Current Mapping Modes (11-Bit)

7.4.2 Fault Flags/Protection Features

The LM3697 contains both LED-open and LED-short fault detection. These fault detections are designed to be used in production level testing and not normal operation. For the fault flags to operate, they must be enabled via the LED Fault Enable Register (see Table 22). The following sections detail the proper procedure for reading back open and short faults in the high-voltage LED strings.

7.4.2.1 Open LED String (HVLED)

An open LED string is detected when the voltage at the input to any active high-voltage current sink has fallen below 200 mV, and the boost output voltage has hit the OVP threshold. This test assumes that the HVLED string that is being detected for an open is connected to the LM3697 device's boost output (COUT+) (see Table 20). For an HVLED string not connected to the LM3697's boost output voltage, but connected to another voltage source, the boost output will not trigger the OVP flag. In this case an open LED string is not detected.

The procedure for detecting an open fault in the HVLED current sinks (provided they are connected to the boost output voltage) is:

- Apply power to the LM3697
- Enable Open Fault (Register 0xB4, bit [0] = 1)
- Assign HVLED1, HVLED2 and HVLED3 to Bank A (Register 0x10, Bits [2:0] = (0, 0, 0)
- Set the start-up ramp times to the fastest setting (Register 0x11 = 0x00)
- Set Bank A full-scale current to 20.2 mA (Register 0x17 = 0x13)
- Configure HVLED1, HVLED2 and HVLED3 for LED string anode connected to COUT (Register 0x19, bits[2:0] = (1,1,1))
- Set Control A Brightness MSB to max (Register 0x21 = 0xFF)
- Enable Bank A (Register 0x24 Bit[0] = 1
- Wait 4 ms
- Read back bits[2:0] of register 0xB0. Bit [0] = 1 (HVLED1 open). Bit [1] = 1 (HVLED2 open). Bit [2] = 1 (HVLED3 open)
- Disable all banks (Register 0x24 = 0x00)

7.4.2.2 Shorted LED String (HVLED)

The LM3697 features an LED short fault flag indicating one or more of the HVLED strings have experienced a short. The method for detecting a shorted HVLED strings is if the current sink is enabled and the string voltage (V_{OUT} - $V_{HVLED1/2/3}$) falls to below (V_{IN} - 1 V) . This test must be performed on one HVLED string at a time. Performing the test with more than one current sink enabled can result in a faulty reading.

The procedure for detecting a short in an HVLED string is:

Device Functional Modes (continued)

- Apply power to the LM3697
- Enable Short Fault (Register 0xB4, bit [1] = 1)
- Assign HVLED1 to Bank A (Register 0x10, Bits [2:0] = (1, 1, 0)
- Set the startup ramp times to the fastest setting (Register 0x11 = 0x00)
- Set Bank A full-scale current to 20.2 mA (Register 0x17 = 0x13)
- Enable Feedback on the HVLED Current Sinks (Register 0x19, bits[2:0] = (1,1,1))
- Set Control A Brightness MSB to max (Register 0x21 = 0xFF)
- Enable Bank A (Register 0x24 Bit[0] = 1)
- Wait 4 ms
- Read back bits[0] of register 0xB2. 1 = HVLED1 short.
- Disable all banks (Register 0x24 = 0x00)
- Repeat the procedure for the HVLED2 and HVLED3 strings

7.4.2.3 Overvoltage Protection (Inductive Boost)

The overvoltage protection threshold (OVP) on the LM3697 has 4 different configurable options (16 V, 24 V, 32 V, and 40 V). The OVP protects the device and associated circuitry from high voltages in the event the high-voltage LED string becomes open. During normal operation, the LM3697 device's inductive boost converter boosts the output up so as to maintain V_{HR} at the active, high-voltage (COUT connected) current sink inputs. When a high-voltage LED string becomes open, the feedback mechanism is broken, and the boost converter over-boosts the output. When the output voltage reaches the OVP threshold the boost converter stops switching, thus allowing the output node to discharge. When the output discharges to V_{OVP} minus 1 V the boost converter begins switching again. The OVP sense is at the OVP pin, so this pin must be connected directly to the inductive boost output capacitor's positive terminal.

For high-voltage current sinks that have the HVLED Current Sink Feedback Enable setting such that the high-voltage current sinks anodes are not connected to COUT (feedback is disabled), the overvoltage sense mechanism is not in place to protect the input to the high-voltage current sink. In this situation the application must ensure that the voltage at HVLED1, HVLED2 or HVLED3 doesn't exceed 40 V.

The default setting for OVP is set at 16 V. For applications that require higher than 16 V at the boost output, the OVP threshold must be programmed to a higher level after power up.

7.4.2.4 Current Limit (Inductive Boost)

The NMOS switch current limit for the LM3697 device's inductive boost is set at 1 A (typical). When the current through the LM3697's NFET switch hits this overcurrent protection threshold (OCP), the device turns the NFET off, and the inductor's energy is discharged into the output capacitor. Switching is then resumed at the next cycle. The current limit protection circuitry can operate continuously each switching cycle. The result is that during high-output power conditions the device can continuously run in current limit. Under these conditions the LM3697's inductive boost converter stops regulating the headroom voltage across the high-voltage current sinks. This results in a drop in the LED current.

7.4.3 I^2C-Compatible Interface

7.4.3.1 Start And Stop Conditions

The LM3697 is controlled via an I^2C-compatible interface. START and STOP conditions classify the beginning and the end of the I^2C session. A START condition is defined as SDA transitioning from HIGH to LOW while SCL is HIGH. A STOP condition is defined as SDA transitioning from LOW to HIGH while SCL is HIGH. The I^2C master always generates START and STOP conditions. The I^2C bus is considered busy after a START condition and free after a STOP condition. During data transmission the I^2C master can generate repeated START conditions. A START and a repeated START condition are equivalent function-wise. The data on SDA must be stable during the HIGH period of the clock signal (SCL). In other words, the state of SDA can only be changed when SCL is LOW.

Device Functional Modes (continued)

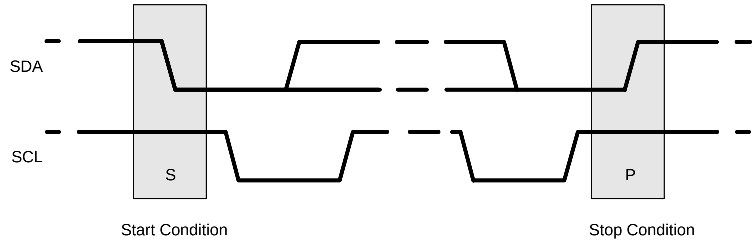


Figure 12. Start And Stop Sequences

7.4.3.2 I²C-Compatible Address

The chip address for the LM3697 is 0110110 (36h). After the START condition, the I²C master sends the 7-bit chip address followed by an eighth read or write bit (R/W). R/W= 0 indicates a WRITE and R/W = 1 indicates a READ. The second byte following the chip address selects the register address to which the data is written. The third byte contains the data for the selected register.

7.4.3.3 Transferring Data

Every byte on the SDA line must be eight bits long, with the most significant bit (MSB) transferred first. Each byte of data must be followed by an acknowledge bit (ACK). The acknowledge related clock pulse (9th clock pulse) is generated by the master. The master releases SDA (HIGH) during the 9th clock pulse. The LM3697 pulls down SDA during the 9th clock pulse signifying an acknowledge. An acknowledge is generated after each byte has been received.

Table 2 lists the available registers within the LM3697.

7.4.3.4 High-Speed Mode

The LM3697 supports only Standard and Fast mode I²C operation. High Speed mode is not supported. If the LM3697 is connected to a I²C-bus with a HS-mode device a dummy I²C cycle is required after the HS-mode command is complete. The dummy cycle can be a read or write to any I²C slave address.

7.5 Register Maps

Table 2. LM3697 Register Descriptions

NAME	ADDRESS	POWER-ON RESET	OPERATION
Revision	0x00	0x01	Dynamic
Software Reset	0x01	0x00	Dynamic
HVLED Current Sink Output Configuration	0x10	0x06	Static
Control A Start-up/Shutdown Ramp Time	0x11	0x00	Static
Control B Start-up/Shutdown Ramp Time	0x12	0x00	Static
Control A/B Run time Ramp Time	0x13	0x00	Static
Control A/B Run time Ramp Configuration	0x14	0x00	Static
Reserved	0x15	0x33	Static
Brightness Configuration	0x16	0x00	Static
Control A Full-Scale Current Setting	0x17	0x13	Static
Control B Full-Scale Current Setting	0x18	0x13	Static
HVLED Current Sink Feedback Enables	0x19	0x07	Static
Boost Control	0x1A	0x00	Static
Auto-Frequency Threshold	0x1B	0xCF	Static
PWM Configuration	0x1C	0x0C	Dynamic (1)
Control A Brightness LSB	0x20	0x00	Dynamic (2)
Control A Brightness MSB	0x21	0x00	Dynamic
Control B Brightness LSB	0x22	0x00	Dynamic (2)
Control B Brightness MSB	0x23	0x00	Dynamic
Control Bank Enables	0x24	0x00	Dynamic
HVLED Open Faults	0xB0	0x00	Production Test Only
HVLED Short Faults	0xB2	0x00	Production Test Only
LED Fault Enables	0xB4	0x00	Production Test Only

(1) The PWM inputmust always be in the inactive state when setting the Control bank PWM Enable bit. The PWM configuration bits must only be changed when the PWM is disabled for both Control Banks.
(2) The Control Brightness MSB Register must be written for the Control Brightness LSB Register value to take effect.

Table 3. Revision (Address 0x00)

Bits [7:4] Not Used	Bits [3:0] Silicon Revision
Reserved	0001 = Rev. A2 Silicon

Table 4. Software Reset (Address 0x01)

Bits [7:1] Not Used	Bit [0] Silicon Revision
Reserved	0 = Normal Operation 1 = Software Reset (self-clearing)

Table 5. HVLED Current Sink Output Configuration (Address 0x10)

Bits [7:3] Not Used	Bit [2] HVLED3 Configuration	Bit [1] HVLED2 Configuration	Bit [0] HVLED1 Configuration
Reserved	0 = Control A 1 = Control B (default)	0 = Control A 1 = Control B (default)	0 = Control A (default) 1 = Control B

Table 6. Control A and B Start-up/Shutdown Ramp Time (Address 0x11 and 0x12)

Bits [7:4] Start-up Ramp	Bits [3:0] Shutdown Ramp
0000 = 2048 µs (default) 0001 = 262 ms 0010 = 524 ms 0011 = 1.049 s 0100 = 2.09 s 0101 = 4.194 s 0110 = 8.389 s 0111 = 16.78 s 1000 = 33.55 s 1001 = 41.94 s 1010 = 50.33 s 1011 = 58.72 s 1100 = 67.11 s 1101 = 83.88 s 1110 = 100.66 s 1111 = 117.44 s	0000 = 2048 µs (default) 0001 = 262 ms 0010 = 524 ms 0011 = 1.049 s 0100 = 2.097 s 0101 = 4.194 s 0110 = 8.389 s 0111 = 16.78 s 1000 = 33.55 s 1001 = 41.94 s 1010 = 50.33 s 1011 = 58.72 s 1100 = 67.11 s 1101 = 83.88 s 1110 = 100.66 s 1111 = 117.44 s

Table 7. Control A and B Run-Time Ramp Time (Address 0x13)

Bits [7:4] Transition Time Ramp Up	Bits [3:0] Transition Time Ramp Down
000 = 2048 µs (default) 001 = 262 ms 010 = 524 ms 011 = 1.049 s 100 = 2.097 s 101 = 4.194 s 110 = 8.389 s 111 = 16.78 s 1000 = 33.55 s 1001 = 41.94 s 1010 = 50.33 s 1011 = 58.72 s 1100 = 67.11 s 1101 = 83.88 s 1110 = 100.66 s 1111 = 117.44 s	000 = 2048 µs (default) 001 = 262 ms 010 = 524 ms 011 = 1.049 s 100 = 2.097 s 101 = 4.194 s 110 = 8.389 s 111 = 16.78 s 1000 = 33.55 s 1001 = 41.94 s 1010 = 50.33 s 1011 = 58.72 s 1100 = 67.11 s 1101 = 83.88 s 1110 = 100.66 s 1111 = 117.44 s

Table 8. Control A and B Run-Time Ramp Configuration (Address 0x14)

Bits [7:4] Not Used	Bits [3:2] Control B Run-time Ramp Select	Bits [1:0] Control A Run-time Ramp Select
Reserved	00 = Control A/B Runtime Ramp Times (default) 01 = Control B Start-up/Shutdown Ramp Times 1x = 0 µs Ramp Time	00 = Control A/B Runtime Ramp Times (default) 01 = Control A Start-up/Shutdown Ramp Times 1x = 0 µs Ramp Time

Table 9. Control A and B Brightness Configuration (Address 0x16)

Bits [7:4] Not Used	Bit [3] Control B Dither Disable	Bit [2] Control A Dither Disable	Bit [1] Not Used	Bit [0] Control A/B Mapping Mode
Reserved	0 Enable (default) 1 Disable	0 Enable (default) 1 Disable	Reserved	0 Exponential (default) 1 Linear

Table 10. Control A and B Full-Scale Current Setting (Address 0x17 and 0x18)

Bits [7:5] Not Used	Bits [4:0] Control A, B Full-Scale Current Select Bits
Reserved	00000 = 5 mA
	10011 = 20.2 mA (default)
	11111 = 29.8 mA (0.8 mA steps, FS = 5 + code * 0.8 mA)

Table 11. HVLED Current Sink Feedback Enables (Address 0x19)

Bits [7:3] Not Used	Bit [2] HVLED3 Feedback Enable	Bit [1] HVLED2 Feedback Enable	Bit [0] HVLED1 Feedback Enable
Reserved	0 = LED anode is NOT CONNECTED to COUT 1 = LED anode is CONNECTED to COUT (default)	0 = LED anode is NOT CONNECTED to COUT 1 = LED anode is CONNECTED to COUT (default)	0 = LED anode is NOT CONNECTED to COUT 1 = LED anode is CONNECTED to COUT (default)

Table 12. Boost Control (Address 0x1A)

Bits [7:5] Not Used	Bit [4] Auto-Headroom Enable	Bit [3] Auto-Frequency Enable	Bits [2:1] Boost OVP Select	Bit [0] Boost Frequency Select
Reserved	0 = Disable (default) 1 = Enable	0 = Disable (default) 1 = Enable	00 = 16 V (default) 01 = 24 V 10 = 32 V 11 = 40 V	0 = 500 kHz (default) 1 = 1 MHz

Table 13. Auto-Frequency Threshold (Address 0x1B)

Bits [7:0]
Auto-Frequency Threshold (default = 11001111)

Table 14. PWM Configuration (Address 0x1C)

Bits [7:4] Not Used	Bit [3] PWM Zero Detection Enable	Bit [2] PWM Polarity	Bit [1] Control B PWM Enable	Bit [0] Control A PWM Enable
Reserved	0 = Disable 1 = Enable (default)	0 = Active Low 1 = Active High (default)	0 = Disable (default) 1 = Enable	0 = Disable (default) 1 = Enable

Table 15. Control A Brightness LSB (Address 0x20)

Bits [7:3] Not Used	Bits [2:0] Control A Brightness [2:0]
Reserved	Brightness LSB

Table 16. Control A Brightness MSB (Address 0x21)

Bits [7:0] Control A Brightness [11:3]
Brightness MSB (LED current ramping does not start until the MSB is written, LSB must always be written before MSB)

Table 17. Control B Brightness LSB (Address 0x22)

Bits [7:3] Not Used	Bits [2:0] Control B Brightness [2:0]
Reserved	Brightness LSB

Table 18. Control B Brightness MSB (Address 0x23)

Bits [7:0] Control B Brightness [11:3]
Brightness MSB (LED current ramping does not start until the MSB is written, LSB must always be written before MSB)

Table 19. Control Bank Enables (Address 0x24)

Bit [7:2] Not Used	**Bit [1] Control B Enable**	**Bit [0] Control A Enable**
Reserved	0 = Disable (default) 1 = Enable	0 = Disable (default) 1 = Enable

Table 20. HVLED Open Faults (Address 0xB0)

Bits [7:3] Not Used	**Bit [2] HVLED3 Open**	**Bit [1] HVLED2 Open**	**Bit [0] HVLED1 Open**
Reserved	0 = Normal Operation 1 = Open	0 = Normal Operation 1 = Open	0 = Normal Operation 1 = Open

Table 21. HVLED Short Faults (Address 0xB2)

Bits [7:3] Not Used	**Bit [2] HVLED3 Short**	**Bit [1] HVLED2 Short**	**Bit [0] HVLED1 Short**
Reserved	0 = Normal Operation 1 = Short	0 = Normal Operation 1 = Short	0 = Normal Operation 1 = Short

Table 22. LED Fault Enable (Address 0xB4)

Bits [7:2] Not Used	**Bit [1] Short Faults Enable**	**Bit [0] Open Faults Enable**
Reserved	0 = Disable (default) 1 = Enable	0 = Disable (default) 1 = Enable

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM3697 provides a complete high-performance LED lighting solution for mobile handsets. The LM3697 is highly configurable and can support the LED configurations summarized in Table 23. The LM3697 provides internal ramp time generators to provide smooth LED dimming with 11-bit control while requiring only 8-bit control from the host controller. The LM3697EVM is available with GUI software to aid understanding of the LM3697 operation.

Table 23. Supported LED Configurations

NUMBER OF LED STRINGS	MAXIMUM OUTPUT VOLTAGE
3	See *Peak Current Limited*
2	39 V
1	39 V

8.2 Typical Applications

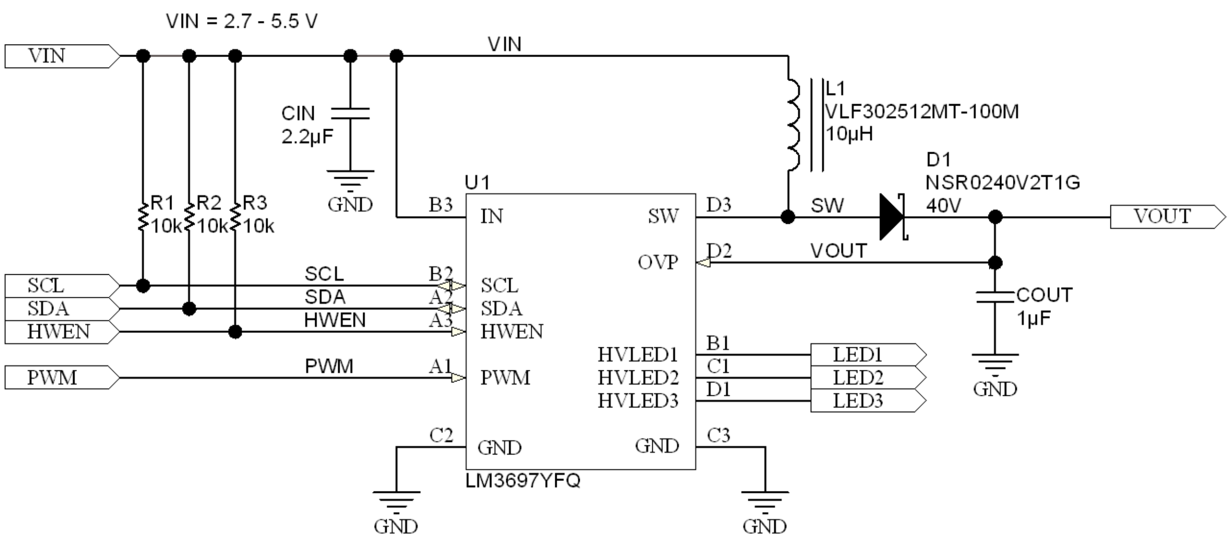


Figure 13. LM3697 Schematic

Typical Applications (continued)

8.2.1 Design Requirements

For 8s3p applications, use the parameters listed in Table 24.

Table 24. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Full-scale current setting	0.0202 A
Minimum Input Voltage	3 V
LED series/parallel configuration	8s3p
LED maximum forward voltage (V_f)	3.5 V
Efficiency	80%
Switching frequency	1 MHz
Inductance	10 µH

The designer needs to know the following:

- Full-scale current setting
- Minimum input voltage (V_{IN_MIN})
- LED series/parallel configuration
- LED maximum V_{F_MAX} voltage
- LM3697 efficiency for LED configuration (efficiency)
- LM3697 boost switching frequency (f_{SW})
- Inductor value (L)

This information guides the designer to make the appropriate inductor selection for the application.

Device boost converter output voltage (V_{OUT_MAX}) is calculated as: number series LEDs × V_{F_MAX} + 0.4 V.

The LM3697 boost converter maximum output current (I_{OUT_MAX}) is calculated as follows: number parallel LED strings × full-scale current.

Using the design parameters from Table 24 I_{L_PEAK} is calculated as:

$$I_{L\_PEAK} = \frac{V_{OUT\_MAX} \times I_{OUT\_MAX}}{V_{IN\_MIN} \times \text{efficiency}} + \frac{V_{IN\_MIN}}{2 \times f_{SW} \times L} \times \frac{V_{OUT\_MAX} - V_{IN\_MIN} \times \text{efficiency}}{V_{OUT\_MAX}} \quad (5)$$

For example:

$$V_{OUT\_MAX} = 8 \times 3.2\text{ V} + 0.4\text{ V} = 26\text{ V} \quad (6)$$

$$I_{OUT\_MAX} = 20.2\text{ mA} \times 3\text{ strings} = 60.6\text{ mA} \quad (7)$$

$$I_{L\_PEAK} = \frac{26\text{ V} \times 60.6\text{ mA}}{3\text{ V} \times 0.8} + \frac{3\text{ V}}{2 \times 1\text{ MHz} \times 10\text{ µH}} \times \frac{26\text{ V} - 3\text{ V} \times 0.8}{26\text{ V}} = 792\text{ mA} \quad (8)$$

This calculated value for I_{L_PEAK} must be less than the minimum spec for the LM3697 boost current limit of 880 mA. Additionally, the chosen inductor must have a saturation current rating that is greater than I_{L_PEAK}.

8.2.2 Detailed Design Procedure

8.2.2.1 Boost Converter Maximum Output Power

The LM3697 devices maximum output power is governed by two factors: the peak current limit (I_{CL} = 880 mA minimum), and the maximum output voltage (V_{OUT}). When the application causes either of these limits to be reached it is possible that the proper current regulation and matching between LED current strings will not be met.

8.2.2.1.1 Peak Current Limited

In the case of a peak current limited situation, when the peak of the inductor current hits the LM3697 device's current limit, the NFET switch turns off for the remainder of the switching period. If this happens each switching cycle the LM3697 regulates the peak of the inductor current instead of the headroom across the current sinks. This can result in the dropout of the boost output connected current sinks, and the LED current dropping below its programmed level.

The peak current in a boost converter is dependent on the value of the inductor, total LED current in the boost (I_{OUT}), the boost output voltage (V_{OUT}) (which is the highest voltage LED string + V_{HR}), the input voltage (V_{IN}), the switching frequency (f_{SW}), and the efficiency (output power/input power). Additionally, the peak current is different depending on whether the inductor current is continuous during the entire switching period (CCM), or discontinuous (DCM) where it goes to 0 before the switching period ends. For CCM the peak inductor current is given by:

$$I_{PEAK} = \frac{I_{OUT} \times V_{OUT}}{V_{IN} \times \text{efficiency}} + \left[\frac{V_{IN}}{2 \times f_{SW} \times L} \times \left(1 - \frac{V_{IN} \times \text{efficiency}}{V_{OUT}} \right) \right] \quad (9)$$

For DCM the peak inductor current is given by:

$$I_{PEAK} = \sqrt{\frac{2 \times I_{OUT}}{f_{SW} \times L \times \text{efficiency}} \times \left(V_{OUT} - V_{IN} \times \text{efficiency} \right)} \quad (10)$$

To determine which mode the circuit is operating in (CCM or DCM) it is necessary to perform a calculation to test whether the inductor current ripple is less than the anticipated input current (I_{IN}). If ΔI_L is less than I_{IN} then the device is operating in CCM. If ΔI_L is greater than I_{IN} then the device is operating in DCM.

$$\frac{I_{OUT} \times V_{OUT}}{V_{IN} \times \text{efficiency}} > \frac{V_{IN}}{f_{SW} \times L} \times \left(1 - \frac{V_{IN} \times \text{efficiency}}{V_{OUT}} \right) \quad (11)$$

Typically at currents high enough to reach the LM3697's peak current limit, the device is operating in CCM.

Figure 14 and Figure 15 show the output current and voltage derating for a 10-µH and a 22-µH inductor. These plots take Equation 9 and Equation 10 and plot V_{OUT} and I_{OUT} with varying V_{IN}, a constant peak current of 880 mA (I_{CL_MIN}), 500-kHz switching frequency, and a constant efficiency of 85%. Using these curves can give a good design guideline on selecting the correct inductor for a given output power requirement. A 10-µH inductor will typically be a smaller device with lower on resistance, but the peak currents is higher. A 22-µH inductor provides for lower peak currents but a larger sized device is required to match the DC resistance of a 10-µH inductor.

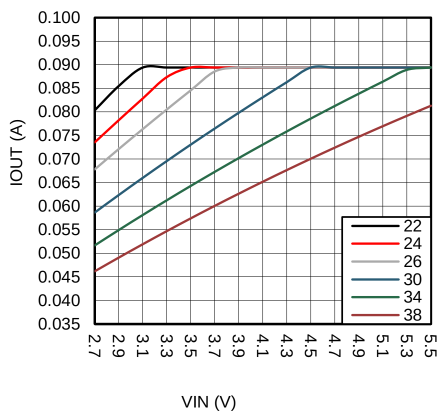


Figure 14. Maximum Output Power (22 µH)

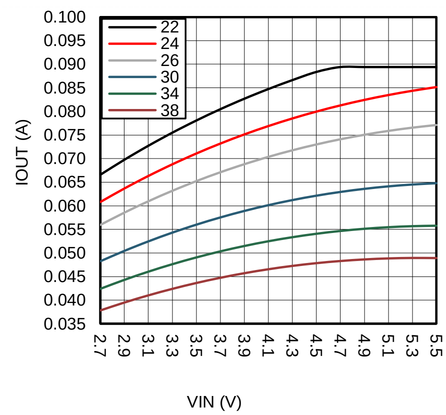


Figure 15. Maximum Output Power (10 µH)

8.2.2.1.2 Output Voltage Limited

In the case of an output voltage limited situation ($V_{OUT} = V_{OVP}$), when the boost output voltage hits the LM3697 device's OVP threshold, the NFET turns off and stays off until the output voltage falls below the hysteresis level (typically 1 V below the OVP threshold). This results in the boost converter regulating the output voltage to the programmed OVP threshold (16 V, 24 V, 32 V, or 40 V), causing the current sinks to go into dropout. The default OVP threshold is set at 16 V. For LED strings higher than typically 4 series LEDs, the OVP has to be programmed higher after power-up, Software Reset, or HWEN reset.

8.2.2.2 Inductor Selection

The boost circuit operates using a 4.7-µH to 22-µH inductor. The inductor selected must have a saturation current greater than the peak operating current.

8.2.2.3 Output Capacitor Selection

The LM3697's inductive boost converter requires a 1-µF (X5R or X7R) ceramic capacitor to filter the output voltage. The voltage rating of the capacitor depends on the selected OVP setting. For the 16 V setting a 16-V capacitor must be used. For the 24-V setting a 25-V capacitor must be used. For the 32-V setting, a 35-V capacitor must be used. For the 40-V setting a 50-V capacitor must be used. Pay careful attention to the capacitor's tolerance and DC bias response. For proper operation the degradation in capacitance due to tolerance, DC bias, and temperature, must stay above 0.4 µF. This might require placing two devices in parallel in order to maintain the required output capacitance over the device operating range, and series LED configuration.

8.2.2.4 Schottky Diode Selection

The Schottky diode must have a reverse breakdown voltage greater than the LM3697 device’s maximum output voltage (see *Overvoltage Protection (Inductive Boost)* section). Additionally, the diode must have an average current rating high enough to handle the LM3697’s maximum output current, and at the same time the diode's peak current rating must be high enough to handle the peak inductor current. Schottky diodes are required due to their lower forward voltage drop (0.3 V to 0.5 V) and their fast recovery time.

8.2.2.5 Input Capacitor Selection

The LM3697 device's inductive boost converter requires a 2.2-µF (X5R or X7R) ceramic capacitor to filter the input voltage. The input capacitor filters the inductor current ripple and the internal MOSFET driver currents during turn on of the internal power switch.

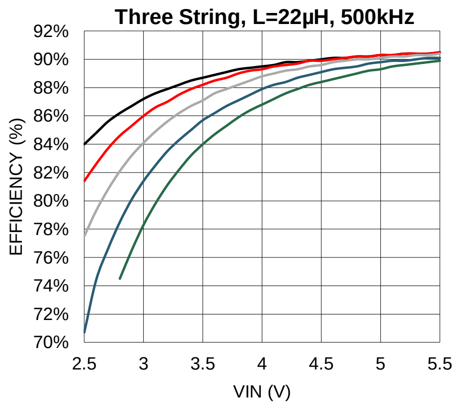
8.2.2.6 Application Circuit Component List

COMPONENT	MANUFACTURER	VALUE	PART NUMBER	SIZE (mm)	CURRENT/VOLTAGE RATING (RESISTANCE)
L	TDK	10 µH	VLF302512MT-100M	2.5 × 3.0 × 1.2	620 mA/0.25 Ω
C_{OUT}	TDK	1.0 µF	C2012X5R1H105	0805	50 V
C_{IN}	TDK	2.2 µF	C1005X5R1A225	0402	10 V
Diode	On-Semi	Schottky	NSR0240V2T1G	SOD-523	40 V, 250 mA

8.2.3 Application Performance Plots

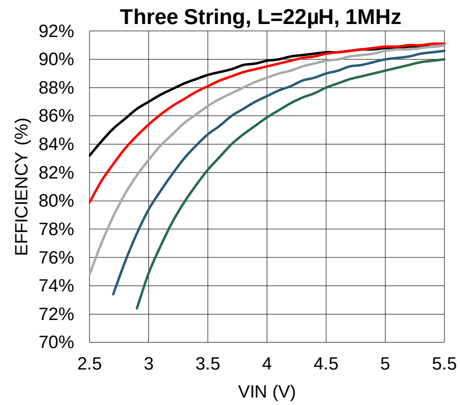
V_{IN} = 3.6 V, full-scale current = 20.2 mA, LEDs are WLEDs part # SML-312WBCW(A), Typical Application Circuit , T_A = 25°C unless otherwise specified. Efficiency is $V_{OUT} \times (I_{HVLED1} + I_{HVLED2} + I_{HVLED3})/(V_{IN} \times I_{IN})$, matching curves are $(\Delta I_{LED\_MAX}/I_{LED\_AVE})$.

V_{IN} = 3.6 V, full-scale current = 20.2 mA, LEDs are WLEDs part # SML-312WBCW(A), Typical Application Circuit , T_A = 25°C unless otherwise specified. Efficiency is $V_{OUT} \times (I_{HVLED1} + I_{HVLED2} + I_{HVLED3})/(V_{IN} \times I_{IN})$, matching curves are $(\Delta I_{LED\_MAX}/I_{LED\_AVE})$.



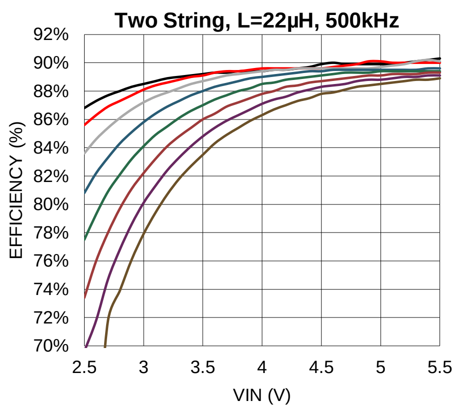
Top to Bottom: 3x3, 3x4, 3x5, 3x6, 3x7 (LEDs)

Figure 16. Boost Efficiency vs V_{IN}



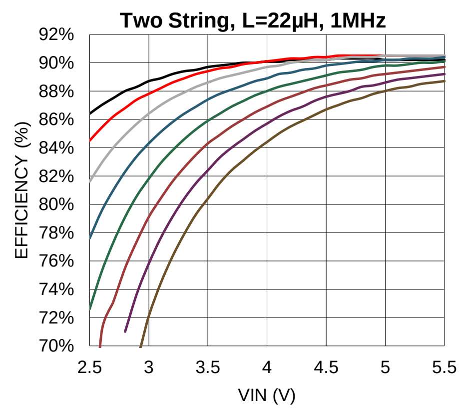
Top to Bottom: 3x3, 3x4, 3x5, 3x6, 3x7 (LEDs)

Figure 17. Boost Efficiency vs V_{IN}



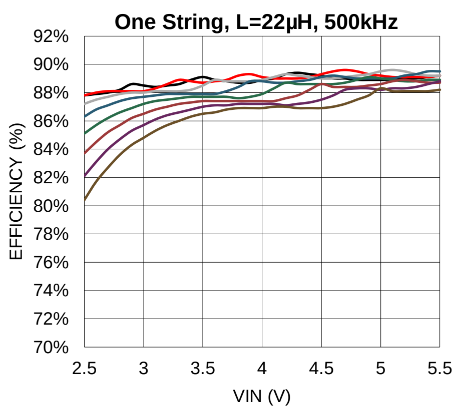
Top to Bottom: 2x3, 2x4, 2x5, 2x6, 2x7, 2x8, 2x9, 2x10 (LEDs)

Figure 18. Boost Efficiency vs V_{IN}



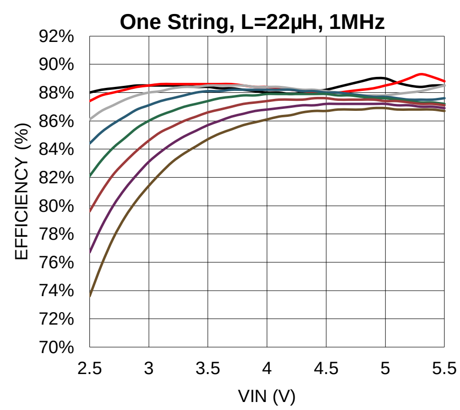
Top to Bottom: 2x3, 2x4, 2x5, 2x6, 2x7, 2x8, 2x9, 2x10 (LEDs)

Figure 19. Boost Efficiency vs V_{IN}



Top to Bottom: 1x3, 1x4, 1x5, 1x6, 1x7, 1x8, 1x9, 1x10 (LEDs)

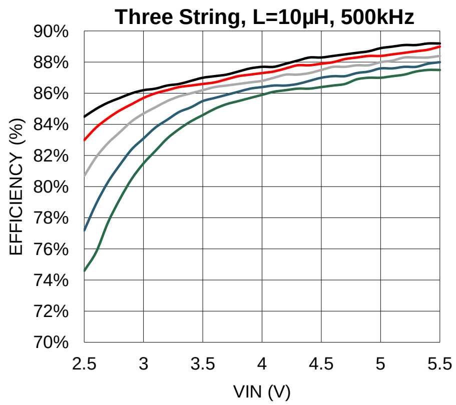
Figure 20. Boost Efficiency vs V_{IN}



Top to Bottom: 1x3, 1x4, 1x5, 1x6, 1x7, 1x8, 1x9, 1x10 (LEDs)

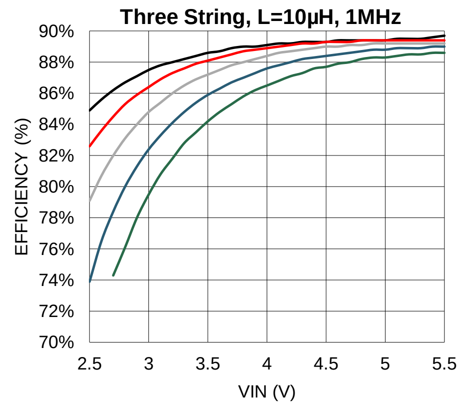
Figure 21. Boost Efficiency vs V_{IN}

V_{IN} = 3.6 V, full-scale current = 20.2 mA, LEDs are WLEDs part # SML-312WBCW(A), Typical Application Circuit , T_A = 25°C unless otherwise specified. Efficiency is $V_{OUT} \times (I_{HVLED1} + I_{HVLED2} + I_{HVLED3})/(V_{IN} \times I_{IN})$, matching curves are $(\Delta I_{LED\_MAX}/I_{LED\_AVE})$.



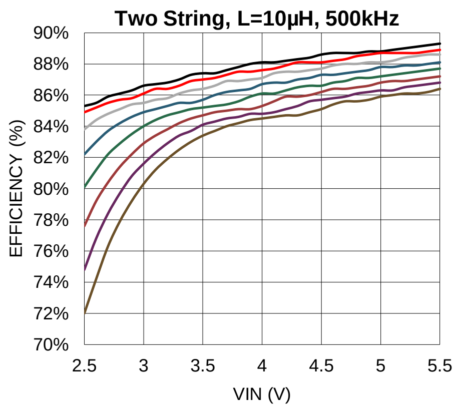
Top to Bottom: 3x3, 3x4, 3x5, 3x6, 3x7 (LEDs)

Figure 22. Boost Efficiency vs V_{IN}



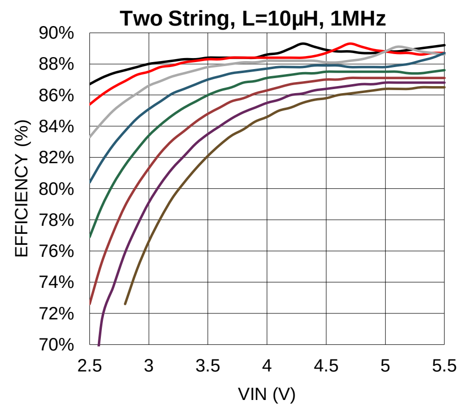
Top to Bottom: 3x3, 3x4, 3x5, 3x6, 3x7 (LEDs)

Figure 23. Boost Efficiency vs V_{IN}



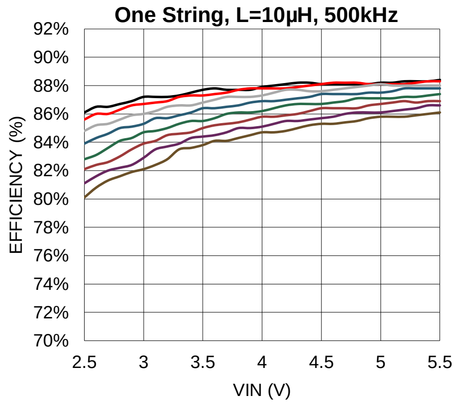
Top to Bottom: 2x3, 2x4, 2x5, 2x6, 2x7, 2x8, 2x9, 2x10 (LEDs)

Figure 24. Boost Efficiency vs V_{IN}



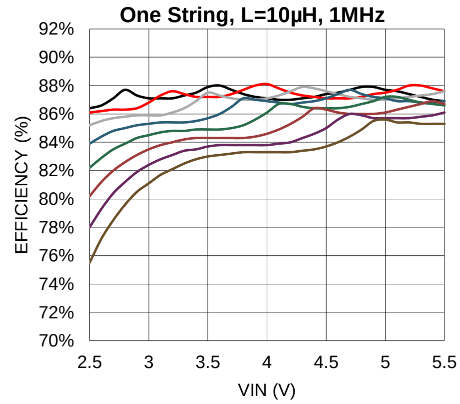
Top to Bottom: 2x3, 2x4, 2x5, 2x6, 2x7, 2x8, 2x9, 2x10 (LEDs)

Figure 25. Boost Efficiency V vs V_{IN}



Top to Bottom: 1x3, 1x4, 1x5, 1x6, 1x7, 1x8, 1x9, 1x10 (LEDs)

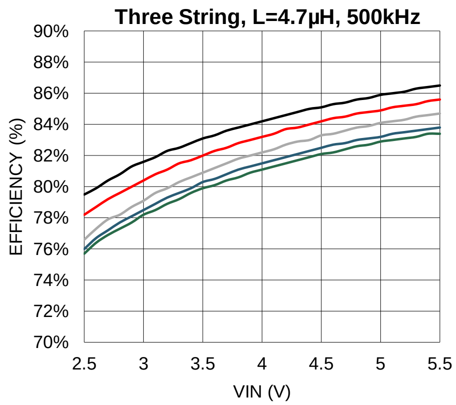
Figure 26. Boost Efficiency vs V_{IN}



Top to Bottom: 1x3, 1x4, 1x5, 1x6, 1x7, 1x8, 1x9, 1x10 (LEDs)

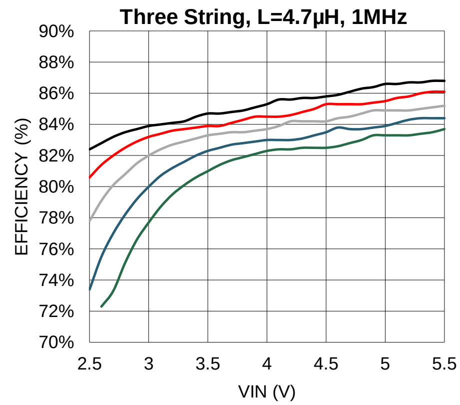
Figure 27. Boost Efficiency vs V_{IN}

V_{IN} = 3.6 V, full-scale current = 20.2 mA, LEDs are WLEDs part # SML-312WBCW(A), Typical Application Circuit , T_A = 25°C unless otherwise specified. Efficiency is $V_{OUT} \times (I_{HVLED1} + I_{HVLED2} + I_{HVLED3})/(V_{IN} \times I_{IN})$, matching curves are ($\Delta I_{LED\_MAX}/I_{LED\_AVE}$).



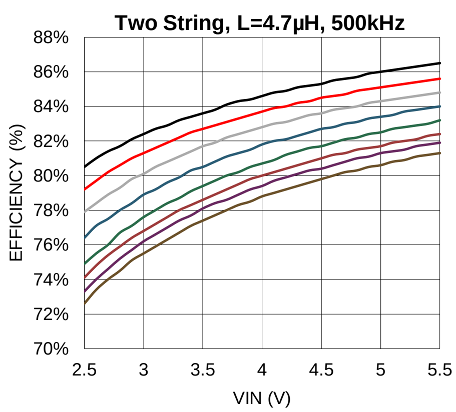
Top to Bottom: 3x3, 3x4, 3x5, 3x6, 3x7 (LEDs)

Figure 28. Boost Efficiency vs V_{IN}



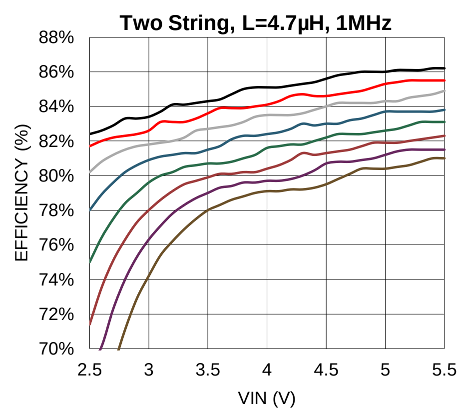
Top to Bottom: 3x3, 3x4, 3x5, 3x6, 3x7 (LEDs)

Figure 29. Boost Efficiency vs V_{IN}



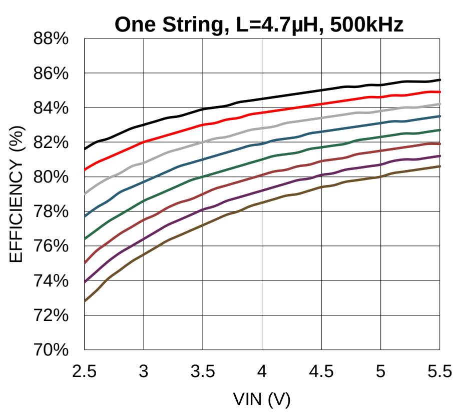
Top to Bottom: 2x3, 2x4, 2x5, 2x6, 2x7, 2x8, 2x9, 2x10 (LEDs)

Figure 30. Boost Efficiency vs V_{IN}



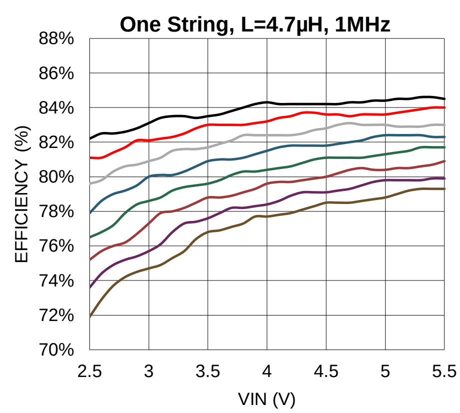
Top to Bottom: 2x3, 2x4, 2x5, 2x6, 2x7, 2x8, 2x9, 2x10 (LEDs)

Figure 31. Boost Efficiency vs V_{IN}



Top to Bottom: 1x3, 1x4, 1x5, 1x6, 1x7, 1x8, 1x9, 1x10 (LEDs)

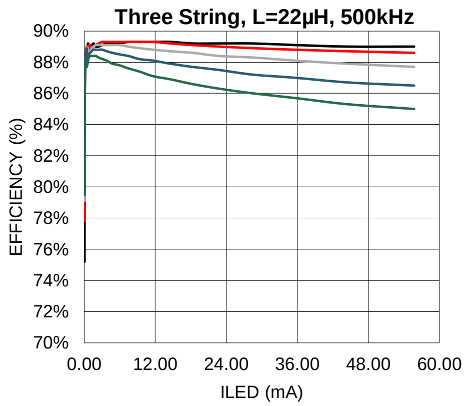
Figure 32. Boost Efficiency vs V_{IN}



Top to Bottom: 1x3, 1x4, 1x5, 1x6, 1x7, 1x8, 1x9, 1x10 (LEDs)

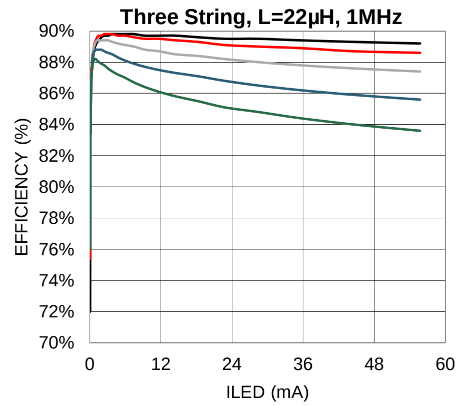
Figure 33. Boost Efficiency vs V_{IN}

V_{IN} = 3.6 V, full-scale current = 20.2 mA, LEDs are WLEDs part # SML-312WBCW(A), Typical Application Circuit , T_A = 25°C unless otherwise specified. Efficiency is $V_{OUT} \times (I_{HVLED1} + I_{HVLED2} + I_{HVLED3})/(V_{IN} \times I_{IN})$, matching curves are $(\Delta I_{LED\_MAX}/I_{LED\_AVE})$.



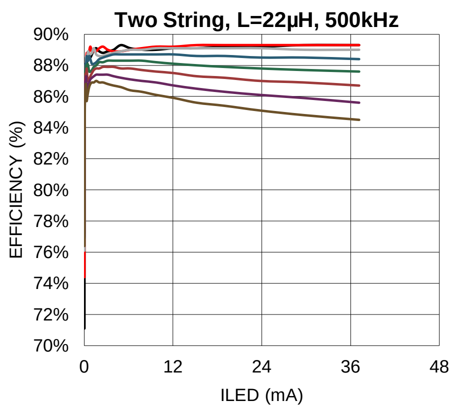
Top to Bottom: 3x3, 3x4, 3x5, 3x6, 3x7 (LEDs)

Figure 34. Boost Efficiency vs I_{LED}



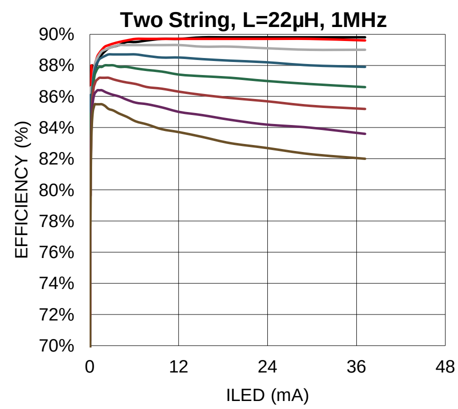
Top to Bottom: 3x3, 3x4, 3x5, 3x6, 3x7 (LEDs)

Figure 35. Boost Efficiency vs I_{LED}



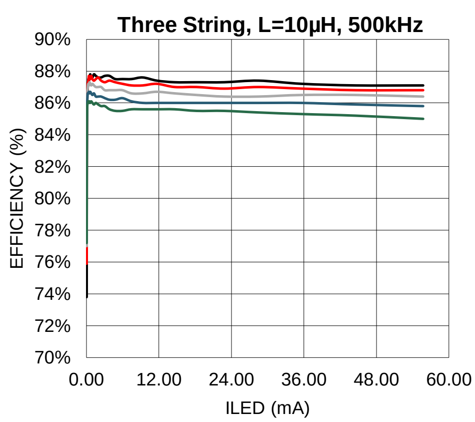
Top to Bottom: 2x3, 2x4, 2x5, 2x6, 2x7, 2x8, 2x9, 2x10 (LEDs)

Figure 36. Boost Efficiency vs I_{LED}



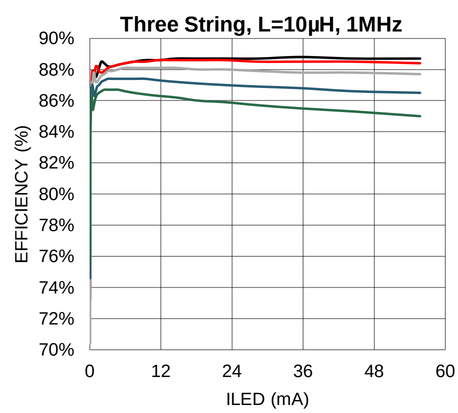
Top to Bottom: 2x3, 2x4, 2x5, 2x6, 2x7, 2x8, 2x9, 2x10 (LEDs)

Figure 37. Boost Efficiency vs I_{LED}



Top to Bottom: 3x3, 3x4, 3x5, 3x6, 3x7 (LEDs)

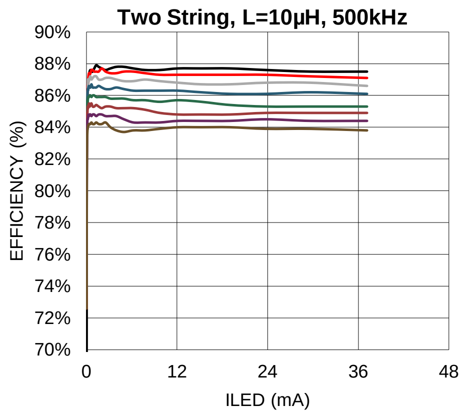
Figure 38. Boost Efficiency vs I_{LED}



Top to Bottom: 3x3, 3x4, 3x5, 3x6, 3x7 (LEDs)

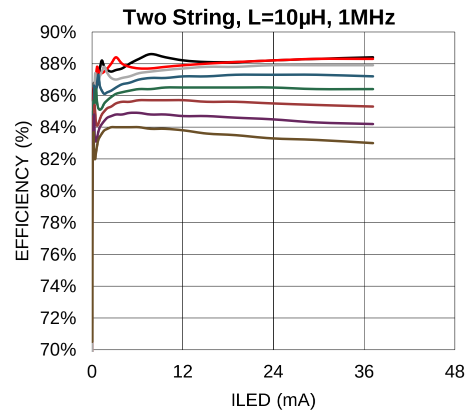
Figure 39. Boost Efficiency vs I_{LED}

V_{IN} = 3.6 V, full-scale current = 20.2 mA, LEDs are WLEDs part # SML-312WBCW(A), Typical Application Circuit , T_A = 25°C unless otherwise specified. Efficiency is $V_{OUT} \times (I_{HVLED1} + I_{HVLED2} + I_{HVLED3})/(V_{IN} \times I_{IN})$, matching curves are ($\Delta I_{LED\_MAX}/I_{LED\_AVE}$).



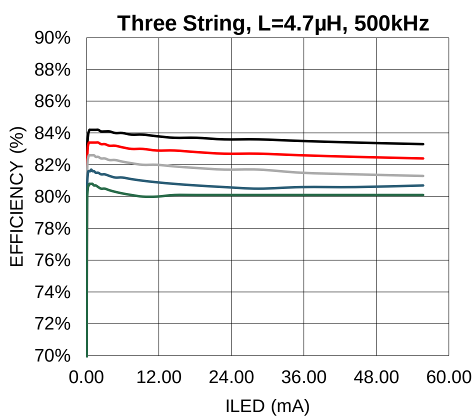
Top to Bottom: 2x3, 2x4, 2x5, 2x6, 2x7, 2x8, 2x9, 2x10 (LEDs)

Figure 40. Boost Efficiency vs I_{LED}



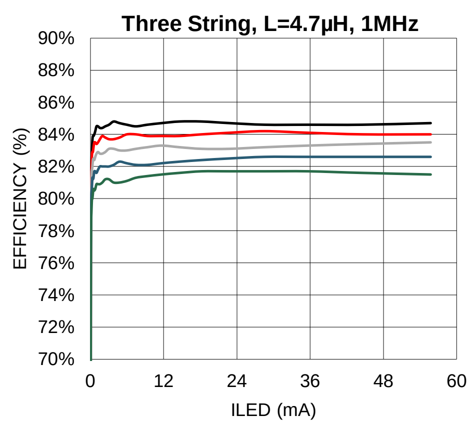
Top to Bottom: 2x3, 2x4, 2x5, 2x6, 2x7, 2x8, 2x9, 2x10 (LEDs)

Figure 41. Boost Efficiency vs I_{LED}



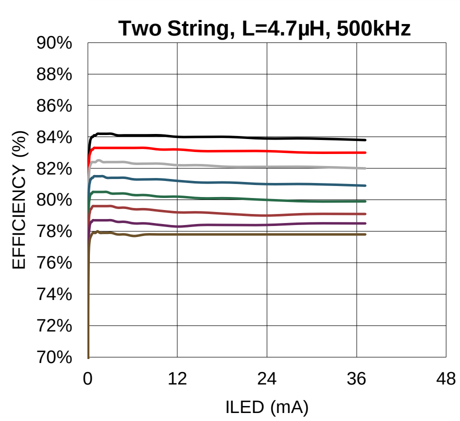
Top to Bottom: 3x3, 3x4, 3x5, 3x6, 3x7 (LEDs)

Figure 42. Boost Efficiency vs I_{LED}



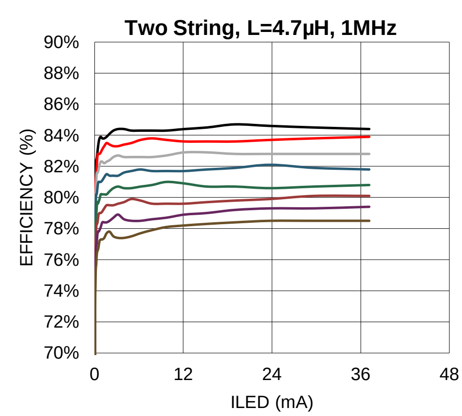
Top to Bottom: 3x3, 3x4, 3x5, 3x6, 3x7 (LEDs)

Figure 43. Boost Efficiency vs I_{LED}



Top to Bottom: 2x3, 2x4, 2x5, 2x6, 2x7, 2x8, 2x9, 2x10 (LEDs)

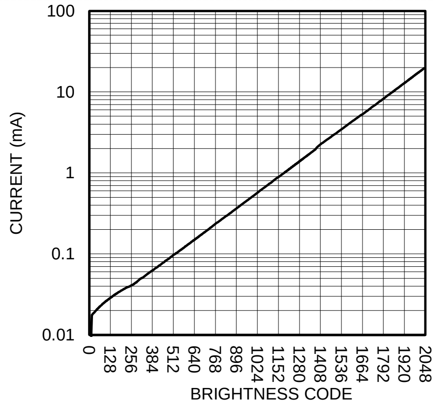
Figure 44. Boost Efficiency vs I_{LED}



Top to Bottom: 2x3, 2x4, 2x5, 2x6, 2x7, 2x8, 2x9, 2x10 (LEDs)

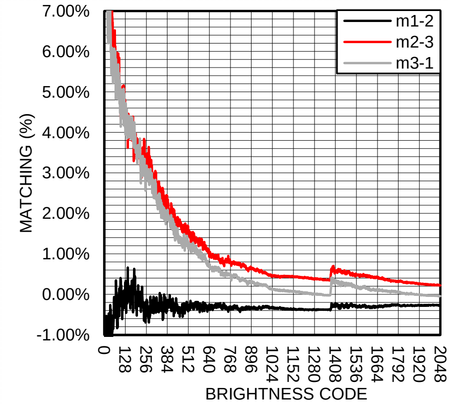
Figure 45. Boost Efficiency vs I_{LED}

V_{IN} = 3.6 V, full-scale current = 20.2 mA, LEDs are WLEDs part # SML-312WBCW(A), Typical Application Circuit , T_A = 25°C unless otherwise specified. Efficiency is $V_{OUT} \times (I_{HVLED1} + I_{HVLED2} + I_{HVLED3})/(V_{IN} \times I_{IN})$, matching curves are $(\Delta I_{LED\_MAX}/I_{LED\_AVE})$.



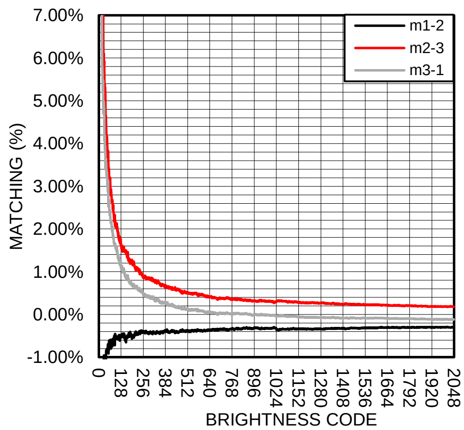
Exponential Mapping

Figure 46. H_{VLED} Current vs. Brightness Code



Exponential Mapping

Figure 47. H_{VLED} Matching Vs. Brightness Code



Linear Mapping

Figure 48. H_{VLED} Matching Vs. Brightness Code

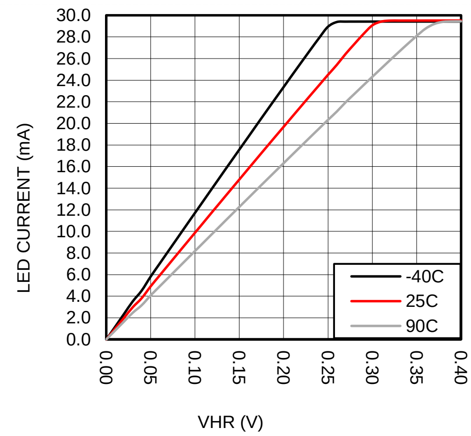


Figure 49. H_{VLED} Current vs. Current Sink Headroom Voltage

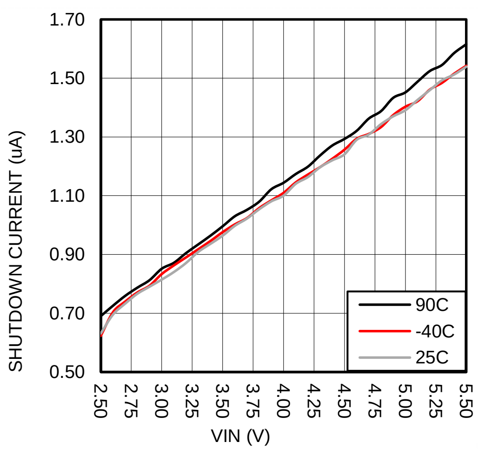


Figure 50. Shutdown Current vs. V_{IN}

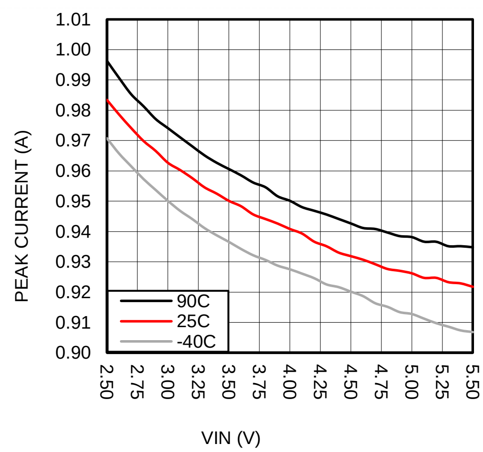


Figure 51. Open Loop Current Limit vs. V_{IN}

V_{IN} = 3.6 V, full-scale current = 20.2 mA, LEDs are WLEDs part # SML-312WBCW(A), Typical Application Circuit , T_A = 25°C unless otherwise specified. Efficiency is $V_{OUT} \times (I_{HVLED1} + I_{HVLED2} + I_{HVLED3})/(V_{IN} \times I_{IN})$, matching curves are $(\Delta I_{LED\_MAX}/I_{LED\_AVE})$.

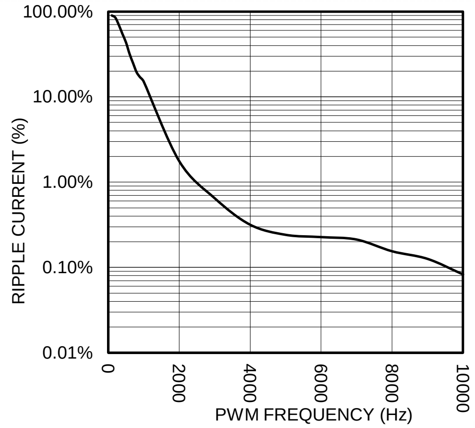
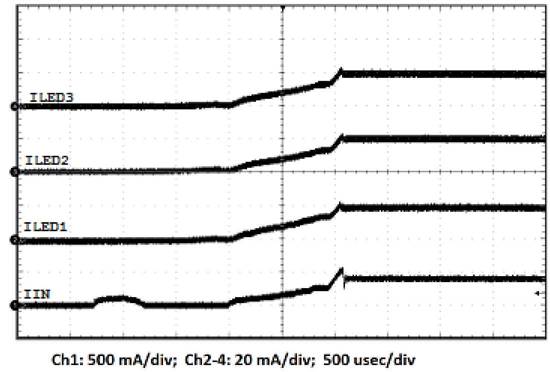


Figure 52. Led Current Ripple vs F_{PWM}



8s2p LED configuration

Figure 53. Start-up Response

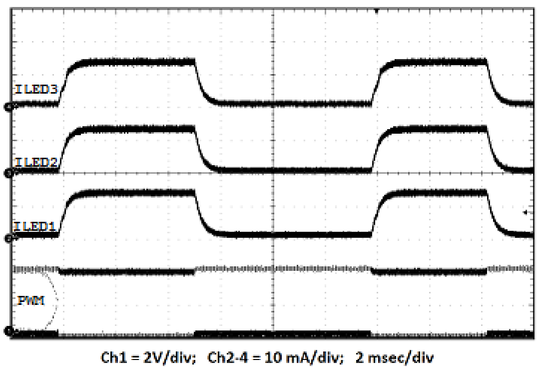


Figure 54. Response To Step Change In PWM Input Duty Cycle

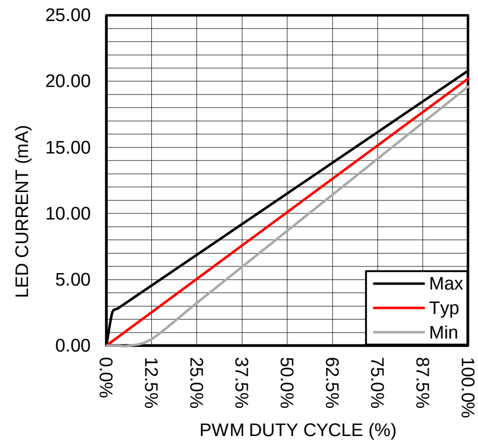


Figure 55. HVLED Current Vs PWM Input Duty Cycle

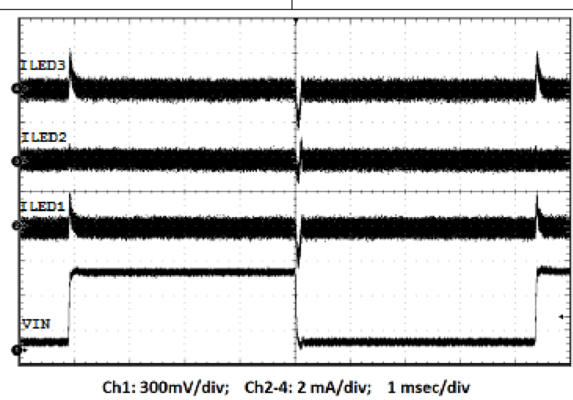


Figure 56. Line Step Response

8.3 Initialization Set Up

Table 25 illustrates the minimum number of register writes required for a two-parallel, seven-series LED configuration. This example uses the default settings for ramp times (2048 µsec), mapping mode (exponential) and full-scale current (20.2 mA). In this mode of operation the LM3697 controls the brightness LSB's to ramp between the 8-bit MSB brightness levels providing 11-bit dimming while requiring only 8-bit commands from the host controller.

Table 25. Control Bank A, 8-Bit Control, Two-String, Seven Series LED Configuration Example

REGISTER NAME	ADDRESS	DATA	DESCRIPTION
HVLED Current Sink Output Configuration	0x10	0x04	HVLED1 & 2 assigned to Control Bank A
HVLED Current Sink Feedback Enables	0x19	0x03	Enable feedback on HVLED1 & 2, disable feedback on HVLED3
Boost Control	0x1A	0x04	OVP = 32V, f_{SW} = 500 kHz
Control Bank Enables	0x24	0x01	Enable Control Bank A
Control A Brightness LSB	0x20	0x00	Control A Brightness LSB written only once
Control A Brightness MSB	0x21	User Value	Control A Brightness MSB updated as required

Table 26 shows the minimum number of register writes required for a two-parallel, six-series LED configuration with PWM Enabled. This example uses the default settings for ramp times (2048 µsec), mapping mode (exponential) and full-scale current (20.2 mA). In this mode of operation the host controller must update both the brightness LSB and MSB registers whenever a brightness change is required.

Table 26. Control Bank A, 11-Bit Control, Two-String, Six Series LED Configuration Example

REGISTER NAME	ADDRESS	DATA	DESCRIPTION
HVLED Current Sink Output Configuration	0x10	0x04	HVLED1 & 2 assigned to Control Bank A
HVLED Current Sink Feedback Enables	0x19	0x03	Enable feedback on HVLED1 & 2, disable feedback on HVLED3
Boost Control	0x1A	0x02	OVP = 24 V, f_{SW} = 500 kHz
PWM Configuration	0x1C	0x0D	PWM Zero Detect = Enabled, PWM Polarity = Active HIgh, Control B PWM = Disabled, Control A PWM = Enabled
Control Bank Enables	0x24	0x01	Enable Control Bank A
Control A Brightness LSB	0x20	User Value	Control A Brightness LSB updated as required (NOTE: The Brightness LSB change does not take effect until the Brightness MSB register is written.)
Control A Brightness MSB	0x21	User Value	Control A Brightness MSB updated as required (NOTE: Anytime the Brightness LSB is changed the Brightness MSB must be written for the Brightness LSB change to take effect.)

9 Power Supply Recommendations

The LM3697 is designed to operate from an input supply range of 2.7 V to 5.5 V. This input supply must be well regulated and provide the peak current required by the LED configuration and inductor selected.

10 Layout

10.1 Layout Guidelines

The LM3697 device's inductive boost converter sees a high switched voltage (up to V_{OVP}) at the SW pin, and a step current (up to I_{CL_BOOST}) through the Schottky diode and output capacitor each switching cycle. The high switching voltage can create interference into nearby nodes due to electric field coupling (I = CdV/dt). The large step current through the diode and the output capacitor can cause a large voltage spike at the SW pin and the OVP pin due to parasitic inductance in the step current conducting path (V = Ldi/dt). Board layout guidelines are geared towards minimizing this electric field coupling and conducted noise. Figure 57 highlights these two noise-generating components.

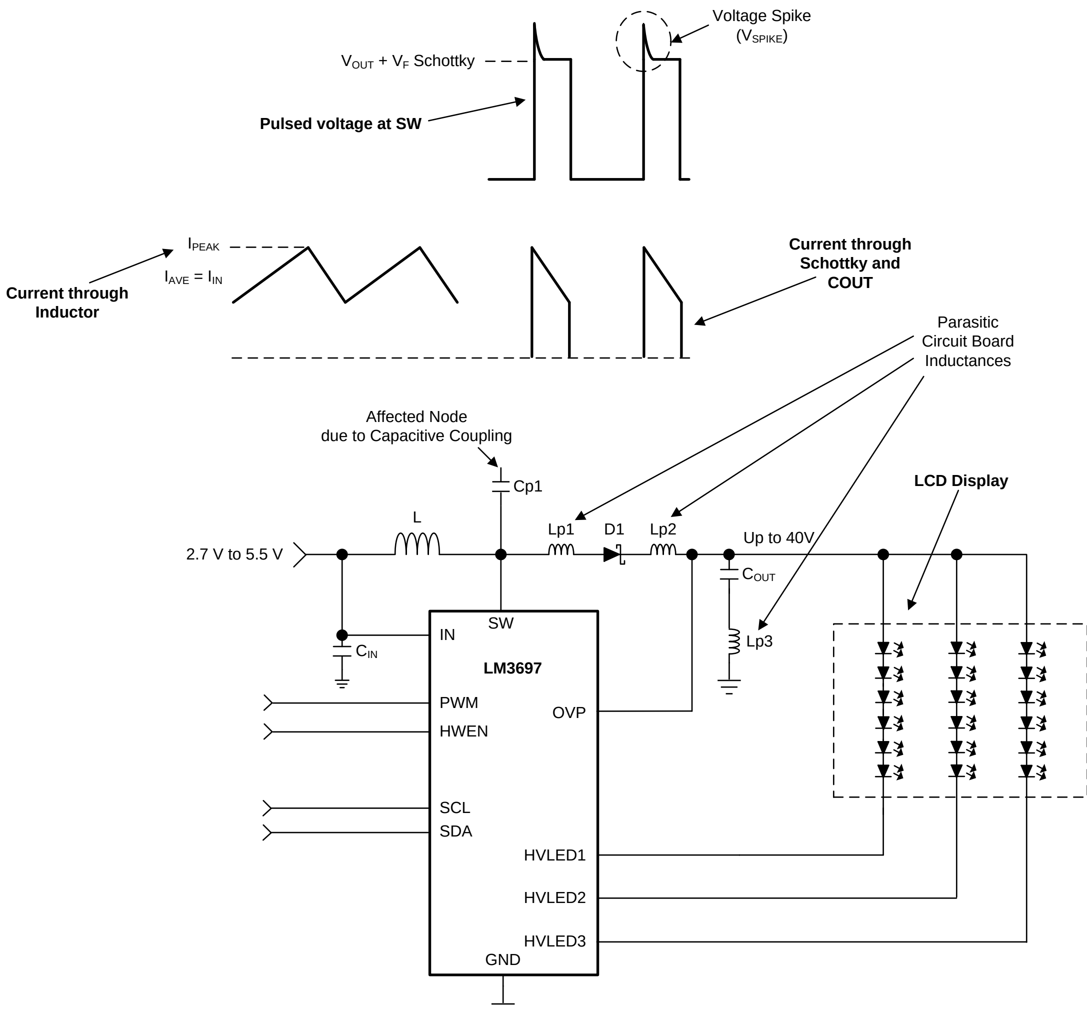


Figure 57. LM3697 Inductive Boost Converter Showing Pulsed Voltage at SW (High Dv/Dt) and Current Through Schottky And COUT (High Di/Dt)

The following list details the main (layout sensitive) areas of the LM3697 device’s inductive boost converter in order of decreasing importance:

1. Output Capacitor
   - Schottky Cathode to COUT+
   - COUT− to GND
2. Schottky Diode
   - SW pin to Schottky Anode
   - Schottky Cathode to COUT+

Layout Guidelines (continued)

3. Inductor
   - SW Node PCB capacitance to other traces
4. Input Capacitor
   - CIN+ to IN terminal

10.1.1 Boost Output Capacitor Placement

Because the output capacitor is in the path of the inductor current discharge path it detects a high-current step from 0 to I_{PEAK} each time the switch turns off and the Schottky diode turns on. Any inductance along this series path from the cathode of the diode through COUT and back into the LM3697 device's GND pin contributes to voltage spikes ($V_{SPIKE} = L_{P\_} \times di/dt$) at SW and OUT. These spikes can potentially over-voltage the SW pin, or feed through to GND. To avoid this, COUT+ must be connected as close as possible to the cathode of the Schottky diode, and COUT− must be connected as close as possible to the LM3697 device's GND bump. The best placement for COUT is on the same layer as the LM3697 in order to avoid any vias that can add excessive series inductance.

10.1.2 Schottky Diode Placement

In the LM3697 device's boost circuit the Schottky diode is in the path of the inductor current discharge. As a result the Schottky diode sees a high-current step from 0 to I_{PEAK} each time the switch turns off and the diode turns on. Any inductance in series with the diode causes a voltage spike ($V_{SPIKE} = L_{P\_} \times di/dt$) at SW and OUT. This can potentially over-voltage the SW pin, or feed through to V_{OUT} and through the output capacitor and into GND. Connecting the anode of the diode as close as possible to the SW pin and the cathode of the diode as close as possible to COUT and reduces the inductance ($L_{P\_}$) and minimize these voltage spikes.

10.1.3 Inductor Placement

The node where the inductor connects to the LM3697 device's SW pin has 2 issues. First, a large switched voltage (0 to $V_{OUT} + V_{F\_SCHOTTKY}$) appears on this node every switching cycle. This switched voltage can be capacitively coupled into nearby nodes. Second, there is a relatively large current (input current) on the traces connecting the input supply to the inductor and connecting the inductor to the SW pin. Any resistance in this path can cause voltage drops that can negatively affect efficiency and reduce the input operating voltage range.

To reduce the capacitive coupling of the signal on SW into nearby traces, the SW pin-to-inductor connection must be minimized in area. This limits the PCB capacitance from SW to other traces. Additionally, high-impedance nodes that are more susceptible to electric field coupling need to be routed away from SW and not directly adjacent or beneath. This is especially true for traces such as SCL, SDA, HWEN, and PWM. A GND plane placed directly below SW dramatically reduces the capacitance from SW into nearby traces.

Lastly, limit the trace resistance of the VIN-to-inductor connection and from the inductor to SW connection, by use of short, wide traces.

10.1.4 Boost Input Capacitor Placement

For the LM3697 device's boost converter, the input capacitor filters the inductor current ripple and the internal MOSFET driver currents during turnon of the internal power switch. The driver current requirement can range from 50 mA at 2.7 V to over 200 mA at 5.5 V with fast durations of approximately 10 ns to 20 ns. This appears as high di/dt current pulses coming from the input capacitor each time the switch turns on. Close placement of the input capacitor to the IN pin and to the GND in is critical because any series inductance between IN and CIN+ or CIN− and GND can create voltage spikes that could appear on the VIN supply line and in the GND plane.

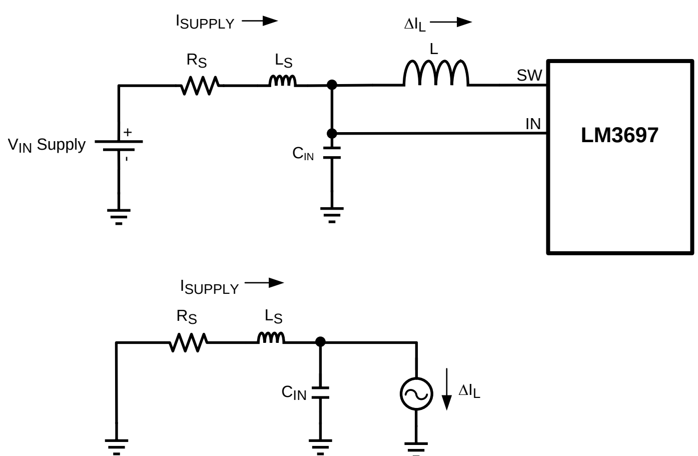
Layout Guidelines (continued)

Close placement of the input bypass capacitor at the input side of the inductor is also critical. The source impedance (inductance and resistance) from the input supply, along with the input capacitor of the LM3697, forms a series RLC circuit. If the output resistance from the source (R_S) is low enough the circuit is underdamped and has a resonant frequency (typically the case). Depending on the size of L_S the resonant frequency could occur below, close to, or above the switching frequency of the device. This can cause the supply current ripple to be:

1. Approximately equal to the inductor current ripple when the resonant frequency occurs well above the LM3697 device's switching frequency;
2. Greater than the inductor current ripple when the resonant frequency occurs near the switching frequency; or
3. Less than the inductor current ripple when the resonant frequency occurs well below the switching frequency.

Figure 58 shows the series RLC circuit formed from the output impedance of the supply and the input capacitor. The circuit is redrawn for the AC case where the V_{IN} supply is replaced with a short to GND, and the LM3697 + Inductor is replaced with a current source (ΔI_L). Equation 1 is the criteria for an underdamped response. Equation 2 is the resonant frequency. Equation 3 is the approximated supply current ripple as a function of L_S, R_S, and C_{IN}.

As an example, consider a 3.6-V supply with 0.1 Ω of series resistance connected to C_{IN} through 50 nH of connecting traces. This results in an underdamped input-filter circuit with a resonant frequency of 712 kHz. Because both the 1-MHz and 500-kHz switching frequency options lie close to the resonant frequency of the input filter, the supply current ripple is probably larger than the inductor current ripple. In this case, using equation 3, the supply current ripple can be approximated as 1.68 times the inductor current ripple (using a 500-kHz switching frequency) and 0.86 times the inductor current ripple using a 1-MHz switching frequency. Increasing the series inductance (L_S) to 500 nH causes the resonant frequency to move to around 225 kHz, and the supply current ripple to be approximately 0.25 times the inductor current ripple (500-kHz switching frequency) and 0.053 times for a 1-MHz switching frequency.



1. $$\frac{1}{L_S \times C_{IN}} > \frac{R_S^2}{4 \times L_S^2}$$

2. $$f_{RESONANT} = \frac{1}{2\pi\sqrt{L_S \times C_{IN}}}$$

3. $$I_{SUPPLYRIPPLE} \approx \Delta I_L \times \frac{\frac{1}{2\pi \times 500\,\text{kHz} \times C_{IN}}}{\sqrt{R_S^2 + \left(2\pi \times 500\,\text{kHz} \times L_S - \frac{1}{2\pi \times 500\,\text{kHz} \times C_{IN}}\right)^2}}$$

Figure 58. Input RLC Network

10.2 Layout Example

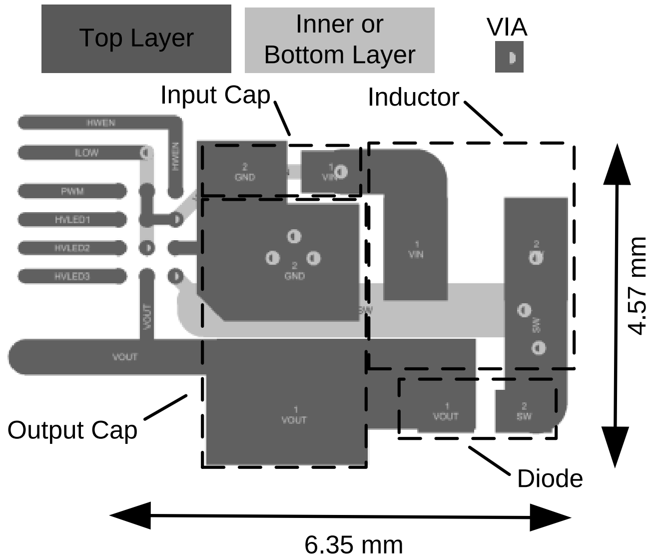


Figure 59. LM3697 Layout Example

11 器件和文档支持

11.1 器件支持

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11.2 相关文档

更多信息，请参见以下文档：

AN-1112 DSBGA 晶圆级芯片级封装

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11.7 术语表

SLYZ022 — *TI 术语表*。
这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3697YFQR	ACTIVE	DSBGA	YFQ	12	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	D8	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
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(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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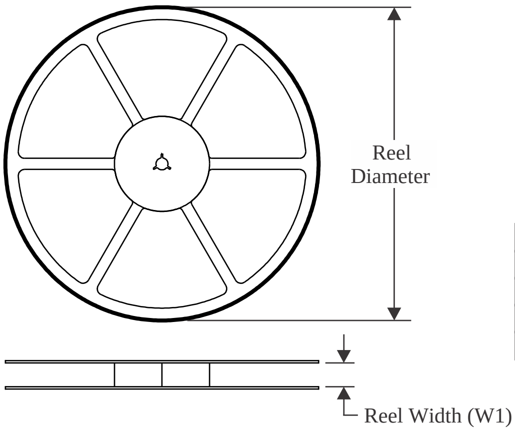
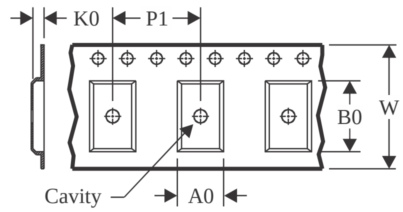
TAPE AND REEL INFORMATION

REEL DIMENSIONS

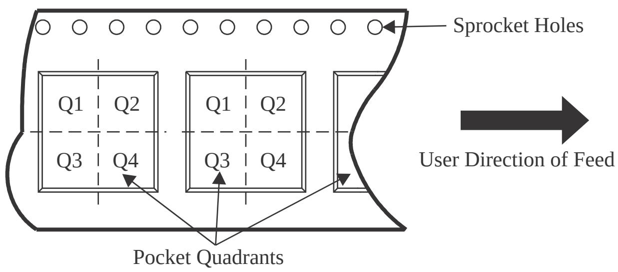


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

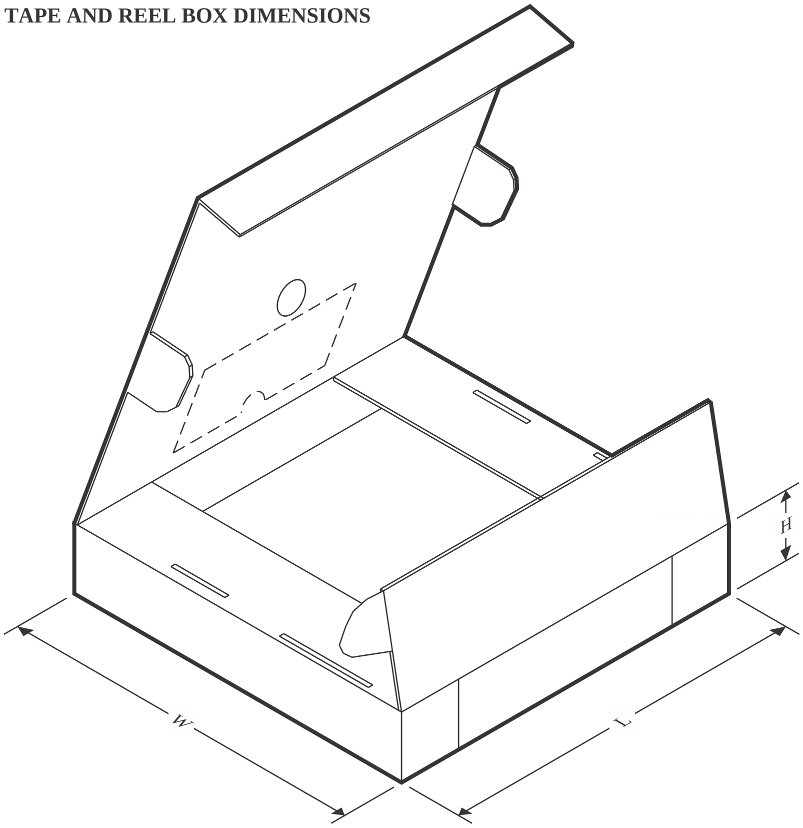
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3697YFQR	DSBGA	YFQ	12	3000	178.0	8.4	1.35	1.75	0.76	4.0	8.0	Q1
LM3697YFQR	DSBGA	YFQ	12	3000	178.0	8.4	1.38	1.78	0.78	4.0	8.0	Q1

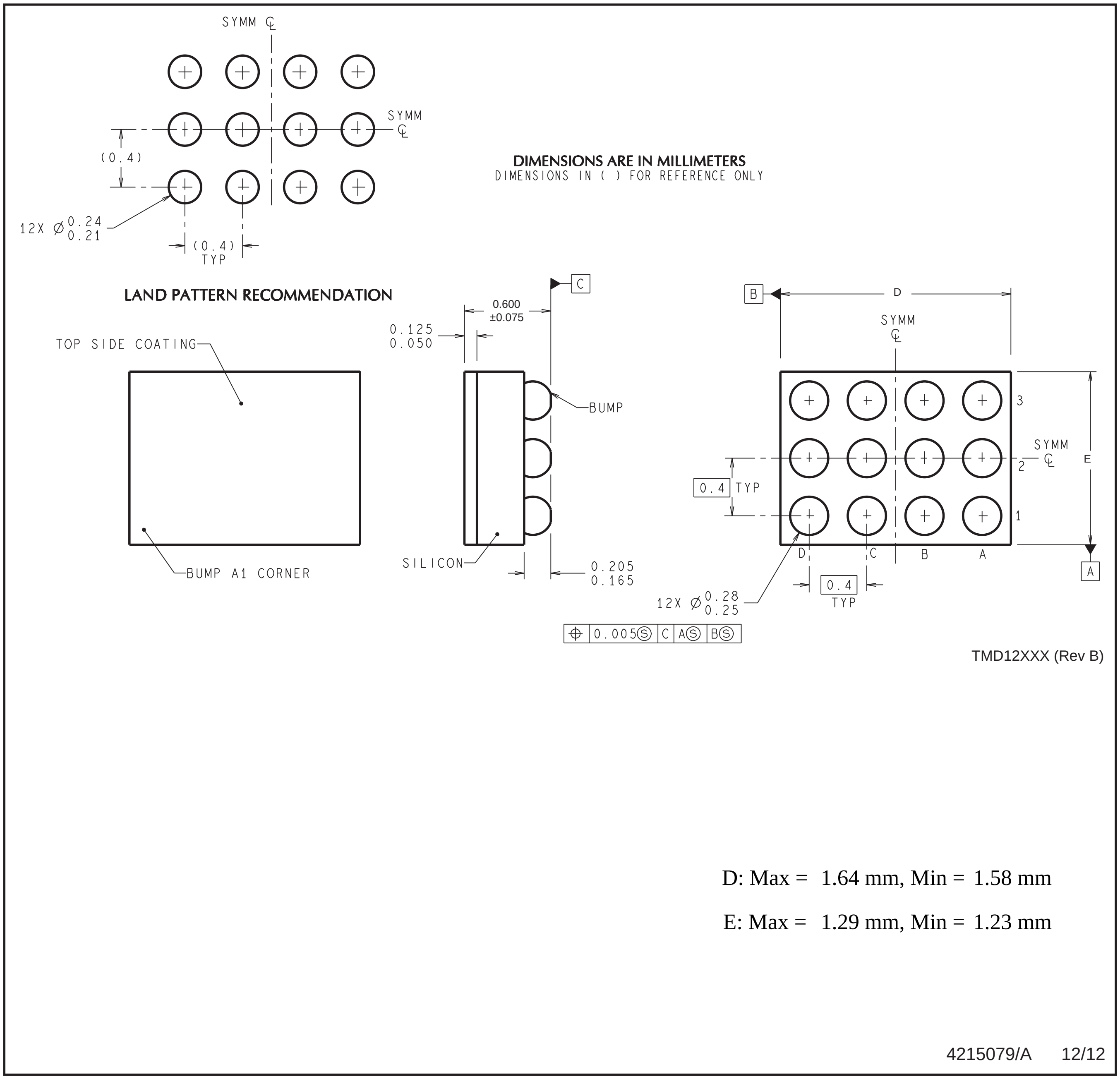
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3697YFQR	DSBGA	YFQ	12	3000	208.0	191.0	35.0
LM3697YFQR	DSBGA	YFQ	12	3000	220.0	220.0	35.0

YFQ0012



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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