具有集成时钟恢复器的 LMH0397 3G-SDI 双向 I/O

1 特性

- 带有集成时钟恢复器的用户可配置型自适应电缆均衡器或电缆驱动器
- 支持 ST-424 (3G)、ST-292 (HD) 和 ST-259 (SD)
- 兼容 DVB-ASI 和 AES10 (MADI)
- 集成时钟恢复器锁定为 2.97Gbps、1.485Gbps 或 1.001 分频子速率和 270Mbps 的 SMPTE 速率
- 片上 75Ω 终端和回损补偿网络
- EQ（均衡器）模式：
  - 带有集成时钟恢复器的自适应电缆均衡器
  - 具有去加重功能的 100Ω 输出驱动器
  - 时钟恢复型 75Ω 环通输出
  - EQ 模式电缆传输距离（Belden 1694A，禁用 SDI_OUT）：
    - 2.97Gbps 时为 200m
    - 1.485Gbps 时为 300m
    - 270Mbps 时为 600m
- CD（电缆驱动器）模式：
  - 带有集成时钟恢复器的双路差分输出电缆驱动器
  - 自适应 PCB 输入均衡器
  - 时钟恢复型 100Ω 环回输出
- 75Ω 输出端的自动预加重和转换率控制
- 75Ω 和 100Ω 输出端的极性反转
- 没有输入信号时自动进入省电工作模式
  - 功率耗散：25mW（典型值）
- 通过 ENABLE 引脚进行断电控制
- 2.5V 单电源
  - EQ 模式功耗：275mW（典型值）
  - CD 模式功耗：290mW（典型值）
- 可通过引脚、SPI 或 SMBus 接口进行编程
- 工作温度范围：-40°C 至 +85°C
- 5mm × 5mm 32 引脚 WQFN 封装
- 与 LMH1297 引脚兼容，便于轻松升级至 12G-SDI

2 应用

- SMPTE 兼容串行数字接口 (SDI)
- 广播视频路由器、交换机、分配放大器和监视器
- IP 媒体网关
- 数字视频处理和编辑

3 说明

LMH0397 是带有集成时钟恢复器的 3G SDI-SDI 75Ω 双向 I/O。此器件可以在输入模式下配置为自适应电缆均衡器，也可以在输出模式下配置为双电缆驱动器，允许系统设计人员灵活地将单个 BNC 用作输入或输出端口，从而简化 HD-SDI 视频硬件设计。集成的时钟恢复器在两种模式下均可锁定到所有支持的高达 2.97Gbps 的 SMPTE 数据速率。此双向 I/O 具有片上 75Ω 终端和回损补偿网络，满足严格的 SMPTE 回损要求。

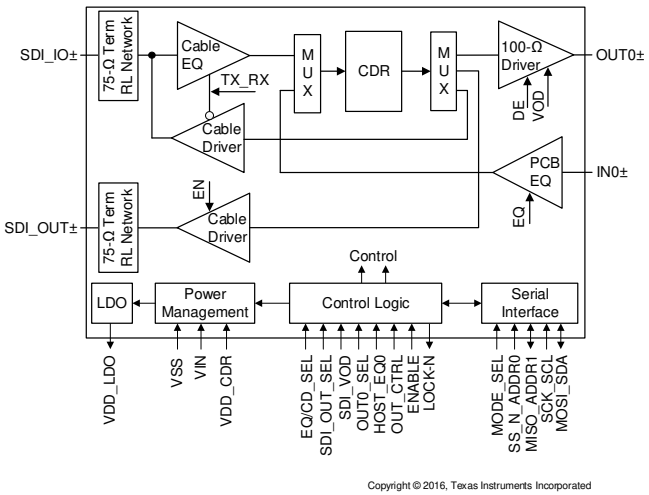
额外的 75Ω 驱动器输出可让 LMH0397 支持各种系统功能。在 EQ（均衡器）模式下，该第二个 75Ω 驱动器可用作环通输出。在电缆驱动器 (CD) 模式下，该 75Ω 驱动器可用作第二个扇出电缆驱动器。主机侧 100Ω 驱动器也可在 CD 模式下用作环回输出，从而用于监控。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
LMH0397	WQFN (32)	5.00mm × 5.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化方框图



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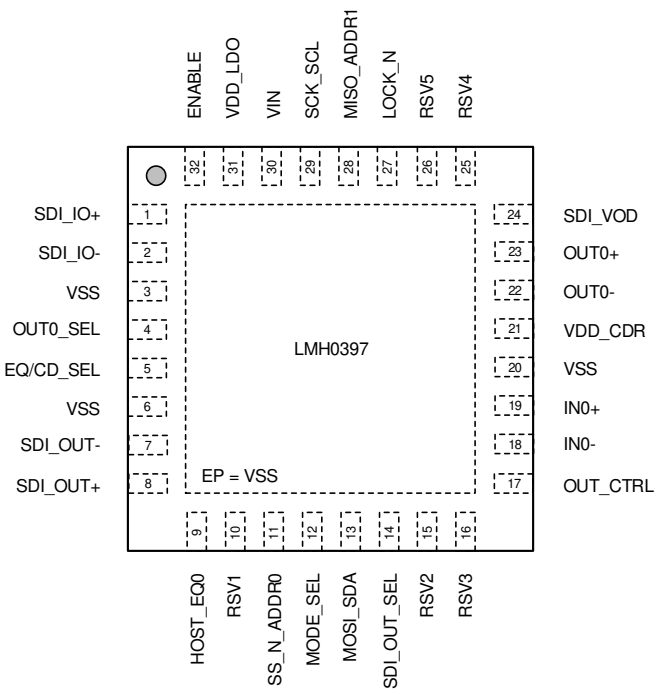
5 说明（续）

片上时钟恢复器可减弱高频抖动并使用纯净的低抖动时钟完全重新生成数据。此时钟恢复器具有内置环路滤波器，且不需要任何输入参考时钟。LMH0397 还有内部眼图张开度监视器和可编程引脚，以便进行 CDR 锁定指示、输入载波检测或硬件中断，从而支持系统诊断和电路板启动。

LMH0397 由 2.5V 单电源供电运行。该器件采用小尺寸 5mm × 5mm 32 引脚 WQFN 封装。LMH0397 还与 LMH1297 的引脚兼容。

6 Pin Configuration and Functions

RTV Package
32-Pin WQFN
Top View



Pin Functions

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
HIGH-SPEED DIFFERENTIAL I/OS			
SDI_IO+	1	I/O, Analog	Single-ended complementary inputs or outputs with on-chip 75-Ω termination at SDI_IO+ and SDI_IO–. SDI_IO± include integrated return loss networks designed to meet the SMPTE input and output return loss requirements. Connect SDI_IO+ to a BNC through a 4.7-µF, AC-coupling capacitor. SDI_IO– should be similarly AC-coupled and terminated with an external 4.7-µF capacitor and 75-Ω resistor to GND. **EQ Mode:** SDI_IO+ is the 75-Ω input port of the adaptive cable equalizer for SMPTE video applications. **CD Mode:** SDI_IO+ is the 75-Ω output port of the cable driver for SMPTE video applications.
SDI_IO–	2	I/O, Analog	
SDI_OUT+	8	O, Analog	Single-ended complementary outputs with on-chip 75-Ω termination at SDI_OUT+ and SDI_OUT–. SDI_OUT± include integrated return loss networks designed to meet the SMPTE output return loss requirements. SDI_OUT± is used as a second cable driver. Connect SDI_OUT+ to a BNC through a 4.7-µF, AC-coupling capacitor. SDI_OUT– should be similarly AC-coupled and terminated with an external 4.7-µF capacitor and 75-Ω resistor to GND. **EQ Mode:** SDI_OUT± can be enabled as a loop-through 75-Ω output port. It outputs the reclocked data from the adaptive cable equalizer to form a loop-through output with adaptive cable equalizer, reclocker, and cable driver. **CD Mode:** SDI_OUT± is the second 75-Ω fan-out cable driver.
SDI_OUT–	7	O, Analog	
IN0–	18	I, Analog	Differential inputs from host video processor. On-chip 100-Ω differential termination. Requires external 4.7-µF, AC-coupling capacitors for SMPTE applications.
IN0+	19	I, Analog	
OUT0–	22	O, Analog	Differential outputs to host video processor. On-chip 100-Ω differential termination. Requires external 4.7-µF, AC-coupling capacitors for SMPTE applications.
OUT0+	23	O, Analog	

(1) I = Input, O = Output, I/O = Input or Output, OD = Open Drain, LVCMOS = 2-State Logic, 4-LEVEL = 4-State Logic

Pin Functions (continued)

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
CONTROL PINS			
OUT0_SEL	4	I, LVCMOS	OUT0_SEL enables the use of the 100-Ω host-side output driver at OUT0±. See Table 3 for details. OUT0_SEL is internally pulled high by default (OUT0 disabled).
EQ/CD_SEL	5	I, LVCMOS	EQ/CD_SEL selects the signal direction of the LMH0397 bidirectional I/O. It configures the LMH0397 as an adaptive equalizer (EQ Mode) or as a cable driver (CD Mode). See Table 2 for details. EQ/CD_SEL is internally pulled low by default (EQ Mode).
HOST_EQ0	9	I, 4-LEVEL	HOST_EQ0 selects the driver output amplitude and de-emphasis level for OUT0± (in EQ Mode) and equalizer setting for IN0± (in CD Mode). See Table 5 and Table 10 for details.
MODE_SEL	12	I, 4-LEVEL	MODE_SEL enables the SPI or SMBus serial control interface. See Table 11 for details.
SDI_OUT_SEL	14	I, LVCMOS	SDI_OUT_SEL enables the use of the 75-Ω output driver at SDI_OUT±. See Table 3 for details. SDI_OUT_SEL is internally pulled high by default (SDI_OUT disabled).
OUT_CTRL	17	I, 4-LEVEL	OUT_CTRL selects the signal being routed to the output. It is used to enable or bypass the reclocker and to enable or bypass the cable equalizer. See Table 7 for details.
SDI_VOD	24	I, 4-LEVEL	SDI_VOD selects one of four output amplitudes for the cable drivers at SDI_IO± and SDI_OUT±. See Table 8 for details.
LOCK_N	27	O, LVCMOS, OD	LOCK_N is the reclocker lock indicator. LOCK_N is pulled low when the reclocker has acquired lock condition. LOCK_N is a 3.3-V tolerant, open-drain output. It requires an external resistor to a logic supply. LOCK_N can be reconfigured to indicate Carrier Detector (CD_N) or Interrupt (INT_N) through register programming. See *Status Indicators and Interrupts*.
ENABLE	32	I, LVCMOS	A logic-high at ENABLE enables normal operation for the LMH0397. A logic-low at ENABLE places the LMH0397 in Power-Down Mode. ENABLE is internally pulled high by default.
SPI SERIAL CONTROL INTERFACE, MODE_SEL = F (FLOAT)			
SS_N	11	I, LVCMOS	SS_N is the Slave Select. When SS_N is at logic Low, it enables SPI access to the LMH0397 slave device. SS_N is a 2.5-V LVCMOS input and is internally pulled high by default.
MOSI	13	I, LVCMOS	MOSI is the SPI serial control data input to the LMH0397 slave device when the SPI bus is enabled. MOSI is a 2.5-V LVCMOS input. An external pullup resistor is recommended.
MISO	28	O, LVCMOS	MISO is the SPI serial control data output from the LMH0397 slave device. MISO is a 2.5-V LVCMOS output.
SCK	29	I, LVCMOS	SCK is the SPI serial input clock to the LMH0397 slave device when the SPI interface is enabled. SCK is a 2.5-V LVCMOS input. An external pullup resistor is recommended.
SMBUS SERIAL CONTROL INTERFACE, MODE_SEL = L (1 KΩ TO VSS)			
ADDR0	11	Strap, 4-LEVEL	ADDR[1:0] are 4-level straps, read into the device at power up. They are used to select one of the 16 supported SMBus addresses when SMBus is enabled. See Table 12 for details.
SDA	13	I/O, LVCMOS, OD	SDA is the SMBus bidirectional data line to or from the LMH0397 slave device when SMBus is enabled. SDA is an open-drain I/O and requires an external pullup resistor to the SMBus termination voltage. SDA is 3.3-V tolerant.
ADDR1	28	Strap, 4-LEVEL	ADDR[1:0] are 4-level straps, read into the device at power up. They are used to select one of the 16 supported SMBus addresses when SMBus is enabled. See Table 12 for details.
SCL	29	I/O, LVCMOS, OD	SCL is the SMBus input clock to the LMH0397 slave device when SMBus is enabled. It is driven by a LVCMOS open-drain driver from the SMBus master. SCL requires an external pullup resistor to the SMBus termination voltage. SCL is 3.3-V tolerant.

Pin Functions (continued)

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
RESERVED			
RSV1	10	—	Reserved pins. Do not connect.
RSV2	15		
RSV3	16		
RSV4	25		
RSV5	26		
POWER			
VSS	3, 6, 20	I, Ground	Ground reference.
VDD_CDR	21	I, Power	VDD_CDR powers the reclocker circuitry. It is connected to the same 2.5-V ± 5% supply as VIN.
VIN	30	I, Power	VIN is connected to an external 2.5-V ± 5% power supply.
VDD_LDO	31	O, Power	VDD_LDO is the output of the internal 1.8-V LDO regulator. VDD_LDO output requires an external 1-µF and 0.1-µF bypass capacitor to VSS. The internal LDO is designed to power internal circuitry only.
EP	—	I, Ground	EP is the exposed pad at the bottom of the RTV package. The exposed pad should be connected to the VSS plane through a 3 × 3 via array.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Supply voltage (VIN, VDD_CDR)	–0.5	2.75	V
Input voltage for 4-level pins	–0.5	2.75	V
Input or output voltage for 2-level control pins	–0.5	2.75	V
SMBus input or output voltage (SDA, SCL)	–0.5	4	V
SPI input or output voltage (SS_N, MISO, MOSI, and SCK)	–0.5	2.75	V
High-speed input or output voltage (IN0±, SDI_IO±, OUT0±, SDI_OUT±)	–0.5	2.75	V
Input current (IN0±, SDI_IO±)	–30	30	mA
Operating junction temperature		125	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins except 13 and 29	±6000	V
		Pins 13 and 29	±5500	
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
	Supply voltage	VIN, VDD_CDR to VSS	2.375	2.5	2.625	V
VDD_{SMBUS}	SMBus: SDA, SCL open-drain termination voltage		2.375		3.6	V
$V_{SDI\_IO\_LAUNCH}$	Source launch amplitude before coaxial cable to SDI_IO+	Normal mode	0.72	0.8	0.88	Vp-p
		Splitter mode	0.36	0.4	0.44	
V_{IN0_LAUNCH}	Source differential launch amplitude		300	500	1000	mVp-p
$T_{JUNCTION}$	Operating junction temperature				110	°C
$T_{AMBIENT}$	Ambient temperature		–40	25	85	°C
$NTps_{max}$	Maximum supply noise(1)	50 Hz to 1 MHz, sinusoidal		< 20		mVp-p
		1.1 MHz to 50 MHz, sinusoidal		< 10		

(1) The sum of the DC supply voltage and AC supply noise must not exceed the recommended supply voltage range.

7.4 Thermal Information

THERMAL METRIC(1)		LMH0397 RTV (WQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	6.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER						
PD_{EQ_MODE}	Power dissipation, EQ Mode, Measured with PRBS10, CDR Locked to 2.97 Gbps, VOD = default, HEO/VEO lock monitor disabled	SDI_OUT± disabled OUT0± enabled		275		mW
		SDI_OUT± enabled OUT0± enabled		405		mW
PD_{CD_MODE}	Power dissipation, CD Mode, Measured with PRBS10, CDR Locked to 2.97 Gbps, VOD = default, HEO/VEO lock monitor disabled	SDI_IO± enabled SDI_OUT± disabled OUT0± disabled		290		mW
		SDI_IO± enabled SDI_OUT± disabled OUT0± enabled		335		mW
		SDI_IO± enabled SDI_OUT± enabled OUT0± disabled		415		mW
		SDI_IO± enabled SDI_OUT± enabled OUT0± enabled		460		mW
PD_Z	Power dissipation, Power Save Mode	EQ Mode, Power Save Mode, ENABLE = H, no signal applied at SDI_IO+		25		mW
		CD Mode, Power Save Mode, ENABLE = H, no signal applied at IN0±		25		
IDD_{EQ_MODE}	Current consumption, EQ Mode, Measured with PRBS10, CDR Locked to 2.97 Gbps, VOD = default, HEO/VEO lock monitor disabled	SDI_OUT± disabled OUT0± enabled		110	131	mA
		SDI_OUT± enabled OUT0± enabled		162	191	mA
IDD_{CD_MODE}	Current consumption, CD Mode, Measured with PRBS10, CDR Locked to 2.97 Gbps, VOD = default, HEO/VEO lock monitor disabled CD Mode	SDI_IO± enabled SDI_OUT± disabled OUT0± disabled		116	137	mA
		SDI_IO± enabled SDI_OUT± disabled OUT0± enabled		134	157	mA
		SDI_IO± enabled SDI_OUT± enabled OUT0± disabled		166	196	mA
		SDI_IO± enabled SDI_OUT± enabled OUT0± enabled		184	217	mA

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IDD_Z	Current consumption, Power Save Mode	EQ Mode, Power Save Mode, ENABLE = H, no signal applied at SDI_IO+		10		mA
		CD Mode, Power Save Mode, ENABLE = H, no signal applied at IN0±		10		
IDD_{Z_PD}	Current consumption, Power-Down Mode	EQ Mode, Power-Down Mode, ENABLE = L, no signal applied at SDI_IO+		10	30	mA
		CD Mode, Power-Down Mode, ENABLE = L, no signal applied at IN0±		10	30	
IDD_{TRANS_EQ}	Current consumption, EQ Mode CDR acquiring lock to 2.97 Gbps, VOD = default, HEO/VEO lock monitor enabled	SDI_OUT± disabled OUT0± enabled			189	mA
		SDI_OUT± enabled OUT0± enabled			257	mA
IDD_{TRANS_CD}	Current consumption, CD Mode CDR acquiring lock to 2.97 Gbps, VOD = default, HEO/VEO lock monitor enabled	SDI_IO± enabled SDI_OUT± disabled OUT0± disabled			200	mA
		SDI_IO± enabled SDI_OUT± disabled OUT0± enabled			222	mA
		SDI_IO± enabled SDI_OUT± enabled OUT0± disabled			271	mA
		SDI_IO± enabled SDI_OUT± enabled OUT0± enabled			290	mA
LVCMOS DC SPECIFICATIONS						
V_{IH}	Logic high input voltage	2-level input (SS_N, SCK, MOSI, EQ/CD_SEL, SDI_OUT_SEL, OUT0_SEL, ENABLE)	0.72 × VIN		VIN + 0.3	V
		2-level input (SCL, SDA)	0.7 × VIN		3.6	
V_{IL}	Logic low input voltage	2-level input (SS_N, SCK, MOSI, EQ/CD_SEL, SDI_OUT_SEL, OUT0_SEL, ENABLE, SCL, SDA)	0		0.3 × VIN	V
V_{OH}	Logic high output voltage	IOH = –2 mA, (MISO)	0.8 × VIN		VIN	V
V_{OL}	Logic low output voltage	IOL = 2 mA, (MISO)	0		0.2 × VIN	V
		IOL = 3 mA, (LOCK_N, SDA)			0.4	
I_{IH}	Input high leakage current (Vinput = VIN)	LVCMOS (EQ/CD_SEL, SDI_OUT_SEL, ENABLE)			15	µA
		LVCMOS (OUT0_SEL)			65	
		LVCMOS (LOCK_N)			10	
		SPI mode: LVCMOS (SS_N, SCK, MOSI)			15	
		SMBus mode: LVCMOS (SCL, SDA)			10	
I_{IL}	Input low leakage current (Vinput = GND)	LVCMOS (EQ/CD_SEL, SDI_OUT_SEL, ENABLE)	–50			µA
		LVCMOS (OUT0_SEL)	–15			
		LVCMOS (LOCK_N)	–10			
		SPI mode: LVCMOS (SCK, MOSI)	–15			
		SPI mode: LVCMOS (SS_N)	–50			
		SMBus mode: LVCMOS (SCL, SDA)	–10			

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
4-LEVEL LOGIC DC SPECIFICATIONS (APPLY TO ALL 4-LEVEL INPUT CONTROL PINS)						
V_{LVL_H}	LEVEL-H input voltage	Measured voltage at 4-level pin with external 1 kΩ to VIN		VIN		V
V_{LVL_F}	LEVEL-F default voltage	Measured voltage 4-level pin at default		2/3 × VIN		V
V_{LVL_R}	LEVEL-R input voltage	Measured voltage at 4-level pin with external 20 kΩ to VSS		1/3 × VIN		V
V_{LVL_L}	LEVEL-L input voltage	Measured voltage at 4-level pin with external 1 kΩ to VSS		0		V
I_{IH}	Input high leakage current (Vinput = VIN)	4-levels (HOST_EQ0, MODE_SEL, OUT_CTRL, SDI_VOD)	20	45	80	µA
		SMBus mode: 4-levels (ADDR0, ADDR1)	20	45	80	
I_{IL}	Input low leakage current (Vinput = GND)	4-levels (HOST_EQ0, MODE_SEL, OUT_CTRL, SDI_VOD)	–160	–93	–40	µA
		SMBus mode: 4-levels (ADDR0, ADDR1)	–160	–93	–40	
RECEIVER SPECIFICATIONS (SDI_IO+, EQ MODE)						
$R_{SDI\_IO\_TERM}$	DC input single-ended termination	SDI_IO+ and SDI_IO– to internal common mode bias	63	75	87	Ω
$RL_{SDI\_IO\_S11}$	Input return loss at SDI_IO+ reference to 75 Ω(1)	S11, 5 MHz to 1.485 GHz		–30		dB
		S11, 1.485 GHz to 3 GHz		–22		
$V_{SDI\_IO\_CM}$	SDI_IO+ DC common-mode voltage	Input DC common-mode voltage at SDI_IO+ or SDI_IO– to GND		1.4		V
$V_{SDI\_IO\_WANDER}$	Input DC wander	SD, input signal at SDI_IO+, Input launch amplitude = 800 mVp-p		100		mVp-p
		HD, 3G input signal at SDI_IO+, Input launch amplitude = 800 mVp-p		50		
RECEIVER SPECIFICATIONS (IN0±, CD MODE)						
R_{IN0_TERM}	DC input differential termination	Measured across IN0+ to IN0–	80	100	120	Ω
RL_{IN0_SDD11}	Input differential return loss(1)	SDD11, 10 MHz to 2.8 GHz		–22		dB
RL_{IN0_SCD11}	Differential to common-mode input conversion(1)	SCD11, 10 MHz to 11.1 GHz		–21		dB
V_{IN0_CM}	DC common-mode voltage	Input common-mode voltage at IN0+ or IN0– to GND		2.06		V
CD_{ON_IN0}	Signal detect (default) Assert ON threshold level for IN0±	2.97 Gbps, EQ and PLL pathological pattern		20		mVp-p
CD_{OFF_IN0}	Signal detect (default) Deassert OFF threshold level for IN0±	2.97 Gbps, EQ and PLL pathological pattern		18		mVp-p
DRIVER OUTPUT (SDI_IO+ AND SDI_OUT+, CD MODE)						
R_{OUT_TERM}	DC output single-ended termination	SDI_IO+ and SDI_IO–, SDI_OUT+ and SDI_OUT– to VIN	63	75	87	Ω
VOD_{CD_OUTP}	Output single-ended voltage	Measure AC signal at SDI_IO+ and SDI_OUT+, with SDI_IO– and SDI_OUT– AC terminated with 75 Ω SDI_VOD = H		840		mVp-p
		SDI_VOD = F	720	800	880	
		SDI_VOD = R		880		
		SDI_VOD = L		760		

(1) This parameter is measured with the LMH1297EVM (Evaluation board for LMH0397).

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOD_{CD_OUTN}	Output single-ended voltage	Measure AC signal at SDI_IO– and SDI_OUT-, with SDI_IO+ and SDI_OUT+ AC terminated with 75 Ω SDI_VOD = H		840		mVp-p
		SDI_VOD = F	720	800	880	
		SDI_VOD = R		880		
		SDI_VOD = L		760		
PRE_{CD_OUTP}	Output pre-emphasis	Output pre-emphasis boost amplitude at SDI_IO+ and SDI_OUT+, programmed to maximum setting through register, measured at SDI_VOD=F		2		dB
PRE_{CD_OUTN}	Output pre-emphasis	Output pre-emphasis boost amplitude at SDI_IO– and SDI_OUT–, programmed to maximum setting through register, measured at SDI_VOD=F		2		dB
$t_{R\_F\_SDI}$	Output rise and fall time(1)	Measured with PRBS10 pattern, default VOD at 20% – 80% amplitude, default pre-emphasis enabled 2.97 Gbps		59	67	ps
		1.485 Gbps		60	73	
		270 Mbps	400	550	700	
$t_{R\_F\_DELTA}$	Output rise and fall time mismatch(1)	Measured with PRBS10 pattern, default VOD at 20% – 80% amplitude, default pre-emphasis enabled 2.97 Gbps		0.8	11	ps
		1.485 Gbps		0.8	12	
		270 Mbps		72	150	
$V_{OVERSHOOT}$	Output overshoot or undershoot	Measured with PRBS10 pattern, default VOD, default pre-emphasis enabled(2) 3G/HD/SD		5%		
V_{DC_OFFSET}	DC offset	3G/HD/SD		±0.2		V
V_{DC_WANDER}	DC wander	3G/HD/SD with EQ pathological pattern		20		mV
RL_{CD_S22}	Output return loss at SDI_IO+ and SDI_OUT+ reference to 75 Ω(1)	S22, 5 MHz to 1.485 GHz		–25		dB
		S22, 1.485 GHz to 3 GHz		–22		dB
DRIVER OUTPUT (OUT0±, EQ AND CD MODE)						
R_{OUT0_TERM}	DC output differential termination	Measured across OUT0+ and OUT0–	80	100	120	Ω
VOD_{OUT0}	Output differential voltage at OUT0±	Measured with 8T pattern HOST_EQ0 = H		410		mVp-p
		HOST_EQ0 = F	485	560	620	
		HOST_EQ0 = R		635		
		HOST_EQ0 = L		810		
VOD_{OUT0_DE}	De-emphasized output differential voltage at OUT0±	Measured with 8T pattern HOST_EQ0 = H		410		mVp-p
		HOST_EQ0 = F		550		
		HOST_EQ0 = R		545		
		HOST_EQ0 = L		532		
t_R/t_F	Output rise and fall time	Measured with 8T Pattern, 20% to 80% amplitude		45		ps

(2) $V_{OVERSHOOT}$ overshoot or undershoot maximum measurements are largely affected by the PCB layout and input test pattern. The maximum value specified in *Electrical Characteristics* for $V_{OVERSHOOT}$ is based on bench evaluation across temperature and supply voltages with the LMH1297EVM.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$RL_{OUT0-SDD22}$	Output differential return loss(1)	Measured with the device powered up and outputs a 10-MHz clock signal. SDD22, 10 MHz to 2.8 GHz		–24		dB
$RL_{OUT0-SCC22}$	Output common-mode return loss(1)	Measured with the device powered up and outputs a 10-MHz clock signal. SCC22, 10 MHz to 4.75 GHz		–12		dB
V_{OUT0_CM}	AC common-mode voltage on OUT0±(1)	Default setting, PRBS31, 2.97 Gbps		8		mV (rms)
RECLOCKER OUTPUT JITTER (EQ MODE)						
TJ_{EQ_MODE}	Total jitter, reclocked output(1)	Measured at OUT0±, with SDI_OUT disabled (BER ≤ 1E-12), PRBS10, TX launch amplitude = 800 mVp-p before cable to SDI_IO+ 2.97 Gbps: 200-m Belden 1694A		0.1		UIp-p
		1.485 Gbps: 300-m Belden 1694A		0.1		
		270 Mbps: 600-m Belden 1694A		0.11		
TJ_{RAW}	Total jitter, with CDR bypassed	Measured at OUT0±, with SDI_OUT disabled (BER ≤ 1E-12), PRBS10, TX launch amplitude = 800 mVp-p before cable to SDI_IO+ 125 Mbps: 600-m Belden 1694A		0.2		UIp-p
RECLOCKER OUTPUT JITTER (CD MODE)						
AJ_{CD_MODE}	Alignment jitter(1)	Measured at SDI_IO+ and SDI_OUT+, OUT0± disabled PRBS10, 3G/HD/SD		0.1	0.14	UI
TMJ_{CD_MODE}	Timing jitter(1)	Measured at SDI_IO+ and SDI_OUT+, OUT0± disabled PRBS10, 3G/HD/SD		0.45		UI
RECLOCKER SPECIFICATIONS (EQ MODE UNLESS OTHERWISE SPECIFIED)						
$LOCK_{RATE}$	Reclocker lock data rates	SMPTE 3G, /1		2.97		Gbps
		SMPTE 3G, /1.001		2.967		
		SMPTE HD, /1		1.485		
		SMPTE HD, /1.001		1.4835		
		SMPTE SD, /1		270		Mbps
$BYPASS_{RATE}$	Reclocker automatically goes to bypass	MADI		125		Mbps
BW_{PLL}	PLL Bandwidth	Applied 0.2 UI input sinusoidal jitter, measure –3-dB bandwidth on input-to-output jitter transfer 2.97 Gbps		5		MHz
		1.485 Gbps		3		
		270 Mbps		1		
$J_{PEAKING}$	PLL jitter peaking	2.97 Gbps, 1.485 Gbps, 270 Mbps		<0.3		dB
J_{TOL_IN}	SDI_IO+ input jitter tolerance	Sinusoidal jitter tolerance, tested at 3G, SJ amplitude swept from 1 MHz to 80 MHz, tested at BER ≤ 1E-12, cable equalizer at SDI_IO+ bypassed		0.65		UI
T_{LOCK}	Lock time	SMPTE supported data rates, disable HEO/VEO monitor, cable equalizer at SDI_IO+ bypassed		5		ms
T_{ADAPT}	EQ adapt time at EQ Mode	Adaptation time for cable equalizer at SDI_IO+, reclocker bypassed		5		ms
$TEMP_{LOCK}$	VCO temperature lock range	Measured with temperature ramp of 5°C per minute, ramp up and down, –40°C to 85°C operating range at 2.97 Gbps		125		°C

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$TLAT_{EQ\_MODE}$	Reclocker latency at EQ Mode	Measured from SDI_IO+ to OUT0, 2.97 Gbps, SDI_IO+, 75-m Belden 1694A at SDI_IO+		1.4 UI + 465		ps
		Measured from SDI_IO+ to SDI_OUT+, 2.97 Gbps, SDI_IO+, 75-m Belden 1694A at SDI_IO+		1.7 UI + 415		
$TLAT_{CD\_MODE}$	Reclocker latency at CD Mode	Measured from IN0± to SDI_IO+, 2.97 Gbps		1.5 UI + 175		ps
		Measured from IN0± to SDI_OUT+, 2.97 Gbps		1.6 UI + 130		

7.6 Recommended SMBus Interface Timing Specifications

over recommended operating supply and temperature ranges unless otherwise specified(1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
F_{SCL}	SMBUS SCL frequency		10		400	kHz
T_{BUF}	Bus free time between stop and start condition	See Figure 1.	1.3			µs
$T_{HD:STA}$	Hold time after (repeated) start condition.	After this period, the first clock is generated.	0.6			µs
$T_{SU:STA}$	Repeated start condition setup time	See Figure 1.	0.6			µs
$T_{SU:STO}$	Stop condition setup time	See Figure 1.	0.6			µs
$T_{HD:DAT}$	Data hold time	See Figure 1.	0			ns
$T_{SU:DAT}$	Data setup time	See Figure 1.	100			ns
T_{LOW}	Clock low period	See Figure 1.	1.3			µs
T_{HIGH}	Clock high period	See Figure 1.	0.6			µs
T_R	Clock and data rise time	See Figure 1.			300	ns
T_F	Clock and data fall time	See Figure 1.			300	ns
T_{POR}	SMBus ready time after POR	Time from minimum VDDIO to SMBus valid write or read access			50	ms

(1) These parameters support SMBus 2.0 specifications.

7.7 Serial Parallel Interface (SPI) Timing Specifications

over recommended operating supply and temperature ranges unless otherwise specified(1)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
F_{SCK}	SPI SCK frequency				20	MHz
T_{PH}	SCK pulse width high	See Figure 2 and Figure 3.	40			% SCK period
T_{PL}	SCK pulse width low		40			% SCK period
T_{SU}	MOSI setup time	See Figure 2 and Figure 3.	4			ns
T_H	MOSI hold time		4			ns
T_{SSSU}	SS setup time	See Figure 2 and Figure 3.	14			ns
T_{SSH}	SS hold time		4			ns
T_{SSOF}	SS off time		1			µs
T_{ODZ}	MISO driven-to-tristate time	See Figure 2 and Figure 3.		20		ns
T_{OZD}	MISO tristate-to-driven time			10		ns
T_{OD}	MISO output delay time			15		ns

(1) Typical SPI load capacitance is 2 pF.

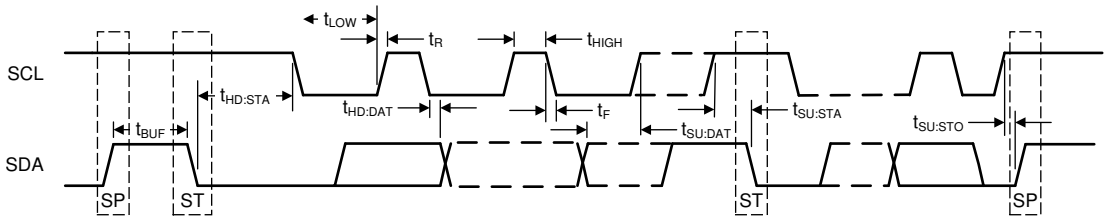


Figure 1. SMBus Timing Parameters

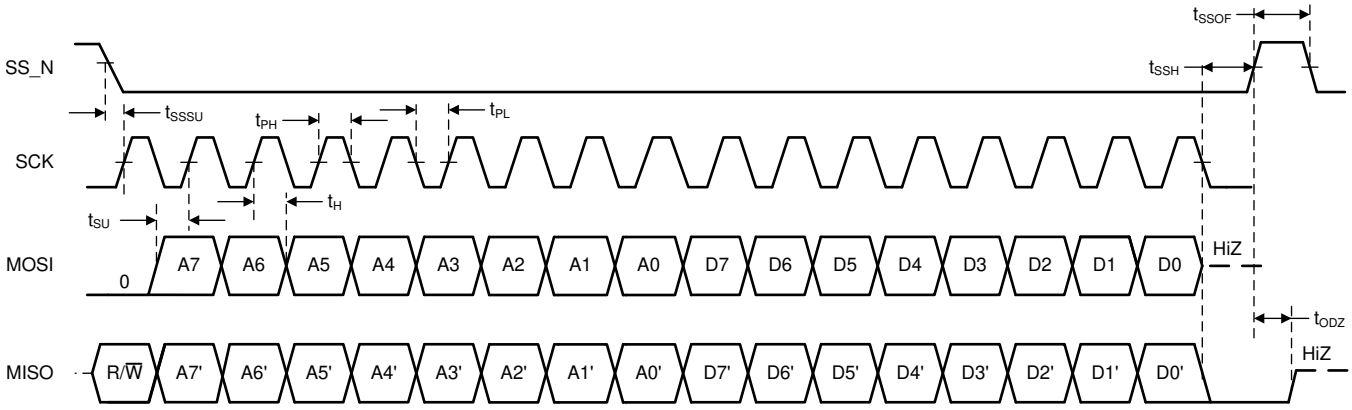


Figure 2. SPI Timing Parameters (Write Operation)

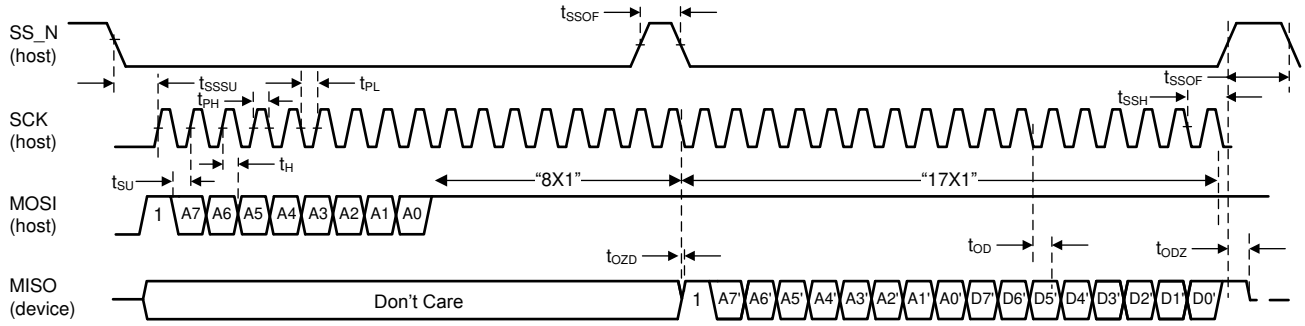


Figure 3. SPI Timing Parameters (Read Operation)

7.8 Typical Characteristics

T_A = 25°C and VIN = VDD_CDR = 2.5 V (unless otherwise noted)

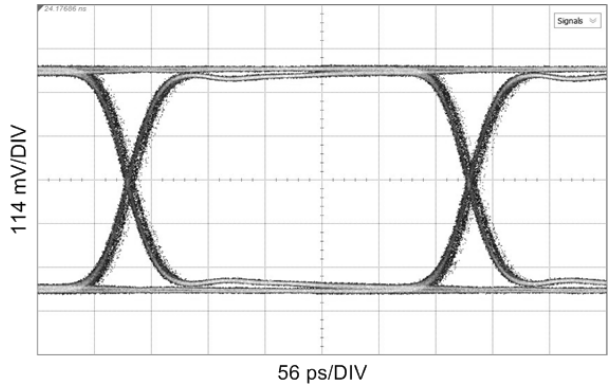


Figure 4. EQ Mode at 2.97 Gbps, Measured at OUT0±, 200-m Belden 1694A Before SDI_IO+

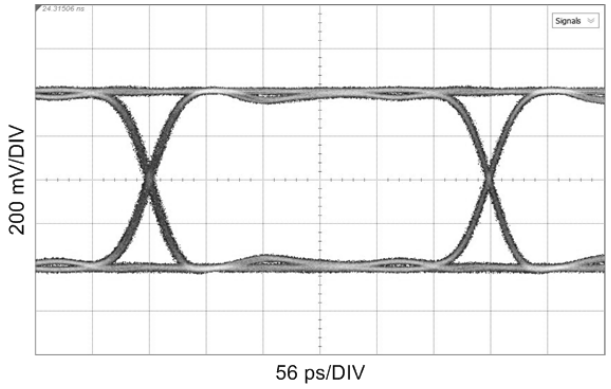


Figure 5. CD Mode at 2.97 Gbps, Measured at SDI_IO+, 20-in. FR4 Before IN0±

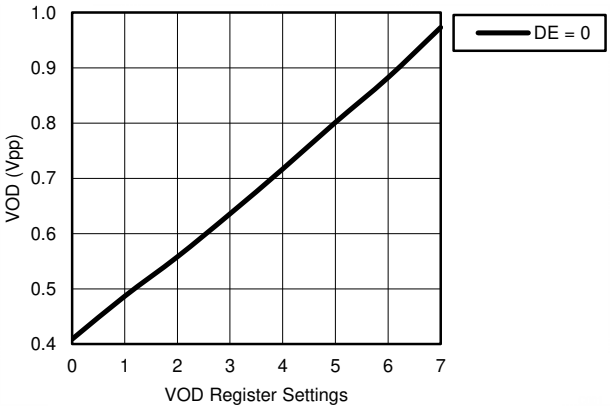


Figure 6. OUT0 VOD vs. OUT0 VOD and DE Register Settings

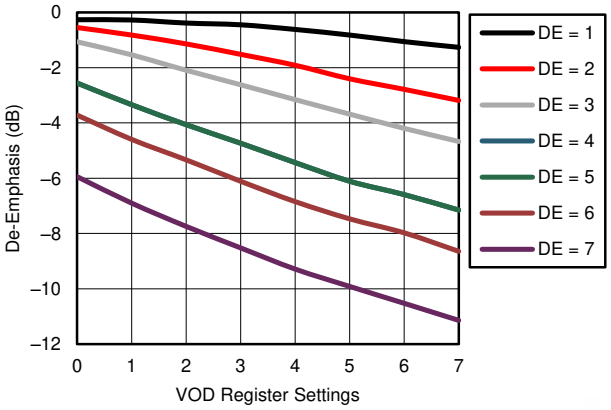
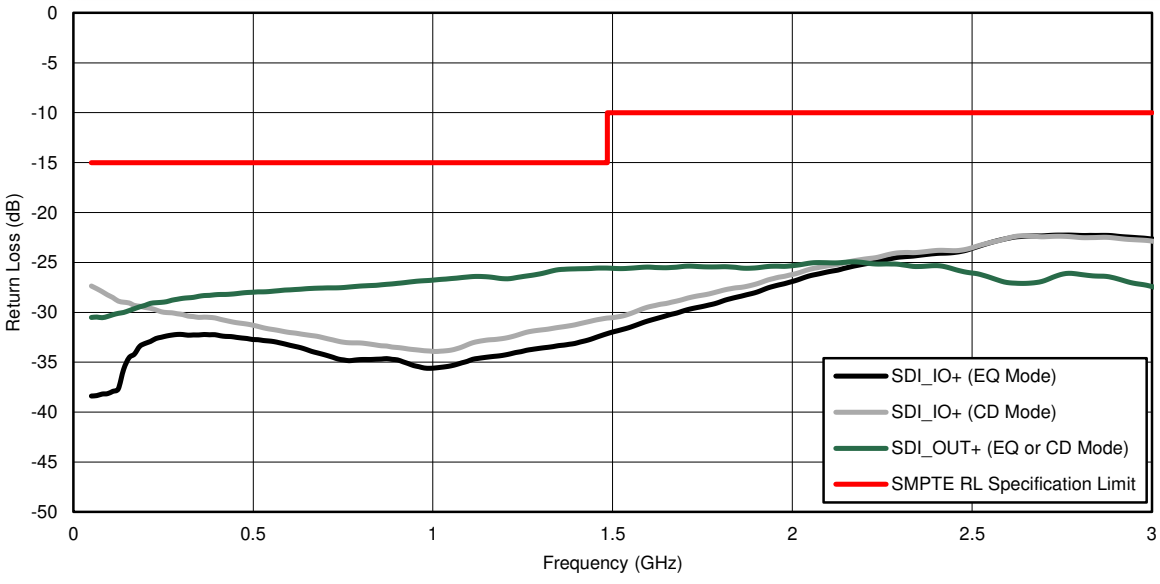


Figure 7. OUT0 De-Emphasis vs. OUT0 VOD and DE Register Settings



Measured with LMH1297EVM

Figure 8. Return Loss (RL) vs Frequency

8 Detailed Description

8.1 Overview

The LMH0397 is a 3G-SDI 75-Ω bidirectional I/O with integrated reclocker. The LMH0397 allows system designers the flexibility to use a single BNC either as an input or output port, simplifying HD video hardware designs.

8.1.1 Equalizer Mode (EQ Mode)

SDI_IO+ is configured as a 75-Ω adaptive cable equalizer. The input signal then goes through a reclocker, followed by a 100-Ω driver with de-emphasis at OUT0±. A second 75-Ω cable driver provides a reclocked loop-through output of SDI_IO+ at SDI_OUT+. This second signal path from SDI_IO+ to SDI_OUT+ forms a SDI cable loop-through.

8.1.2 Cable Driver Mode (CD Mode)

SDI_IO+ is configured as a 75-Ω cable driver with a reclocked signal sourced from IN0±. SDI_OUT+ serves as a second 75-Ω cable driver to offer 1:2 fan-out buffering from IN0± to SDI_IO+ and SDI_OUT+. The 100-Ω driver at OUT0± can be used as a host-side loopback output for monitoring purposes.

8.2 Functional Block Diagram

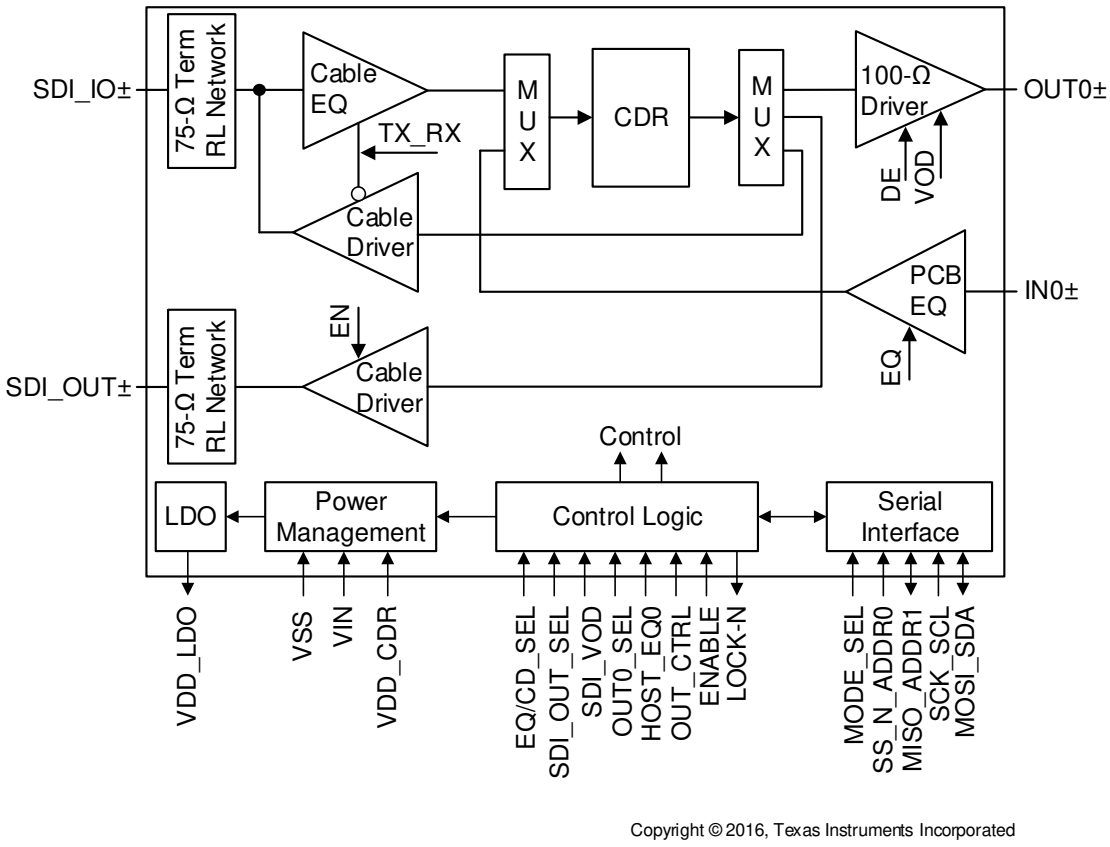


Figure 9. LMH0397 Block Diagram Overview

NOTE

Only one I/O path can be active at a time. In EQ Mode, the cable equalizer at SDI_IO is enabled, and the SDI_IO cable driver is powered down. In CD Mode, the cable driver at SDI_IO is enabled, and the SDI_IO cable equalizer is powered down.

8.3 Feature Description

The LMH0397 data path consists of several key blocks as shown in the functional block diagram. These key blocks are:

- *4-Level Input Pins and Thresholds*
- *Equalizer (EQ) and Cable Driver (CD) Mode Control*
- *Input Carrier Detect*
- *–6-dB Splitter Mode Launch Amplitude for SDI_IO+ (EQ Mode Only)*
- *Continuous Time Linear Equalizer (CTLE)*
- *Clock and Data (CDR) Recovery*
- *Internal Eye Opening Monitor (EOM)*
- *Output Function Control*
- *Output Driver Control*
- *Status Indicators and Interrupts*

8.3.1 4-Level Input Pins and Thresholds

The 4-level input configuration pins use a resistor divider to provide four logic states for each control pin. There is an internal 30-kΩ pullup and a 60-kΩ pulldown connected to the control pin that sets the default voltage at 2/3 × VIN. These resistors, together with the external resistor, combine to achieve the desired voltage level. By using the 1-kΩ pulldown, 20-kΩ pulldown, no connect, and 1-kΩ pullup, the optimal voltage levels for each of the four input states are achieved as shown in Table 1.

Table 1. 4-Level Control Pin Settings

LEVEL	SETTING	NOMINAL PIN VOLTAGE
H	Tie 1 kΩ to VIN	VIN
F	Float (leave pin open)	2/3 × VIN
R	Tie 20 kΩ to VSS	1/3 × VIN
L	Tie 1 kΩ to VSS	0

Typical 4-Level Input Thresholds:

- Internal Threshold between L and R = 0.2 × VIN
- Internal Threshold between R and F = 0.5 × VIN
- Internal Threshold between F and H = 0.8 × VIN

8.3.2 Equalizer (EQ) and Cable Driver (CD) Mode Control

The input and output signal flow of the LMH0397 is determined by the EQ/CD_SEL, OUT0_SEL, and SDI_OUT_SEL pins.

8.3.2.1 EQ/CD_SEL Control

The EQ/CD_SEL pin selects the I/O as either an input (EQ Mode) or an output (CD Mode). The logic level applied to the EQ/CD_SEL pin automatically powers down the unused I/O direction. For example, if the LMH0397 is in EQ Mode (EQ/CD_SEL = L), the SDI_IO cable driver is powered down as shown in Table 2.

Table 2. EQ/CD_SEL Pin Settings

EQ/CD_SEL	INPUT	MODE	NOTES
L	SDI_IO+	EQ Mode	75-Ω video input to SDI_IO+. OUT0± automatically enabled. SDI_IO Cable Driver powered down.
H	IN0±	CD Mode	100-Ω input to IN0±. SDI_IO+ enabled as a cable driver output. SDI_OUT programmable as a secondary cable driver output. SDI_IO Equalizer powered down.

The EQ/CD_SEL pin should be strapped at power up for normal operation. After power up, the EQ/CD_SEL pin state can be dynamically changed from EQ Mode to CD Mode and vice versa. When changing the EQ/CD_SEL state after power up, the signal flow to the reclocker is momentarily disturbed, and the chip automatically initiates a CDR reset to relock to the new input signal.

8.3.2.2 OUT0_SEL and SDI_OUT_SEL Control

The OUT0_SEL and SDI_OUT_SEL pins work in conjunction with the EQ/CD_SEL pin to select the LMH0397 data-path routes. Table 3 shows all possible signal path combinations and typical use cases for each configuration.

Table 3. LMH0397 Signal Path Combinations

EQ/CD_SEL (MODE)	OUT0_SEL	SDI_OUT_SEL	INPUT	MAIN OUTPUT	LINE SIDE LOOP-THRU OUTPUT	HOST SIDE LOOPBACK OUTPUT	TYPICAL APPLICATION
L (EQ Mode)	X	H	SDI_IO+	OUT0±			Adaptive cable equalizer
	X	L	SDI_IO+	OUT0±	SDI_OUT±		Adaptive cable equalizer with line-side loop-through output
H (CD Mode)	H	H	IN0±	SDI_IO±			Single cable driver
	H	L	IN0±	SDI_IO±	SDI_OUT±		Dual cable drivers
	L	H	IN0±	SDI_IO±		OUT0±	Single cable driver with host-side loopback enabled
	L	L	IN0±	SDI_IO±	SDI_OUT±	OUT0±	Dual cable drivers with host-side loopback enabled

8.3.3 Input Carrier Detect

SDI_IO (in EQ Mode) and IN0 have a carrier detect circuit to monitor the presence or absence of an input signal. When the input signal amplitude for the selected input exceeds the carrier detect assert threshold, the LMH0397 operates in normal operation mode.

In the absence of an input signal, the LMH0397 automatically goes into Power Save Mode to conserve power dissipation. When a valid signal is detected, the LMH0397 automatically exits Power Save Mode and returns to the normal operation mode. If the ENABLE pin is pulled low, the LMH0397 is forced into Power-Down Mode. In Power Save Mode, both the carrier detect circuit and the serial interface remain active. In Power-Down Mode, only the serial interface remains active.

Users can monitor the status of the carrier detect through register programming. This can be done either by configuring the LOCK_N pin to output the CD_N status or by monitoring the carrier detect status register. See Table 4 for more details.

Table 4. Input Carrier Detect Modes of Operation

ENABLE	EQ/CD_SEL	SIGNAL INPUT	OPERATING MODE
H	L	75-Ω video input at SDI_IO+	EQ Mode, normal operation Carrier detector at SDI_IO+ Serial interface active OUT0 automatically enabled, regardless of OUT0_SEL setting
H	L	No signal at SDI_IO+	Power Save Mode Carrier detector at SDI_IO+ Serial interface active
H	H	100-Ω signal input at IN0±	CD Mode, normal operation Carrier detector at IN0± Serial interface active
H	H	No signal at IN0±	Power Save Mode Carrier detector at IN0± Serial interface active
L	X	Input signal ignored	Power-Down Mode Forced device power down Serial interface active

8.3.4 –6-dB Splitter Mode Launch Amplitude for SDI_IO+ (EQ Mode Only)

When placed in EQ Mode, the LMH0397 equalizes data transmitted into SDI_IO through a coaxial cable driven by a SMPTE compatible cable driver with launch amplitude of 800 mVp-p ± 10%. In applications where a 1:2 passive splitter is used, the signal amplitude is reduced by half due to the 6-dB insertion loss of the splitter. The LMH0397 can support –6-dB splitter mode for the SDI_IO input through register control. For more information, refer to the *LMH0397 Programming Guide* (SNLU225).

8.3.5 Continuous Time Linear Equalizer (CTLE)

The LMH0397 has two continuous time linear equalizer (CTLE) blocks, one for SDI_IO in EQ Mode and another for IN0 in CD Mode. The CTLE compensates for frequency-dependent loss due to the transmission media before the device input. The CTLE accomplishes this by applying variable gain to the input signal, thereby boosting higher frequencies more than lower frequencies. The CTLE block extends the signal bandwidth, restores the signal amplitude, and reduces ISI caused by the transmission medium.

8.3.5.1 Line-Side Adaptive Cable Equalizer (SDI_IO+ in EQ Mode)

If the LMH0397 is placed in EQ Mode (EQ/CD_SEL = L), adaptive cable equalization is enabled for SDI_IO. While the LMH0397 is in EQ Mode, IN0 EQ is powered down.

SDI_IO has an on-chip 75-Ω termination to the input common-mode voltage and includes a series return loss compensation network for meeting stringent SMPTE return loss requirements (see Figure 8). The adaptive cable equalizer is designed for AC coupling, requiring a 4.7-µF, AC-coupling capacitor for minimizing base-line wander due to the rare-occurring pathological bit pattern. The cable equalizer is designed with high gain and low noise circuitry to compensate for the insertion loss of a coaxial cable, such as Belden 1694A, which is widely used in broadcast video infrastructures.

Internal control loops are used to monitor the input signal quality and automatically select the optimal EQ boost and DC offset compensation. The LMH0397 is designed to handle the stringent pathological patterns defined in the SMPTE RP 198 and SMPTE RP 178 standards.

8.3.5.2 Host-Side Adaptive PCB Trace Equalizer (IN0± in CD Mode)

If the LMH0397 is placed in CD Mode (EQ/CD_SEL = H), PCB trace equalization is enabled for IN0. While the LMH0397 is in CD Mode, SDI_IO EQ is powered down.

IN0 has an on-chip 100-Ω termination and is designed for AC coupling, requiring a 4.7-µF, AC-coupling capacitor for minimizing base-line wander. The PCB equalizer can compensate board trace insertion losses of –17 dB at data rates up to 2.97 Gbps. There are two adapt modes for IN0: AM0 manual mode and AM1 adaptive mode. In AM0 manual mode, fixed EQ boost settings are applied through user-programmable control. In AM1 adaptive mode, state machines automatically find the optimal EQ boost from a set of 16 predetermined settings defined in Registers 0x40-0x4F.

In CD Mode, the HOST_EQ0 pin determines the IN0 adapt mode and EQ boost level. For normal operation, HOST_EQ0 = F is recommended. HOST_EQ0 pin logic settings are shown in Table 5. These HOST_EQ0 pin settings can be overridden by register control. For more information, refer to the *LMH0397 Programming Guide* (SNLU225).

Table 5. HOST_EQ0 Pin EQ Settings in CD Mode (EQ/CD_SEL = H)

HOST_EQ0 (1)	IN0± EQ BOOST (2)	RECOMMENDED INSERTION LOSS BEFORE IN0± (3)
H	All Rates: AM0 Manual Mode, EQ=0x00	< –4 dB
F	**Normal Operation** 3G Rate: AM1 Adaptive Mode 1.5G, 270M Rates: AM0 Manual Mode, EQ= 0x00	0 to –17 dB
R	All Rates: AM0 Manual Mode, EQ=0x80	–8 dB
L	All Rates: AM0 Manual Mode, EQ=0x90	–10 dB

(1) The HOST_EQ0 pin is also used to set OUT0 VOD and de-emphasis values. See *Host-Side 100-Ω Output Driver (OUT0± in EQ or CD Mode)* for more information.
(2) When the LMH0397 is in EQ Mode, IN0 EQ settings are ignored, because IN0 EQ is powered down.
(3) Recommended insertion loss at 2.97 Gbps.

8.3.6 Clock and Data (CDR) Recovery

After the input signal passes through the CTLE, the equalized data is fed into the clock and data recovery (CDR) block. Using an internal PLL, the CDR locks to the incoming equalized data and recovers a clean internal clock to re-sample the equalized data. The LMH0397 CDR is able to tolerate high input jitter, tracking low-frequency input jitter below the PLL bandwidth while reducing high-frequency input jitter above the PLL bandwidth. The supported data rates are listed in Table 6.

Table 6. Supported Data Rates

INPUT	DATA RATE	RECLOCKER
SDI_IO+ (EQ Mode), IN0± (CD Mode)	2.97 Gbps, 1.485 Gbps, 270 Mbps(1)	Enable
	125 Mbps	Bypass

(1) The LMH0397 supports divide-by-1.001 lock rates for 2.97 Gbps, and 1.485 Gbps.

8.3.7 Internal Eye Opening Monitor (EOM)

The LMH0397 has an on-chip eye opening monitor (EOM) that can be used to analyze, monitor, and diagnose the post-equalized waveform, just before the CDR reclocker. The EOM is operational for 2.97 Gbps and higher data rates.

The EOM monitors the post-equalized waveform in a time window that spans one unit interval and a configurable voltage range that spans up to ±400 mV. The time window and voltage range are divided into 64 steps, so the result of the eye capture is a 64 × 64 matrix of hits, where each point represents a specific voltage and phase offset relative to the main data sampler. The number of hits registered at each point must be taken in context with the total number of bits observed at that voltage and phase offset to determine the corresponding probability for that point.

The resulting 64 × 64 matrix produced by the EOM can be processed by software and visualized in a number of ways. Two common ways to visualize this data are shown in Figure 10 and Figure 11. These diagrams depict examples of eye monitor plots implemented by software. The first plot is an example using the EOM data to plot a basic eye using ASCII characters, which can be useful for diagnostic software. The second plot shows the first derivative of the EOM data, revealing the density of hits and the actual waveforms and crossings that comprise the eye.

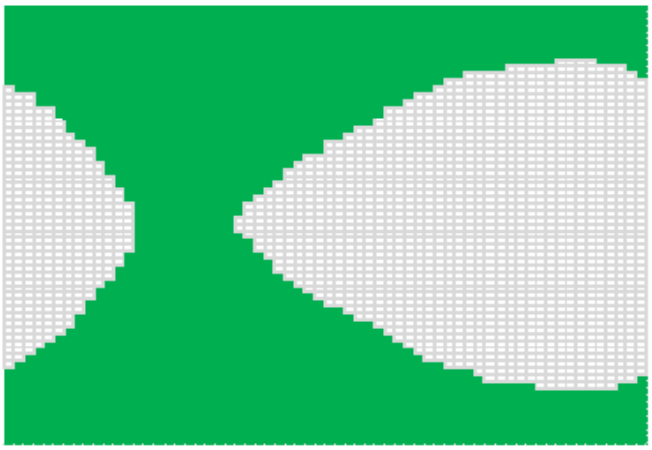


Figure 10. Internal Input Eye Monitor Plot

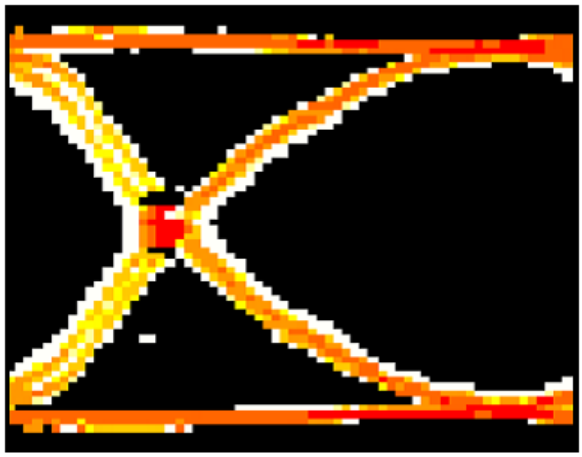


Figure 11. Internal Eye Monitor Hit Density Plot

A common measurement performed by the EOM is the horizontal and vertical eye opening. The horizontal eye opening (HEO) represents the width of the post-equalized eye at 0-V differential amplitude, measured in unit intervals or picoseconds (ps). The vertical eye opening (VEO) represents the height of the post-equalized eye, measured midway between the mean zero crossing of the eye. This position in time approximates the CDR sampling phase. HEO and VEO measurements can be read back through register control.

8.3.8 Output Function Control

The LMH0397 output function control for data routed to outputs SDI_IO (in CD Mode), SDI_OUT, and OUT0 is configured by the OUT_CTRL pin. The OUT_CTRL pin determines whether to bypass the input equalizer, reclocker, or both. In normal operation (OUT_CTRL = F), both input equalizer and reclocker are enabled.

OUT_CTRL pin logic settings are shown in Table 7. These settings can be overridden through register control by applying the appropriate override bit values. For more information, refer to the *LMH0397 Programming Guide* (SNLU225).

Table 7. OUT_CTRL Settings for Bypass Modes

EQ/CD_SEL (MODE)	OUT_CTRL	SDI_IO+ CABLE EQUALIZER	IN0± PCB EQUALIZER	RECLOCKER	SUMMARY
L (EQ Mode)	H	Bypass	N/A	Enable	Input SDI_IO cable equalizer bypassed Reclocker enabled
	F	Enable	N/A	Enable	Normal operation Input SDI_IO cable equalizer enabled Reclocker enabled
	R	Bypass	N/A	Bypass	Input SDI_IO cable equalizer bypassed Reclocker bypassed
	L	Enable	N/A	Bypass	Input SDI_IO cable equalizer enabled Reclocker bypassed
H (CD Mode)	H, F	N/A	Enable	Enable	Normal operation Input IN0 equalizer enabled Reclocker enabled
	R, L	N/A	Enable	Bypass	Input IN0 equalizer enabled in AM0 manual mode. IN0 EQ settings configurable by HOST_EQ0 pin. Reclocker bypassed

8.3.9 Output Driver Control

8.3.9.1 Line-Side Output Cable Driver (SDI_IO+ in CD Mode, SDI_OUT+ in EQ or CD Mode)

The LMH0397 has two output cable driver (CD) blocks, one for SDI_IO in CD Mode and another for SDI_OUT. These SDI outputs are designed to drive 75-Ω single-ended coaxial cables at data rates up to 2.97 Gbps. Both SDI_IO and SDI_OUT feature an integrated 75-Ω termination and return loss compensation network for meeting stringent SMPTE return loss requirements (see Figure 8). The cable drivers are designed for AC coupling, requiring a 4.7-μF, AC-coupling capacitor for minimizing base-line wander due to the rare-occurring pathological bit pattern.

8.3.9.1.1 Output Amplitude (VOD)

In CD Mode (EQ/CD_SEL = H), SDI_IO is enabled as an SDI cable driver output. In either CD or EQ Mode, SDI_OUT is an SDI cable driver output. In EQ Mode, SDI_OUT serves as a loop-through output, and in CD Mode, SDI_OUT serves as a secondary cable driver output.

SDI_IO (in CD Mode) and SDI_OUT are designed for transmission across 75-Ω single-ended impedance. The nominal SDI cable driver output amplitude (VOD) is 800 mVp-p single-ended. In the presence of long output cable lengths or crosstalk, the SDI_VOD pin can be used to optimize the cable driver output with respect to the nominal amplitude. Table 8 details VOD settings that can be applied to both SDI_IO and SDI_OUT. The SDI_VOD pin can be overridden through register control. In addition, the nominal VOD amplitude can be changed by register control. For more information, refer to the *LMH0397 Programming Guide* (SNLU225).

Table 8. SDI_VOD Settings for Line-Side Output Amplitude

SDI_VOD	DESCRIPTION
H	about +5% of nominal
F	800 mVp-p (nominal)
R	about +10% of nominal
L	about –5% of nominal

8.3.9.1.2 Output Pre-Emphasis

In addition to SDI cable driver VOD control, the LMH0397 can add pre-emphasis on the cable driver output to improve output signal integrity when the reclocker recovers an HD (3G, 1.5G) input data rate. By default, the LMH0397 in CD Mode automatically disables pre-emphasis at SDI_IO for all data rates. When enabled, the amount of pre-emphasis applied to the cable driver outputs is determined by register control. If the reclocker is bypassed or if the user desires to disable automatic pre-emphasis, pre-emphasis can be enabled manually through register control. For more information, refer to the *LMH0397 Programming Guide* (SNLU225).

8.3.9.1.3 Output Slew Rate

SMPTE specifications require different output driver rise and fall times depending on the operating data rate. To meet these requirements, the output edge rate of SDI_IO and SDI_OUT is automatically programmed according to the signal recovered by the reclocker. Typical edge rates at the cable driver output are shown in Table 9.

Table 9. SDI_IO and SDI_OUT Output Edge Rate

DETECTED DATA RATE	CABLE DRIVER OUTPUT EDGE RATE (TYPICAL)
2.97 Gbps	59 ps
1.485 Gbps	60 ps
270 Mbps	550 ps

If the reclocker is bypassed, users must program the desired edge rate manually through register control. For more information, refer to the *LMH0397 Programming Guide* (SNLU225).

8.3.9.1.4 Output Polarity Inversion

Polarity inversion is supported on both SDI_IO and SDI_OUT outputs through register control.

8.3.9.2 Host-Side 100-Ω Output Driver (OUT0± in EQ or CD Mode)

OUT0 is a 100-Ω driver output. In EQ Mode, OUT0 serves as a host-side output from the SDI_IO cable equalizer. In CD Mode, OUT0 serves as a host-side loopback output. OUT0 also supports polarity inversion.

NOTE

In EQ Mode, OUT0 is enabled by default, regardless of the logic applied to the OUT0_SEL pin.

The driver offers users the capability to select higher output amplitude and de-emphasis levels for longer board trace that connects the drivers to their downstream receivers. Driver de-emphasis provides transmitter equalization to reduce the ISI caused by the board trace.

In EQ Mode, the HOST_EQ0 pin determines the output amplitude (VOD) and de-emphasis levels applied to the OUT0 PCB driver. In CD Mode, the VOD and de-emphasis levels for OUT0 are set by default to 570 mVp-p and –0.4 dB. These settings can be changed through register control if desired.

Table 10 details the OUT0 VOD and de-emphasis settings that can be applied. The HOST_EQ0 pin settings can be overridden by register control. When these parameters are controlled by registers, the VOD and de-emphasis levels can be programmed independently. For more information, refer to the *LMH0397 Programming Guide* (SNLU225).

Table 10. HOST_EQ0 Pin VOD and DEM Settings

EQ/CD_SEL (MODE)	HOST_EQ(1)	OUT0± VOD (mVp-p)	OUT0± DEM (dB)
L (EQ Mode)	H	400	0
	F	570	–0.4
	R	660	–2.1
	L	830	–4.4
H (CD Mode)	X	570	–0.4

(1) The HOST_EQ0 pin is also used to set the IN0 EQ values when the LMH0397 is in CD Mode. See *Host-Side Adaptive PCB Trace Equalizer (IN0± in CD Mode)* for more information.

8.3.10 Status Indicators and Interrupts

The LOCK_N pin is a 3.3-V tolerant, active-low, open-drain output. An external resistor to the logic supply is required. The LOCK_N pin can be configured to indicate reclocker lock, input carrier detect, or an interrupt event.

8.3.10.1 LOCK_N (Lock Indicator)

By default, LOCK_N is the reclocker lock indicator, and this pin asserts low when the LMH0397 achieves lock to a valid SMPTE data rate. The LOCK_N pin functionality can also be configured through register control to indicate CD_N (carrier detect) or INT_N (interrupt) events. For more information about how to reconfigure the LOCK_N pin functionality, refer to the *LMH0397 Programming Guide* (SNLU225).

8.3.10.2 CD_N (Carrier Detect)

The LOCK_N pin can be reconfigured through register control to indicate a CD_N (carrier detect) event. When configured as a CD_N output, the pin asserts low at the end of adaptation after a valid signal is detected by the carrier detect circuit of the selected input. Under register control, this pin can be reconfigured to indicate CD_N for SDI_IO (in EQ Mode) or IN0 (in CD Mode). For more information about how to configure the LOCK_N pin for CD_N functionality, refer to the *LMH0397 Programming Guide* (SNLU225).

8.3.10.3 INT_N (Interrupt)

The LOCK_N pin can be configured to indicate an INT_N (interrupt) event. When configured as an INT_N output, the pin asserts low when an interrupt occurs, according to the programmed interrupt masks. Seven separate masks can be programmed through register control as interrupt sources:

- If there is a loss of signal (LOS) event on SDI_IO in EQ Mode (2 separate masks).
- If there is a loss of signal (LOS) event on IN0 in CD Mode (2 separate masks).
- If HEO or VEO falls below a certain threshold after CDR is locked (1 mask).
- If a CDR Lock event has occurred (2 separate masks).

INT_N is a sticky bit, meaning that it will flag after an interrupt occurs and will not clear until read-back. Once the Interrupt Status Register is read, the INT_N pin will assert high again. For more information about how to configure the LOCK_N pin for INT_N functionality, refer to the *LMH0397 Programming Guide* (SNLU225).

8.3.11 Additional Programmability

The LMH0397 supports extended programmability through SPI or SMBus serial control interface. Such added programmability includes:

- Cable EQ Index (CEI)
- Digital $MUTE_{REF}$

8.3.11.1 Cable EQ Index (CEI)

The Cable EQ Index (CEI) indicates the cable EQ boost index used at SDI_IO+ in EQ Mode. CEI is accessible through ConfigIO Page Reg 0x25[5:0]. The 6-bit setting ranges in decimal value from 0 to 55 (000000'b to 110111'b in binary), with higher values corresponding to larger gain applied at the SDI_IO+ input.

8.3.11.2 Digital $MUTE_{REF}$

Digital $MUTE_{REF}$ ConfigIO Page Reg 0x03[5:0] sets the threshold for the maximum cable length at SDI_IO+ to be equalized before muting the outputs. The $MUTE_{REF}$ register value is directly proportional to the cable length being equalized. $MUTE_{REF}$ is data rate dependent. Perform the steps that follow to set the $MUTE_{REF}$ register setting for any desired SDI rate:

1. Connect the desired input cable length at which the driver output must be muted.
2. Send video patterns to SDI_IO+ at the SD rate (270 Mbps). At SD, the Cable EQ Index (CEI) has the largest dynamic range.
3. Read back ConfigIO Page Reg 0x25[5:0] to record the CEI value.
4. Copy the CEI value, and write this value to Digital $MUTE_{REF}$ ConfigIO Page Reg 0x03[5:0].

8.4 Device Functional Modes

The LMH0397 operates in one of two modes: System Management Bus (SMBus) or Serial Peripheral Interface (SPI) mode. To determine the mode of operation, the proper setting must be applied to the MODE_SEL pin at power up, as detailed in Table 11.

Table 11. MODE_SEL Pin Settings

LEVEL	DESCRIPTION
H	Reserved for factory testing – do not use
F	Selects SPI Interface for register access
R	Reserved for factory testing – do not use
L	Selects SMBus Interface for register access

8.4.1 System Management Bus (SMBus) Mode

The SMBus interface can also be used to control the device. If MODE_SEL = Low (1 kΩ to VSS), Pins 13 and 29 are configured as SDA and SCL. Pins 11 and 28 are address straps ADDR0 and ADDR1 during power up. The maximum operating speed supported on the SMBUS pins is 400 kHz. See Table 12 for more information.

Table 12. SMBus Device Slave Addresses(1)

ADDR0 (LEVEL)	ADDR1 (LEVEL)	7-BIT SLAVE ADDRESS [HEX]	8-BIT WRITE COMMAND [HEX]
L	L	2D	5A
L	R	2E	5C
L	F	2F	5E
L	H	30	60
R	L	31	62
R	R	32	64
R	F	33	66
R	H	34	68
F	L	35	6A
F	R	36	6C
F	F	37	6E
F	H	38	70
H	L	39	72
H	R	3A	74
H	F	3B	76
H	H	3C	78

(1) The 8-bit write command consists of the 7-bit slave address (Bits 7:1) with 0 appended to the LSB to indicate an SMBus write. For example, if the 7-bit slave address is 0x2D (010 1101'b), the 8-bit write command is 0x5A (0101 1010'b).

8.4.1.1 SMBus Read and Write Transaction

SMBus is a 2-wire serial interface through which various system component chips can communicate with the master. Slave devices are identified by having a unique device address. The 2-wire serial interface consists of SCL and SDA signals. SCL is a clock output from the master to all of the slave devices on the bus. SDA is a bidirectional data signal between the master and slave devices. The LMH0397 SMBus SCL and SDA signals are open-drain and require external pullup resistors.

Start and Stop:

The master generates Start and Stop patterns at the beginning and end of each transaction, as shown in Figure 12.

- Start: High-to-low transition (falling edge) of SDA while SCL is high.
- Start: High-to-low transition (falling edge) of SDA while SCL is high.

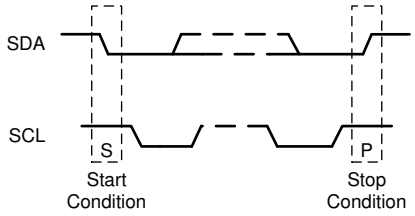


Figure 12. Start and Stop Conditions

The master generates nine clock pulses for each byte transfer as shown in Figure 13. The 9th clock pulse constitutes the ACK cycle. The transmitter releases SDA to allow the receiver to send the ACK signal. An ACK is recorded when the device pulls SDA low, while a NACK is recorded if the line remains high.

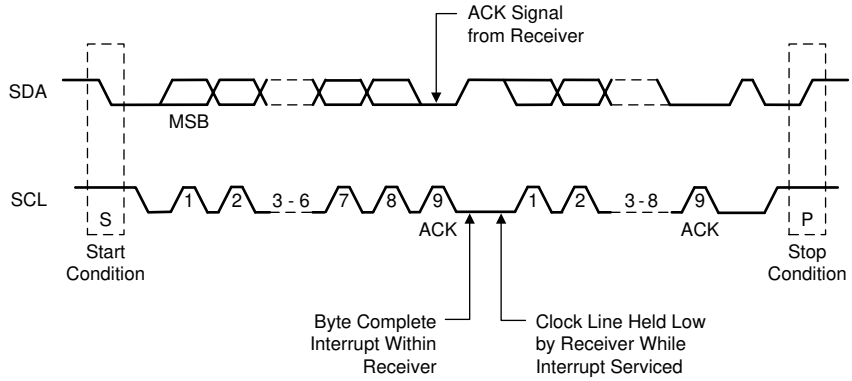


Figure 13. Acknowledge (ACK)

8.4.1.1.1 SMBus Write Operation Format

Writing data to a slave device consists of three parts, as shown in Figure 14:

1. The master begins with a start condition followed by the slave device address with the R/$\overline{W}$ bit set to 0'b.
2. After an ACK from the slave device, the 8-bit register word address is written.
3. After an ACK from the slave device, the 8-bit data is written, followed by a stop condition.

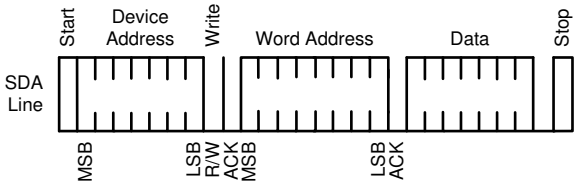


Figure 14. SMBus Write Operation

8.4.1.1.2 SMBus Read Operation Format

SMBus read operation consists of four parts, as shown in Figure 15:

1. The master begins with a start condition, followed by the slave device address with the R/$\overline{W}$ bit set to 0'b.
2. After an ACK from the slave device, the 8-bit register word address is written.
3. After an ACK from the slave device, the master initiates a restart condition, followed by the slave address with the R/$\overline{W}$ bit set to 1'b.
4. After an ACK from the slave device, the 8-bit data is read-back. The last ACK is high if there are no more bytes to read, and the last read is followed by a stop condition.

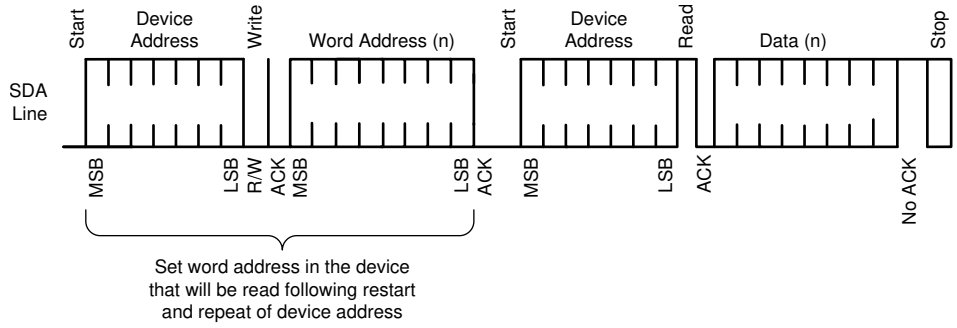


Figure 15. SMBus Read Operation

8.4.2 Serial Peripheral Interface (SPI) Mode

If MODE_SEL = F or H, the LMH0397 is in SPI mode. In SPI mode, the following pins are used for SPI bus communication:

- MOSI (pin 13): Master Output Slave Input
- MISO (pin 28): Master Input Slave Output
- SS_N (pin 11): Slave Select (Active Low)
- SCK (pin 29): Serial Clock (Input to the LMH0397 Slave Device)

8.4.2.1 SPI Read and Write Transactions

Each SPI transaction to a single device is 17 bits long and is framed by SS_N when asserted low. The MOSI input is ignored, and the MISO output is floated whenever SS_N is deasserted (high).

The bits are shifted in left-to-right. The first bit is R/$\overline{W}$, which is 1'b for *read* and 0'b for *write*. Bits A7-A0 are the 8-bit register address, and bits D7-D0 are the 8-bit read or write data. The previous SPI command, address, and data are shifted out on MISO as the current command, address, and data are shifted in on MOSI. In all SPI transactions, the MISO output signal is enabled asynchronously when SS_N asserts low. The contents of a single MOSI or MISO transaction frame are shown in Figure 16.

Figure 16. 17-Bit Single SPI Transaction Frame

R/W	A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

8.4.2.2 SPI Write Transaction Format

For SPI writes, the R/W bit is 0'b. SPI write transactions are 17 bits per device, and the command is executed on the rising edge of SS_N. The SPI transaction always starts on the rising edge of the clock.

The signal timing for a SPI Write transaction is shown in Figure 2. The *prime* values on MISO (for example, A7') reflect the contents of the shift register from the previous SPI transaction and are don't-care for the current transaction.

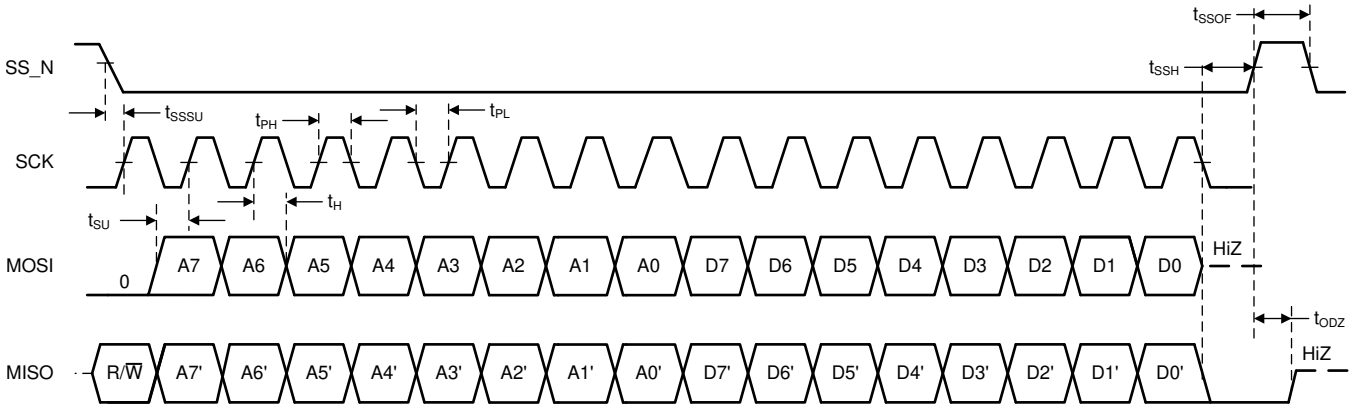


Figure 17. Signal Timing for a SPI Write Transaction

8.4.2.3 SPI Read Transaction Format

A SPI read transaction is 34 bits per device and consists of two 17-bit frames. The first 17-bit read transaction frame shifts in the address to be read, followed by a dummy transaction second frame to shift out 17-bit read data. The R/W bit is 1'b for the read transaction, as shown in Figure 3.

The first 17 bits from the read transaction specifies 1 bit of R/W and 8 bits of address A7-A0 in the first 8 bits. The eight 1s following the address are ignored. The second dummy transaction acts like a read operation on address 0xFF and must be ignored. However, the transaction is necessary to shift out the read data D7-D0 in the last 8 bits of the MISO output. As with the SPI Write, the *prime* values on MISO during the first 16 clocks are listed as don't care for this portion of the transaction. The values shifted out on MISO during the last 17 clocks reflect the read address and 8-bit read data for the current transaction.

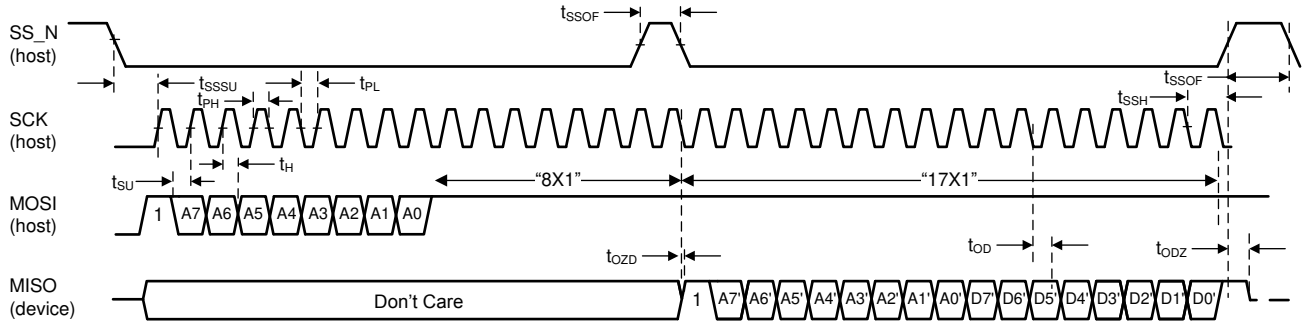


Figure 18. Signal Timing for a SPI Read Transaction

8.4.2.4 SPI Daisy Chain

The LMH0397 supports SPI daisy-chaining among multiple devices, as shown in Figure 19.

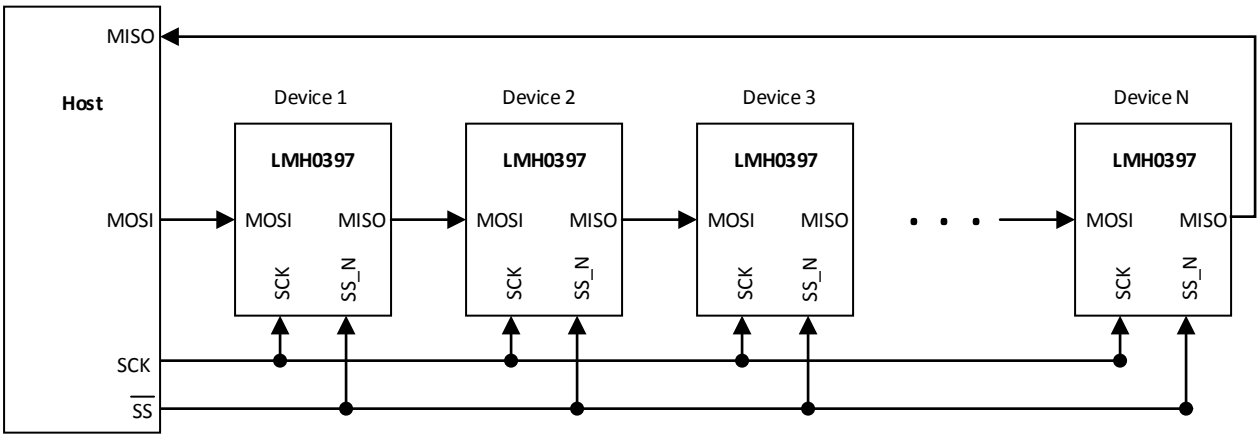


Figure 19. Daisy-Chain Configuration

Each LMH0397 device is directly connected to the SCK and SS_N pins of the host. The first LMH0397 device in the chain is connected to the MOSI pin of the host, and the last device in the chain is connected to the MISO pin of the host. The MOSI pin of each intermediate LMH0397 device in the chain is connected to the MISO pin of the previous LMH0397 device, thereby creating a serial shift register. In a daisy-chain configuration of N × LMH0397 devices, the host conceptually sees a shift register of length 17 × N for a basic SPI transaction, during which SS_N is asserted low for 17 × N clock cycles.

8.5 Register Maps

The LMH0397 register map is divided into three register pages. These register pages are used to control different aspects of the LMH0397 functionality. A brief summary of the pages follows:

1. **Share Register Page:** This page corresponds to global parameters, such as LMH0397 device ID, I/O direction override, and LOCK_N status configuration. This is the default page at start-up. Access this page by setting Reg 0xFF[2:0] = 000'b.
2. **CTLE/CDR Register Page:** This page corresponds to IN0 PCB CTLE, input and output mux settings, CDR settings, and output interrupt overrides. Access this page by setting Reg 0xFF[2:0] = 100'b.
3. **ConfigIO Register Page:** This page corresponds to SDI_IO Cable Equalizer settings. This page also controls the OUT0, SDI_IO, and SDI_OUT driver output settings. Access this page by setting Reg 0xFF[2:0] = 101'b.

For the complete register map, typical device configurations, and proper register reset sequencing, refer to the *LMH0397 Programming Guide* (SNLU225).

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 SMPTE Requirements and Specifications

SMPTE specifies several key requirements for the Serial Digital Interface to transport digital video over coaxial cables. Such requirements include return loss, AC coupling, and data rate dependency with rise and fall times.

1. **Return Loss:** This specification details how closely the port resembles 75-Ω impedance across a specified frequency band. The LMH0397 features a built-in 75-Ω return-loss network on SDI_IO and SDI_OUT to minimize parasitics and improve overall signal integrity.
2. **AC Coupling:** AC-coupling capacitors are required for transporting uncompressed serial data streams with heavy low-frequency content. The use of 4.7-μF, AC-coupling capacitors is recommended to avoid low-frequency DC wander.
3. **Rise/Fall Time:** Output 75-Ω signals are required to meet certain rise and fall timing depending on the data rate. This improves the eye opening observed for the receiving device. The LMH0397 SDI_IO (in CD Mode) and SDI_OUT cable drivers feature automatic edge rate adjustment to meet SMPTE rise and fall time requirements.

TI recommends placing the LMH0397 as close as possible to the 75-Ω BNC ports to meet SMPTE specifications.

9.1.2 Low-Power Optimization in CD Mode

In CD Mode, the LMH0397 IN0 CTLE operates in either AM1 Adaptive Mode or AM0 Manual Mode. When operating in AM1, the LMH0397 uses HEO/VEO Lock Monitoring as a key parameter to achieve lock. HEO/VEO Lock Monitoring determines the CTLE boost setting that produces the best horizontal and vertical eye opening after the CTLE. When AM1 adaptation is complete and the LMH0397 asserts CDR lock at the optimal IN0 CTLE setting, HEO/VEO Lock Monitoring is no longer required to maintain lock. Therefore, HEO/VEO Lock Monitoring can be disabled by setting CTLE/CDR Reg 0x3E[7] = 0'b **after** lock is declared. Disabling HEO/VEO Lock Monitoring optimizes power dissipation in CD Mode, reducing the overall power by approximately 25 mW.

When operating in AM0, the LMH0397 does not use HEO/VEO Lock Monitoring, because the user manually sets the IN0 CTLE setting. In AM0, HEO/VEO Lock Monitoring can be disabled at any time.

9.2 Typical Applications

The LMH0397 is a bidirectional I/O with integrated reclocker that supports SDI data rates up to 2.97 Gbps. This device supports multiple configurations and can be programmed as a cable equalizer or cable driver. Figure 20 shows a typical application circuit for the LMH0397.

Specific examples of typical applications for the LMH0397 as a bidirectional I/O and cable equalizer with loop-through are detailed in the following subsections.

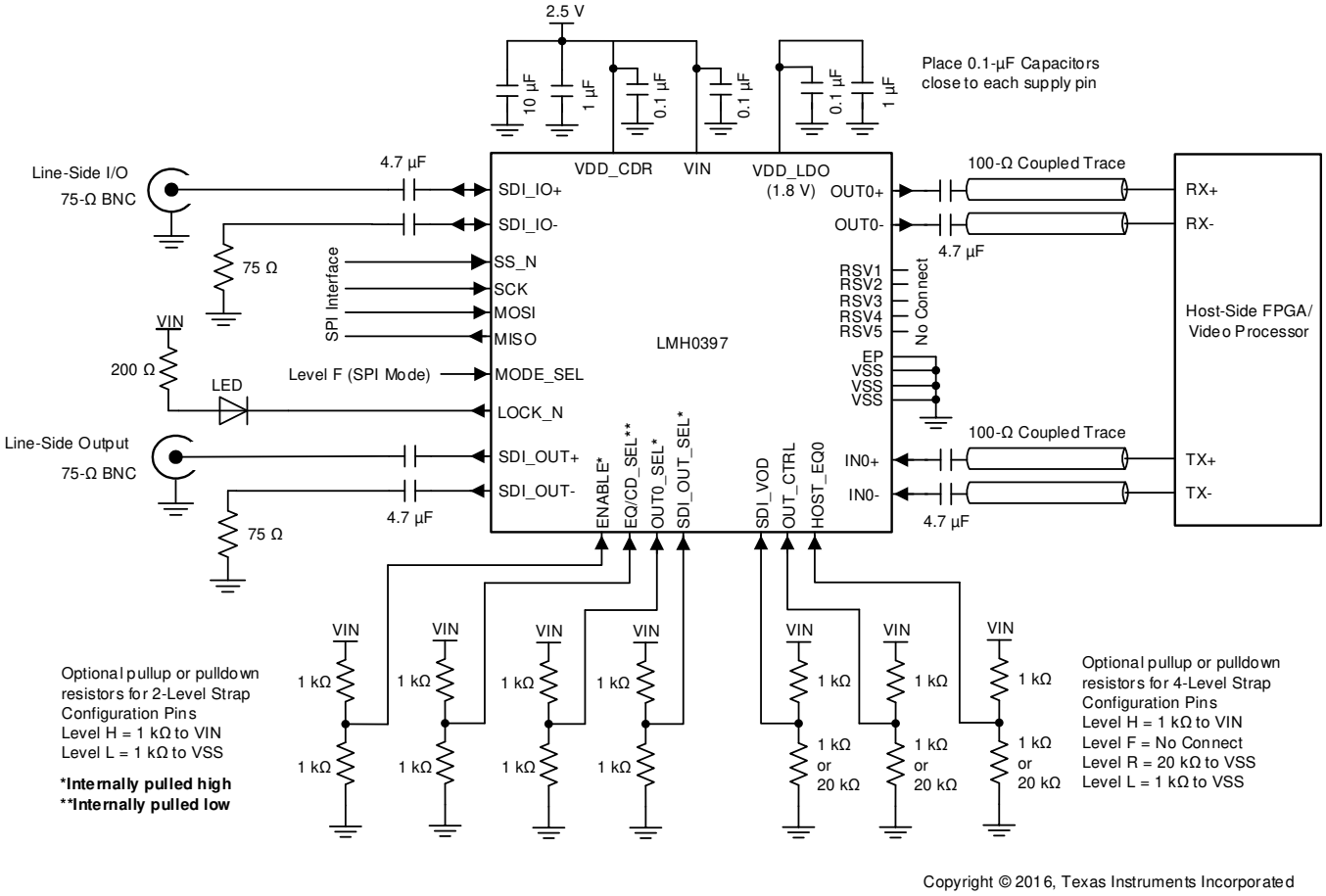


Figure 20. LMH0397 Typical Application Circuit

Typical Applications (continued)

9.2.1 Bidirectional I/O

The LMH0397 can be configured as a bidirectional I/O to improve BNC port function flexibility. In EQ Mode, the LMH0397 equalizes 75-Ω SDI input data at SDI_IO and outputs from OUT0 to an FPGA Rx. SDI_OUT is used as an optional loop-through SDI output. In CD Mode, the LMH0397 equalizes 100-Ω SDI input data at IN0 and uses the dual cable drivers at SDI_IO and SDI_OUT to drive out the SDI signal. OUT0 can be used as a loopback output for system monitoring.

Figure 21 shows a typical application where an LMH0397 is used alongside an SDI FPGA to enable bidirectional I/O port functionality.

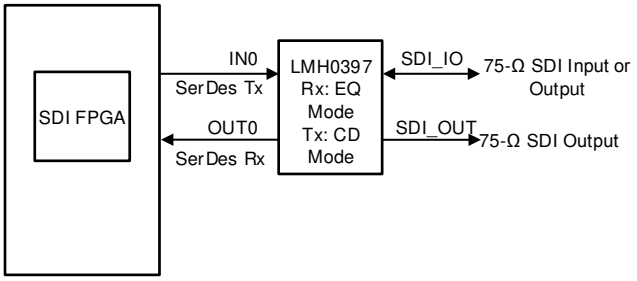


Figure 21. LMH0397 Bidirectional I/O Application

9.2.1.1 Design Requirements

For general LMH0397 design requirements, see the guidelines in Table 13.

For bidirectional I/O application-specific requirements, see the guidelines in Table 14.

Table 13. LMH0397 General Design Requirements

DESIGN PARAMETER	REQUIREMENTS
SDI_IO+, SDI_OUT+ AC-coupling capacitors	4.7-µF capacitors recommended
SDI_IO–, SDI_OUT– AC-coupling capacitors	4.7-µF capacitors recommended, AC terminated with 75 Ω to VSS.
IN0± and OUT0± AC-coupling capacitors	4.7-µF capacitors recommended
Input and output terminations	Input and output terminations provided internally. Do **not** add external terminations.
DC power supply decoupling capacitors	10-µF and 1-µF bulk capacitors; place close to each device. 0.1-µF capacitor; place close to each supply pin.
VDD_LDO decoupling capacitors	1-µF and 0.1-µF capacitors; place as close as possible to the device VDD_LDO pin.
MODE_SEL pin	SPI: Leave MODE_SEL unconnected (Level F) SMBus: Connect 1 kΩ to VSS (Level L)
Input reclocked data rate (SDI_IO in EQ Mode or IN0 in CD Mode)	2.97 Gbps, 1.485 Gbps, or divide-by-1.001 subrates and 270 Mbps. For all other input data rates, the reclocker is automatically bypassed.

Table 14. LMH0397 Bidirectional I/O Requirements

DESIGN PARAMETER	REQUIREMENTS
EQ/CD_SEL pin	1 kΩ to VSS (Level L) when SDI_IO is used as a cable EQ input 1 kΩ to VIN (Level H) when SDI_IO is used as a cable driver output
OUT0_SEL pin	1 kΩ to VSS (Level L) to enable OUT0 for monitoring purposes 1 kΩ to VIN (Level H) to disable OUT0 (available only in CD Mode)
SDI_OUT_SEL pin	1 kΩ to VSS (Level L) to enable cable loop-through (EQ Mode) or secondary cable output (CD Mode) 1 kΩ to VIN (Level H) to disable cable loop-through (EQ Mode) or secondary cable output (CD Mode)

9.2.1.2 Detailed Design Procedure

Follow this design procedure for bidirectional I/O applications:

1. Select a power supply that meets the DC and AC requirements in *Recommended Operating Conditions*.
2. Choose a small 0402 surface-mount ceramic capacitor for AC-coupling capacitors to maintain characteristic impedance.
3. Choose a high-quality, 75-Ω BNC connector that can support 2.97-Gbps applications. Consult a BNC supplier regarding insertion loss, impedance specifications, and recommended footprint for meeting SMPTE return loss.
4. Follow detailed high-speed layout recommendations provided in *Layout Guidelines* to ensure optimal signal quality when interconnecting 75-Ω and 100-Ω signals to the LMH0397.
5. Determine whether SPI or SMBus communication is necessary. If the LMH0397 must be programmed with settings other than what is offered by pin control, users must use SPI or SMBus Mode for additional programming.
6. Configure EQ/CD_SEL, OUT0_SEL, and SDI_OUT_SEL pins according to the desired default use case. In a bidirectional I/O application, the EQ/CD_SEL pin or register settings may be modified to switch between EQ Mode and CD Mode.
7. Configure the LMH0397 in EQ Mode. Tune the HOST_EQ0 100-Ω driver control pin to equalize the PCB output trace following OUT0±. Use register control for more tuning options if necessary.
8. Configure the LMH0397 in CD Mode. Tune the SDI_VOD output amplitude control pin for optimal signal quality depending on the cable length attached at SDI_IO+ and SDI_OUT+. Use register control for more tuning options if necessary.

9.2.1.3 Application Curves

Depending on operation in EQ or CD Mode, the LMH0397 performance was measured with the test setups shown in Figure 22 and Figure 23.

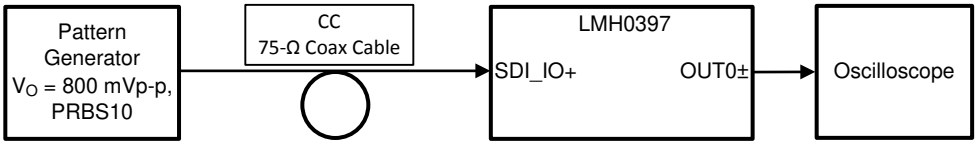


Figure 22. Test Setup for LMH0397 in EQ Mode

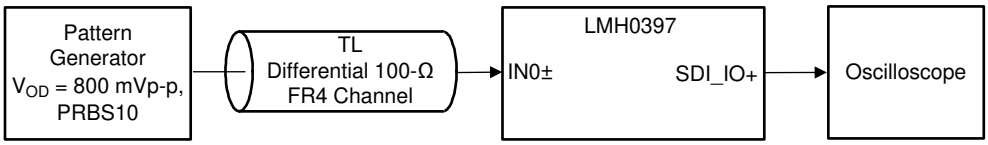
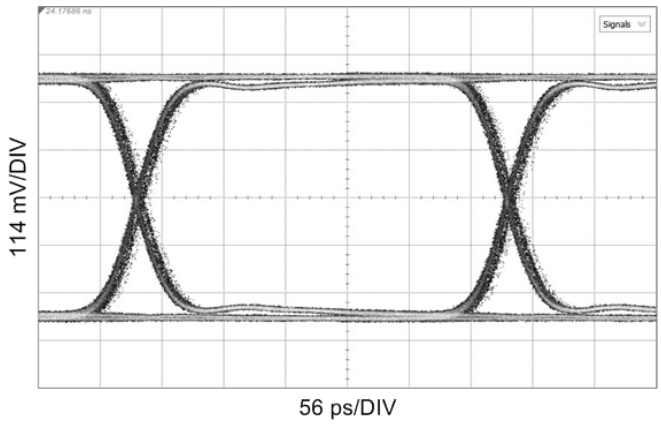


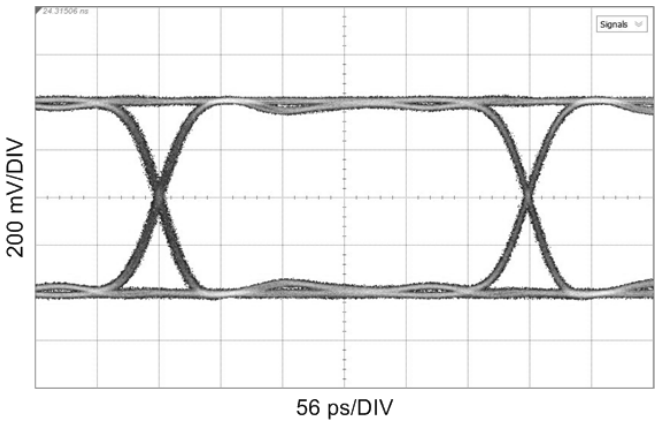
Figure 23. Test Setup for LMH0397 in CD Mode

The eye diagrams in this subsection show how the LMH0397 improves overall signal integrity in the data path for 75-Ω coax at SDI_IO+ when operating in EQ Mode and 100-Ω differential FR4 PCB trace at IN0± when operating in CD Mode.



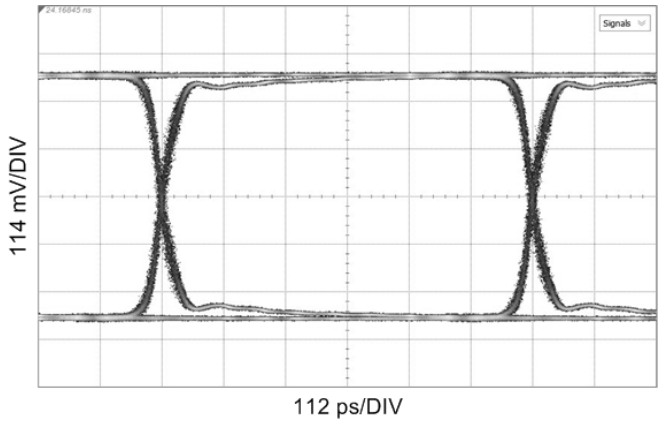
EQ Mode, measured at OUT0±
HOST_EQ0 = F, SDI_OUT_SEL = H, OUT_CTRL = F

Figure 24. 2.97 Gbps, CC = 200-m Belden 1694A, Reclocked



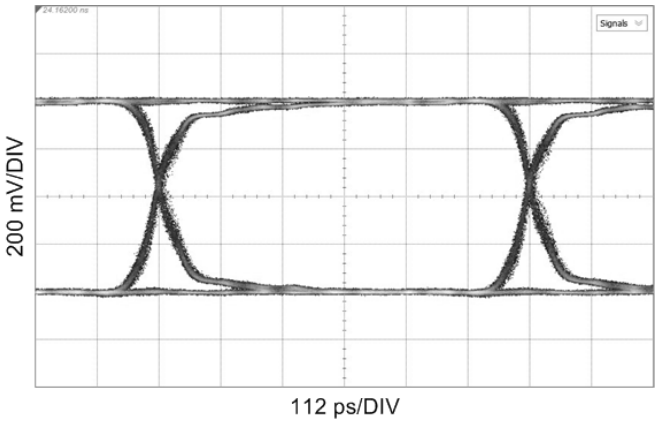
CD Mode, measured at SDI_IO+
HOST_EQ0 = F, SDI_OUT_SEL = H, OUT_CTRL = F

Figure 25. 2.97 Gbps, TL = 20" FR4, Reclocked



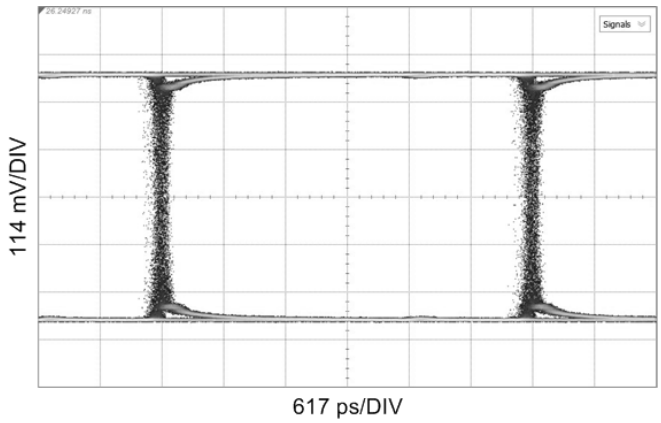
EQ Mode, measured at OUT0±
HOST_EQ0 = F, SDI_OUT_SEL = H, OUT_CTRL = F

Figure 26. 1.485 Gbps, CC = 300-m Belden 1694A, Reclocked



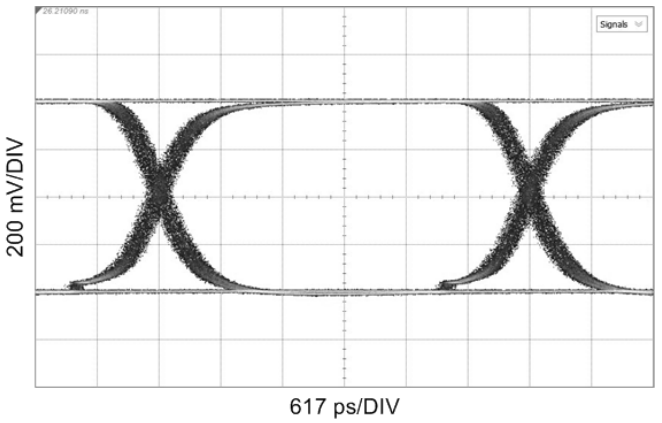
CD Mode, measured at SDI_IO+
HOST_EQ0 = F, SDI_OUT_SEL = H, OUT_CTRL = F

Figure 27. 1.485 Gbps, TL = 20" FR4, Reclocked



EQ Mode, measured at OUT0±
HOST_EQ0 = F, SDI_OUT_SEL = H, OUT_CTRL = F

Figure 28. 270 Mbps, CC = 600-m Belden 1694A, Reclocked



CD Mode, measured at SDI_IO+
HOST_EQ0 = F, SDI_OUT_SEL = H, OUT_CTRL = F

Figure 29. 270 Mbps, TL = 20" FR4, Reclocked

9.2.2 Cable Equalizer With Loop-Through

The LMH0397 can be configured as a cable equalizer with loop-through output. In EQ Mode, the LMH0397 takes in SDI data at the SDI_IO adaptive cable equalizer input and outputs the reclocked SDI signal at OUT0. Meanwhile, a redundant reclocked loop-through SDI signal is output on SDI_OUT for system monitoring purposes.

Figure 30 shows a typical application of an LMH0397 as a cable loop-through device. In this example, the LMH0397 provides an SDI input to the SDI FPGA. Concurrently, the equalized and reclocked SDI_IO signal is sent to the loop-through SDI_OUT cable driver output. Meanwhile, the FPGA sends post-processed SDI data out on an LMH1218 cable driver with integrated reclocker.

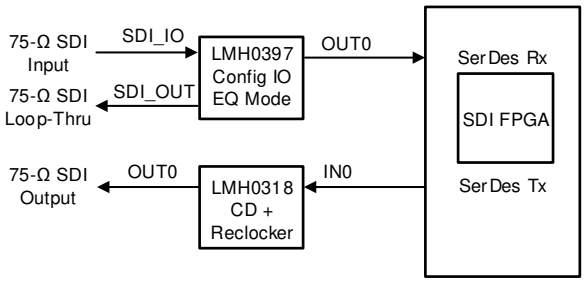


Figure 30. LMH0397 Cable Loop-Through Application

9.2.2.1 Design Requirements

See Table 13 in *Bidirectional I/O Design Requirements* for general LMH0397 design requirements.

For cable equalizer with loop-through application-specific requirements, see the guidelines in Table 15.

Table 15. LMH0397 Cable Loop-Through Requirements

DESIGN PARAMETER	REQUIREMENTS
EQ/CD_SEL pin	1 kΩ to VSS (Level L) to enable SDI_IO as a cable EQ input
OUT0_SEL pin	1 kΩ to VSS (Level L) to enable OUT0 as PCB output to the FPGA
SDI_OUT_SEL pin	1 kΩ to VSS (Level L) to enable SDI_OUT as a loop-through output

9.2.2.2 Detailed Design Procedure

See *Bidirectional I/O Detailed Design Procedure* and follow Steps 1 through 5. See the steps that follow for cable equalizer with loop-through applications.

1. Configure EQ/CD_SEL and SDI_OUT_SEL pins according to the desired default use case. In a cable loop-through application, the EQ/CD_SEL pin must be set to Level L so that the LMH0397 operates in EQ Mode. Also, OUT0 in EQ Mode is always enabled regardless of the logic applied to OUT0_SEL.
2. Tune the HOST_EQ0 100-Ω driver control pin to equalize the PCB output trace following OUT0±. Use register control for more tuning options if necessary.

9.2.2.3 Application Curves

In EQ Mode, the LMH0397 SDI_OUT performance was measured with the test setup shown in Figure 31.

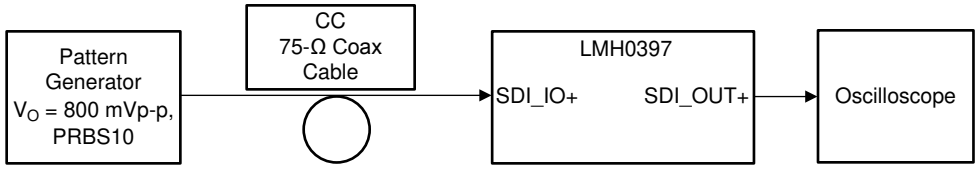
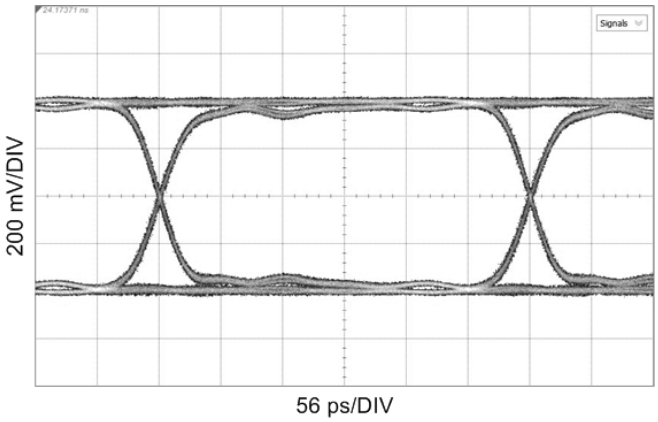


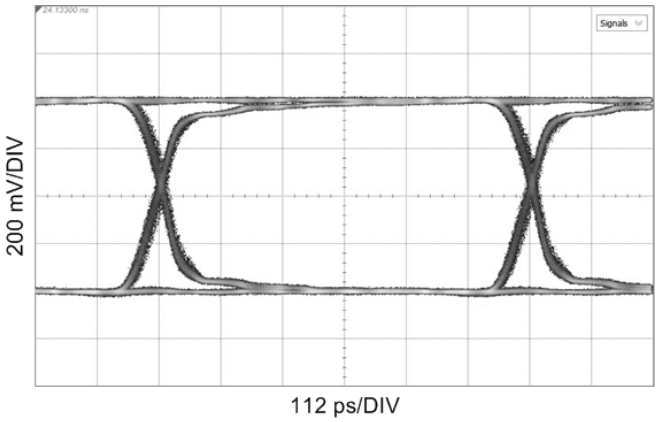
Figure 31. Test Setup for LMH0397 Loop-Through in EQ Mode

The eye diagrams in this subsection show the LMH0397 75-Ω loop-through output at SDI_OUT+.



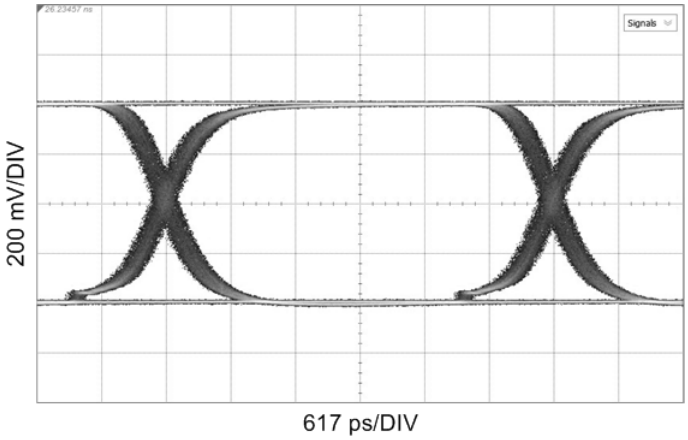
EQ Mode, measured at SDI_OUT+
HOST_EQ0 = F, SDI_OUT_SEL = L, OUT_CTRL = F

Figure 32. 2.97 Gbps, CC = 200-m Belden 1694A, Reclocked



EQ Mode, measured at SDI_OUT+
HOST_EQ0 = F, SDI_OUT_SEL = L, OUT_CTRL = F

Figure 33. 1.485 Gbps, CC = 280-m Belden 1694A, Reclocked



EQ Mode, measured at SDI_OUT+
HOST_EQ0 = F, SDI_OUT_SEL = L, OUT_CTRL = F

Figure 34. 270 Mbps, CC = 600-m Belden 1694A, Reclocked

10 Power Supply Recommendations

The LMH0397 requires decoupling capacitors to ensure a stable power supply. For power supply decoupling, 0.1-μF surface-mount ceramic capacitors must be placed close to each VDD_CDR, VDD_LDO, and VIN supply pin to VSS. Larger bulk capacitors (for example, 10 μF and 1 μF) are recommended for VDD_CDR and VIN.

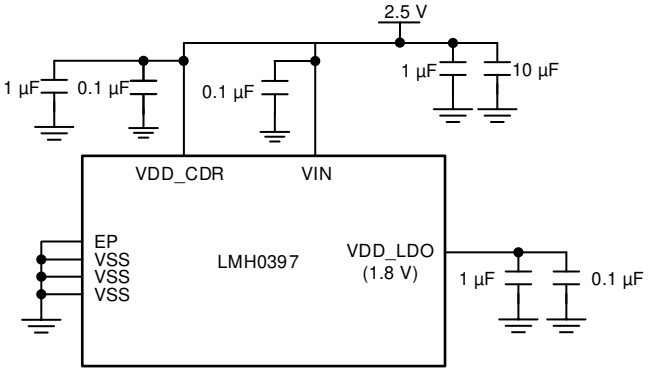


Figure 35. Recommended Power Supply Decoupling

Good supply bypassing requires low inductance capacitors. This can be achieved through an array of multiple small body size surface-mount bypass capacitors to keep low supply impedance. Better results can be achieved through the use of a buried capacitor formed by a VDD and VSS plane separated by 2-mil to 4-mil dielectric in a printed-circuit board.

11 Layout

11.1 Layout Guidelines

The following guidelines are recommended to optimize the board layout for the LMH0397.

11.1.1 Board Stack-Up and Ground References

- Choose a suitable board stack-up that supports 75-Ω single-ended trace and 100-Ω differential trace routing on the top layer of the board. This is typically done with a Layer-2 ground plane reference for the 100-Ω differential traces and a Layer-3 ground plane reference for the 75-Ω single-end traces.
- Maintain a distance of at least five times the trace width between signal trace and ground reference if they are on the same layer. This prevents unwanted changes in the characteristic impedance.
- Maintain a consistent ground plane reference for each high-speed trace from source to endpoint. Ground reference discontinuities lead to characteristic impedance mismatch.

11.1.2 High-Speed PCB Trace Routing and Coupling

Observe the following general high-speed recommendations for high-speed trace routing:

- For differential pairs, maintain a uniform width and gap for each differential pair where possible. When traces must diverge (for example, due to AC-coupling capacitors), ensure that the traces branch out or merge uniformly.
- To prevent reflections due to trace routing, ensure that trace bends are at most 45°. Right-angle bends must be implemented with at least two 45° corners. Radial bends are ideal.
- Avoid using signal vias. If signal vias must be used, a return path (GND) via must be placed near the signal via to provide a consistent ground reference and minimize impedance discontinuities.
- Avoid via stubs by back-drilling as necessary.

Layout Guidelines (continued)

11.1.2.1 SDI_IO± and SDI_OUT±

- Use an uncoupled trace with 75-Ω single-ended impedance for signal routing to SDI_IO± and SDI_OUT±.
- The trace width is typically 8 to 10 mils with reference to a Layer-3 ground plane.

11.1.2.2 IN0± and OUT0±

- Use coupled traces with 100-Ω differential impedance for signal routing to IN0± and OUT0±.
- The trace width is typically 5 to 8 mils with reference to a Layer-2 ground plane.

11.1.3 Anti-Pads

- Place anti-pads (ground relief) on the power and ground planes directly under the 4.7-µF, AC-coupling capacitor and IC landing pads to minimize parasitic capacitance. The size of the anti-pad and the number of layers to use the anti-pad depend on the board stack-up and can be determined by a 3-dimension electromagnetic simulation tool.

11.1.4 BNC Connector Layout and Routing

- Use a well-designed BNC footprint to ensure the signal landing pad achieves 75-Ω characteristic impedance. BNC suppliers usually provide recommendations on BNC footprint for best results.
- Keep trace length short between the BNC and SDI_IO±. The trace routing for SDI_IO+ and SDI_IO– must be as symmetrical as possible, with approximately equal lengths and equal loading. The same is true for SDI_OUT+ and SDI_OUT–.

11.1.5 Power Supply and Ground Connections

- Connect each supply pin (VDD_CDR, VIN, VDD_LDO) directly to the power or ground planes with a short via. The via is usually placed tangent to the landing pads of the supply pins with the shortest trace possible.
- Power supply decoupling capacitors must be a small physical size (0402 or smaller) and placed close to the supply pins to minimize inductance. The capacitors are commonly placed on the bottom layer and share the ground of the EP (Exposed Pad).

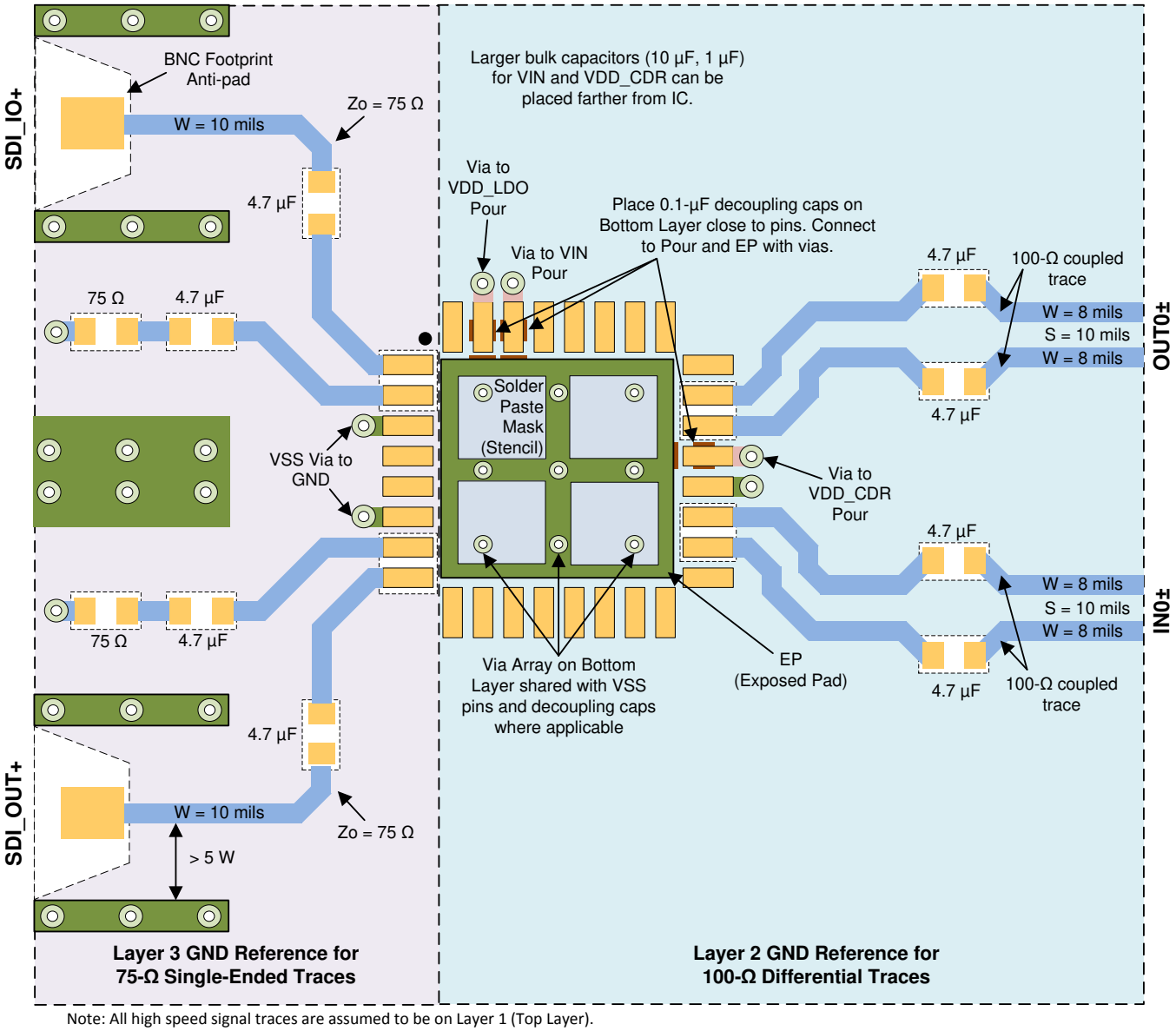
11.1.6 Footprint Recommendations

- Stencil parameters for the EP (Exposed Pad) such as aperture area ratio and the fabrication process have a significant impact on paste deposition. TI highly recommends inspecting the stencil before setting the placement of the WQFN package to improve board assembly yields. If the via and aperture openings are not carefully monitored, the solder may flow unevenly through the EP. Stencil parameters for aperture opening and via locations are shown in the RTV package drawing in *机械、封装和可订购信息*.
- The EP of the package must be connected to the ground plane through a 3 × 3 via array. These vias are solder-masked to avoid solder flowing into the plated-through holes during the board manufacturing process. Details about via dimensions are also shown in the RTV package drawing in *机械、封装和可订购信息*.

More information on the WQFN style package is provided in *QFN/SON PCB Attachment Application Report* (SLUA271).

11.2 Layout Example

The example shown in Figure 36 demonstrates the LMH0397 layout guidelines highlighted in *Layout Guidelines*.



Note: All high speed signal traces are assumed to be on Layer 1 (Top Layer).

Figure 36. LMH0397 High-Speed Trace Layout Example

12 器件和文档支持

12.1 器件支持

12.1.1 开发支持

如需开发支持，请参阅以下文档：

LMH1297。

12.2 文档支持

12.2.1 相关文档

请参阅如下相关文档：

- *《焊接的绝对最大额定值》*(SNOA549)
- *《LMH0397 编程指南》* (SNLU225)
- *《QFN/SON PCB 连接应用报告》*(SLUA271)

12.3 接收文档更新通知

如需接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 支持资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.5 商标

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12.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.7 出口管制提示

接收方同意：如果美国或其他适用法律限制或禁止将通过本协议的披露方获得的任何产品或技术数据（其中包括软件）（见美国、欧盟和其他出口管理条例之定义）、或者其他适用国家条例限制的任何受管制产品或此项技术的任何直接产品出口或再出口至任何目的地，那么在没有事先获得美国商务部和其他相关政府机构授权的情况下，接收方不得在知情的情况下，以直接或间接的方式将其出口。

12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

13.1 Package Option Addendum

13.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (3)	MSL Peak Temp (4)	Op Temp (°C)	Device Marking (5) (6)
LMH0397RTVR	ACTIVE	WQFN	RTV	32	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	L0397
LMH0397RTVT	ACTIVE	WQFN	RTV	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	L0397

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

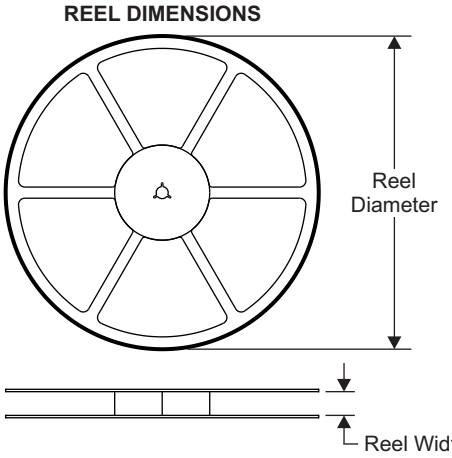
(3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

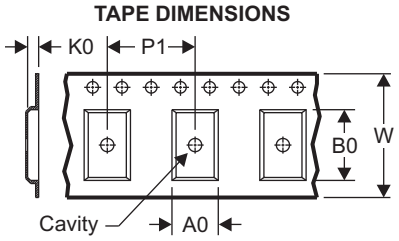
(4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

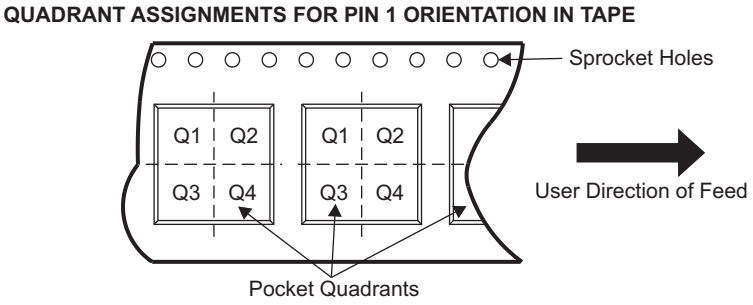
(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

13.1.2 Tape and Reel Information



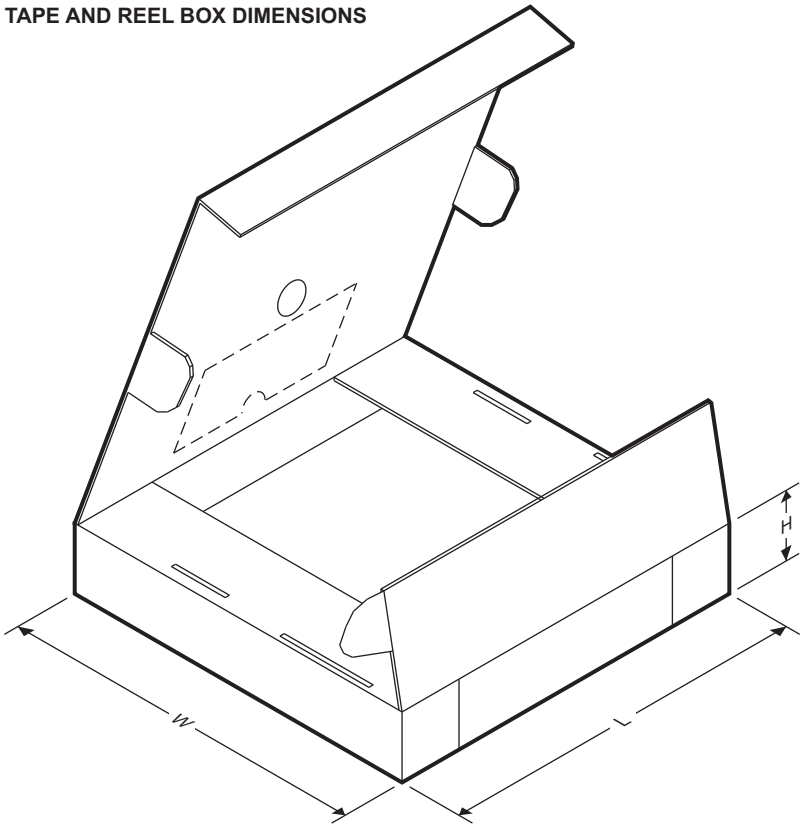


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH0397RTVR	WQFN	RTV	32	1000	178.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
LMH0397RTVT	WQFN	RTV	32	250	178.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

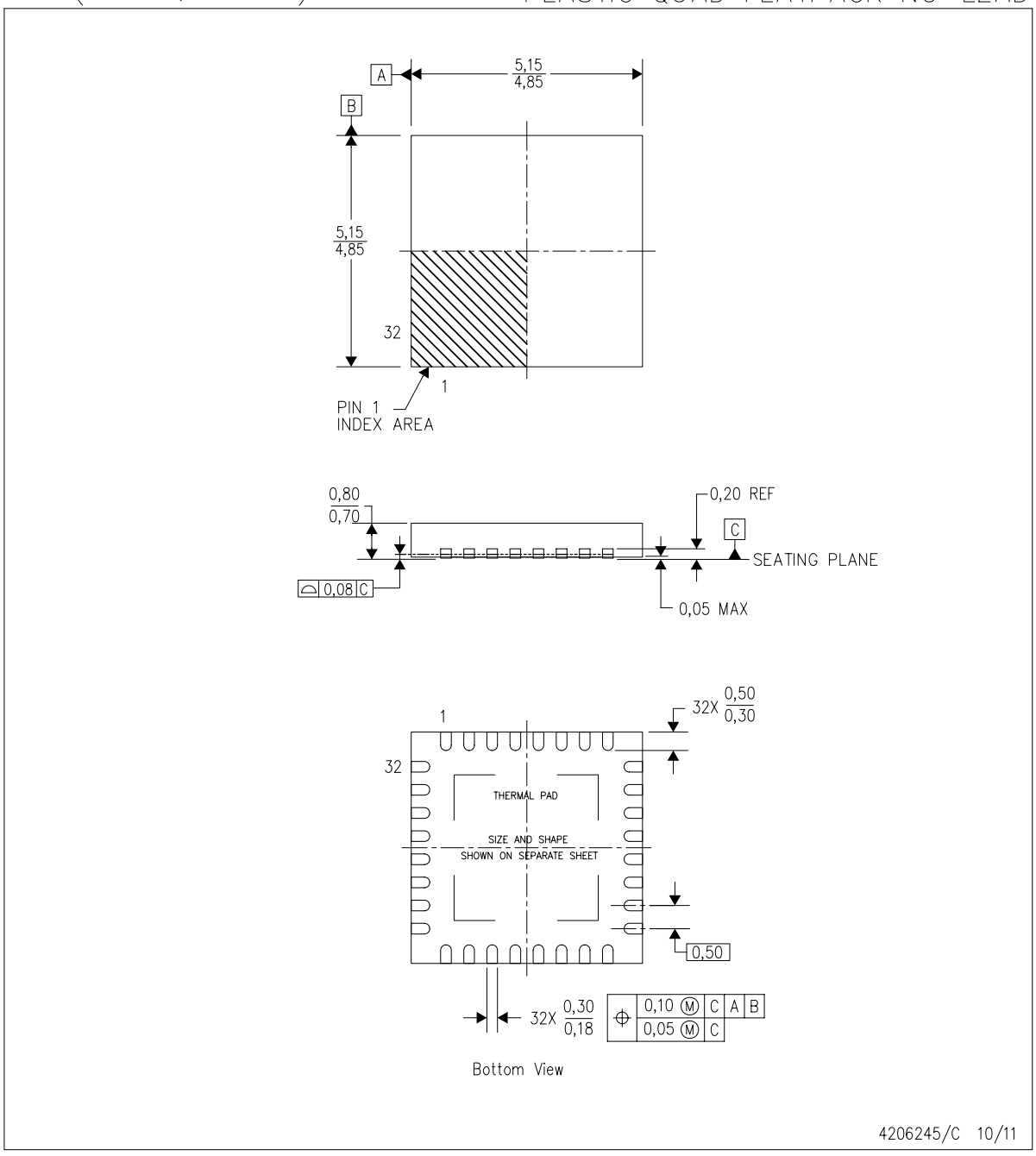
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH0397RTVR	WQFN	RTV	32	1000	210.0	185.0	35.0
LMH0397RTVT	WQFN	RTV	32	250	210.0	185.0	35.0

MECHANICAL DATA

RTV (S–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

THERMAL PAD MECHANICAL DATA

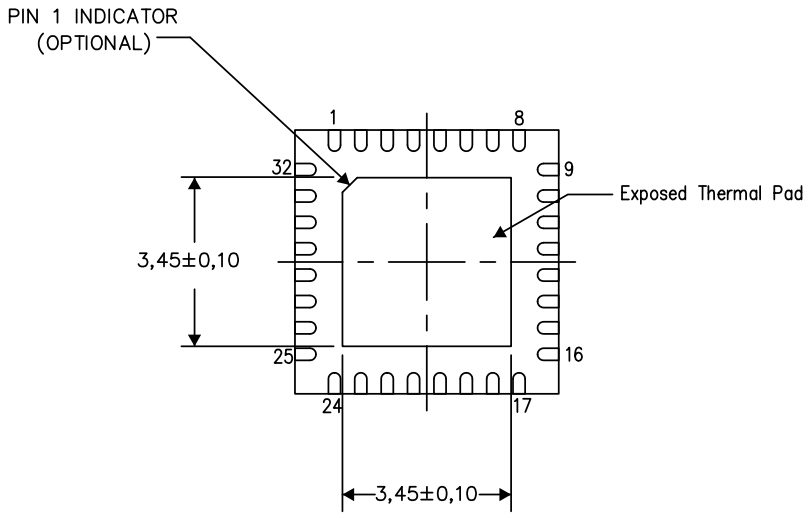
RTV (S–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

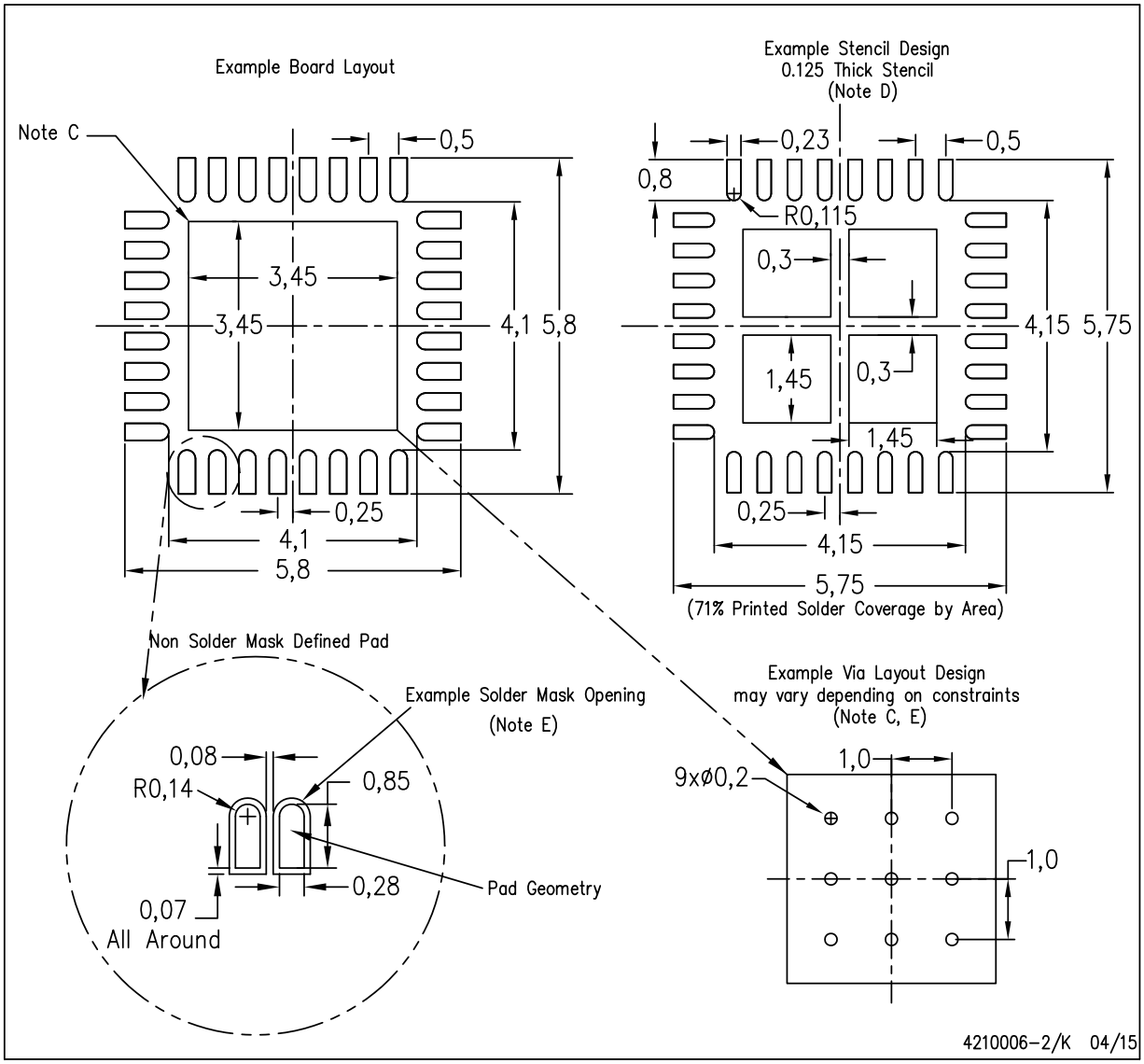
Exposed Thermal Pad Dimensions

4206250–2/Q 05/15

NOTE: All linear dimensions are in millimeters

LAND PATTERN DATA

RTV (S–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMH0397RTVR	ACTIVE	WQFN	RTV	32	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	L0397	Samples
LMH0397RTVT	ACTIVE	WQFN	RTV	32	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	L0397	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

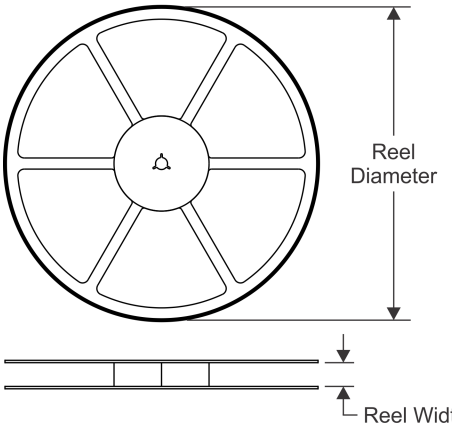
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

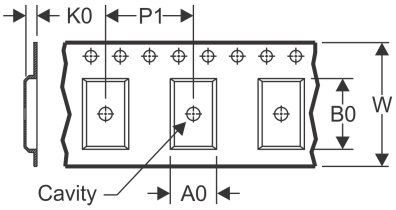
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

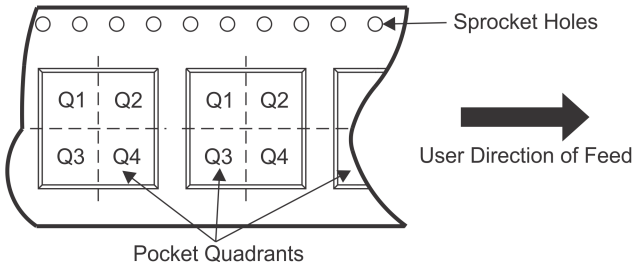


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

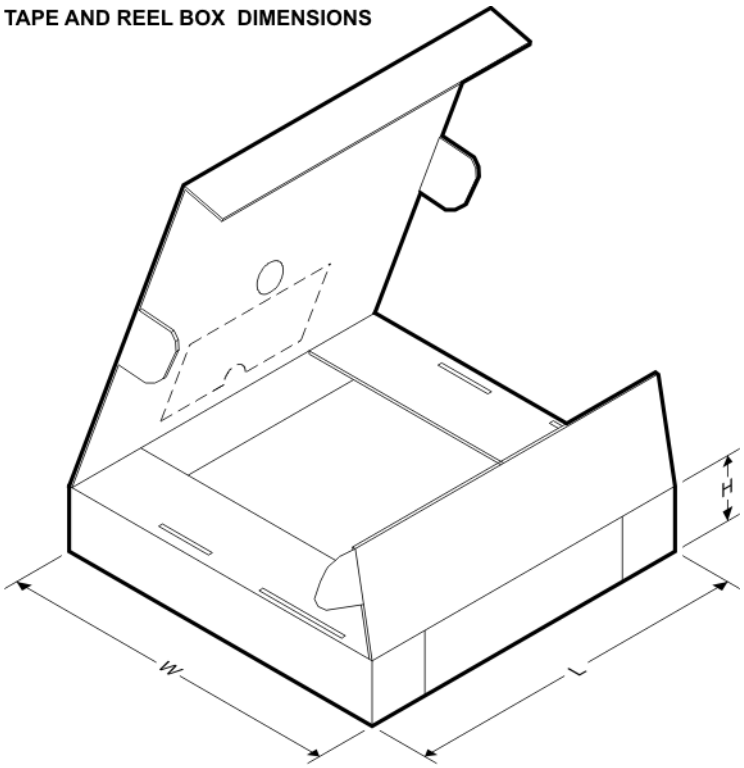
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMH0397RTVR	WQFN	RTV	32	1000	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
LMH0397RTVT	WQFN	RTV	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

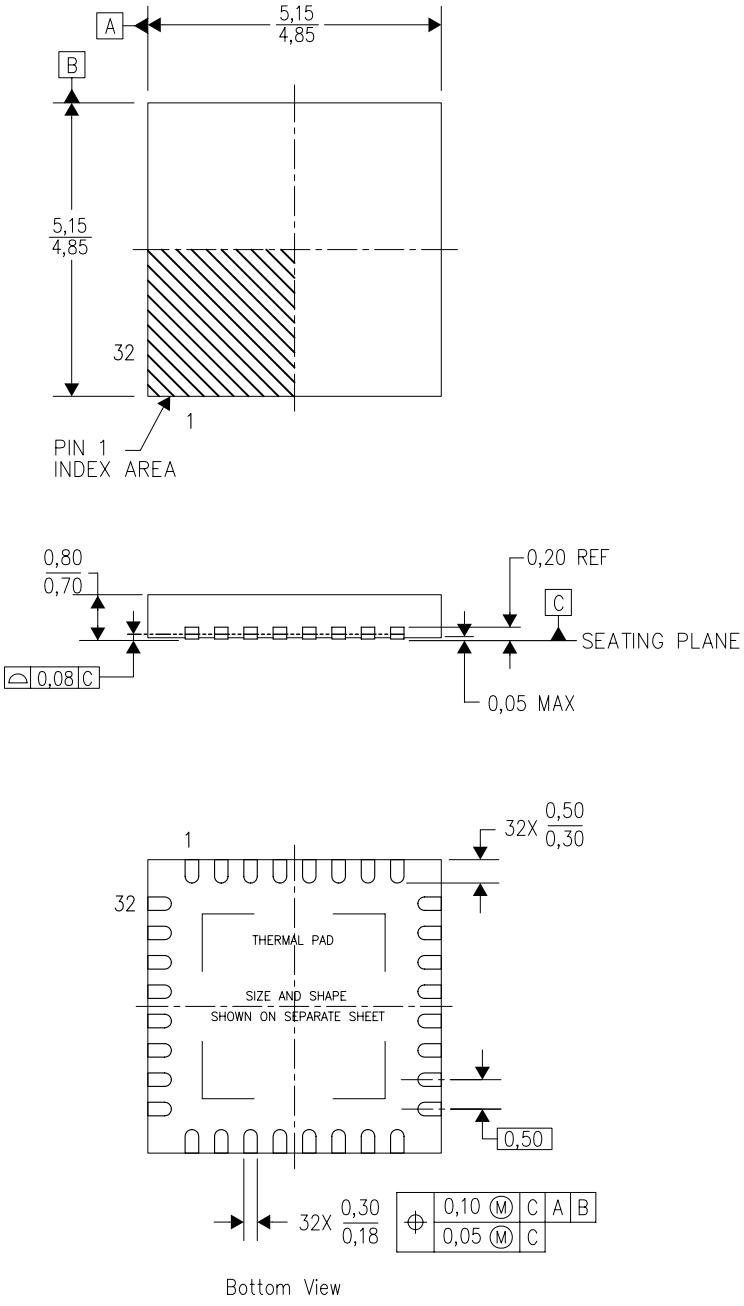
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMH0397RTVR	WQFN	RTV	32	1000	210.0	185.0	35.0
LMH0397RTVT	WQFN	RTV	32	250	210.0	185.0	35.0

RTV (S–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



4206245/C 10/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

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