# LMH6401 直流至 4.5GHz、全差分数字可变增益放大器

## 1 特性

- 3dB 带宽：4.5GHz（26dB 增益时）
- 增益范围：–6dB 至 26dB（步长为 1dB）
- 差分输入阻抗：100Ω
- 支持共模控制的差分输出
- 最大增益条件下的失真（$V_O$ = 2 $V_{PPD}$，$R_L$ = 200Ω）：
  - 200MHz：HD2 为 –73dBc，HD3 为 –80dBc
  - 500 MHz：HD2 为 –68dBc，HD3 为 –72dBc
  - 1 GHz：HD2 为 –63dBc，HD3 为 –63dBc
  - 2 GHz：HD2 为 –58dBc，HD3 为 –54dBc
- 输出 IP3：
  - 200MHz 时为 43dBm
  - 1GHz 时为 33dBm
  - 2GHz 时为 27dBm
- 输出 IP2：
  - 200MHz 时为 67dBm
  - 1GHz 时为 60dBm
  - 2GHz 时为 52dBm
- 1GHz、$R_S$ = 100Ω 时的噪声系数为 8dB
- 82ps 上升/下降时间脉冲响应
- 供电电源：5.0V/69mA
- 支持单电源和 (±) 分离电源供电：
  - 直流和交流耦合应用
- 采用先进的互补 BiCMOS 工艺制成
- 3mm × 3mm 超薄四方扁平无引线 (UQFN)-16 封装

## 2 应用

- 测试和测量
- 超宽带模数转换器 (ADC) 驱动器
- 通信接收器
- 射频 (RF) 采样子系统
- 表面声波 (SAW) 滤波缓冲器和驱动器
- 国防设备和雷达

## 3 说明

LMH6401 是一款面向直流到射频 (RF)、中频 (IF) 和高速时域应用的宽带、数控可变增益放大器 (DVGA)。对于需要自动增益控制 (AGC) 的直流或交流耦合应用而言，该器件是一款理想的 ADC 驱动器。

该器件对噪声和失真性能进行了优化，以便驱动超宽带 ADC。 放大器在最大增益条件下的噪声系数为 8dB，在 1GHz 满量程信号电平条件下的谐波失真为 -63dBc。 该器件支持单电源和分离电源供电，以驱动 ADC。 该器件提供了共模参考输入引脚，以便使放大器输出共模符合 ADC 输入要求。

该器件通过 SPI™ 接口执行增益控制，并且支持 32dB 的增益范围（–6dB 至 26dB，步长为 1dB）。 此外，还可以通过外部 PD 引脚或串行外设接口 (SPI) 控制提供掉电功能。

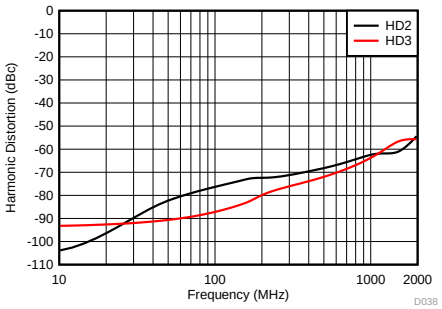
这一性能水平在 345mW 的低功耗下才能实现。 器件工作的环境温度范围为 –40°C 至 85°C。

器件信息(1)

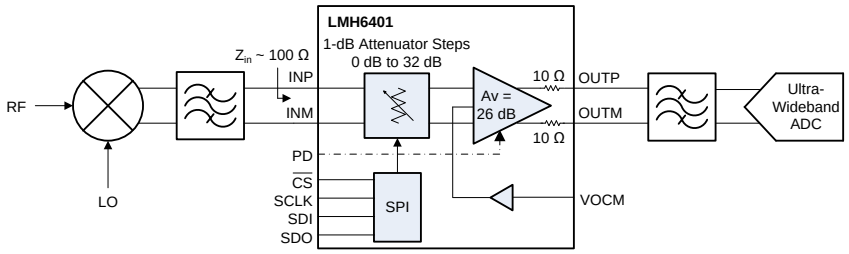
| 器件型号 | 封装 | 封装尺寸（标称值） |
|---|---|---|
| LMH6401 | UQFN (16) | 3.00mm x 3.00mm |

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

谐波失真与频率间的关系 ($V_O$ = 2 $V_{PPD}$)




IF 采样接收器应用



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# 5 Device Options

**Table 1. FDA Device Companion**

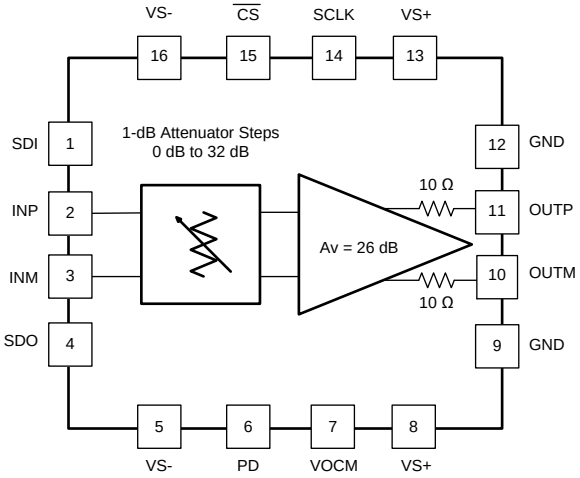
| DEVICE | BW ($A_V$ = 12 dB) | DISTORTION | NOISE |
|---|---|---|---|
| LMH5401 | 6.2 GHz | –75-dBc HD2, –75-dBc HD3 at 500 MHz | 1.25 nV/√Hz |
| LMH3401 | 7 GHz, G = 16 dB | –79-dBc HD2, –77-dBc HD3 at 500 MHz | 1.4 nV/√Hz |
| LMH6554 | 1.6 GHz | –79-dBc HD2, –70-dBc HD3 at 250 MHz | 0.9 nV/√Hz |

**Table 2. DVGA Device Comparison**

| DEVICE | MAX GAIN, BW | DISTORTION | NOISE FIGURE |
|---|---|---|---|
| LMH6517 | 22 dB, 1.2 GHz | 43-dBm OIP3 at 200 MHz, –74-dBc HD3 at 200 MHz | 5.5 dB |
| LMH6521 | 26 dB, 1.2 GHz | 49-dBm OIP3 at 200 MHz, –84-dBc HD3 at 200 MHz | 7.3 dB |
| LMH6881 | 26 dB, 2.4 GHz | 42-dBm OIP3 at 200 MHz, –76-dBc HD3 at 200 MHz | 9.7 dB |

# 6 Pin Configuration and Functions

**RMZ Package**
**UQFN-16**
**Top View**




**Pin Functions**

| PIN | | FUNCTION | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | SDI | Input | Serial interface input data |
| 2 | INP | Input | Positive input pin |
| 3 | INM | Input | Negative input pin |
| 4 | SDO | Output | Serial interface output data |
| 5 | VS– | Power | Negative supply voltage |
| 6 | PD | Input | Power-down pin.<br>0 = amplifier enabled, 1 = amplifier disabled |
| 7 | VOCM | Input | Input pin to set amplifier output common-mode voltage |
| 8 | VS+ | Power | Positive supply voltage |
| 9 | GND | Power | Ground |
| 10 | OUTM | Output | Negative output pin |
| 11 | OUTP | Output | Positive output pin |
| 12 | GND | Power | Ground |
| 13 | VS+ | Power | Positive supply voltage |
| 14 | SCLK | Input | Serial interface clock |
| 15 | $\overline{CS}$ | Input | Chip select |
| 16 | VS– | Power | Negative supply voltage |

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage | V = (VS+) – (VS–) | | 5.5 | V |
| Digital input pins | | –0.3 | VS+ | V |
| Maximum input difference voltage | | | 2.1 | V |
| Maximum input voltage | | VS– | VS+ | V |
| Temperature | Maximum junction, $T_J$ | | 150 | °C |
| | Maximum junction, continuous operation, long-term reliability | | 125 | °C |
| | Operating free-air, $T_A$ | –40 | 85 | °C |
| | Storage, $T_{stg}$ | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1) | ±2000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101(2) | ±1000 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage | 4.0 | 5.0 | 5.25 | V |
| Minimum operating positive (VS+) supply voltage | 2.0 | | | V |
| Ambient operating air temperature, $T_A$ | –40 | 25 | 85 | °C |
| Operating junction temperature, $T_J$ | –40 | | 125 | °C |

## 7.4 Thermal Information

| THERMAL METRIC(1) | | LMH6401 RMZ (UQFN) 16 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 78 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 43 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 24 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 2.3 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 24 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | °C/W |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## 7.5 Electrical Characteristics

At $T_A$ = 25°C, VS– = –2.5 V, VS+ = 2.5 V, VOCM = 0 V, $R_{LOAD}$ = 200-Ω differential ($R_{o(internal,\ diff)}$ = 20 Ω), $V_O$ = 2 $V_{PPD}$, and $A_V$ = 26 dB, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT | TEST LEVEL(1) |
|---|---|---|---|---|---|---|---|---|
| **DYNAMIC PERFORMANCE** | | | | | | | | |
| SSBW | Small-signal, –3-dB bandwidth | $A_V$ = 26 dB, $V_O$ = 200 $mV_{PPD}$ | | | 4.5 | | GHz | C |
| LSBW | Large-signal, –3-dB bandwidth | $A_V$ = 26 dB, $V_O$ = 2.0 $V_{PPD}$ | | | 4.5 | | GHz | C |
| | Bandwidth for 0.1-dB flatness | $A_V$ = 26 dB, $V_O$ = 2.0 $V_{PPD}$ | | | 500 | | MHz | C |
| SR | Slew rate | $V_O$ = 2-V step | | | 18200 | | V/µs | C |
| $t_R$, $t_F$ | Rise and fall time | $V_O$ = 2-V step, 10% to 90% | | | 82 | | ps | C |
| | Overdrive recovery | Overdrive = ±0.5 V | | | 600 | | ps | C |
| | Output balance error | f = 1 GHz | | | –47 | | dB | C |
| $t_s$ | Settling time to 1% | $V_O$ = 2-V step, $R_L$= 200 Ω | | | 700 | | ps | C |
| HD2 | Second-harmonic distortion | f = 200 MHz, $V_O$ = 2.0 $V_{PPD}$ | | | –73 | | dBc | C |
| | | f = 500 MHz, $V_O$ = 2.0 $V_{PPD}$ | | | –68 | | dBc | C |
| | | f = 1 GHz, $V_O$ = 2.0 $V_{PPD}$ | | | –63 | | dBc | C |
| | | f = 2 GHz, $V_O$ = 2.0 $V_{PPD}$ | | | –58 | | dBc | C |
| HD3 | Third-harmonic distortion | f = 200 MHz, $V_O$ = 2.0 $V_{PPD}$ | | | –80 | | dBc | C |
| | | f = 500 MHz, $V_O$ = 2.0 $V_{PPD}$ | | | –72 | | dBc | C |
| | | f = 1 GHz, $V_O$ = 2.0 $V_{PPD}$ | | | –63 | | dBc | C |
| | | f = 2 GHz, $V_O$ = 2.0 $V_{PPD}$ | | | –54 | | dBc | C |
| OIP2 | Output second-order intercept point | f = 200 MHz, $P_O$ = –2 dBm per tone | | | 67 | | dBm | C |
| | | f = 500 MHz, $P_O$ = –2 dBm per tone | | | 65 | | dBm | C |
| | | f = 1 GHz, $P_O$ = –2 dBm per tone | | | 60 | | dBm | C |
| | | f = 2 GHz, $P_O$ = –2 dBm per tone | | | 52 | | dBm | C |
| OIP3 | Output third-order intercept point | f = 200 MHz, $P_O$ = –2 dBm per tone | | | 43 | | dBm | C |
| | | f = 500 MHz, $P_O$ = –2 dBm per tone | | | 40 | | dBm | C |
| | | f = 1 GHz, $P_O$ = –2 dBm per tone | | | 33 | | dBm | C |
| | | f = 2 GHz, $P_O$ = –2 dBm per tone | | | 27 | | dBm | C |
| IMD2 | Second-order intermodulation distortion | f = 500 MHz, $V_O$ = 1.0 $V_{PP}$ per tone | | | –68 | | dBc | C |
| IMD3 | Third-order intermodulation distortion | f = 500 MHz, $V_O$ = 1.0 $V_{PP}$ per tone | | | –83 | | dBc | C |
| P1dB | 1-dB compression point | f = 500 MHz, power measured at amplifier output | | | 18.3 | | dBm | C |
| NF | Noise figure | $R_S$ = 100 Ω | f = 200 MHz | | 7.7 | | dB | C |
| | | | f = 1 GHz | | 8 | | dB | C |
| | Output-referred noise voltage | $A_V$ = 26 dB, f > 1 MHz | | | 30.4 | | nV/√Hz | C |
| S12 | Reverse transmission (S12) | f = 1 GHz | | | –65 | | dB | C |
| S11 | Input return loss (S11) | 100-Ω system, f = 2 GHz | | | –15 | | dB | C |
| **GAIN PARAMETERS** | | | | | | | | |
| | Maximum voltage gain | | | 25.5 | 26.0 | 26.5 | dB | A |
| | Minimum voltage gain | | | –7.5 | –6.0 | –4.5 | dB | A |
| | Gain range | | | | 32 | | dB | C |
| | Gain step size | | | 0.9 | 1 | 1.1 | dB | A |
| | Cumulative gain error | $A_V$ = 26 dB to 10 dB (referenced to 26-dB gain) | | –0.5 | | 0.5 | dB | A |
| | | $A_V$ = 26 dB to –6 dB (referenced to 26-dB gain) | | –1 | | 1 | dB | A |
| | Gain step transition time | | | | 1 | | ns | C |

(1) Test levels: (A) 100% DC tested at 25°C unless otherwise specified. Over-temperature limits by characterization and simulation. (B) Limits set by bench verification and simulation. (C) Typical value only for information.

## Electrical Characteristics (continued)

At $T_A$ = 25°C, VS– = –2.5 V, VS+ = 2.5 V, VOCM = 0 V, $R_{LOAD}$ = 200-Ω differential ($R_{o(internal,\ diff)}$ = 20 Ω), $V_O$ = 2 $V_{PPD}$, and $A_V$ = 26 dB, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT | TEST LEVEL (1) |
|---|---|---|---|---|---|---|---|
| **ANALOG INPUT CHARACTERISTICS** | | | | | | | |
| $R_i$ | Input resistance | Differential | 85 | 100 | 112 | Ω | A |
| $C_i$ | Input capacitance | Differential | | 0.8 | | pF | C |
| $V_{ICM}$ | Input common-mode voltage | Self-biased to mid-supply | –0.3 | | 0.3 | V | A |
| $V_{ICLR}$ | Low-level input common-mode voltage range | Differential gain shift < 1 dB | | (VS–) + 1.5 | | V | C |
| $V_{ICHR}$ | High-level input common-mode voltage range | Differential gain shift < 1 dB | | (VS+) – 1.5 | | V | C |
| **ANALOG OUTPUT CHARACTERISTICS** | | | | | | | |
| $R_o$ | Output resistance | Differential | 18 | 20 | 25 | Ω | A |
| $V_{OL}$ | Low-level output voltage range | Low-level clipping level | | (VS–) + 1 | (VS–) + 1.1 | V | A |
| $V_{OH}$ | High-level output voltage range | High-level clipping level | (VS+) – 1.1 | (VS+) – 1 | | V | A |
| $V_{OM}$ | Maximum output voltage swing | Differential | | 6.0 | | $V_{PPD}$ | C |
| CMRR | Common-mode rejection ratio | ±0.3-V input common-mode shift | 38.4 | 45 | | dB | A |
| **POWER SUPPLY** | | | | | | | |
| $V_S$ | Supply voltage [V = (VS+) – (VS–)] | | 4.0 | 5.0 | 5.25 | V | A |
| | Minimum positive (VS+) supply voltage | | 2.0 | | | V | A |
| PSRR | Power-supply rejection ratio | VS–, measured at 1-kHz sine-wave | 66 | 70 | | dB | A |
| | | VS+, measured at 1-kHz sine-wave | 66 | 70 | | dB | A |
| $I_Q$ | Quiescent current | PD = 0 (device enabled) | 60 | 69 | 78 | mA | A |
| | | PD = 1 (device disabled) | 1 | 7 | 12 | mA | A |
| **OUTPUT COMMON-MODE CONTROL (VOCM Pin)** | | | | | | | |
| SSBW | Small-signal bandwidth | VOCM = 200 $mV_{PP}$ | | 160 | | MHz | C |
| | VOCM voltage range low | VOCM gain < 2% | –0.5 | | | V | A |
| | VOCM voltage range high | VOCM gain < 2% | | | 0.5 | V | A |
| $V_{OO}$ | Output offset voltage | All gain settings | –40 | | 40 | mV | A |
| | VOCM gain | | | 1.0 | | V | C |
| $V_{OCM}$ | Common-mode offset voltage | VOCM pin driven to GND | –10 | | 10 | mV | A |
| **POWER DOWN (PD Pin)** | | | | | | | |
| | Power-down quiescent current | | 1 | 7 | 12 | mA | A |
| | PD bias current | PD = 2.5 V | | 80 | 100 | µA | A |
| | Turn-on time delay | Time to $V_O$ = 90% of final value | | 70 | | ns | C |
| | Turn-off time delay | Time to $V_O$ = 10% of original value | | 10 | | ns | C |
| **DIGITAL INPUT/OUTPUT** | | | | | | | |
| $V_{IH}$ | High-level input voltage | Referred to GND | 1.2 | | VS+ | V | A |
| $V_{IL}$ | Low-level input voltage | Referred to GND | | | 0.8 | V | A |
| $V_{OH}$ | High-level output voltage | 1 kΩ to GND | 1.4 | | | V | A |
| $V_{OL}$ | Low-level output voltage | 1 kΩ to GND | | | 0.4 | V | A |

## 7.6 SPI Timing Requirements(1)

At $T_A$ = 25°C, VS– = –2.5 V, VS+ = 2.5 V, VOCM = 0 V, $R_{LOAD}$ = 200-Ω differential ($R_{o(internal,\ diff)}$ = 20 Ω), $V_O$ = 2 $V_{PPD}$, and $A_V$ = 26 dB, unless otherwise noted. Limits set by bench verification and simulation.

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $f_{s\_c}$ | SCLK frequency | | | 50 | MHz |
| $t_{PH}$ | SCLK pulse duration, high | 10 | | | ns |
| $t_{PL}$ | SCLK pulse duration, low | 10 | | | ns |
| $t_{SU}$ | SDI setup | 3 | | | ns |
| $t_H$ | SDO hold | 3 | | | ns |
| $t_{IZ}$ | SDO tri-state | | | 3 | ns |
| $t_{ODZ}$ | SDO driven to tri-state(2) | | | 5 | ns |
| $t_{OZD}$ | SDO tri-state to driven | | | 3 | ns |
| $t_{OD}$ | SDO output delay(2) | | | 3 | ns |
| $t_{CSS}$ | $\overline{CS}$ setup(3) | 3 | | | ns |
| $t_{CSH}$ | $\overline{CS}$ hold | 3 | | | ns |
| $t_{IAG}$ | Inter-access gap | 20 | | | ns |

(1) Ensured by design.
(2) Reference to negative edge of SCLK.
(3) Reference to positive edge of SCLK.

## 7.7 Typical Characteristics

At $T_A$ = 25°C, VS– = –2.5 V, VS+ = 2.5 V, VOCM = 0 V, $R_{LOAD}$ = 200-Ω differential ($R_{o(internal,\ diff)}$ = 20 Ω), $V_O$ = 2 $V_{PPD}$, and $A_V$ = 26 dB, unless otherwise noted. Differential input and output, and input and output pins referenced to mid-supply, unless otherwise noted. Measured using an EVM as discussed in the *Parameter Measurement Information* section.

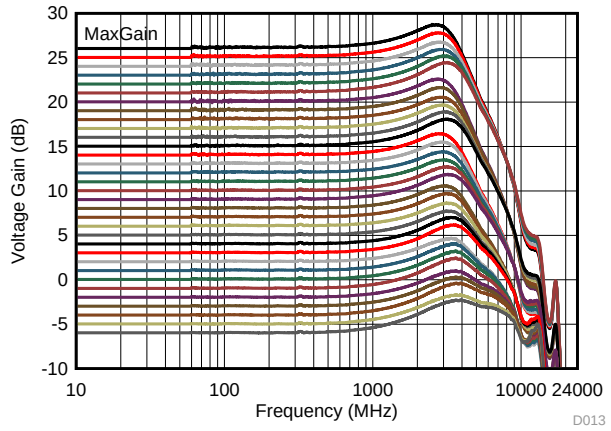



**Figure 1. Voltage Gain vs Frequency (1-dB Gain Steps)**

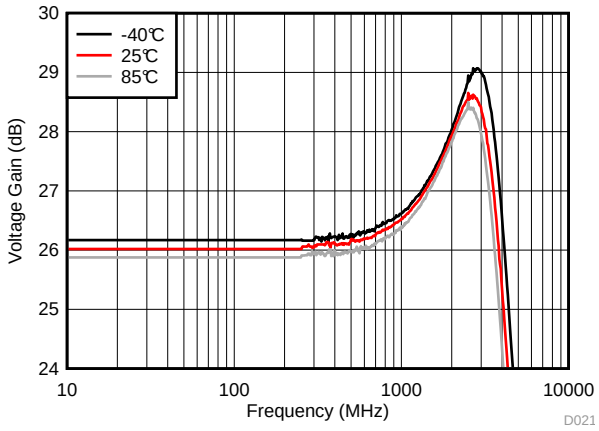



**Figure 2. Maximum Gain vs Temperature**

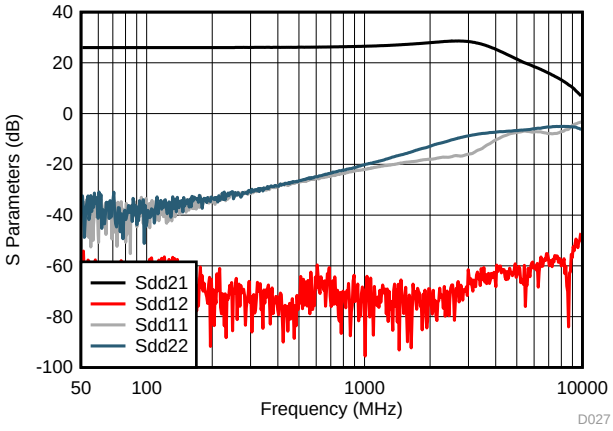



**Figure 3. S-Parameters vs Frequency**

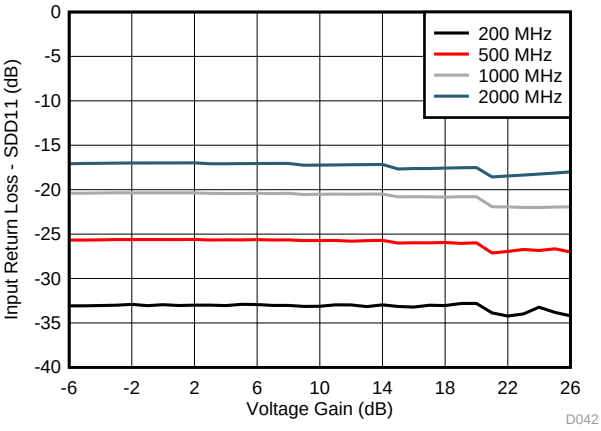



**Figure 4. Input Return Loss vs Gain Settings**

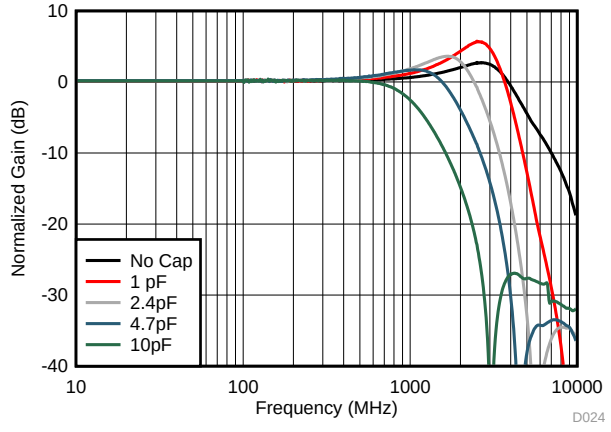
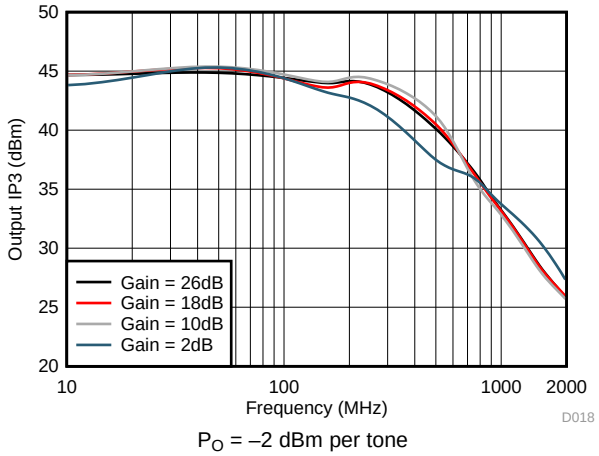



**Figure 5. Frequency Response vs Capacitive Load**

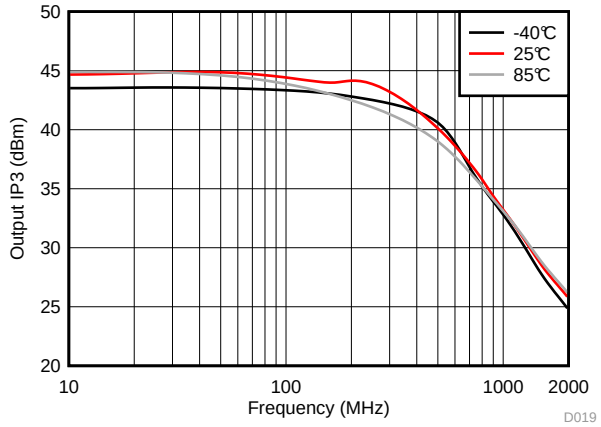



$P_O$ = –2 dBm per tone

**Figure 6. Output IP3 vs Frequency and Gain Settings**

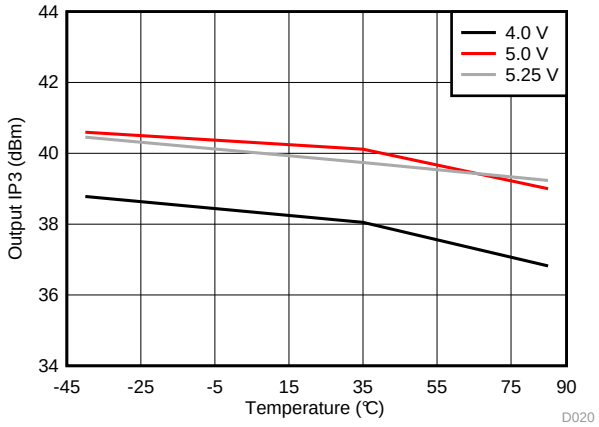
## Typical Characteristics (continued)

At $T_A$ = 25°C, VS– = –2.5 V, VS+ = 2.5 V, VOCM = 0 V, $R_{LOAD}$ = 200-Ω differential ($R_{o(internal,\ diff)}$ = 20 Ω), $V_O$ = 2 $V_{PPD}$, and $A_V$ = 26 dB, unless otherwise noted. Differential input and output, and input and output pins referenced to mid-supply, unless otherwise noted. Measured using an EVM as discussed in the *Parameter Measurement Information* section.




$P_O$ = –2 dBm per tone

**Figure 7. Output IP3 vs Frequency and Temperature**




f = 500 MHz, $P_O$ = –2 dBm per tone

**Figure 8. Output IP3 vs Supply Voltage and Temperature**

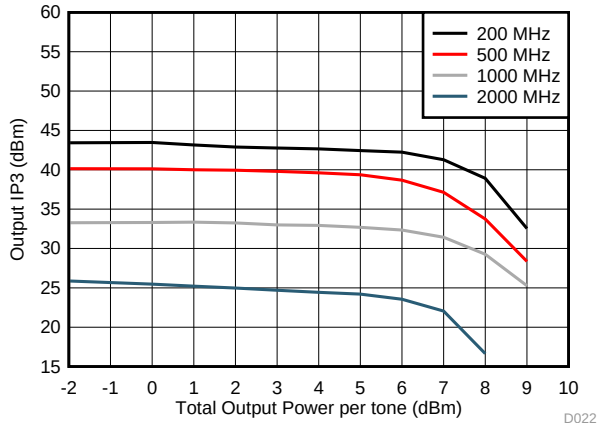
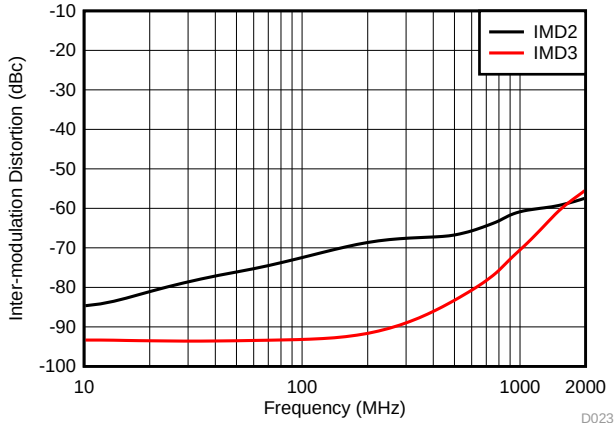



**Figure 9. Output IP3 vs Total Output Power per Tone**




$P_O$ = –2 dBm per tone

**Figure 10. Intermodulation Distortion vs Frequency**

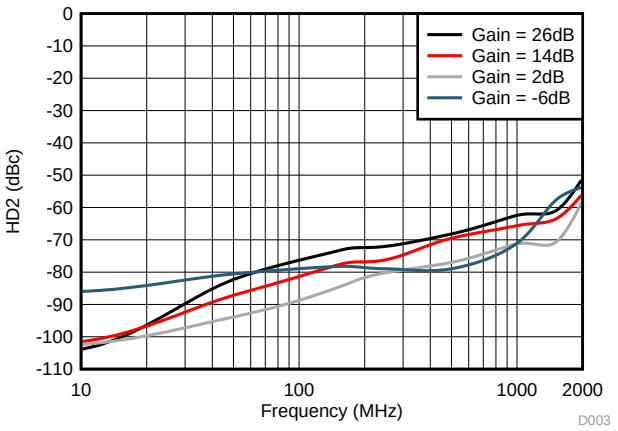



**Figure 11. Second-Order Harmonic Distortion vs Frequency**

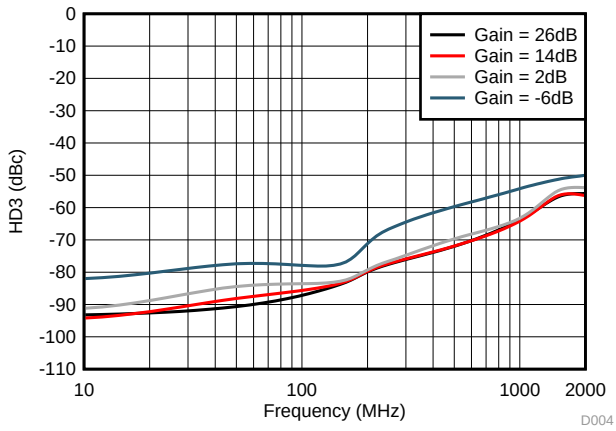



**Figure 12. Third-Order Harmonic Distortion vs Frequency**

## Typical Characteristics (continued)

At $T_A$ = 25°C, VS– = –2.5 V, VS+ = 2.5 V, VOCM = 0 V, $R_{LOAD}$ = 200-Ω differential ($R_{o(internal,\ diff)}$ = 20 Ω), $V_O$ = 2 $V_{PPD}$, and $A_V$ = 26 dB, unless otherwise noted. Differential input and output, and input and output pins referenced to mid-supply, unless otherwise noted. Measured using an EVM as discussed in the *Parameter Measurement Information* section.

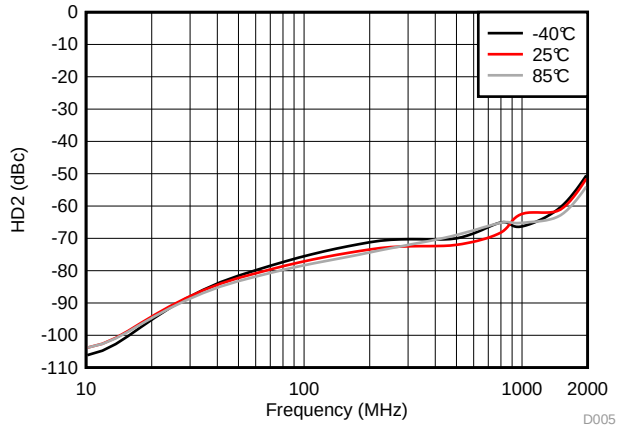



**Figure 13. Second-Order Harmonic Distortion vs Frequency**

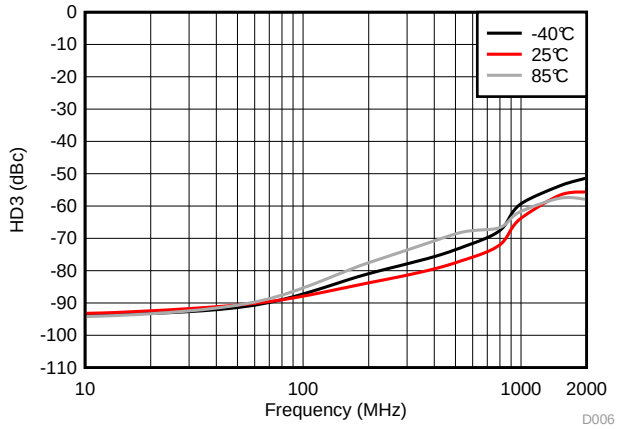



**Figure 14. Third-Order Harmonic Distortion vs Frequency**

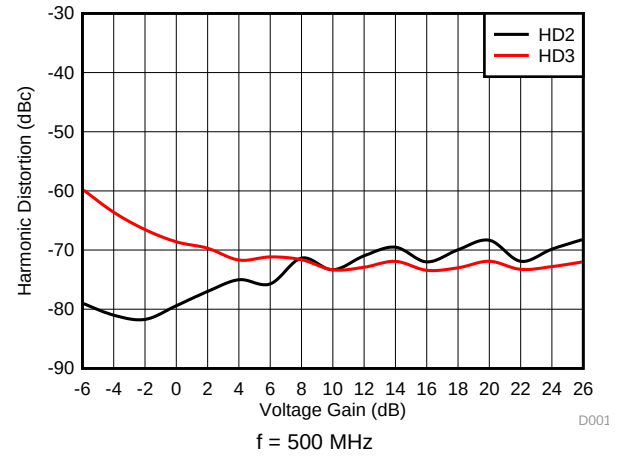



**Figure 15. Harmonic Distortion vs Gain Settings**

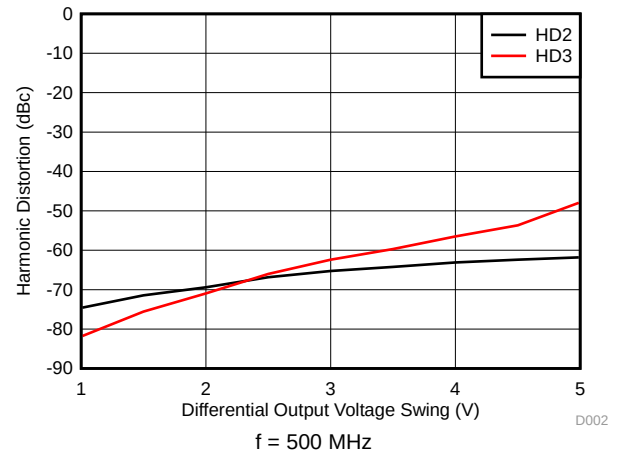



**Figure 16. Harmonic Distortion vs Differential $V_{PP}$**

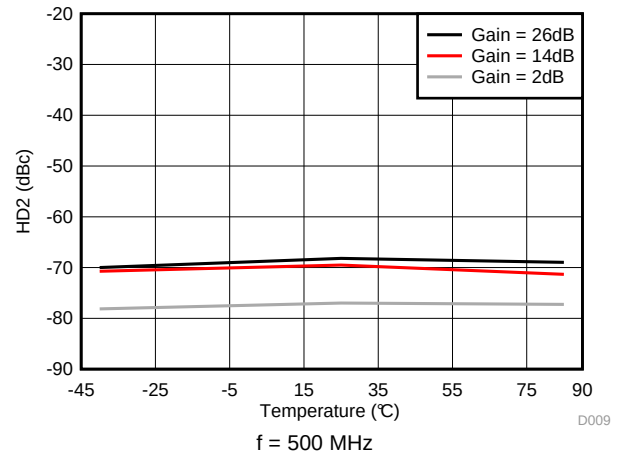



**Figure 17. Second-Order Harmonic Distortion vs Temperature**

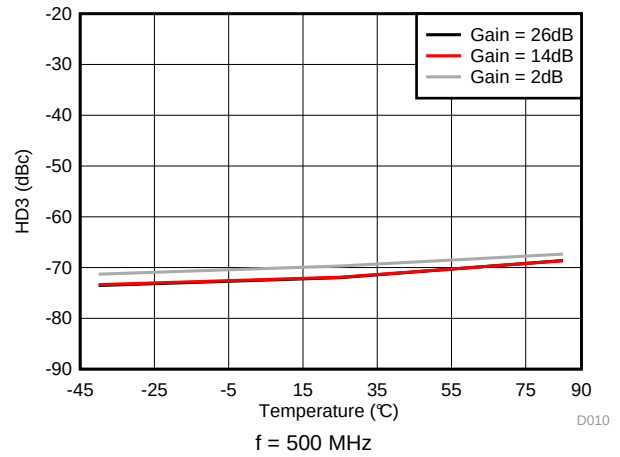
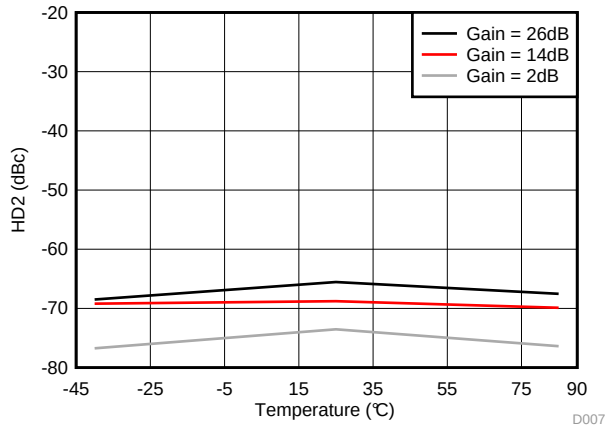



**Figure 18. Third-Order Harmonic Distortion vs Temperature**

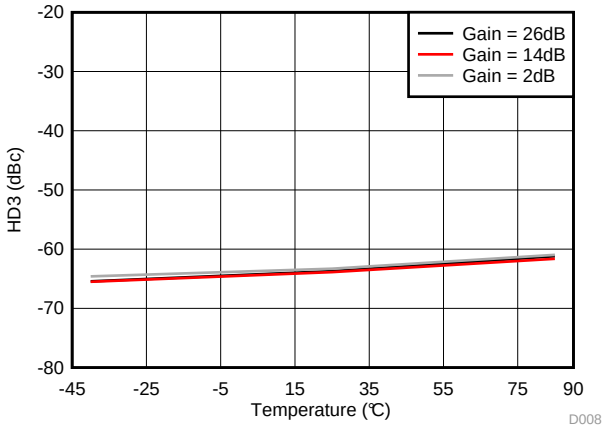
## Typical Characteristics (continued)

At $T_A$ = 25°C, VS– = –2.5 V, VS+ = 2.5 V, VOCM = 0 V, $R_{LOAD}$ = 200-Ω differential ($R_{o(internal,\ diff)}$ = 20 Ω), $V_O$ = 2 $V_{PPD}$, and $A_V$ = 26 dB, unless otherwise noted. Differential input and output, and input and output pins referenced to mid-supply, unless otherwise noted. Measured using an EVM as discussed in the *Parameter Measurement Information* section.



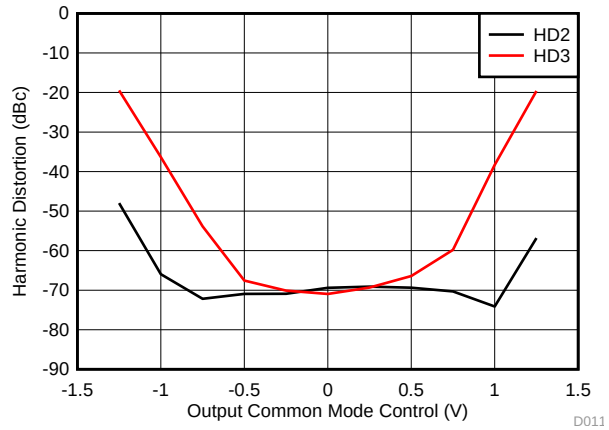

f = 500 MHz, (VS+) – (VS–) = 4 V

**Figure 19. Second-Order Harmonic Distortion vs Temperature**



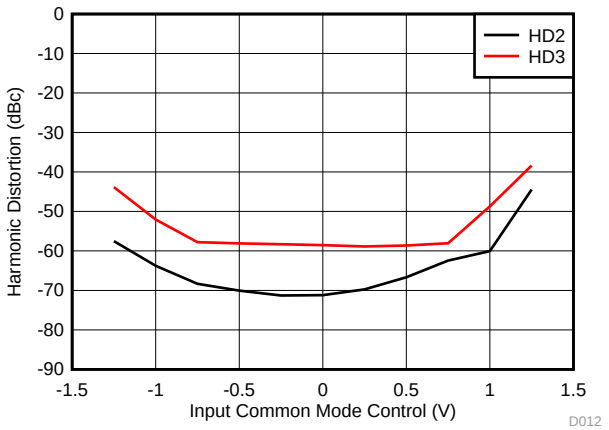

f = 500 MHz, (VS+) – (VS–) = 4 V

**Figure 20. Third-Order Harmonic Distortion vs Temperature**




f = 500 MHz

**Figure 21. Harmonic Distortion vs Output Common-Mode Voltage**




f = 500 MHz, gain = –6 dB

**Figure 22. Harmonic Distortion vs Input CM Voltage**

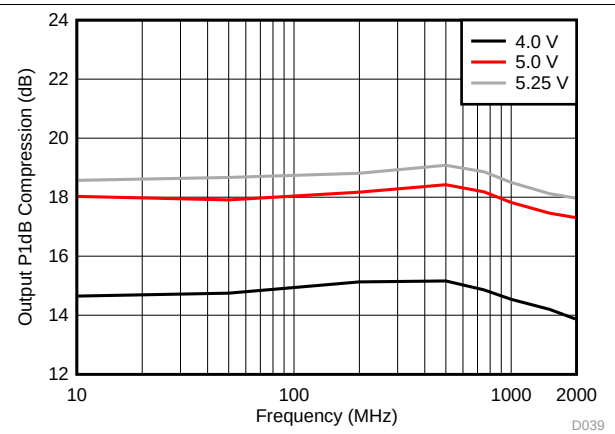



**Figure 23. Output P1dB vs Frequency**

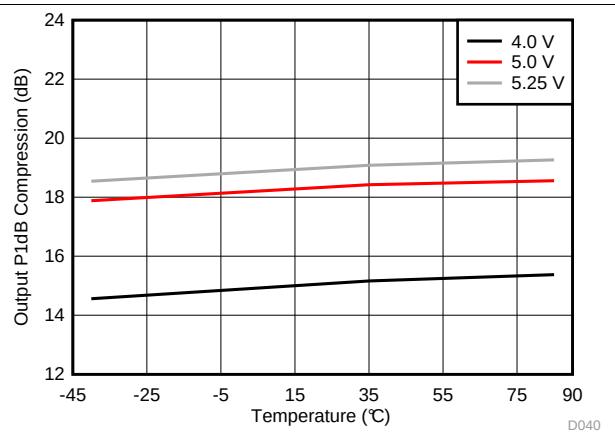



**Figure 24. Output P1dB vs Temperature**

## Typical Characteristics (continued)

At $T_A$ = 25°C, VS– = –2.5 V, VS+ = 2.5 V, VOCM = 0 V, $R_{LOAD}$ = 200-Ω differential ($R_{o(internal,\ diff)}$ = 20 Ω), $V_O$ = 2 $V_{PPD}$, and $A_V$ = 26 dB, unless otherwise noted. Differential input and output, and input and output pins referenced to mid-supply, unless otherwise noted. Measured using an EVM as discussed in the *Parameter Measurement Information* section.

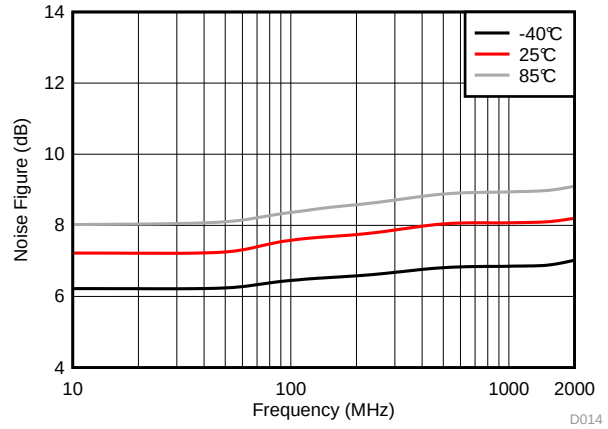



**Figure 25. Noise Figure vs Frequency**

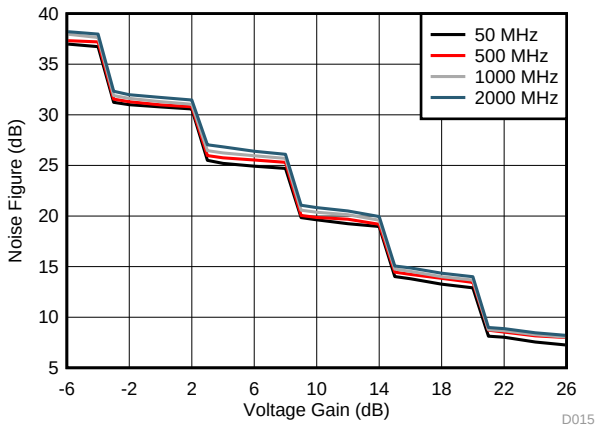



**Figure 26. Noise Figure vs Gain Settings**

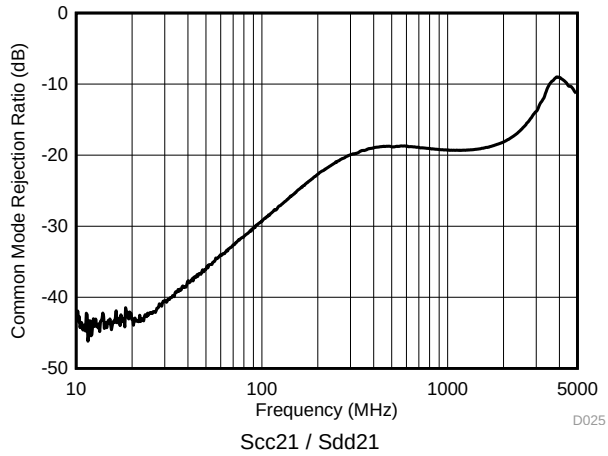



**Figure 27. CMRR vs Frequency**

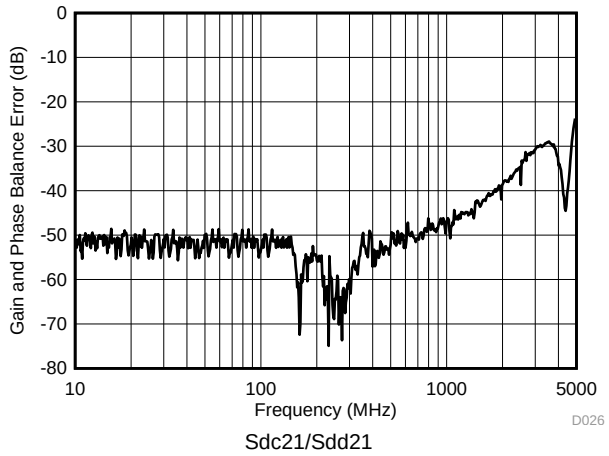



**Figure 28. Output Balance Error vs Frequency**

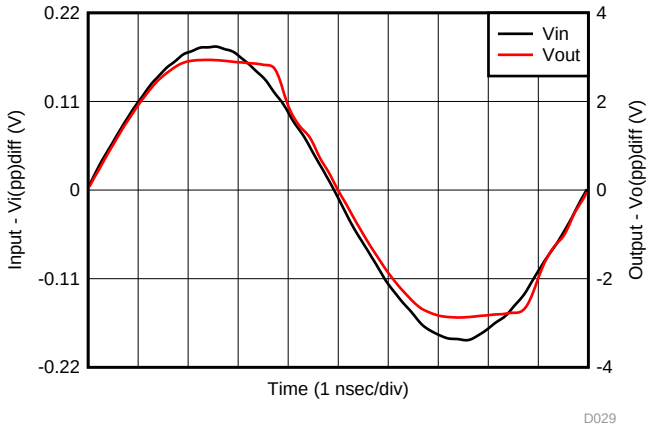



**Figure 29. Overdrive Recovery ($A_V$ = 26 dB)**

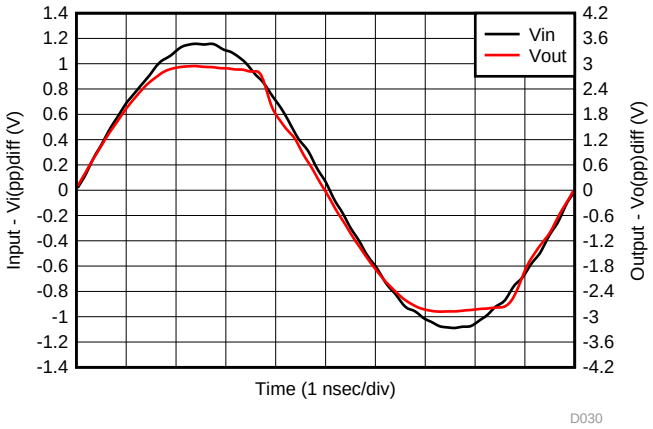



**Figure 30. Overdrive Recovery ($A_V$ = 10 dB)**

## Typical Characteristics (continued)

At $T_A$ = 25°C, VS– = –2.5 V, VS+ = 2.5 V, VOCM = 0 V, $R_{LOAD}$ = 200-Ω differential ($R_{o(internal,\ diff)}$ = 20 Ω), $V_O$ = 2 $V_{PPD}$, and $A_V$ = 26 dB, unless otherwise noted. Differential input and output, and input and output pins referenced to mid-supply, unless otherwise noted. Measured using an EVM as discussed in the *Parameter Measurement Information* section.

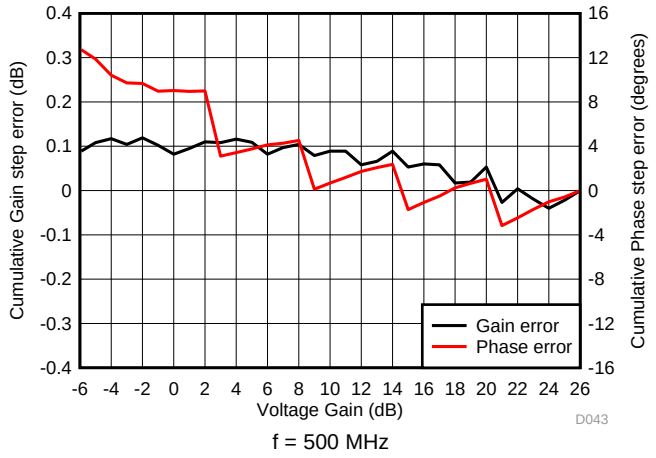



**Figure 31. Cumulative Gain and Phase Step Error vs Gain Settings**

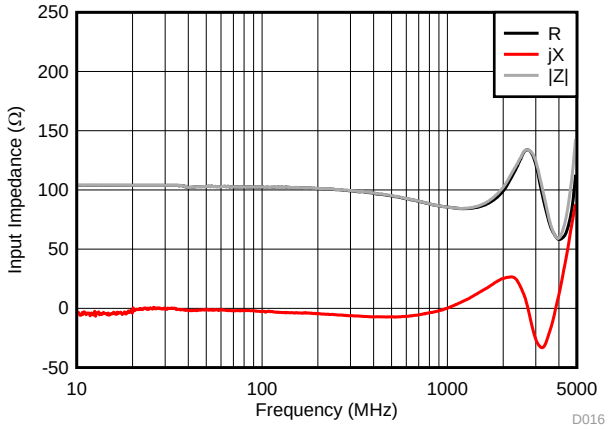



**Figure 32. Input Impedance vs Frequency**

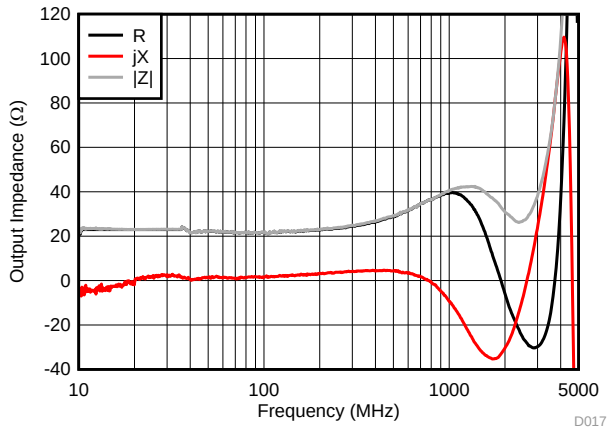



**Figure 33. Output Impedance vs Frequency**

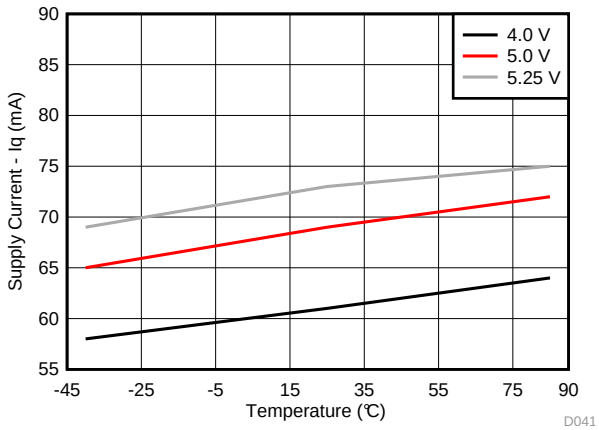



**Figure 34. Supply Current vs Temperature**

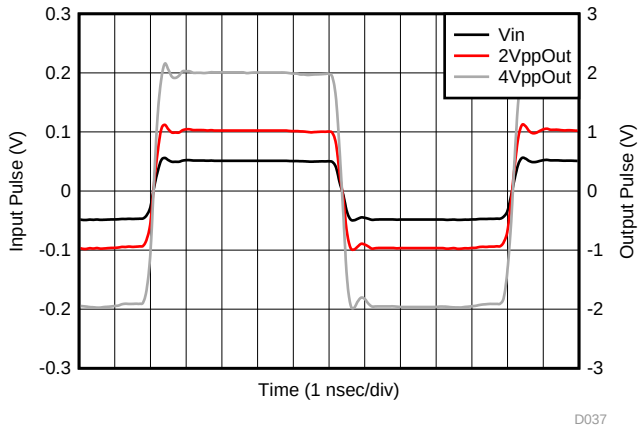



**Figure 35. Output Step Response**

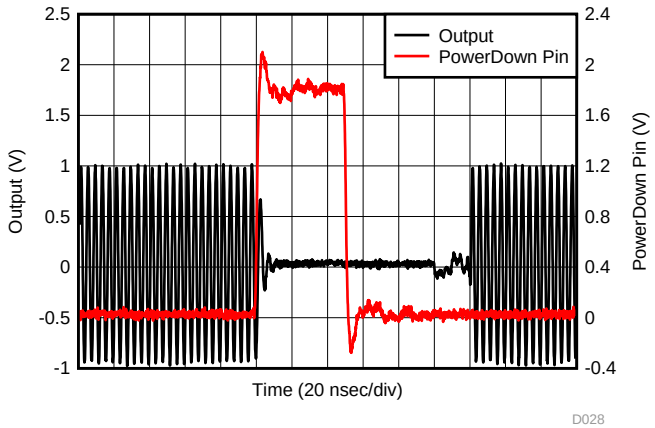



**Figure 36. Power-Down Transition Response**

## Typical Characteristics (continued)

At $T_A$ = 25°C, VS– = –2.5 V, VS+ = 2.5 V, VOCM = 0 V, $R_{LOAD}$ = 200-Ω differential ($R_{o(internal,\ diff)}$ = 20 Ω), $V_O$ = 2 $V_{PPD}$, and $A_V$ = 26 dB, unless otherwise noted. Differential input and output, and input and output pins referenced to mid-supply, unless otherwise noted. Measured using an EVM as discussed in the *Parameter Measurement Information* section.

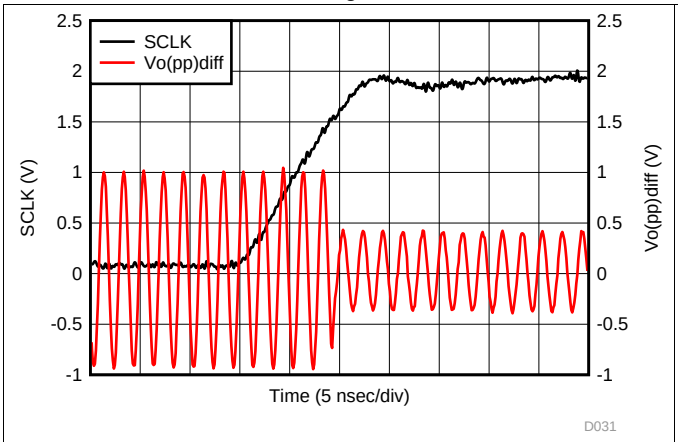



**Figure 37. Gain Switching Response ($A_V$ = 26 dB to 18 dB)**

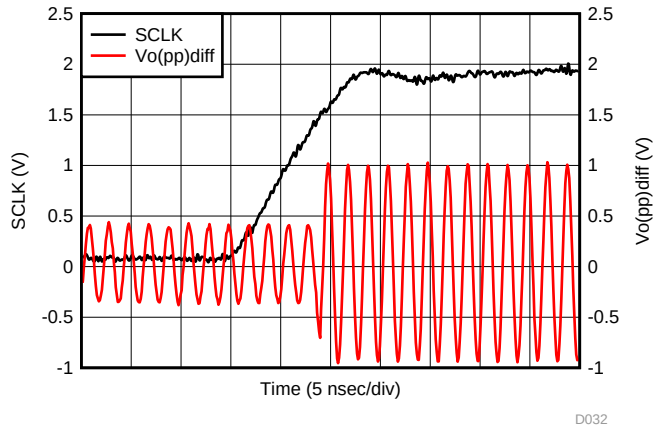



**Figure 38. Gain Switching Response ($A_V$ = 18 dB to 26 dB)**

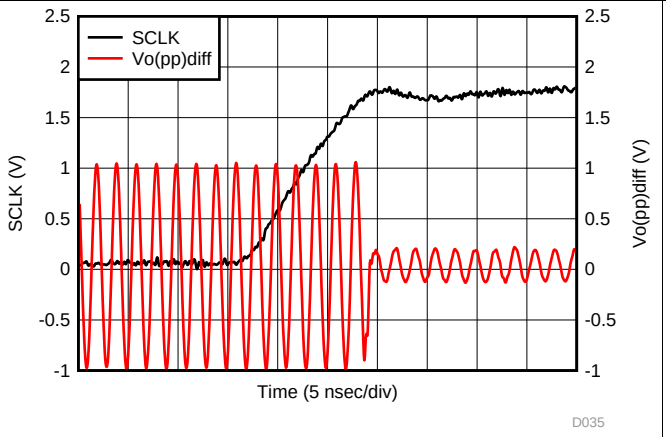



**Figure 39. Gain Switching Response ($A_V$ = 26 dB to 10 dB)**

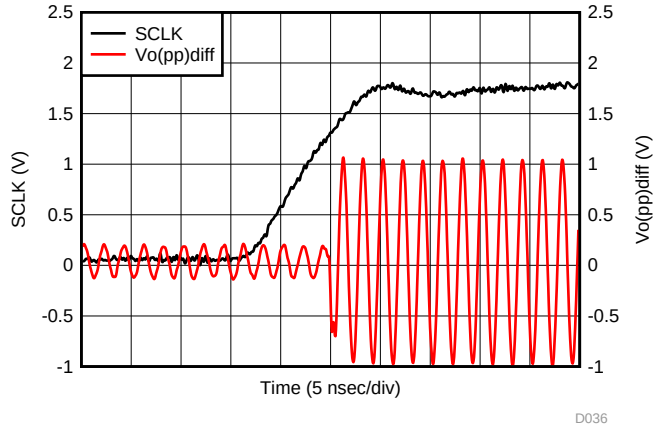



**Figure 40. Gain Switching Response ($A_V$ = 10 dB to 26 dB)**

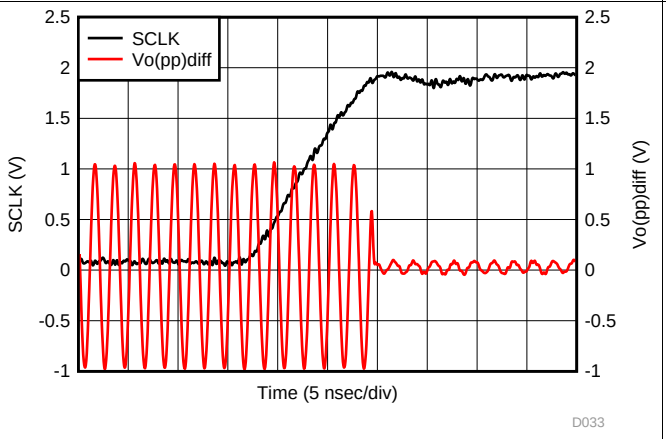



**Figure 41. Gain Switching Response ($A_V$ = 26 dB to 2 dB)**

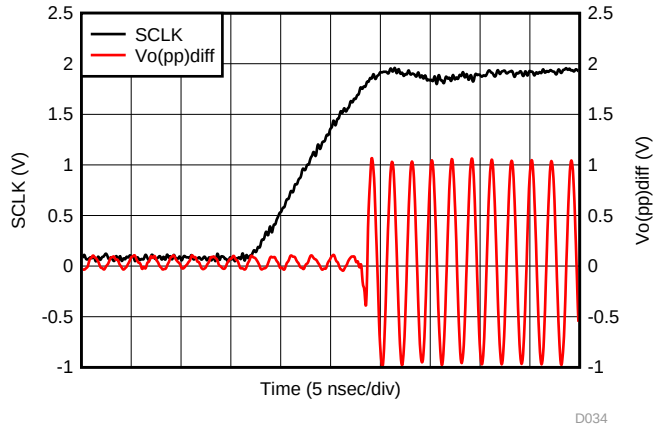



**Figure 42. Gain Switching Response ($A_V$ = 2 dB to 26 dB)**

# 8 Parameter Measurement Information

## 8.1 Setup Diagrams

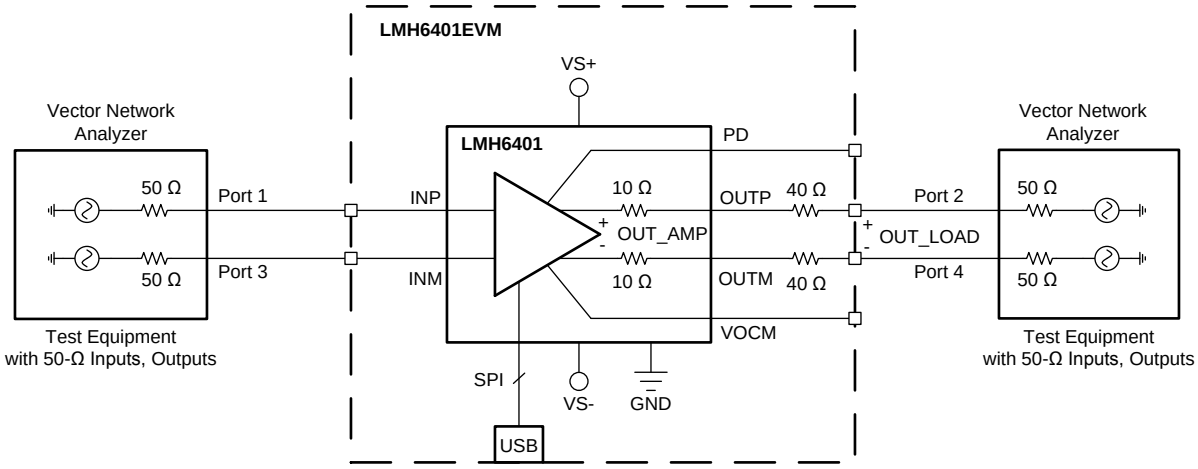



**Figure 43. Frequency Response Differential Test Setup**

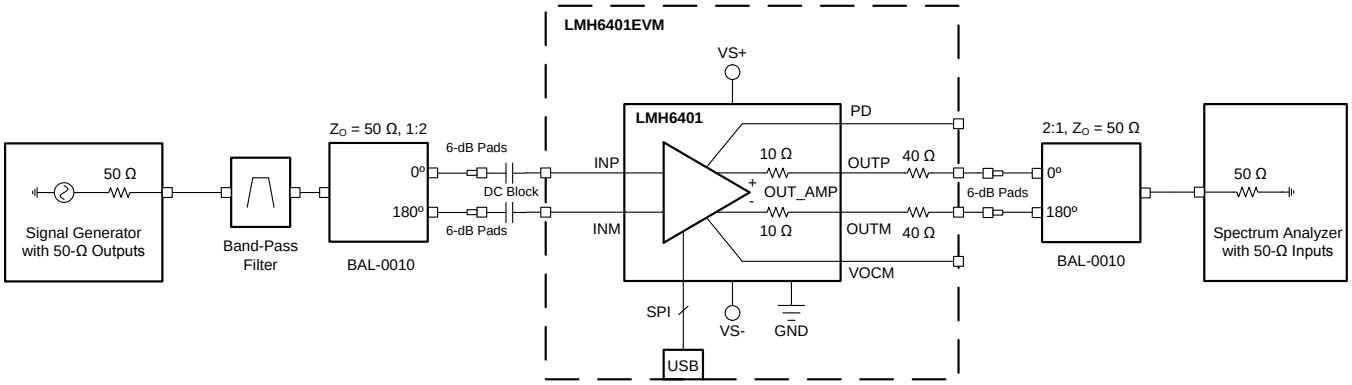



**Figure 44. Single-Tone Harmonic Distortion Test Setup**

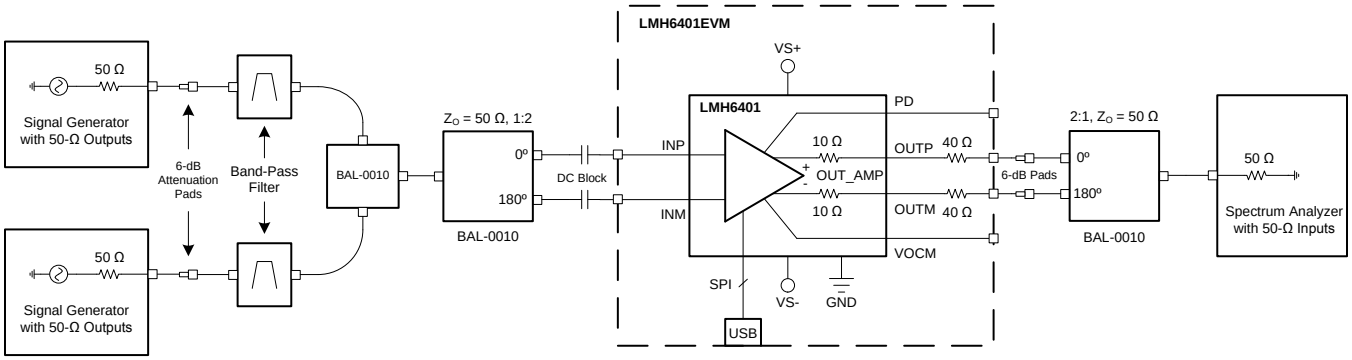



**Figure 45. Two-Tone Linearity Test Setup (OIP3, OIP2)**

## Setup Diagrams (continued)

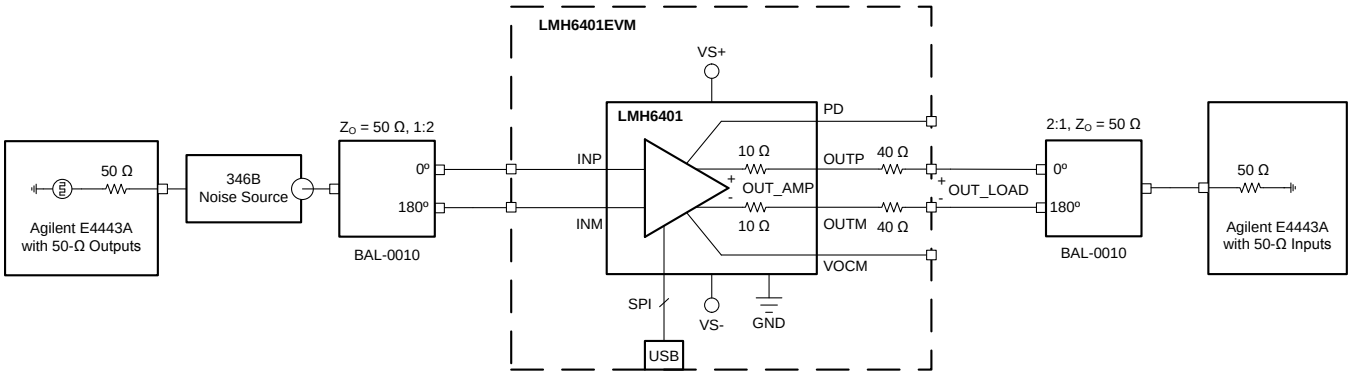



**Figure 46. Noise Figure Test Setup**

### 8.2 Output Measurement Reference Points

The LMH6401 has two on-chip, 10-Ω output resistors. When matching the output to a 100-Ω load, the evaluation module (EVM) uses an external 40-Ω resistor on each output leg to complete the output matching. Having on-chip output resistors creates two potential reference points for measuring the output voltage. The first reference point is at the internal amplifier output (OUT_AMP), and the second reference point is at the externally-matched 100-Ω load (OUT_LOAD). The measurements in the *Electrical Characteristics* table and in the *Typical Characteristics* section are referred to the (OUT_AMP) reference point unless otherwise specified. The conversion between reference points is a straightforward correction of 3 dB for power and 6 dB for voltage, as shown in Equation 1 and Equation 2. The measurements are referenced to OUT_AMP when not specified.

VOUT_LOAD = (VOUT_AMP – 6 dB) (1)

POUT_LOAD = (POUT_AMP – 3 dB) (2)

### 8.3 ATE Testing and DC Measurements

All production testing and dc parameters are measured on automated test equipment capable of dc measurements only. Some measurements (such as voltage gain) are referenced to the output of the internal amplifier and do not include losses attributed to the on-chip output resistors. The *Electrical Characteristics* values specify these conditions. When the measurement is referred to the amplifier output, the output resistors are not included in the measurement. If the measurement is referred to the device pins, then the output resistor loss is included in the measurement.

### 8.4 Frequency Response

This test is done by running an S-parameter sweep on a 4-port differential network analyzer using the standard EVM with no baluns; see Figure 43. The inputs and outputs of the EVM are connected to the network analyzer using 50-Ω coaxial cables with all the ports set to a characteristic impedance ($Z_O$) of 50 Ω.

The frequency response test with capacitive load is done by soldering the capacitor across the LMH6401 output pins. In this configuration, the on-chip, 10-Ω resistors on each output leg isolate the capacitive load from the amplifier output pins.

### 8.5 Distortion

The standard EVM is used for measuring both the single-tone harmonic distortion and two-tone intermodulation distortion; see Figure 44 and Figure 45, respectively. The distortion is measured with differential input signals to the LMH6401. In order to interface with single-ended test equipment, external baluns (1:2, $Z_O$ = 50 Ω) are required between the EVM output ports and the test equipment. The *Typical Characteristics* plots are created with Marki™ baluns, model number BAL-0010. These baluns are used to combine two single tones in the two-tone test plots as well as convert the single-ended input to differential output for harmonic distortion tests. The use of 6-dB attenuator pads on both the inputs and outputs is recommended to provide a balanced match between the external balun and the EVM.

## 8.6 Noise Figure

This test is done by matching the input of the LMH6401 to a 50-Ω noise source using a 1:2 balun (see Figure 46), with the noise figure being referred to the input impedance ($R_S$ = 100 Ω). As noted in Figure 46, an Agilent E4443A with NF features is used for the testing.

## 8.7 Pulse Response, Slew Rate, and Overdrive Recovery

For time-domain measurements, the standard EVM is driven through a balun again to convert a single-ended output from the test equipment to the differential inputs of the LMH6401. The differential outputs are directly connected to the oscilloscope inputs, with the differential signal response calculated using trace math from the two separate oscilloscope inputs.

## 8.8 Power Down

The standard EVM is used for this test by completely removing the shorting block on jumper JPD. A high-speed, 50-Ω pulse generator is used to drive the PD pin, which toggles the output signal on or off depending upon the PD pin voltage.

## 8.9 VOCM Frequency Response

The standard EVM is used for this test. A network analyzer is connected to the VOCM input of the EVM and the EVM outputs are connected to the network analyzer with 50-Ω coaxial cables. The network analyzer analysis mode is set to single-ended input and differential output, and the output common-mode response is measured with respect to the single-ended input (Scs21). The input signal frequency is swept with the signal level set for 100 mV (–16 dBm). Note that the common-mode control circuit gain is approximately one.

# 9 Detailed Description

## 9.1 Overview

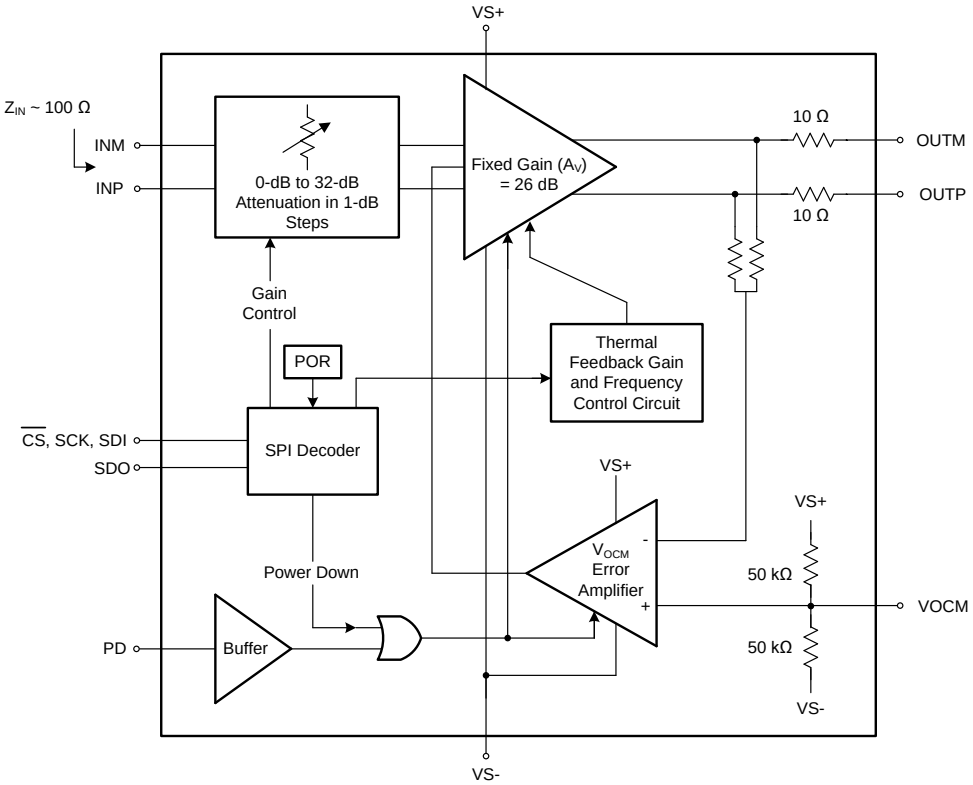
The LMH6401 is a very high-performance, differential I/O, digitally-controlled variable gain amplifier (DVGA). The device is optimized for radio frequency (RF), intermediate frequency (IF), or high-speed time-domain applications with 3-dB bandwidths up to 4.5 GHz. The device is ideal for dc- or ac-coupled applications requiring a variable gain stage when driving an analog-to-digital converter (ADC).

The LMH6401 is best suited to optimize system linearity and noise performance over the entire gain range in the RF and IF bands. Operating on a nominal 5-V supply or ±2.5-V split supplies, the device consists of an attenuator stage followed by a fixed-gain amplifier to provide voltage gain control from –6 dB to 26 dB in 1-dB steps (as shown in the *Functional Block Diagram* section) with an overall 32-dB gain range. The variable gain control for the device is offered through the digital serial peripheral interface (SPI) register. The device has a unique attenuator ladder architecture providing dynamic range improvements where the overall noise figure (NF) remains relatively constant for the first 5-dB attenuator steps, with NF degrading proportional to the attenuator steps on the sixth step. This behavior repeats over the entire gain range; see Figure 26.

The device has a differential input impedance of 100-Ω and is intended to be driven differentially by a matched 100-Ω differential source impedance for the best linearity and noise performance. The LMH6401 has two on-chip, 10-Ω resistors, one on each output (as shown in the *Functional Block Diagram* section). For most load conditions, the 10-Ω resistors are only a partial termination. Consequently, external termination resistors are required in most applications. See Table 11 for common load values and the matching resistors.

The LMH6401 supports a common-mode reference input (VOCM) pin to align the amplifier output common-mode with the subsequent stage (ADC) input requirements. The output common-mode of the LMH6401 is self-biased to mid-supply when the VOCM pin is not driven externally. The device can be operated on a power-supply voltage range of 4.0 V to 5.25 V and supports both single- and split-supply operation. For correct digital operation, the positive supply must not be below 2 V for ground reference logic. A power-down feature is also available through the SPI register and the external PD pin.

## 9.2 Functional Block Diagram



## 9.3 Feature Description

The LMH6401 includes the following features:

- Fully-differential amplifier
- Digitally-controlled variable gain: –6 dB to 26 dB in 1-dB steps
- Output common-mode control
- Single- or split-supply operation
- Large-signal bandwidth of 4.5 GHz
- Usable bandwidth up to 2 GHz
- Power-down control

## 9.4 Device Functional Modes

### 9.4.1 Power-On Reset (POR)

The LMH6401 has a built-in, power-on reset (POR) that sets the device registers to their default state (see Table 3) on power-up. Note that the LMH6401 register information is lost each time power is removed. When power is reapplied, the POR ensures the device enters a default state. Power glitches (of sufficient duration) can also initiate the POR and return the device to a default state.

### 9.4.2 Power-Down (PD)

The device supports power-down control using an external power-down (PD) pin or by writing a logic high to bit 6 of SPI register 2h (see the *Register Maps* section). The external PD is an active high pin. When left floating, the device defaults to an *on* condition when the PD pin defaults to logic low as a result of the internal pulldown resistor. The device PD thresholds are noted in the *Electrical Characteristics* table. The device consumes approximately 7 mA in power-down mode. Note that the SPI register contents are preserved in power-down mode.

### 9.4.3 Thermal Feedback Control

The LMH6401 has a thermal feedback gain and frequency control feature that allows for improved low-frequency settling performance. The Thermal Feedback Gain Control and Thermal Feedback Frequency Control registers set through the SPI control this feature. The default setting is described in Table 3. Graphs are Included in the *Application and Implementation* section that illustrate how the thermal feedback gain and frequency control allows for enhanced performance.

### 9.4.4 Gain Control

The LMH6401 gain can be controlled from 26-dB gain (0-dB attenuation) to –6-dB gain in 1-dB steps by digitally programming the SPI register 2h. See the *Register Maps* section for more details.

## 9.5 Programming

### 9.5.1 Details of the Serial Interface

The LMH6401 has a set of internal registers that can be accessed by the serial interface controlled by the $\overline{CS}$ (chip select), SCLK (serial interface clock), SDI (serial interface input data), and SDO (serial interface readback data) pins. Serial input to the device is enabled when $\overline{CS}$ is low. SDI serial data are latched at every SCLK rising edge when $\overline{CS}$ is active (low). Serial data are loaded into the register at every 16th SCLK rising edge when $\overline{CS}$ is low. When the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiples of 16-bit words within a single active $\overline{CS}$ pulse. The first eight bits form the register address and the remaining eight bits form the register data. The interface can function with SCLK frequencies from 50 MHz down to very low speeds (of a few Hertz) and also with a non-50% SCLK duty cycle. A summary of the LMH6401 SPI protocol follows:

- SPI-1.1 compliant interface
- SPI register contents protected in power-down
- SPI-controlled power-down
- Powered from the main VS+ power supply
- 1.8-V logic compliant

## Programming (continued)

### 9.5.2 Timing Diagrams

Figure 47 and Figure 48 show timing diagrams for the SPI write and read bus cycles, respectively. Figure 49 and Figure 50 show timing diagrams for the write and read operations, respectively, of the LMH6401. Figure 51 and Figure 52 illustrate example SPI stream write and read timing diagrams, respectively. Refer to the *Electrical Characteristics* table for SPI timing requirements.

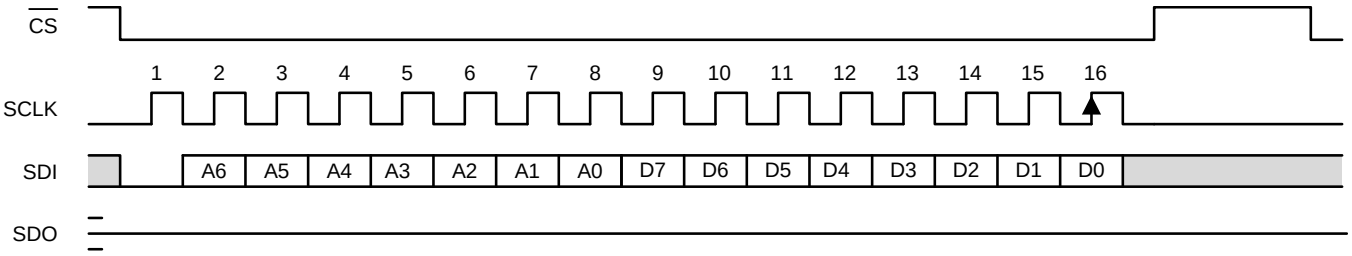



**Figure 47. SPI Write Bus Cycle**

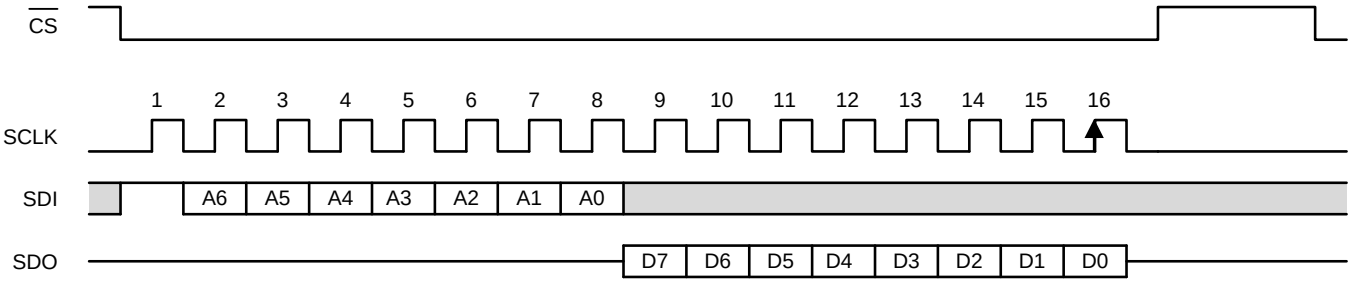



**Figure 48. SPI Read Bus Cycle**

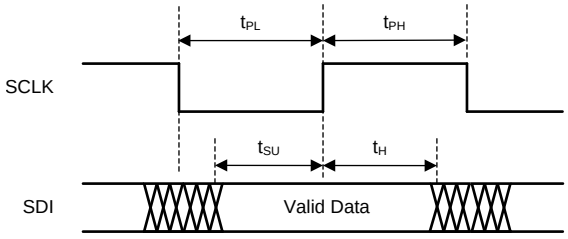



**Figure 49. Write Operation Timing Diagram**

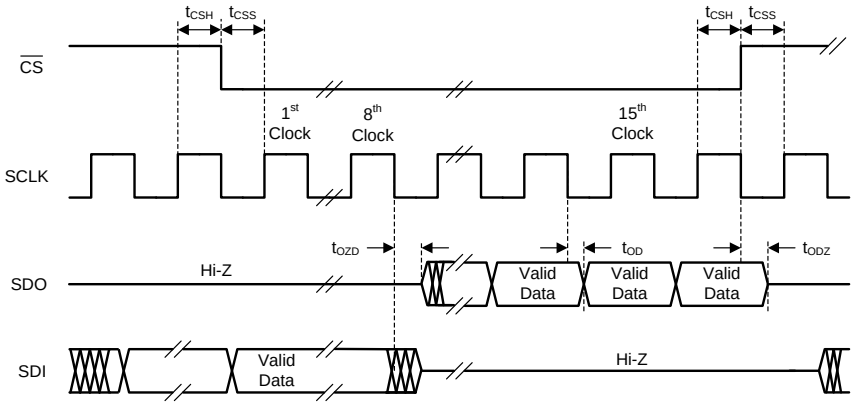



**Figure 50. Read Operation Timing Diagram**

## Programming (continued)

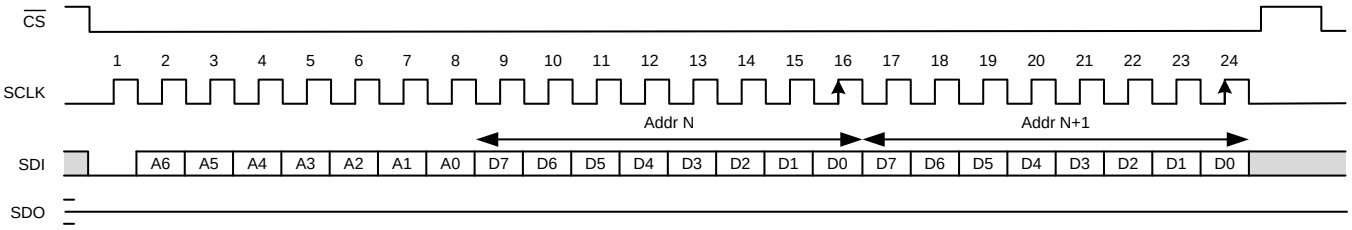



**Figure 51. SPI Streaming Write Example**

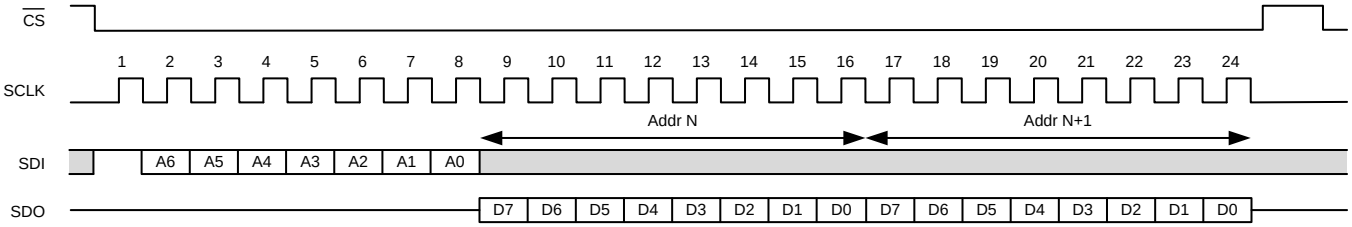



**Figure 52. SPI Streaming Read Example**

## 9.6 Register Maps

Table 3 lists the SPI register map.

**Table 3. SPI Register Map**

| ADDRESS (A[6:0]) | R/W | REGISTER | DEFAULT (Hex) |
|---|---|---|---|
| 0 | R | Revision ID | 03h |
| 1 | R | Product ID | 00h |
| 2 | R/W | Gain Control | 20h (minimum gain) |
| 3 | R/W | Reserved | 8Ch |
| 4 | R/W | Thermal feedback gain control | 27h |
| 5 | R/W | Thermal feedback frequency control | 45h |
| 6-127 | R | Reserved | 00h |

### 9.6.1 Revision ID (address = 0h, Read-Only) [default = 03h]

**Figure 53. Revision ID**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Revision ID | | | | | | | |
| R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R-1b | R-1b |

LEGEND: R = Read only; -n = value after reset

**Table 4. Revision ID Field Descriptions**

| Bit | Field | Type | Default | Description |
|---|---|---|---|---|
| 7-0 | Revision ID | R | 00000011 | Revision identification bits. |

### 9.6.2 Product ID (address = 1h, Read-Only) [default = 00h]

**Figure 54. Product ID**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Product ID | | | | | | | |
| R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R-0b | R-0b |

LEGEND: R = Read only; -n = value after reset

**Table 5. Product ID Field Descriptions**

| Bit | Field | Type | Default | Description |
|---|---|---|---|---|
| 7-0 | Product ID | R | 00000000 | Product identification bits. |

### 9.6.3 Gain Control (address = 2h) [default = 20h]

**Figure 55. Gain Control**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | Power Down | Gain Control | | | | | |
| R/W-0b | R/W-0b | R/W-1b | R/W-0b | R/W-0b | R/W-0b | R/W-0b | R/W-0b |

LEGEND: R/W = Read/Write; -n = value after reset

**Table 6. Gain Control Field Description**

| Bit | Field | Type | Default | Description |
|---|---|---|---|---|
| 7 | Reserved | R/W | 0 | Reserved, always program to 0 |
| 6 | Power Down | R/W | 0 | 0 = Active<br>1 = Power down |
| 5-0 | Gain Control | R/W | 100000 | Gain control (see Table 10 for gain settings) |

### 9.6.4 Reserved (address = 3h) [default = 8Ch]

**Figure 56. Reserved**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | | | | | | | |
| R/W-1b | R/W-0b | R/W-0b | R/W-0b | R/W-1b | R/W-1b | R/W-0b | R/W-0b |

LEGEND: R/W = Read/Write; -n = value after reset

**Table 7. Reserved Field Descriptions**

| Bit | Field | Type | Default | Description |
|---|---|---|---|---|
| 7-0 | Reserved | R/W | 10001100 | Reserved |

### 9.6.5 Thermal Feedback Gain Control (address = 4h) [default = 27h]

**Figure 57. Thermal Feedback Gain Control**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | Thermal SD | Thermal Feedback Gain Control | | | | |
| R/W-0b | R/W-0b | R/W-1b | R/W-0b | R/W-0b | R/W-1b | R/W-1b | R/W-1b |

LEGEND: R/W = Read/Write; *-n* = value after reset

**Table 8. Thermal Feedback Gain Control Field Descriptions**

| Bit | Field | Type | Default | Description |
|---|---|---|---|---|
| 7-6 | Reserved | R/W | 00 | Reserved, always program to 00 |
| 5 | Thermal SD | R/W | 1 | 0 = Thermal feedback control enabled<br>1 = Thermal feedback control disabled |
| 4-0 | Thermal Feedback Gain Control | R/W | 00111 | 00000 = Minimum thermal feedback gain (see Figure 61)<br>11111 = Maximum thermal feedback gain (see Figure 61) |

### 9.6.6 Thermal Feedback Frequency Control (address = 5h) [default = 45h]

**Figure 58. Thermal Feedback Frequency Control**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reserved | Reserved | Reserved | Thermal Feedback Frequency Control | | | | |
| R/W-0b | R/W-1b | R/W-0b | R/W-0b | R/W-0b | R/W-1b | R/W-0b | R/W-1b |

LEGEND: R/W = Read/Write; -n = value after reset

**Table 9. Thermal Feedback Frequency Control Field Descriptions**

| Bit | Field | Type | Default | Description |
|---|---|---|---|---|
| 7-5 | Reserved | R/W | 010 | Reserved, always program to 010 |
| 4-0 | Thermal Feedback Frequency Control | R/W | 00101 | 00000 = Minimum thermal feedback frequency (see Figure 62)<br>11111 = Maximum thermal feedback frequency (see Figure 62) |

**Table 10. Gain Control Register Controls**

| ATTENUATION (dB) | GAIN (dB) | REGISTER SETTING (Address = 02h) |
|---|---|---|
| 0 | 26 | 00h |
| 1 | 25 | 01h |
| 2 | 24 | 02h |
| 3 | 23 | 03h |
| 4 | 22 | 04h |
| 5 | 21 | 05h |
| 6 | 20 | 06h |
| 7 | 19 | 07h |
| 8 | 18 | 08h |
| 9 | 17 | 09h |
| 10 | 16 | 0Ah |
| 11 | 15 | 0Bh |
| 12 | 14 | 0Ch |
| 13 | 13 | 0Dh |
| 14 | 12 | 0Eh |
| 15 | 11 | 0Fh |
| 16 | 10 | 10h |
| 17 | 9 | 11h |
| 18 | 8 | 12h |
| 19 | 7 | 13h |
| 20 | 6 | 14h |
| 21 | 5 | 15h |
| 22 | 4 | 16h |
| 23 | 3 | 17h |
| 24 | 2 | 18h |
| 25 | 1 | 19h |
| 26 | 0 | 1Ah |
| 27 | –1 | 1Bh |
| 28 | –2 | 1Ch |
| 29 | –3 | 1Dh |
| 30 | –4 | 1Eh |
| 31 | –5 | 1Fh |
| 32 | –6 | 20h-3Fh |

# 10 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 10.1 Application Information

### 10.1.1 Analog Input Characteristics

The LMH6401 is a single-channel device with analog input signal pins (INP and INM) that denote the positive and negative input pins, respectively. The device inputs can be either ac- or dc-coupled. In order to dc-couple the inputs, care must be taken to ensure the common-mode voltage is set within the input common-mode range of the device, as described in the *Electrical Characteristics* table. For optimal linearity and noise performance, TI recommends setting the input common-mode voltage as close to mid-supply as possible. The LMH6401 device can be ac-coupled at the inputs using input capacitors that allow the inputs to self-bias close to mid-supply and isolates the common-mode voltage of the driving circuitry. The LMH6401 inputs must be driven differentially. For single-ended input source applications, care must be taken to select an appropriate balun or fully-differential amplifier (such as the LMH3401 or LMH5401) that can convert single-ended signals into differential signals with minimal distortion.

At maximum gain, the digital attenuator is set to 0-dB attenuation, the input signal is much smaller than the output, and the maximum output voltage swing is limited by the output stage of the device. At minimum gain, however, the maximum output voltage swing is limited by the input stage because the output is 6 dB lower than the inputs. In the minimum gain configuration, the input signal begins to clip against the electrostatic discharge (ESD) protection diodes before the output reaches maximum swing limits. This clipping is a result of the input signal being unable to swing below the negative supply voltage and being unable to exceed the positive supply voltage because of the protection diodes. For linear operation, care must be taken to ensure that the input is kept within the maximum input voltage ratings, as described in the *Absolute Maximum Ratings* table. The supply voltage imposes the limit for the input voltage swing because the input stage self-biases to approximately mid-rail.

The device input impedance is set by the internal input termination resistors to a nominal value of 100 Ω. Process variations result in a range of values, as described in the *Electrical Characteristics* table. The input impedance is also affected by device parasitic reactance at higher frequencies, thus shifting the impedance away from a nominal 100 Ω. The LMH6401 exhibits a well-matched, 100-Ω differential input impedance in the usable bandwidth, achieving a –15-dB input return loss at 2 GHz across the gain settings; see Figure 3. Figure 59 illustrates a Smith chart plot of the LMH6401 differential input impedance referenced to a 100-Ω characteristic impedance.

## Application Information (continued)

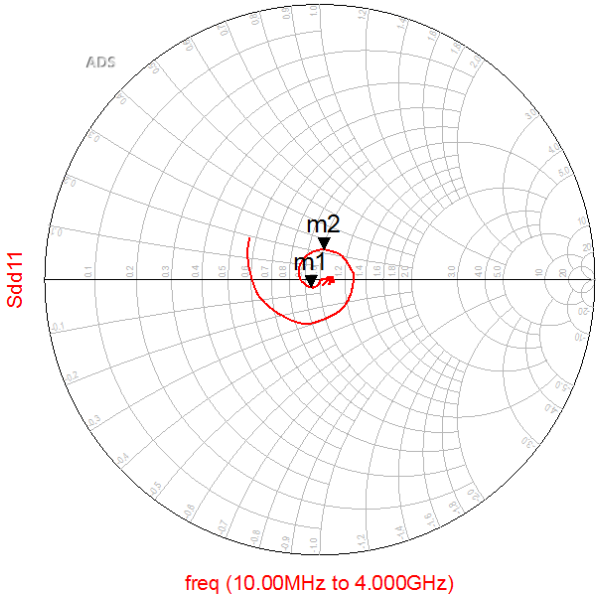



**Figure 59. Smith Chart Showing Differential Input Impedance ($z_O$ = 100 Ω)**

### 10.1.2 Analog Output Characteristics

The LMH6401, as with most RF amplifiers, has two 10-Ω, on-chip resistors on each output leg to provide isolation from board parasitics at the output pins; see the *Functional Block Diagram* section. When designing a filter between the LMH6401 and the interfacing circuitry (ADC), the filter source impedance must be calculated by taking into account the two 10-Ω, on-chip resistors. Table 11 shows the calculated external source impedance values ($R_{O+}$ and $R_{O–}$) required for various matched filter loads ($R_L$). An important note is that the filter design between the LMH6401 and the ADC is not limited to a matched filter, and source impedance values ($R_{O+}$ and $R_{O–}$) can be reduced to achieve higher swing at the filter outputs. Achieving lower loss in the filter source impedance resistors or higher swing at the filter outputs is often desirable because the amplifier must output reduced swing to maintain the same full-scale input at the ADC and, thus, better linearity performance. An example 370-MHz, un-matched, low-pass filter between the LMH6401 and ADS54J60 is illustrated in Figure 64, with ($R_{O+}$ and $R_{O–}$) set to 20 Ω and $R_L$ set to 100 Ω.

**Table 11. Load Component Values(1)**

| LOAD ($R_L$) | $R_{O+}$ AND $R_{O–}$ FOR A MATCHED TERMINATION | TOTAL LOAD RESISTANCE AT AMPLIFIER OUTPUT | TERMINATION LOSS |
|---|---|---|---|
| 50 Ω | 15 Ω | 100 Ω | 6 dB |
| 100 Ω | 40 Ω | 200 Ω | 6 dB |
| 200 Ω | 90 Ω | 400 Ω | 6 dB |
| 400 Ω | 190 Ω | 800 Ω | 6 dB |
| 1 kΩ | 490 Ω | 2000 Ω | 6 dB |

(1) The total load includes termination resistors.

The LMH6401 can be either dc- or ac-coupled at the outputs. For dc-coupled applications, the device provides an option to control the output common-mode voltage using the VOCM pin. Device performance is optimal when the output common-mode voltage is within ±0.5 V of mid-supply (see Figure 21) and performance degrades outside the range when the output swing approaches clipping levels. The LMH6401 can achieve a maximum output swing of 6 $V_{PPD}$ with the output common-mode voltage centered at mid-supply.

Note that by default, the output common-mode voltage is set to mid-supply before the two 10-Ω, on-chip resistors; see the *Functional Block Diagram* section. On a single-supply operation when dc-coupling the device outputs to an ADC using common-mode, level-shifting resistors, the output common-mode voltage and resistor values being calculated must include the two internal 10-Ω resistors in the equation. When operating the LMH6401 on split supplies and dc-coupling the outputs, TI recommends matching the output common-mode voltage of the LMH6401 with the input common-mode voltage of the ADC. A simple design procedure is to select the supply voltages (VS+ and VS–) such that the default output common-mode voltage being set is equal to the input common-mode voltage of the ADC. As illustrated in Figure 66, the supplies of the LMH6401 are selected such that the default output common-mode voltage is set to mid-supply or 1.23 V, which is within the input common-mode voltage range of the ADC (1.185 V to 1.265 V).

#### *10.1.2.1 Driving Capacitive Loads*

With high-speed signal paths, capacitive loading at the output is highly detrimental to the signal path, as shown in Figure 60. The device on-chip resistors are included in order to isolate the parasitic capacitance associated with the package and the printed circuit board (PCB) pads that the device is soldered to. However, designers must make every effort to reduce parasitic loading on the amplifier output pins. The LMH6401 is stable with most capacitive loads up to 10 pF; however, bandwidth suffers with capacitive loading on the output.

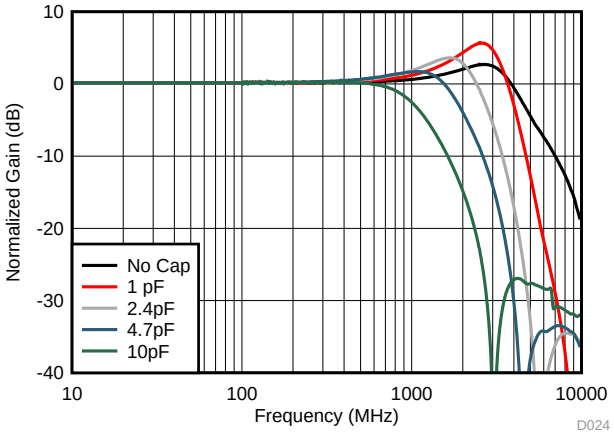



**Figure 60. Frequency Response vs Capacitive Load**

### 10.1.3 Thermal Feedback Control

The LMH6401 can be used to optimize long-term settling responses using thermal feedback gain and frequency control registers. These registers are disabled on power-up and can be enabled by clearing the thermal SD bit; see the Thermal Feedback Gain Control register. The thermal feedback gain control bits increase the low-frequency gain and the thermal feedback frequency control bits shift the boost frequency. The thermal feedback gain and frequency registers both have a range of 32 steps. When the function is enabled, there is a small initial gain offset to optimize the control range. The thermal feedback off condition is illustrated in the gain control plot (Figure 61), along with a sweep of gain settings of 0, 4, 8…28, and 31 with a 0 register value representing the minimum gain setting. The frequency control is illustrated in Figure 62 with the optimal gain setting from the gain sweep over the values of 0, 4, 8…28, and 31 with a 0 register value representing the minimum frequency boost setting.

### 10.1.3.1 Step Response Optimization using Thermal Feedback Control

The LMH6401 has an adjustable frequency compensation scheme that is designed to dramatically improve the step response for long-term settling. The structure of the LMH6401 gives the best distortion performance for signals ranging from dc to 2 GHz over a wide range of gain settings. Thermal heating causes a small change in gain at low frequencies close to 500 kHz. This change in gain is shown in Figure 61 in the ac response for the trace labeled *Thermal Feedback OFF*. The amount of gain change is approximately 0.18 dB at maximum gain. This gain change resulting from thermal heating leads to approximately 1.7% overshoot that settles over a relatively long time period. A patent pending technique is added that allows for the reduction of this overshoot to approximately 0.35%, thus eliminating the long-term settling and still retaining the wide dynamic performance range. The circuit also corrects for small systematic changes that occur at different gain settings and tracks temperature changes as well. This low-frequency gain correction is accomplished by the addition of a circuit that alters the gain at low frequencies to nearly eliminate the variation from low to high frequencies.

The step response optimization circuit is disabled on power-up and can be enabled by clearing bit 5 in the Thermal Feedback Gain Control register (register 4h). The power-on default setting for thermal gain and frequency are adjusted for the evaluation board for typical silicon performance. These registers are made available for customization in the final system because board layout characteristics or other components in the system can change the required correction needed.

Figure 63 demonstrates the initial step response and the corrected response that corresponds to the default register values for a typical device on the evaluation board displaying long-term settling correction.

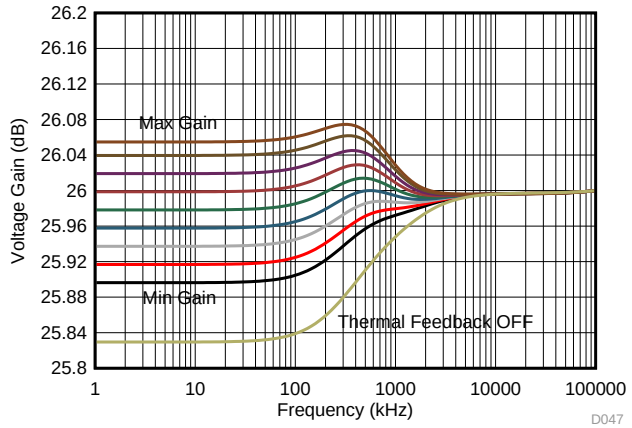



**Figure 61. Thermal Gain Control Sweep (Frequency = 9)**

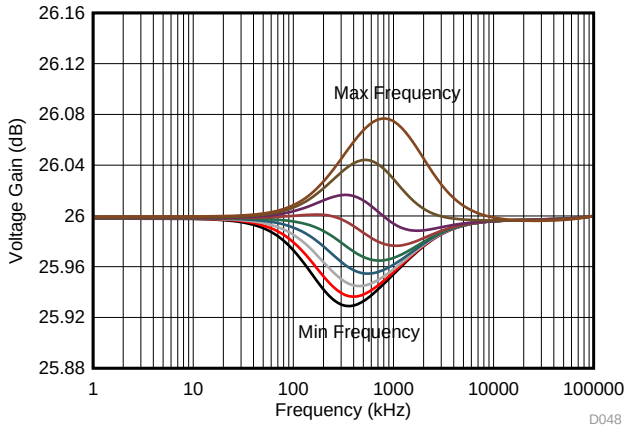



**Figure 62. Thermal Frequency Control Sweep (Gain = 10)**

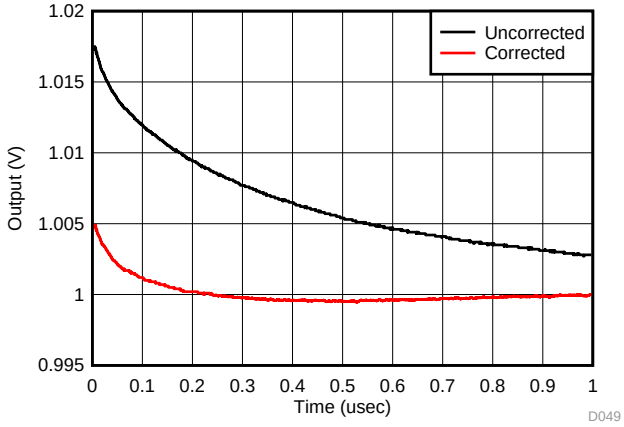



**Figure 63. Long-Term Settling Response using Thermal Feedback (Gain = 10, Frequency = 9)**

### 10.1.4 Thermal Considerations

The LMH6401 is packaged in a space-saving UQFN package that has a thermal coefficient ($R_{\theta JA}$) of 78°C/W. Limit the total power dissipation in order to keep the device junction temperature below 150°C for instantaneous power and below 125°C for continuous power.

## 10.2 Typical Application

The LMH6401 is designed and optimized for the highest performance when driving differential input ADCs. Figure 64 shows a block diagram of the LMH6401 driving an ADC with a fourth-order, low-pass filter. The primary interface circuit between the amplifier and the ADC is usually an antialiasing filter to suppress high-frequency harmonics aliasing into the ADC FFT spectrum. The interface circuit also provides a means to bias the signal to the input common-mode voltage required by the ADC. Filters range from single-order real RC poles to higher-order RLC filters, depending on the application requirements. Output resistors ($R_O$) in series with the amplifier outputs isolate the amplifier from any capacitive load presented by the filter.

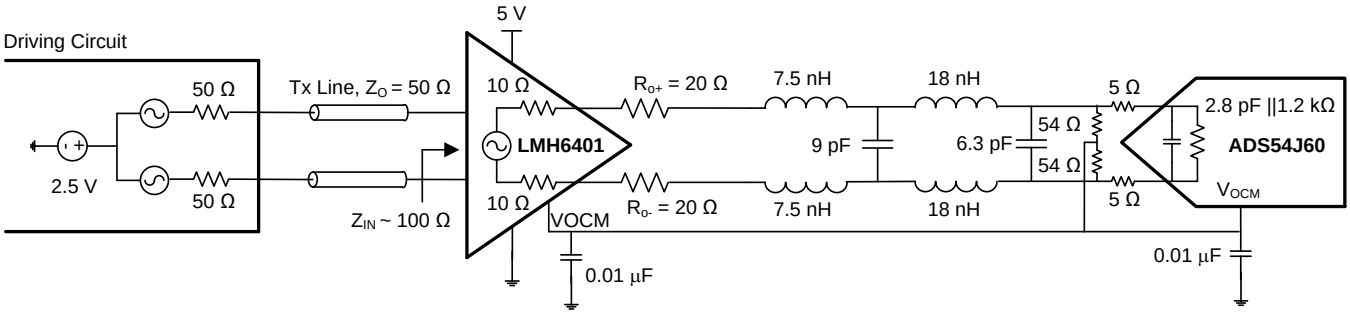



**Figure 64. The LMH6401 Driving an ADS54J60 with a 370 MHz Fourth-Order Chebyshev Low-Pass Filter**

Low distortion and low noise figure, along-with low power dissipation make the LMH6401 an ideal device for use in front-end radio applications. Figure 65 shows a block diagram of a one-transmit and one-receive (1T/1R) radio architecture with a digital pre-distortion path, where the LMH6401 can be used as a variable-gain IF amplifier on both the transmit and receive signal chain.

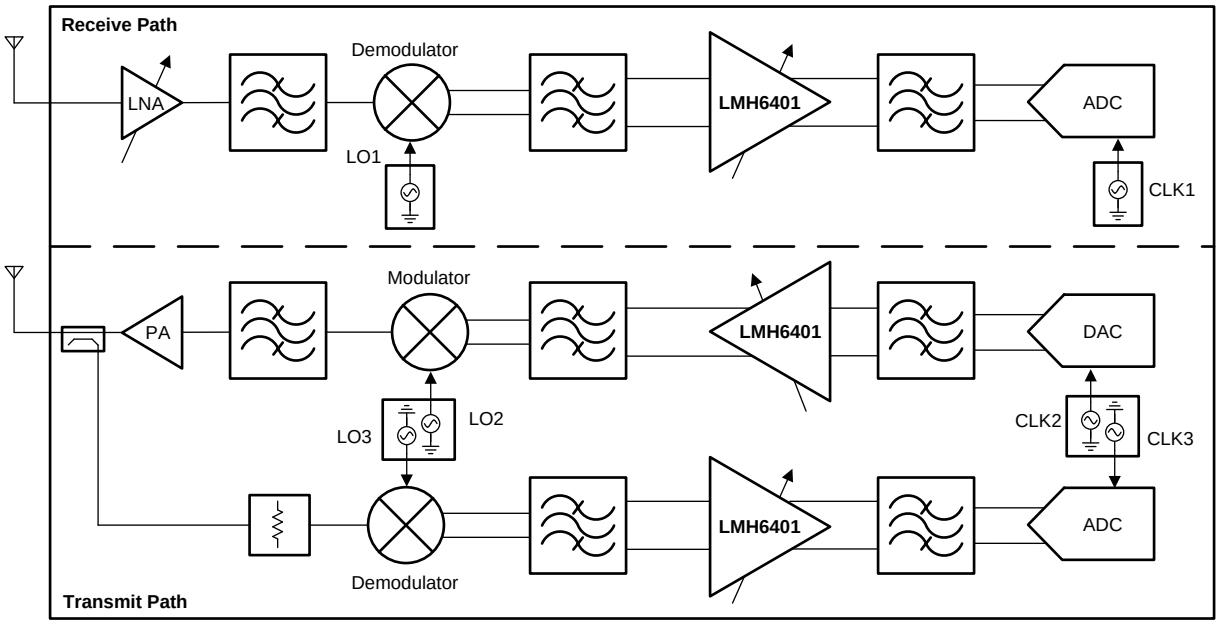



**Figure 65. 1T/1R with Digital Pre-Distortion Front-End Radio Application**

## Typical Application (continued)

### 10.2.1 Design Requirements

Table 12 shows example design requirements for an amplifier in an oscilloscope front-end application; the LMH6401 meets these requirements.

**Table 12. Example Design Requirements for an Oscilloscope Front-End application**

| SPECIFICATION | DESIGN REQUIREMENTS |
|---|---|
| Supply voltage and current | 4.0 V to 5.25 V with typically less than a 100-mA current and split-supply operation supported |
| Usable input frequency range | DC to 2 GHz |
| Voltage gain and gain range | 26-dB to 10-dB voltage gain with x2 attenuation supported (ideal 32-dB gain range) |
| OIP3 ($P_O$= –2 dBm per tone, $R_L$= 200 Ω) and noise figure ($R_S$ = 100 Ω) at 1 GHz | > 30 dBm and less than 10 dB, respectively. |
| Rise and fall time ($V_O$= 2-V step) from 10% to 90% | Less than 100 ps |
| Settling time to 1% of $V_O$ = 2-V step | Less than 1 ns with long-term settling correction required |

### 10.2.2 Detailed Design Procedure

#### *10.2.2.1 Driving ADCs*

When the amplifier is driving an ADC, the key points to consider for implementation are the signal-to-noise ratio (SNR), spurious-free dynamic range (SFDR), and ADC input considerations, as described in this section.

A typical application of the LMH6401 involves driving an ultra-wideband, 12-bit ADC (such as the ADC12J4000), as shown in Figure 66. The LMH6401 can drive the full Nyquist bandwidth of ADCs with sampling rates up to 4 GSPS. If the front-end bandwidth of the ADC is more than 2 GHz, use a simple noise filter to improve SNR. Otherwise, the ADC can be connected directly to the amplifier output pins with appropriate matching resistors to limit the full-scale input of the ADC. Note that the LMH6401 inputs must be driven differentially using a balun or fully-differential amplifiers (FDAs). For dc-coupled applications, an FDA (such as the LMH3401 or LMH5401) that can convert a single-ended input to a differential output with low distortion is preferred.

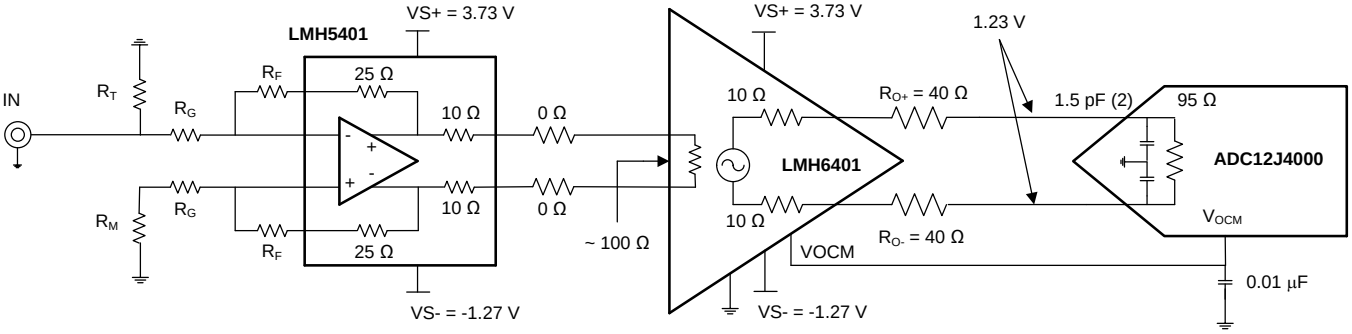



**Figure 66. DC-Coupled Oscilloscope Front-End Application**

#### 10.2.2.1.1 SNR Considerations

The signal-to-noise ratio (SNR) of the amplifier and filter can be calculated from the amplitude of the signal and the bandwidth of the filter. The noise from the amplifier is band-limited by the filter with the equivalent brick-wall filter bandwidth. The amplifier and filter noise can be calculated using Equation 3:

$$SNR_{AMP+FILTER} = 10 \cdot \log \left( \frac{V^2_O}{e^2_{FILTEROUT}} \right) = 20 \cdot \log \left( \frac{V_O}{e_{FILTEROUT}} \right)$$

where:

- $e_{FILTEROUT} = e_{NAMPOUT} \bullet \sqrt{ENB}$,
- $e_{NAMPOUT}$ = the output noise density of the LMH6401 (30.4 nV/$\sqrt{Hz}$) at $A_V$ = 26 dB,
- ENB = the brick-wall equivalent noise bandwidth of the filter, and
- $V_O$ = the amplifier output signal. (3)

For example, with a first-order (N = 1) band-pass or low-pass filter with a 1000-MHz cutoff, ENB is 1.57 • $f_{–3dB}$ = 1.57 • 1000 MHz = 1570 MHz. For second-order (N = 2) filters, ENB is 1.22 • $f_{–3dB}$. When the filter order increases, ENB approaches $f_{–3dB}$ (N = 3 → ENB = 1.15 • $f_{–3dB}$; N = 4 → ENB = 1.13 • $f_{–3dB}$). Both $V_O$ and $e_{FILTEROUT}$ are in RMS voltages. For example, with a 2-$V_{PP}$ (0.707 $V_{RMS}$) output signal and a 1000-MHz first-order, low-pass filter, the SNR of the amplifier and filter is 55.4 dB with $e_{FILTEROUT}$ = 30.4 nV/$\sqrt{Hz}$ • $\sqrt{1570\ MHz}$ = 1204.5 $\mu V_{RMS}$.

The SNR of the amplifier, filter, and ADC sum in RMS fashion, as shown in Equation 4 (SNR values in dB):

$$SNR_{SYSTEM} = -20 \cdot \log \left( \sqrt{10^{\frac{-SNR_{AMP+FILTER}}{10}} + 10^{\frac{-SNR_{ADC}}{10}}} \right) \quad (4)$$

This formula shows that if the SNR of the amplifier and filter equals the SNR of the ADC, the combined SNR is 3 dB lower (worse). Thus, for minimal degradation (< 1 dB) on the ADC SNR, the SNR of the amplifier and filter must be ≥ 10 dB greater than the ADC SNR. The combined SNR calculated in this manner is usually accurate to within ±1 dB of the actual implementation.

#### 10.2.2.1.2 SFDR Considerations

The SFDR of the amplifier is usually set by the second- or third-harmonic distortion for single-tone inputs, and by the second-order or third-order intermodulation distortion for two-tone inputs. Harmonics and second-order intermodulation distortion can be filtered to some degree, but third-order intermodulation spurs cannot be filtered. The ADC generates the same distortion products as the amplifier, but also generates additional spurs (not harmonically related to the input signal) as a result of sampling and clock feed through.

When the spurs from the amplifier and filter are known, each individual spur can be directly added to the same spur from the ADC, as shown in Equation 5, to estimate the combined spur (spur amplitudes in dBc):

$$HDx_{SYSTEM} = -20 \cdot \log \left( 10^{\frac{-HDx_{AMP+FILTER}}{20}} + 10^{\frac{-HDx_{ADC}}{20}} \right) \quad (5)$$

This calculation assumes the spurs are in phase, but usually provides a good estimate of the final combined distortion.

For example, if the spur of the amplifier and filter equals the spur of the ADC, then the combined spur is 6 dB higher. To minimize the amplifier contribution (< 1 dB) to the overall system distortion, the spur from the amplifier and filter must be approximately 15 dB lower in amplitude than that of the converter. The combined spur calculated in this manner is usually accurate to within ±6 dB of the actual implementation; however, higher variations can be detected as a result of phase shift in the filter, especially in second-order harmonic performance.

This worst-case spur calculation assumes that the amplifier and filter spur of interest is in phase with the corresponding spur in the ADC, such that the two spur amplitudes can be added linearly. There are two phase-shift mechanisms that cause the measured distortion performance of the amplifier-ADC chain to deviate from the expected performance calculated using Equation 5; one is the common-mode phase shift and other is the differential phase shift.

*Common-mode phase shift* is the phase shift detected equally in both branches of the differential signal path including the filter. Common-mode phase shift nullifies the basic assumption that the amplifier, filter, and ADC spur sources are in phase. This phase shift can lead to better performance than predicted when the spurs become phase shifted, and there is the potential for cancellation when the phase shift reaches 180°. However, there is a significant challenge in designing an amplifier-ADC interface circuit to take advantage of a common-mode phase shift for cancellation: the phase characteristics of the ADC spur sources are unknown, thus the necessary phase shift in the filter and signal path for cancellation is also unknown.

*Differential phase shift* is the difference in the phase response between the two branches of the differential filter signal path. Differential phase shift in the filter is a result of mismatched components caused by nominal tolerances and can severely degrade the even harmonic distortion of the amplifier-ADC chain. This effect has the same result as mismatched path lengths for the two differential traces, and causes more phase shift in one path than the other. Ideally, the phase responses over frequency through the two sides of a differential signal path are identical, such that even harmonics remain optimally out of phase and cancel when the signal is taken differentially. However, if one side has more phase shift than the other, then the even harmonic cancellation is not as effective.

Single-order RC filters cause very little differential phase shift with nominal tolerances of 5% or less, but higher-order LC filters are very sensitive to component mismatch. For instance, a third-order Butterworth band-pass filter with a 100-MHz center frequency and a 20-MHz bandwidth shows as much as 20° of differential phase imbalance in a SPICE Monte Carlo analysis with 2% component tolerances. Therefore, although a prototype may work, production variance is unacceptable. For ac-coupled or dc-coupled applications where a transformer or balun cannot be used, using first- or second-order filters is recommended to minimize the effect of differential phase shift.

#### 10.2.2.1.3 ADC Input Common-Mode Voltage Considerations—AC-Coupled Input

When interfacing to an ADC, the input common-mode voltage range of the ADC must be taken into account for proper operation. In an ac-coupled application between the amplifier and the ADC, the input common-mode voltage bias of the ADC can be accomplished in different ways. Some ADCs use internal bias networks such that the analog inputs are automatically biased to the required input common-mode voltage if the inputs are ac-coupled with capacitors (or if the filter between the amplifier and ADC is a band-pass filter). Other ADCs supply their required input common-mode voltage from a reference voltage output pin (often termed CM or $V_{CM}$). With these ADCs, the ac-coupled input signal can be re-biased to the input common-mode voltage by connecting resistors from each input to the CM output of the ADC, as shown in Figure 67. AC coupling provides dc common-mode isolation between the amplifier and the ADC; thus, the output common-mode voltage of the amplifier is a *don't care* for the ADC.

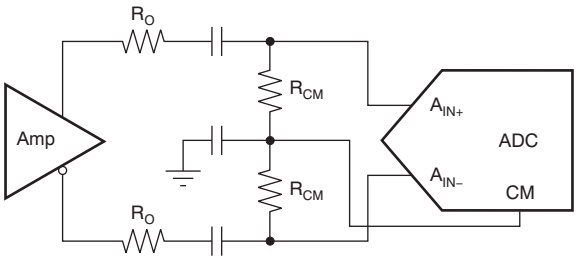



**Figure 67. Biasing AC-Coupled ADC Inputs Using the ADC CM Output**

#### 10.2.2.1.4 ADC Input Common-Mode Voltage Considerations—DC-Coupled Input

DC-coupled applications vary in complexity and requirements, depending on the ADC (a split supply for the CMV is applicable). One typical requirement is resolving the mismatch between the common-mode voltage of the driving amplifier and the ADC. Devices such as the ADC12J4000 require a nominal 1.23-V input common-mode, whereas other devices such as the ADS54J60 require a nominal 2.1-V input common-mode. The simplest approach when dc-coupling the LMH6401 with the input common-mode voltage of the ADC is to select the supply voltages (VS+) and (VS–) such that the default output common-mode voltage being set is equal to the input common-mode voltage of the ADC; see Figure 66. The default common-mode voltage being set can be controlled externally using the VOCM pin. The device performance is optimal when the output common-mode voltage is within ±0.5 V of mid-supply and degrades outside the range when the output swing approaches clipping levels.

A second approach is shown in Figure 68 when dc-coupling on a single supply, where a resistor network can be used to perform the common-mode level shift. This resistor network consists of the amplifier series output resistors and pullup or pulldown resistors to a reference voltage. This resistor network introduces signal attenuation that may prevent the use of the full-scale input range of the ADC. ADCs with an input common-mode closer to the typical 2.5-V output common-mode of the LMH6401 are easier to dc-couple, and require little or no level shifting.

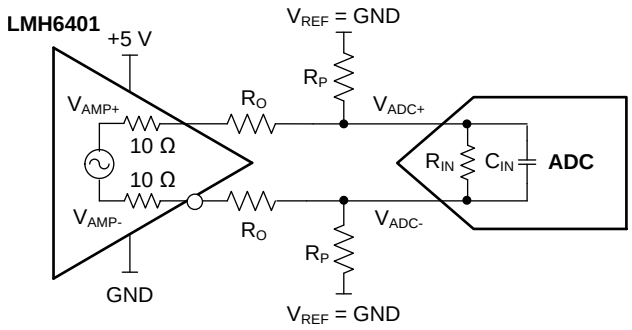



**Figure 68. Resistor Network to DC Level-Shift Common-Mode Voltage using $V_{REF}$ as GND**

For common-mode analysis of the circuit in Figure 68, assume that $V_{AMP±} = V_{CM}$ and $V_{ADC±} = V_{CM}$ (the specification for the ADC input common-mode voltage). Note that the $V_{AMP±}$ common-mode voltage is set before the two internal 10-Ω resistors, making these resistors necessary to include in the common-mode level-shift resistor calculation. $V_{REF}$ is chosen to be a voltage within the system higher than $V_{CM}$ (such as the ADC or amplifier analog supply) or ground, depending on whether the voltage must be pulled up or down, respectively; $R_O$ is chosen to be a reasonable value, such as 24.9 Ω. With these known values, $R_P$ can be found by using Equation 6:

$$R_P = (10 + R_O) \times (V_{ADC} - V_{REF}) / (V_{AMP} - V_{ADC}) \quad (6)$$

Shifting the common-mode voltage with the resistor network comes at the expense of signal attenuation. Modeling the ADC input as the parallel combination of a resistance ($R_{IN}$) and capacitance ($C_{IN}$) using values taken from the ADC data sheet, the approximate differential input impedance ($Z_{IN}$) for the ADC can be calculated at the signal frequency. The effect of $C_{IN}$ on the overall calculation of gain is typically minimal and can be ignored for simplicity (that is, $Z_{IN} = R_{IN}$). The ADC input impedance creates a divider with the resistor network; the gain (attenuation) for this divider can be calculated by Equation 7:

$$\text{Gain} = (2R_P \parallel Z_{IN}) / (20 + 2R_O + 2R_P \parallel Z_{IN}) \quad (7)$$

With ADCs that have internal resistors that bias the ADC input to the ADC input common-mode voltage, the effective $R_{IN}$ is equal to twice the value of the bias resistor. For example, the ADS54J60 has a 0.6-kΩ resistor tying each input to the ADC $V_{CM}$; therefore, the effective differential $R_{IN}$ is 1.2 kΩ.

The introduction of the $R_P$ resistors also modifies the effective load that must be driven by the amplifier. Equation 8 shows the effective load created when using the $R_P$ resistors.

$$R_L = 20 + 2R_O + 2R_P \parallel Z_{IN} \quad (8)$$

The $R_P$ resistors function in parallel to the ADC input such that the effective load (output current) at the amplifier output is increased. Higher current loads limit the LMH6401 differential output swing.

Using the gain and knowing the full-scale input of the ADC ($V_{ADC\ FS}$), the required amplitude to drive the ADC with the network can be calculated using Equation 9:

$$V_{AMP\ PP} = \frac{V_{ADC\ FS}}{GAIN} \quad (9)$$

As with any design, testing is recommended to validate whether the specific design goals are met.

### 10.2.3 Application Curves

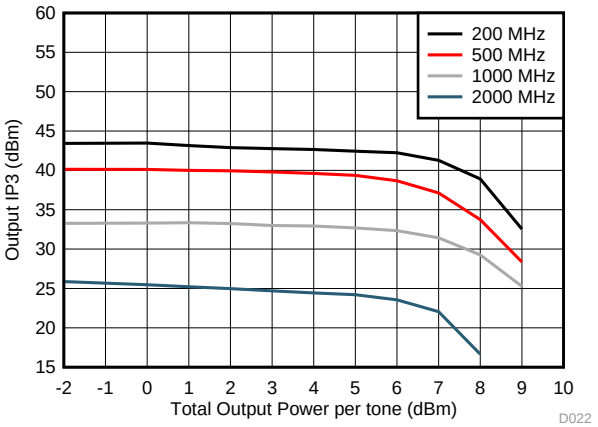



**Figure 69. Output IP3 vs Total Output Power per Tone**

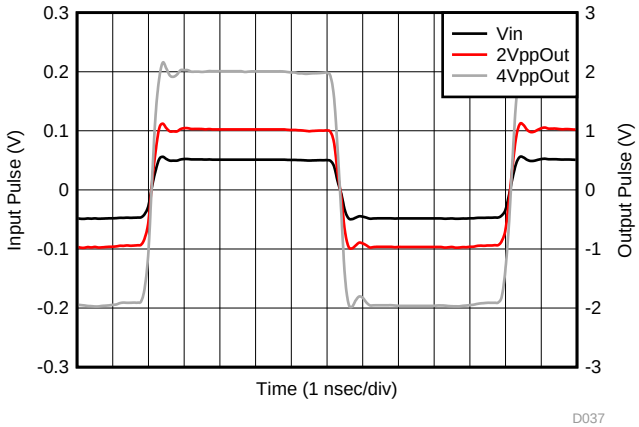



**Figure 70. Output Pulse Response**

## 10.3 Do's and Don'ts

### 10.3.1 Do:

- Include a thermal analysis at the beginning of the project.
- Use well-terminated transmission lines for all signals.
- Maintain symmetrical input and output trace layouts
- Use solid metal layers for the power supplies.
- Keep signal lines as straight as possible.
- Use split supplies where required.

### 10.3.2 Don't:

- Use a lower supply voltage than necessary.
- Use thin metal traces to supply power.
- Forget about the common-mode response of filters and transmission lines.
- Rout digital line traces close to the analog signals and supply line traces

# 11 Power-Supply Recommendations

The LMH6401 supports both single- or split-supply operation with a total recommended supply operating range [(VS+) – (VS–)] from 4.0 V to 5.25 V. Note that supply voltages do not need to be symmetrical when using split supplies, provided the total supply voltage is within the recommended operating range. Any combination of positive (VS+) and negative (VS–) supply voltages is acceptable, as long as the minimum positive (VS+) supply voltage to ground is 2 V, or greater.

Using a single 5-V power supply gives the best balance of performance and power dissipation. If power dissipation is a critical design parameter, a power supply as low as 4.0 V (±2.0 V) can be used. The input common-mode and output swing limitations of the device scale with supply voltage. TI recommends studying the common-mode voltage and output swing limitations (see the *Electrical Characteristics* table) before deciding to use a lower supply voltage.

## 11.1 Single-Supply Operation

The device supports single-ended supply voltages with VS+ connected to a positive voltage from 4.0 V to 5.25 V and VS– connected to ground reference. When using a single supply, check to make sure the input and output common-mode voltages are within the operating range of the device. Best performance is achieved when the input and output common-mode voltages are centered close to mid-supply.

## 11.2 Split-Supply Operation

Using split supplies provides the most flexibility in system design. To operate on split supplies, apply the positive supply voltage to VS+, the negative supply voltage to VS–, and the ground reference to GND. Note that supply voltages do not need to be symmetrical, as long as the minimum positive (VS+) supply voltage to ground is 2 V, or greater. The split-supply operation is often beneficial when the output common-mode of the device must be set to a particular voltage. For best performance (see Figure 21 and Figure 22), TI recommends that the power-supply voltages be symmetrical around the desired output common-mode voltage. The input common-mode voltage range is much more flexible than the output. For example, if the LMH6401 is used to drive an ADC with a 1.0-V input common mode, then the ideal supply voltages are 3.5 V and –1.5 V with the output common-mode voltage of the LMH6401 centered at 1.0 V for best linearity and noise performance. The GND pin can then be connected to the system ground and the PD pin and SPI pins are ground referenced.

TI recommends powering up the device with low-noise, LDO-type regulators. If a switching-type regulator is used to improve system power efficiency, following the switching-type regulator with a low-noise LDO is recommended to provide the best possible filtering of the switching noise. An example low-noise switcher and LDO for generating negative supply voltages are the LMR70503 and TPS72301, respectively. In a system with multiple devices being powered on from the same voltage regulator, a high possibility of noise being coupled between the multiple devices exists. Additionally, when operated on a board with high-speed digital signals, isolation must be provided between the digital signal noise and the LMH6401 supply pins. Therefore, adding additional series ferrite beads or isolation devices and decoupling capacitors is recommended to filter out any power-supply noise and improve isolation.

Power-supply decoupling is critical to filter out high-frequency switching noise coupling into the supply pins. Decoupling the supply pins with low ESL, 0306-size ceramic capacitors of X7R-type 0.01-µF and 2200-pF values are recommended. In addition to the decoupling capacitors, the supply bypassing can be provided by the PCB, as illustrated in *Layout Guidelines* section.

# 12 Layout

## 12.1 Layout Guidelines

When dealing with a device with relatively high gain and bandwidth in excess of 1 GHz, certain board layout precautions must be taken to ensure stability and optimum performance. TI recommends that the LMH6401 board be multi-layered to improve thermal performance, grounding, and power-supply decoupling. The differential input and output traces must be symmetrical in order to achieve the best linearity performance.

By sandwiching the power-supply layer between ground layers on either side (with thin dielectric thicknesses), parasitic capacitance between power and ground functions as a distributed, high-resonance frequency capacitor to help with power-supply decoupling. The LMH6401 evaluation board includes a total of six layers and the positive (VS+) and negative (VS–) power planes are sandwiched in the middle with a board stack-up (dielectric thickness), as shown in Figure 71, to help with supply decoupling. Both VS+ and VS– must be connected to the internal power planes through multiple vias in the immediate vicinity of the supply pins. In addition, low ESL, ceramic, 0.01-µF decoupling capacitors to the supplies are placed on the same layer as the device to provide supply decoupling.

Routing high-frequency signal traces on a PCB requires careful attention to maintain signal integrity. A board layout software package can simplify the trace thickness design to maintain impedances for controlled impedance signals. In order to isolate the affect of board parasitic on frequency response, TI recommends placing the external output matching resistors close to the amplifier output pins. A 0.01-µF bypass capacitor is also recommended close to the VOCM pins to suppress high-frequency common-mode noise. Refer to the user guide *LMH6401EVM Evaluation Module* (SLOU406) for more details on board layout and design.

In order to improve board mechanical reliability, the LMH6401 has square anchor pins on four corners of the package that must be soldered to the board for mechanical strength.

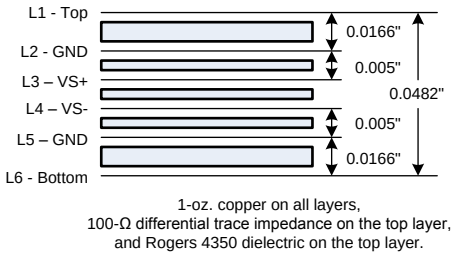



**Figure 71. Recommended PCB Layer Stack-Up for a Six-Layer Board**

## 12.2 Layout Examples

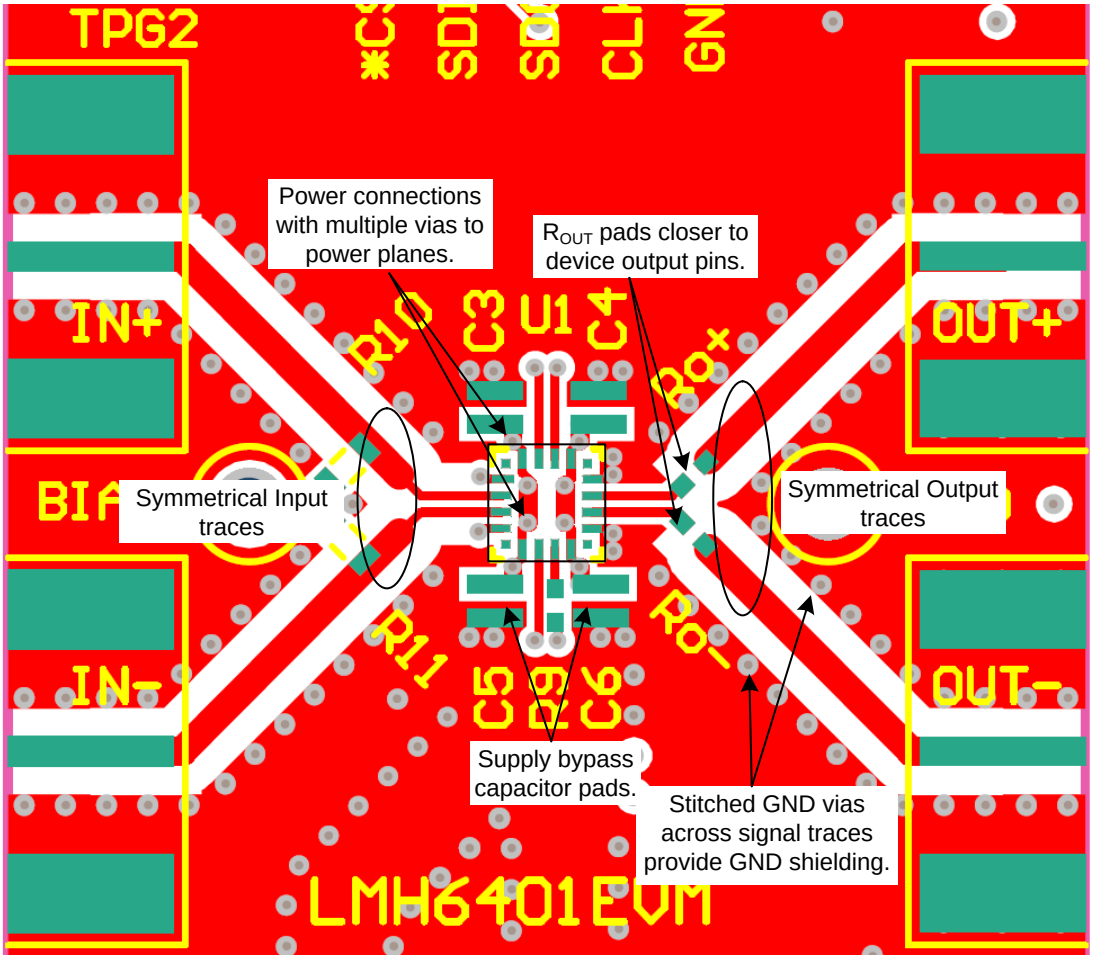



**Figure 72. EVM Top Layer**

**Figure 73. EVM Second Layer Showing a Solid GND Plane**

# 13 器件和文档支持

## 13.1 文档支持

### 13.1.1 相关文档

相关文档如下：

- 《ADS12D1800RF 数据表》，SNAS518
- 《ADC12J1600 和 ADC12J2700 数据表》，SLAS969
- 《ADC12J4000 数据表》，SLAS989
- 《ADS54J40 数据表》，SBAS714
- 《ADS54J60 数据表》，SBAS706
- 《LMH3401 数据表》，SBOS695
- 《LMH5401 数据表》，SBOS710
- 《LMH6517 数据表》，SNOSB19
- 《LMH6521 数据表》，SNOSB47
- 《LMH6554 数据表》，SNOSB30
- 《LMH6881 数据表》，SNOSC72
- 《LMR70503 数据表》，SNVS850
- 《TPS72301 数据表》，SLVS346
- *《AN-2188 在放大器和 ADC 之间：管理通信系统中的滤波器损耗》*，SNOA567
- *《AN-2235 LMH6517/21/22 和其它高速 IF/RF 反馈放大器的电路板设计》*，SNOA869
- *《LMH6401EVM 评估模块》*，SLOU406

## 13.2 社区资源

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## 13.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

## 14 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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| 电源管理 | www.ti.com.cn/power | 视频和影像 | www.ti.com.cn/video |
| 微控制器 (MCU) | www.ti.com.cn/microcontrollers | | |
| RFID 系统 | www.ti.com.cn/rfidsys | | |
| OMAP应用处理器 | www.ti.com/omap | | |
| 无线连通性 | www.ti.com.cn/wirelessconnectivity | 德州仪器在线技术支持社区 | www.deyisupport.com |

邮寄地址： 上海市浦东新区世纪大道1568 号，中建大厦32 楼邮政编码： 200122

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| LMH6401IRMZR | ACTIVE | UQFN-HR | RMZ | 16 | 3000 | RoHS & Green | SN | Level-2-260C-1 YEAR | -40 to 85 | MH6401 | Samples |
| LMH6401IRMZT | ACTIVE | UQFN-HR | RMZ | 16 | 250 | RoHS & Green | SN | Level-2-260C-1 YEAR | -40 to 85 | MH6401 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

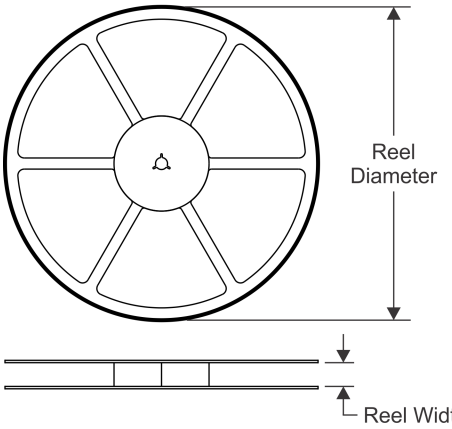
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

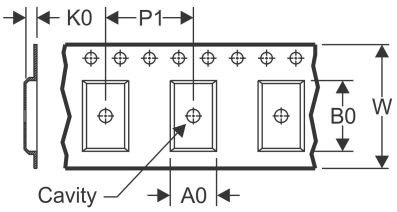
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

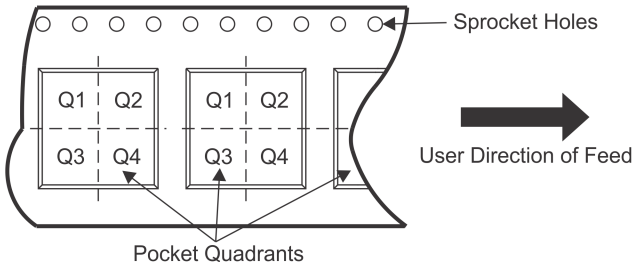



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

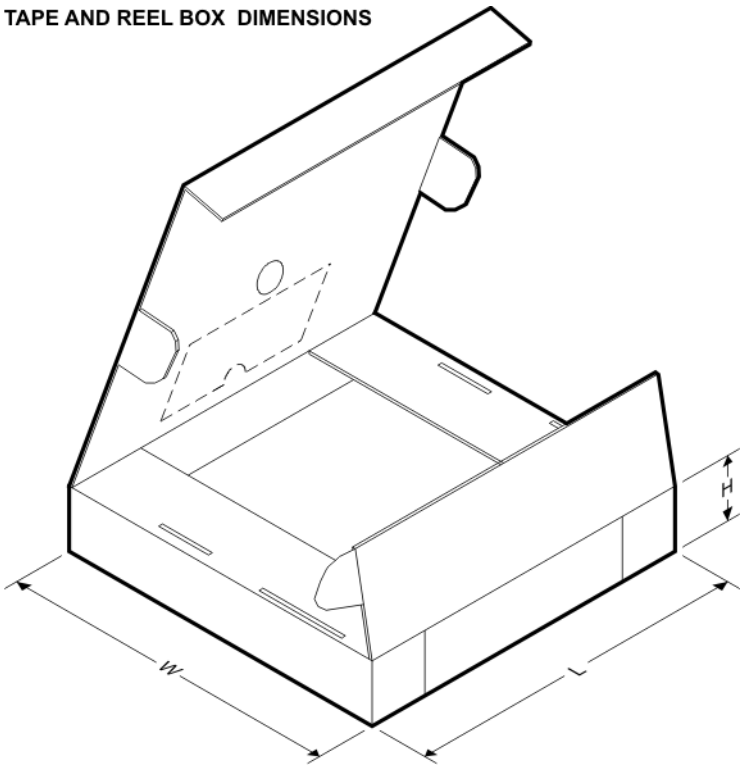
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LMH6401IRMZR | UQFN-HR | RMZ | 16 | 3000 | 180.0 | 16.5 | 3.3 | 3.3 | 0.75 | 8.0 | 12.0 | Q2 |
| LMH6401IRMZT | UQFN-HR | RMZ | 16 | 250 | 180.0 | 16.5 | 3.3 | 3.3 | 0.75 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

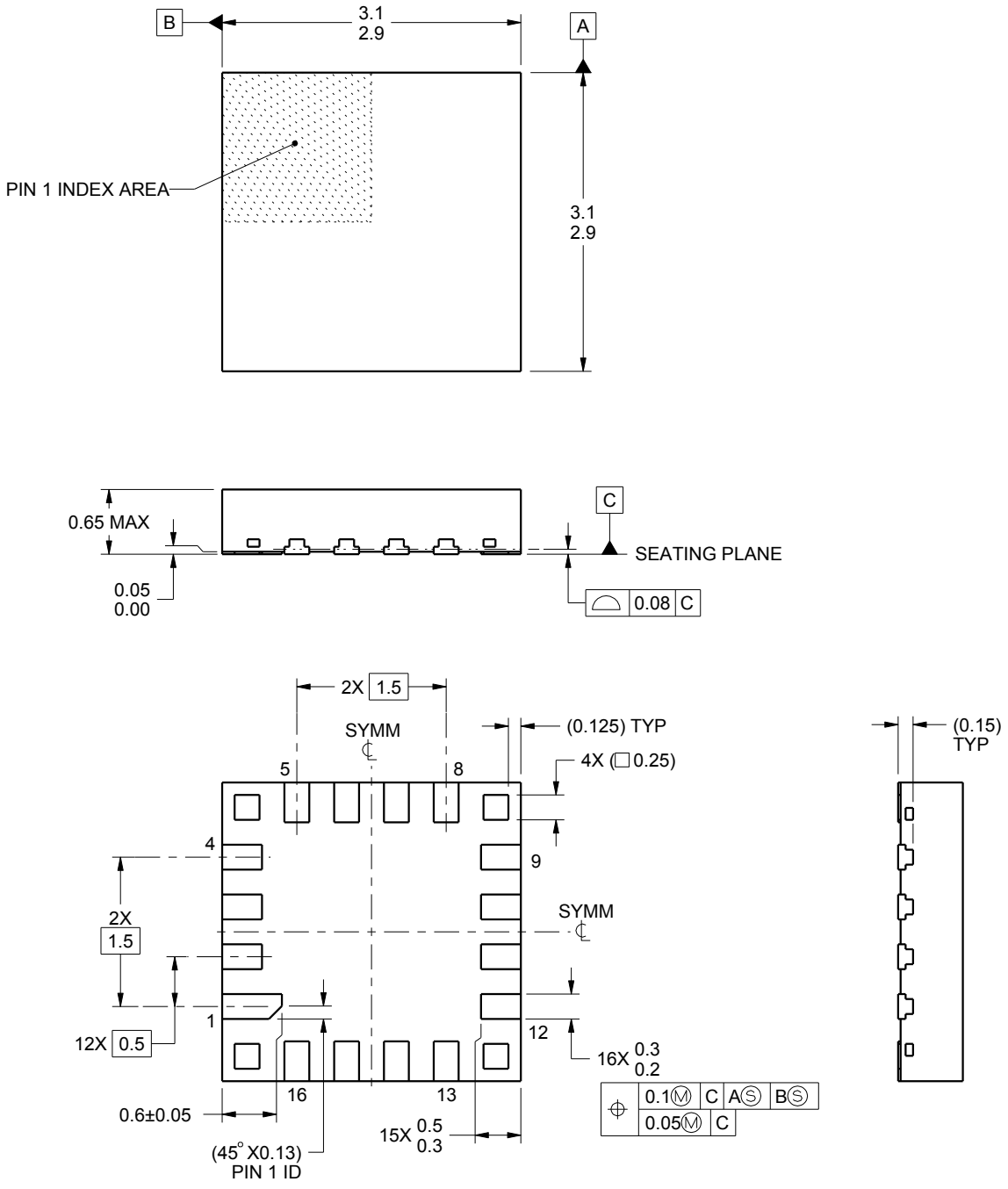
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| LMH6401IRMZR | UQFN-HR | RMZ | 16 | 3000 | 205.0 | 200.0 | 30.0 |
| LMH6401IRMZT | UQFN-HR | RMZ | 16 | 250 | 205.0 | 200.0 | 30.0 |

# PACKAGE OUTLINE

## RMZ0016A

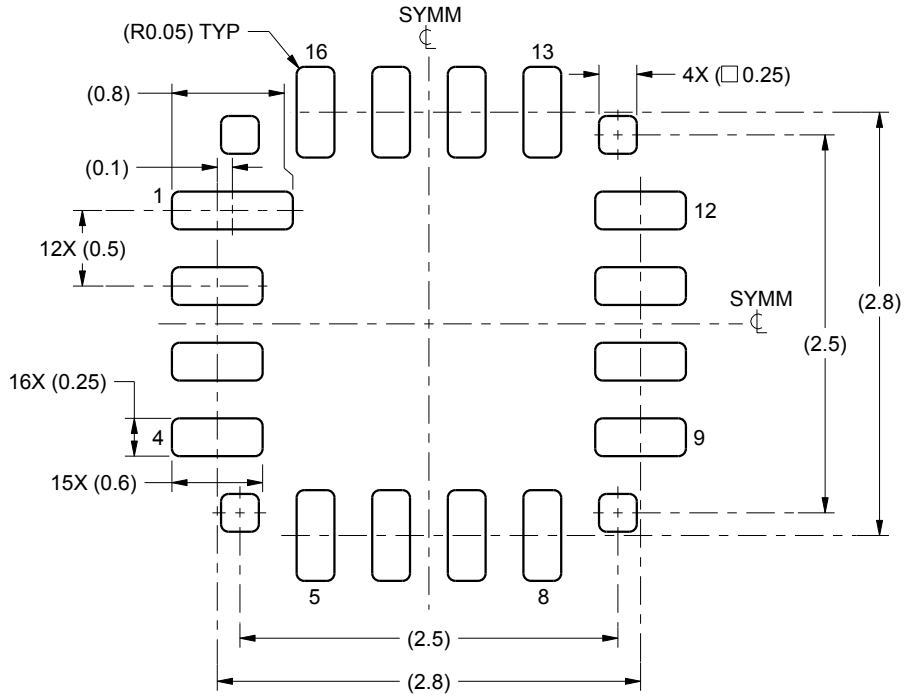
## UQFN - 0.65 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

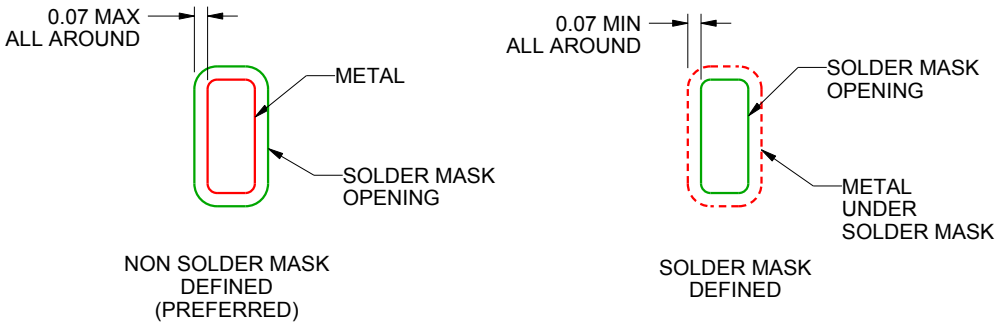



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.




LAND PATTERN EXAMPLE
SCALE:20X

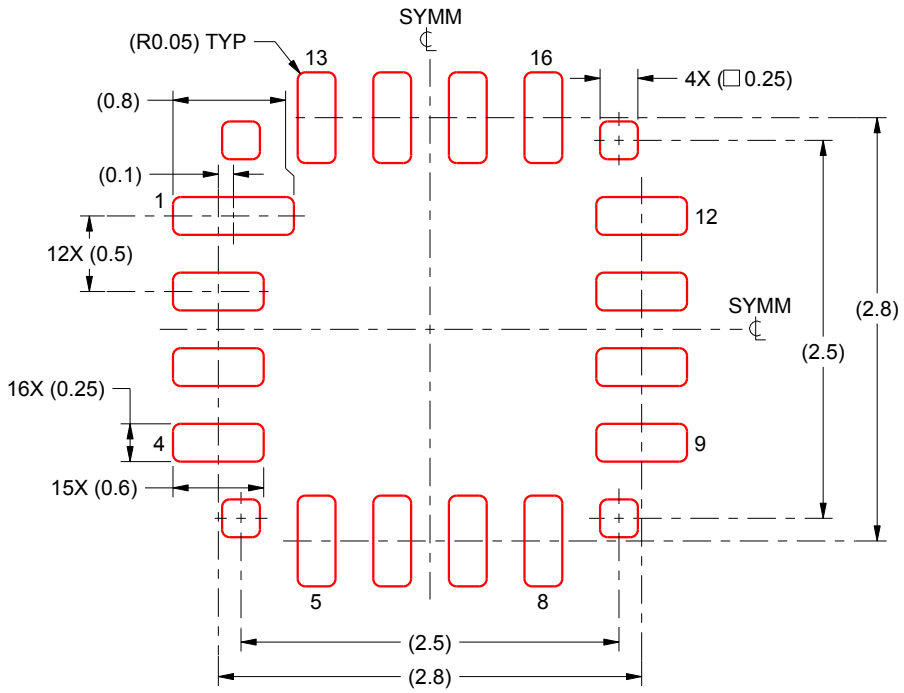



SOLDER MASK DETAILS
NOT TO SCALE

4221506/B 01/2015

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICKNESS
SCALE:20X

4221506/B 01/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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