LP3850x-ADJ, LP3850xA-ADJ 1.5-A Flexcap Low-Dropout Linear Regulator for 2.7-V to 5.5-V Inputs

1 Features

- Input Voltage: 2.7 V to 5.5 V
- Adjustable Output Voltage: 0.6 V to 5 V
- FlexCap: Stable with Ceramic, Tantalum, or Aluminum Capacitors
- Stable with 10-µF Input and Output Capacitors
- Low Ground-Pin Current
- 25-nA Quiescent Current in Shutdown Mode
- Ensured Output Current of 1.5 A
- Ensured V_{ADJ} Accuracy of ±1.5% at 25°C (A Grade)
- Ensured Accuracy of ±3.5% at 25°C (STD)
- Overtemperature and Overcurrent Protection
- ENABLE Pin (LP38502)

2 Applications

- ASIC Power Supplies In:
  - Printers, Graphics Cards, DVD Players
  - Set Top Boxes, Copiers, Routers
- DSP and FPGA Power Supplies
- SMPS Regulator
- Conversion from 3.3-V or 5-V Rail

3 Description

TI's FlexCap low-dropout (LDO) linear regulators feature unique compensation that allow use of any type of output capacitor with no limits on minimum or maximum equivalent series resistance (ESR). The LP38500 and LP38502 series of LDOs operates from a 2.7-V to 5.5-V input supply. These ultra-low-dropout linear regulators respond very quickly to step changes in load, making them suitable for low-voltage microprocessor applications. Developed on a CMOS process (utilizing a PMOS pass transistor) the LP38500-ADJ and LP38502-ADJ have low quiescent currents that changes little with load current.

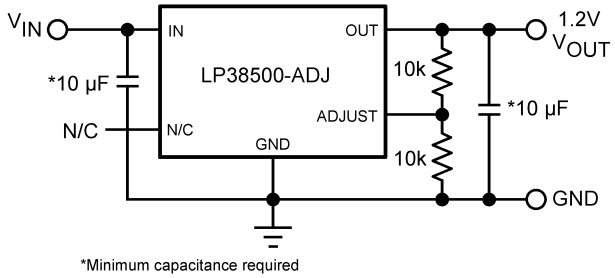
- GND Pin Current: Typically 2 mA at 1.5-A load current.
- Disable Mode: Typically 25-nA quiescent current when the EN pin is pulled low. (LP38502-ADJ)
- Simplified Compensation: Stable with any type of output capacitor, regardless of ESR.
- Precision Output: *A* grade versions available with 1.5% V_{ADJ} tolerance (25°C) and 3% over line, load, and temperature.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP38500 LP38502	DDPAK/TO-263 (5)	10.16 mm x 8.42 mm
	TO-263 (5)	10.16 mm x 9.85 mm
	WSON (8)	3.00 mm x 2.50 mm

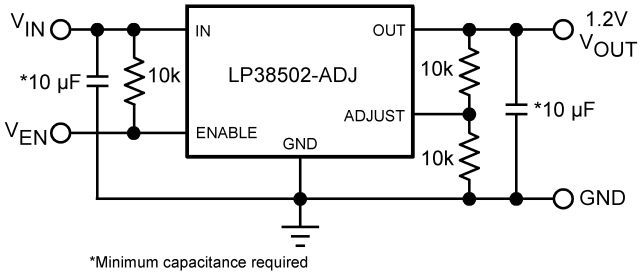
(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Circuit (LP38500)



*Minimum capacitance required

Typical Circuit (LP38502)



*Minimum capacitance required

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (June 2015) to Revision H — **Page**

- Changed thermal values for KTT (DDPAK/TO-263); add notes 2 and 3 to *Thermal Information* table ... 4

Changes from Revision F (April 2013) to Revision G — **Page**

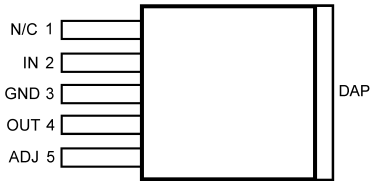
- Added Added *Device Information* and *Pin Configuration and Functions* sections, *ESD Ratings* and updated *Thermal Information* tables, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support* , and *Mechanical, Packaging, and Orderable Information* sections ... 1
- Deleted obsolete heatsinking information for DDPAK/TO-263 package ... 16

Changes from Revision E (April 2013) to Revision F — **Page**

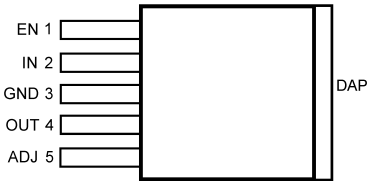
- Changed layout of National Data Sheet to TI format ... 19

5 Pin Configurations and Functions

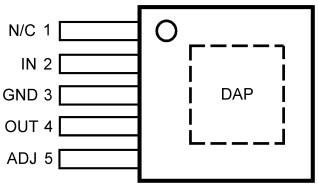
KTT Package (LP38500)
5-Pin DDPAK/TO-263
Top View



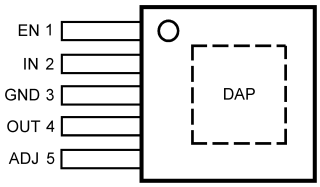
KTT Package (LP38502)
5-Pin DDPAK/TO-263
Top View



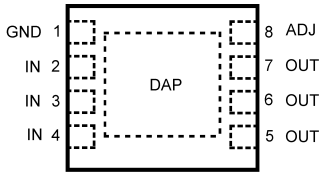
NDQ Package (LP38500)
5-Pin TO-263
Top View



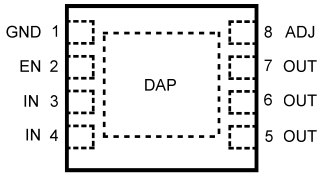
NDQ Package (LP38502)
5-Pin TO-263
Top View



NGS Package (LP38500A)
8-Pin WSON
Top View



NGS Package (LP38502A)
8-Pin WSON
Top View



Pin Functions

PIN				TYPE	DESCRIPTION
NAME	KTT	NDQ	NGS		
ADJ	5	5	8	O	Sets output voltage
EN	1	1	2	I	Enable (LP38502-ADJ only). Pull high to enable the output, low to disable the output. This pin has no internal bias and must be either tied to the input voltage, or actively driven.
GND	3	3	1	G	Ground
IN	—	—	2	I	Input supply (LP38500-ADJ only). Input supply pins share current and must be connected together on the PC board.
IN	2	2	3, 4	I	Input supply. Input Supply pins share current and must be connected together on the PC board.
N/C	1	1	—	—	In the LP38500-ADJ, this pin has no internal connections. It can be left floating or used for trace routing.
OUT	4	4	5, 6, 7	O	Regulated output voltage. Output pins share current and must be connected together on the PC board.
DAP	√	√	√	—	The DAP is used to remove heat from the device by conducting it to a copper clad area on the PCB which acts as a heatsink. The DAP is electrically connected to the backside of the die. The DAP must be connected to ground potential, but can not be used as the only ground connection.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
Input pin voltage (survival)	−0.3	6	V
Enable pin voltage (survival)	−0.3	6	V
Output pin voltage (survival)	−0.3	6	V
I_{OUT} (survival)	Internally limited		
Power dissipation(3)	Internally limited		
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Office/ Distributors for availability and specifications.
(3) Operating junction temperature must be evaluated, and derated as needed, based on ambient temperature (T_A), power dissipation (P_D), maximum allowable operating junction temperature ($T_{J(MAX)}$), and package thermal resistance ($R_{\theta JA}$). See *Application and Implementation*.

6.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	NOM	MAX	UNIT
Input supply voltage	2.7		5.5	V
Enable input voltage	0		5.5	V
Output current (DC)	0		1.5	A
V_{OUT}	0.6		5	V
Junction temperature(1)	−40		125	°C

(1) Operating junction temperature must be evaluated, and derated as needed, based on ambient temperature (T_A), power dissipation (P_D), maximum allowable operating junction temperature ($T_{J(MAX)}$), and package thermal resistance ($R_{\theta JA}$). See *Application and Implementation*.

6.4 Thermal Information

THERMAL METRIC(1)		LP38500 and LP38502			UNIT
		KTT(DDPAK/TO-263)	NDQ (TO-263)	NGS (WSON)	
		5 PINS	5 PINS	8 PINS	
$R_{\theta JA}$(2)	Junction-to-ambient thermal resistance	41.8	33.3	52.5(3)	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.0	22.1	53.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	24.8	16.9	26.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.1	5.8	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.8	16.8	26.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.4	2.3	7.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Thermal resistance value $R_{\theta JA}$ is based on the EIA/JEDEC High-K printed circuit board defined by: JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*.
(3) The PCB for the NGN (WSON) package $R_{\theta JA}$ includes thermal vias under the exposed thermal pad per EIA/JEDEC JESD51-5.

6.5 Electrical Characteristics

Unless otherwise specified V_{IN} = 3.3 V, I_{OUT} = 10 mA, C_{IN} = 10 µF, C_{OUT} = 10 µF, V_{EN} = V_{IN}, V_{OUT} = 1.8 V. Minimum and maximum limits apply over the junction temperature (T_J) range of –40°C to +125°C and are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ADJ}	Adjust pin voltage (1)	2.7 V ≤ V_{IN} ≤ 5.5 V 10 mA ≤ I_{OUT} ≤ 1.5 A T_J = 25°C	0.584	0.605	0.626	V
		2.7 V ≤ V_{IN} ≤ 5.5 V 10 mA ≤ I_{OUT} ≤ 1.5 A	0.575		0.635	
V_{ADJ}	Adjust pin voltage (A grade) (1)	2.7 V ≤ V_{IN} ≤ 5.5 V 10 mA ≤ I_{OUT} ≤ 1.5 A T_J = 25°C	0.596	0.605	0.614	V
		2.7 V ≤ V_{IN} ≤ 5.5 V 10 mA ≤ I_{OUT} ≤ 1.5 A	0.587		0.623	
I_{ADJ}	ADJUST pin bias current	2.7 V ≤ V_{IN} ≤ 5.5 V T_J = 25°C		50		nA
		2.7 V ≤ V_{IN} ≤ 5.5 V			750	nA
V_{DO}	Dropout voltage (2)	I_{OUT} = 1.5 A T_J = 25°C		220	275	mV
		I_{OUT} = 1.5 A			375	mV
ΔV_{OUT} / ΔV_{IN}	Output voltage line regulation (1) (3)	2.7 V ≤ V_{IN} ≤ 5.5 V T_J = 25°C		0.04		%/V
		2.7 V ≤ V_{IN} ≤ 5.5 V		0.05		%/V
ΔV_{OUT} / ΔI_{OUT}	Output voltage load regulation (1) (4)	10 mA < I_{OUT} < 1.5 A T_J = 25°C		0.18		%/A
		10 mA < I_{OUT} < 1.5 A		0.33		%/A
I_{GND}	Ground pin current in normal operation mode	10 mA < I_{OUT} < 1.5 A T_J = 25°C		2	3.5	mA
		10 mA < I_{OUT} < 1.5 A			4.5	
$I_{DISABLED}$	Ground pin current	V_{EN} < $V_{IL(EN)}$, T_J = 25°C		0.025	0.125	µA
		V_{EN} < $V_{IL(EN)}$			15	
$I_{OUT(PK)GND}$	Peak output current	V_{OUT} ≥ $V_{OUT(NOM)}$ – 5%		3.6		A
I_{SC}	Short-circuit current	V_{OUT} = 0 V, T_J = 25°C		3.7		A
		V_{OUT} = 0 V	2			
ENABLE INPUT (LP38502 Only)						
$V_{IH(EN)}$	Enable logic high	V_{OUT} = ON	1.4			V
$V_{IL(EN)}$	Enable logic low	V_{OUT} = OFF			0.65	V
$t_{d(off)}$	Turnoff delay	Time from V_{EN} < $V_{IL(EN)}$ to V_{OUT} = OFF I_{LOAD} = 1.5 A		25		µs
$t_{d(on)}$	Turnon delay	Time from V_{EN} >$V_{IH(EN)}$ to V_{OUT} = ON I_{LOAD} = 1.5A		25		µs
$I_{IH(EN)}$	Enable pin high current	V_{EN} = V_{IN}		1		nA
$I_{IL(EN)}$	Enable pin low current	V_{EN} = 0 V		0.1		

(1) The line and load regulation specification contains only the typical number. However, the limits for line and load regulation are included in the adjust voltage tolerance specification.
(2) Dropout voltage is defined as the minimum input to output differential voltage at which the output drops 2% below the nominal value. For any output voltage less than 2.5V, the minimum VIN operating voltage is the limiting factor.
(3) Output voltage line regulation is defined as the change in output voltage from the nominal value due to change in the input line voltage.
(4) Output voltage load regulation is defined as the change in output voltage from the nominal value due to change in the load current.

Electrical Characteristics (continued)

Unless otherwise specified V_{IN} = 3.3 V, I_{OUT} = 10 mA, C_{IN} = 10 µF, C_{OUT} = 10 µF, V_{EN} = V_{IN}, V_{OUT} = 1.8 V. Minimum and maximum limits apply over the junction temperature (T_J) range of –40°C to +125°C and are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC PARAMETERS						
PSRR	Ripple rejection	V_{IN} = 3 V, I_{OUT} = 1.5 A, f = 120 Hz		58		dB
		V_{IN} = 3 V, I_{OUT} = 1.5 A, f = 1 kHz		56		
$\rho_{n(l/f)}$	Output noise density	f = 120 Hz, C_{OUT} = 10 µF CER		1		µV/√Hz
e_n	Output noise voltage	BW = 100 Hz – 100 kHz C_{OUT} = 10 µF CER		100		µV(rms)
THERMALS						
T_{SD}	Thermal shutdown	T_J rising		170	—	°C
ΔT_{SD}	Thermal shutdown hysteresis	T_J falling from T_{SD}		10	—	°C

6.6 Typical Characteristics

Unless otherwise specified: T_J = 25°C, V_{IN} = 2.7 V, V_{EN} = V_{IN}, C_{IN} = 10 µF, C_{OUT} = 10 µF, I_{OUT} = 10 mA, V_{OUT} = 1.8 V.

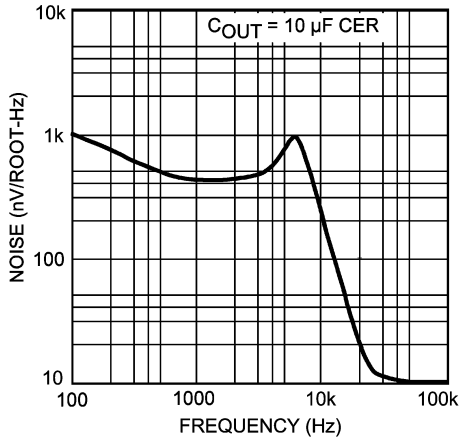


Figure 1. Noise Density

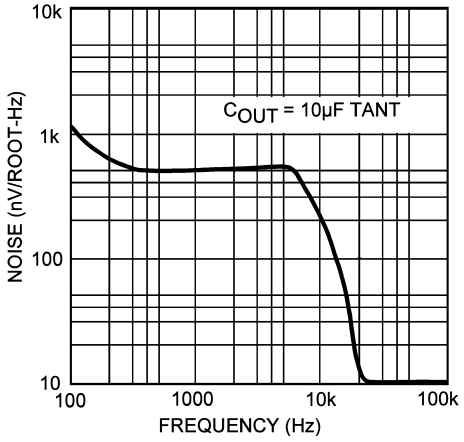


Figure 2. Noise Density

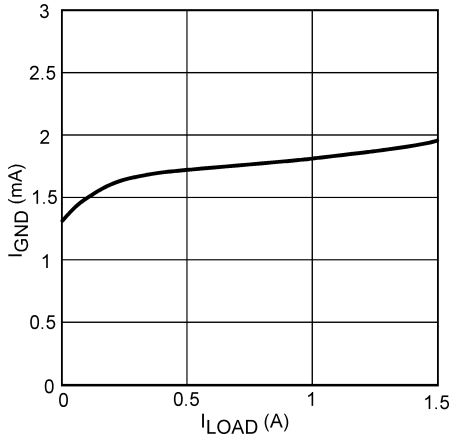


Figure 3. I_{GND} vs Load Current

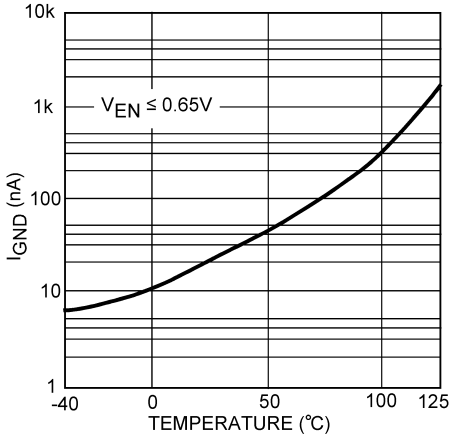


Figure 4. $I_{GND(OFF)}$ vs Temperature

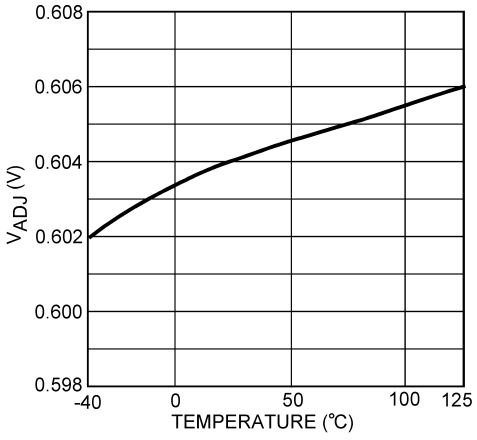


Figure 5. V_{ADJ} vs Temperature

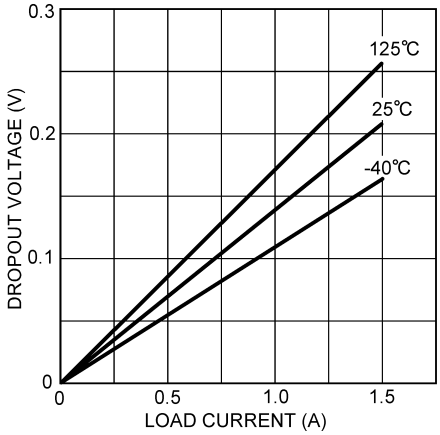


Figure 6. Dropout Voltage vs Load Current

Typical Characteristics (continued)

Unless otherwise specified: T_J = 25°C, V_{IN} = 2.7 V, V_{EN} = V_{IN}, C_{IN} = 10 µF, C_{OUT} = 10 µF, I_{OUT} = 10 mA, V_{OUT} = 1.8 V.

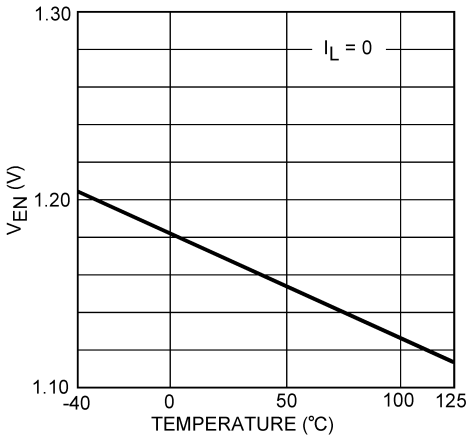


Figure 7. V_{EN} vs Temperature

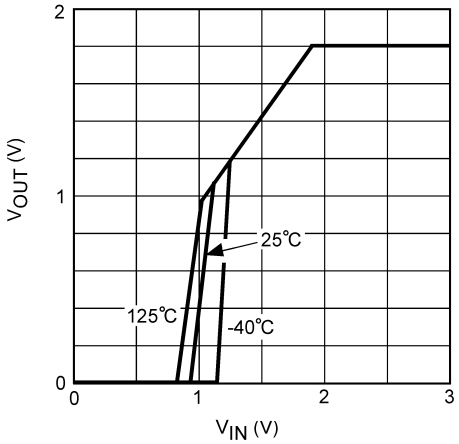


Figure 8. Turnon Characteristics

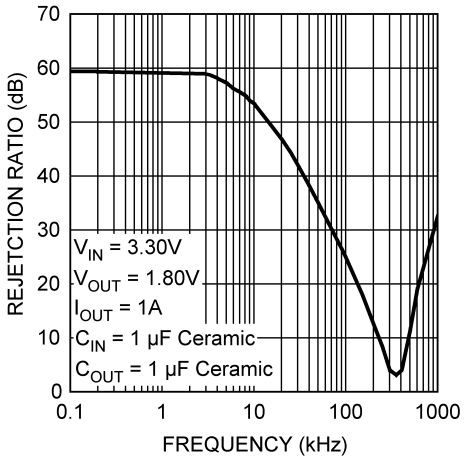


Figure 9. PSRR

7 Detailed Description

7.1 Overview

The LP38500-ADJ and LP38502-ADJ are flex-cap and low-dropout adjustable regulators, the output voltage can be set from 0.6 V to 5 V. Standard regulator features, such as overcurrent and overtemperature protections, are also included.

The LP38500-ADJ and LP38502-ADJ contains several features:

- Stable with any type of output capacitor
- Fast load transient response
- Disable Mode (LP38502-ADJ only)

7.2 Functional Block Diagrams

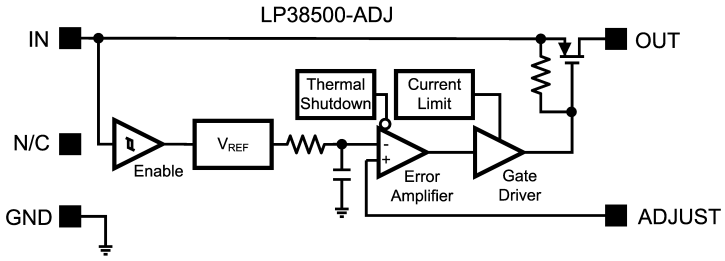


Figure 10. LP38500-ADJ DDPAK/TO-263 Block Diagram

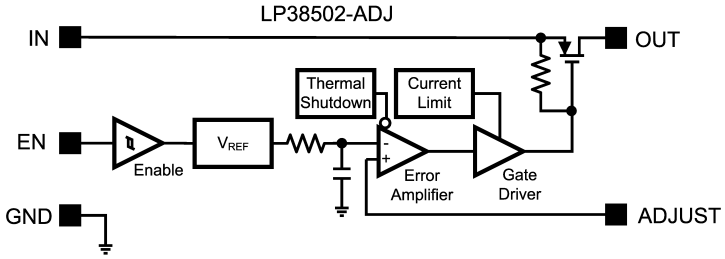


Figure 11. LP38502-ADJ DDPAK/TO-263 Block Diagram

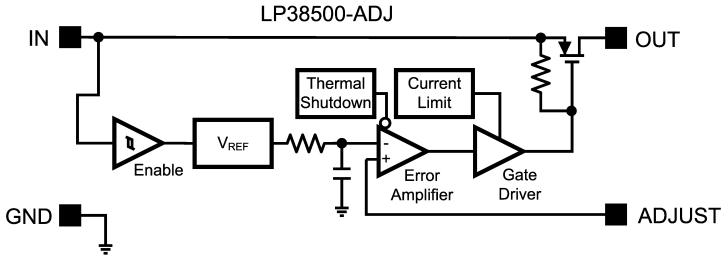


Figure 12. LP38500-ADJ WSON Block Diagram

Functional Block Diagrams (continued)

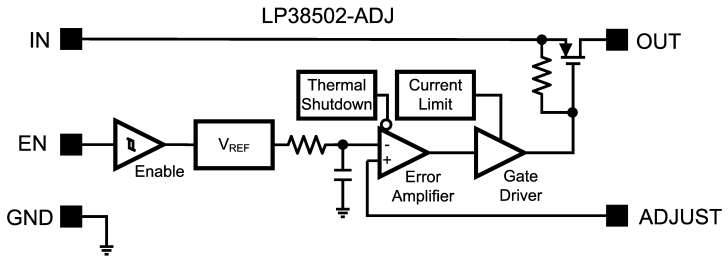


Figure 13. LP38502-ADJ WSON Block Diagram

7.3 Feature Description

7.3.1 Stability And Phase Margin

Any regulator which operates using a feedback loop must be compensated in such a way as to ensure adequate phase margin, which is defined as the difference between the phase shift and –180 degrees at the frequency where the loop gain crosses unity (0 dB). For most LDO regulators, the ESR of the output capacitor is required to create a zero to add enough phase lead to ensure stable operation. The LP38500-ADJ and LP38502-ADJ each have a unique internal compensation circuit which maintains phase margin regardless of the ESR of the output capacitor, so any type of capacitor may be used.

Figure 14 shows the gain/phase plot of the LP38500-ADJ and LP38502-ADJ with an output of 1.2 V, a 10-µF ceramic output capacitor, delivering 1.5 A of load current. It can be seen that the unity-gain crossover occurs at 150 kHz, and the phase margin is about 40° (which is very stable).

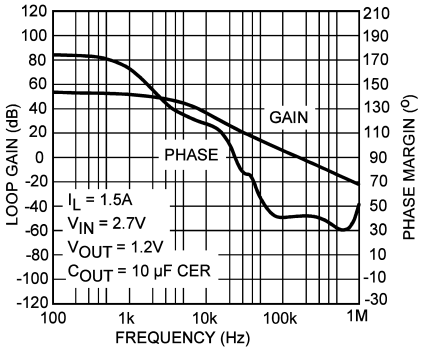


Figure 14. Gain-Bandwidth Plot for 1.5-A Load

Figure 15 shows the gain and phase with no external load. In this case, the only load is provided by the gain setting resistors (about 12 kΩ total in this test). It is immediately obvious that the unity-gain frequency is significantly lower (dropping to about 500 Hz), at which point the phase margin is 125°.

Feature Description (continued)

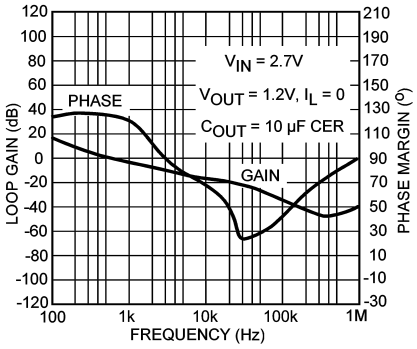


Figure 15. Gain-Bandwidth Plot for No Load

The reduction in unity-gain bandwidth as load current is reduced is normal for any LDO regulator using a P-FET or PNP pass transistor, because they have a pole in the loop gain function given by:

$$F_P = \frac{1}{2 \times \pi \times R_L \times C_{OUT}} \quad (1)$$

This illustrates how the pole goes to the highest frequency when R_L is minimum value (maximum load current). In general, LDOs have maximum bandwidth (and lowest phase margin) at full load current. In the case of the LP38500-ADJ or LP38502-ADJ, it can be seen that it has good phase margin even when using ceramic capacitors with ESR values of only a few mΩ.

7.3.2 Load Transient Response

Load transient response is defined as the change in regulated output voltage which occurs as a result of a change in load current. Many applications have loads which vary, and the control loop of the voltage regulator must adjust the current in the pass FET transistor in response to load current changes. For this reason, regulators with wider bandwidths often have better transient response.

The LP38500-ADJ and LP38502-ADJ employs an internal feed-forward design which makes the load transient response much faster than would be predicted simply by loop speed: this feedforward means any voltage changes appearing on the output are coupled through to the high-speed driver used to control the gate of the pass FET along a signal path using very fast FET devices. Because of this, the pass transistor's current can change very quickly.

Figure 15 shows the output voltage load transient which occurs on a 1.8-V output when the load changes from 0.1 A to 1.5 A at an average slew rate of 0.5 A/µs. As shown, the peak output voltage change from nominal is about 40 mV, which is about 2.2%.

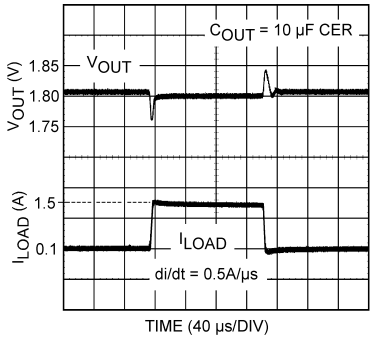


Figure 16. Load Transient Response

Feature Description (continued)

In cases where extremely fast load changes occur, the output capacitance may have to be increased. For fast changing loads, the internal parasitics of ESR (equivalent series resistance) and ESL (equivalent series inductance) degrade the capacitor's ability to source current quickly to the load. The best capacitor types for transient performance are (in order):

1. Multilayer Ceramic: with the lowest values of ESR and ESL, they can have ESR values in the range of a few mΩ. Disadvantage: capacitance values above about 22 µF significantly increase in cost.
2. Low-ESR Aluminum Electrolytics: these are aluminum types (like OSCON) with a special electrolyte which provides extremely low ESR values, and are the closest to ceramic performance while still providing large amounts of capacitance. These are cheaper (by capacitance) than ceramic.
3. Solid tantalum: can provide several hundred µF of capacitance, transient performance is slightly worse than OSCON type capacitors, cheaper than ceramic in large values.
4. General purpose aluminum electrolytics: cheap and provide a lot of capacitance, but give the worst performance.

In general, managing load transients is done by paralleling ceramic capacitance with a larger bulk capacitance. In this way, the ceramic can source current during the rapidly changing edge and the bulk capacitor can support the load current after the first initial spike in current.

7.3.3 Dropout Voltage

The dropout voltage of a regulator is defined as the input-to-output differential required by the regulator to keep the output voltage within 2% of the nominal value. For CMOS LDOs, the dropout voltage is the product of the load current and the $R_{DS(on)}$ of the internal MOSFET pass element.

Since the output voltage is beginning to "drop out" of regulation when it drops by 2%, electrical performance of the device will be reduced compared to the values listed in the Electrical Characteristics table for some parameters (line and load regulation and PSRR would be affected).

7.3.4 Reverse Current Path

The internal MOSFET pass element in the LP38500-ADJ and LP38502-ADJ has an inherent parasitic diode. During normal operation, the input voltage is higher than the output voltage and the parasitic diode is reverse biased. However, if the output is pulled above the input in an application, then current flows from the output to the input as the parasitic diode gets forward biased. The output can be pulled above the input as long as the current in the parasitic diode is limited to 200-mA continuous and 1-A peak. The regulator output pin should not be taken below ground potential. If the LP38500-ADJ and LP38502-ADJ is used in a dual-supply system where the regulator load is returned to a negative supply, the output must be diode-clamped to ground.

7.4 Device Functional Modes

7.4.1 Short-Circuit Protection

The LP38500-ADJ and LP38502-ADJ contain internal current limiting which will reduce output current to a safe value if the output is overloaded or shorted. Depending upon the value of V_{IN}, thermal limiting may also become active as the average power dissipated causes the die temperature to increase to the limit value (about 170°C). The hysteresis of the thermal shutdown circuitry can result in a "cyclic" behavior on the output as the die temperature heats and cools.

7.4.2 Enable Operation (LP38502-ADJ Only)

The Enable pin (EN) must be actively terminated by either a 10-kΩ pull-up resistor to V_{IN}, or a driver which actively pulls high and low (such as a CMOS rail to rail comparator). If active drive is used, the pull-up resistor is not required. This pin must be tied to V_{IN} if not used (it must not be left floating).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LP38500-ADJ and LP38502-ADJ devices can provide 1.5-A output current with 2.7-V to 5.5-V input voltage. These ultra-low-dropout linear regulators respond very quickly to step changes in load, making them suitable for low-voltage microprocessor applications. Input and output capacitors of at least 10 µF are required.

8.2 Typical Applications

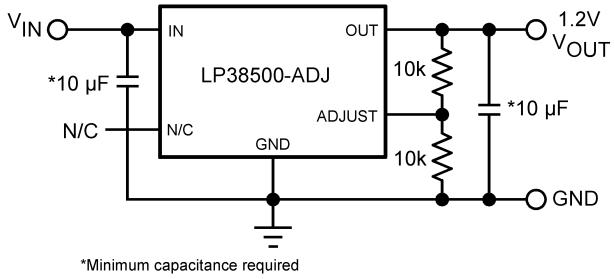


Figure 17. Typical Circuit (LP38500)

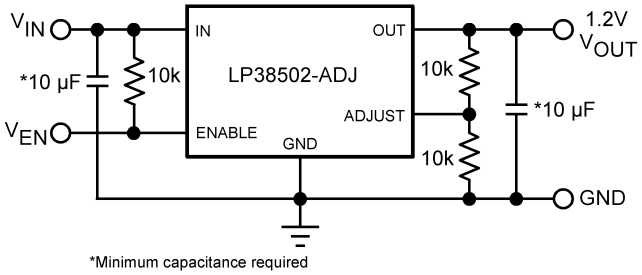


Figure 18. Typical Circuit (LP38502)

8.2.1 Design Requirements

For LP3850x-ADJ typical applications, use the parameters listed in Table 1 as the input parameters.

Table 1. Design Parameters

DESIGN PARAMETERS	VALUE
Input voltage	2.7 V to 5.5 V
Output voltage	0.6 V to 5 V (adjustable)
Output current	1.5 A (maximum)
Input capacitor	10 µF (minimum)
Output capacitor	10 uF (minimum)

8.2.2 Detailed Design Procedure

8.2.2.1 External Capacitors

The LP38500-ADJ and LP38502-ADJ require that at least 10-µF (±20%) capacitors be used at the input and output pins located within one cm of the device. Larger capacitors may be used without limit on size for both C_{IN} and C_{OUT}. Capacitor tolerances such as temperature variation and voltage loading effects must be considered when selecting capacitors to ensure that they will provide the minimum required amount of capacitance under all operating conditions for the application.

In general, ceramic capacitors are best for noise bypassing and transient response because of their ultra low ESR. It must be noted that if ceramics are used, only the types with X5R or X7R dielectric ratings should be used (never Z5U or Y5F). Capacitors which have the Z5U or Y5F characteristics will see a drop in capacitance of as much as 50% if their temperature increases from 25°C to 85°C. In addition, the capacitance drops significantly with applied voltage: a typical Z5U or Y5F capacitor can lose as much as 60% of its rated capacitance if only half of the rated voltage is applied to it. For these reasons, only X5R and X7R ceramics should be used.

8.2.2.2 Input Capacitor

All linear regulators can be affected by the source impedance of the voltage which is connected to the input. If the source impedance is too high, the reactive component of the source may affect the control loop's phase margin. *To ensure proper loop operation, the ESR of the capacitor used for C_{IN} must not exceed 0.5 Ω.* Any good quality ceramic capacitor will meet this requirement, as well as many good quality tantalums. Aluminum electrolytic capacitors may also work, but can possibly have an ESR which increases significantly at cold temperatures. If the ESR of the input capacitor may exceed 0.5 Ω, it is recommended that a 2.2-µF ceramic capacitor be used in parallel, as this will assure stable loop operation.

8.2.2.3 Output Capacitor

Any type of capacitor may be used for C_{OUT}, with no limitations on minimum or maximum ESR, as long as the minimum amount of capacitance is present. The amount of capacitance can be increased without limit. Increasing the size of C_{OUT} typically will give improved load transient response.

8.2.2.4 Setting The Output Voltage

The output voltage of the LP38500/2-ADJ can be set to any value between 0.6V and 5V using two external resistors shown as R1 and R2 in Figure 19.

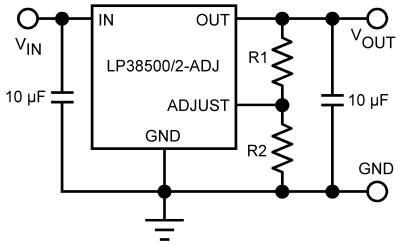


Figure 19. Setting Output Voltage

The value of R2 should always be less than or equal to 10 kΩ for good loop compensation. R1 can be selected for a given V_{OUT} using the following formula:

$$V_{OUT} = V_{ADJ} (1 + R1/R2) + I_{ADJ} (R1) \quad (2)$$

where

- V_{ADJ} is the adjust pin voltage
- I_{ADJ} is the bias current flowing into the adjust pin

8.2.2.5 RFI/EMI Susceptibility

Radio Frequency Interference (RFI) and Electro-Magnetic Interference (EMI) can degrade any integrated circuit's performance because of the small dimensions of the geometries inside the device. In applications where circuit sources are present which generate signals with significant high frequency energy content (> 1 MHz), care must be taken to ensure that this does not affect the device regulator.

If RFI/EMI noise is present on the input side of the regulator (such as applications where the input source comes from the output of a switching regulator), good ceramic bypass capacitors must be used at the input pin of the device to reduce the amount of EMI conducted into the device.

If the LP38500, LP38502-ADJ output is connected to a load which switches at high speed (such as a clock), the high-frequency current pulses required by the load must be supplied by the capacitors on the device output. Since the bandwidth of the regulator loop is less than 300 kHz, the control circuitry cannot respond to load changes above that frequency. This means the effective output impedance of the device at frequencies above 300 kHz is determined only by the output capacitor(s). Ceramic capacitors provide the best performance in this type of application.

In applications where the load is switching at high speed, the output of the device may need RF isolation from the load. In such cases, it is recommended that some inductance be placed between the output capacitor and the load, and good RF bypass capacitors be placed directly across the load. PCB layout is also critical in high noise environments, since RFI/EMI is easily radiated directly into PC traces. Noisy circuitry should be isolated from *clean* circuits where possible, and grounded through a separate path. At MHz frequencies, ground planes begin to look inductive and RFI/EMI can cause ground bounce across the ground plane. In multi-layer PC Board applications, care should be taken in layout so that noisy power and ground planes do not radiate directly into adjacent layers which carry analog power and ground.

8.2.2.6 Output Noise

Noise is specified in two ways:

- Spot noise or output noise density is the RMS sum of all noise sources, measured at the regulator output, at a specific frequency (measured with a 1-Hz bandwidth). This type of noise is usually plotted on a curve as a function of frequency.
- Total output noise or broadband noise is the RMS sum of spot noise over a specified bandwidth, usually several decades of frequencies.

Spot noise is measured in units μV/√Hz or nV/√Hz and total output noise is measured in $\mu_{V(rms)}$. The primary source of noise in low-dropout regulators is the internal reference. In CMOS regulators, noise has a low-frequency component and a high frequency component, which depend strongly on the silicon area and quiescent current.

Noise can generally be reduced in two ways: increase the transistor area or increase the reference current. However, enlarging the transistors will increase die size, and increasing the reference current means higher total supply current (ground pin current).

8.2.3 Application Curves

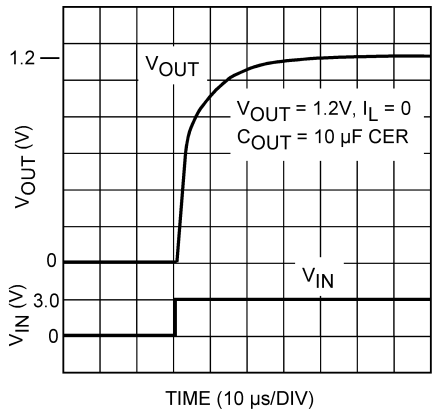


Figure 20. Turnon Time

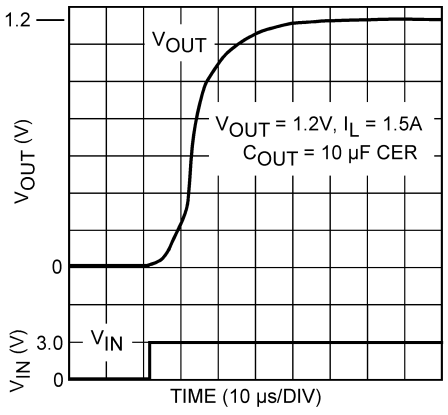


Figure 21. Turnon Time

9 Power Supply Recommendations

The LP38500-ADJ and LP38502-ADJ devices are designed to operate from an input voltage supply range between 2.7 V and 5.5 V. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. An input capacitor of at least 10 µF is required.

9.1 Power Dissipation/Heatsinking

The maximum power dissipation ($P_{D(MAX)}$) of the LP38500-ADJ and LP38502-ADJ is limited by the maximum junction temperature of 125°C, along with the maximum ambient temperature ($T_{A(MAX)}$) of the application, and the thermal resistance ($R_{\theta JA}$) of the package. Under all possible conditions, the junction temperature (T_J) must be within the range specified in the *Recommended Operating Conditions*. The total power dissipation of the device is given by:

$$P_D = ((V_{IN} - V_{OUT}) \times I_{OUT}) + (V_{IN} \times I_{GND})$$

where

- I_{GND} is the operating ground current of the device (specified under *Electrical Characteristics*) (3)

The maximum allowable junction temperature rise (ΔT_J) depends on the maximum expected ambient temperature ($T_{A(MAX)}$) of the application, and the maximum allowable junction temperature ($T_{J(MAX)}$):

$$\Delta T_J = T_{J(MAX)} - T_{A(MAX)} \quad (4)$$

The maximum allowable value for junction-to-ambient thermal resistance, $R_{\theta JA}$, can be calculated using the formula:

$$R_{\theta JA} = \Delta T_J / P_{D(MAX)} \quad (5)$$

The LP38500-ADJ and LP38502-ADJ are available in the DDPAK/TO-263, TO-263, and WSON packages. The thermal resistance depends on the amount of copper area allocated to heat transfer.

10 Layout

10.1 Layout Guidelines

10.1.1 Printed Circuit Board Layout

Good layout practices will minimize voltage error and prevent instability which can result from ground loops. The input and output capacitors should be directly connected to the device pins with short traces that have no other current flowing in them (Kelvin connect).

The best way to do this is to place the capacitors very near the device and make connections directly to the device pins via short traces on the top layer of the PCB. The regulator's ground pin should be connected through vias to the internal or backside ground plane so that the regulator has a single point ground.

The external resistors which set the output voltage must also be located very near the device with all connections directly tied via short traces to the pins of the device (Kelvin connect). Do not connect the resistive divider to the load point or DC error will be induced.

10.2 Layout Examples

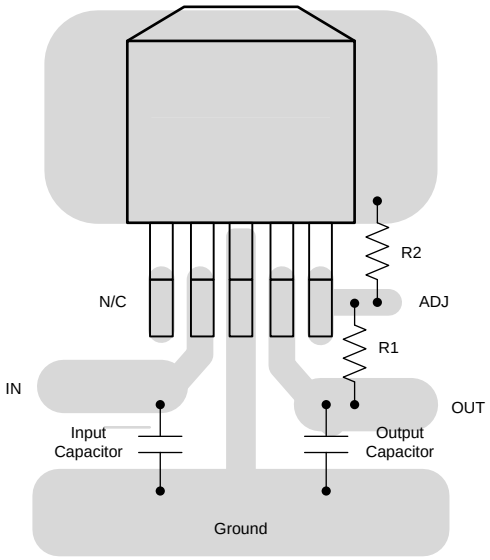


Figure 22. LP38500-ADJ TO-263 Layout (LP38500)

Layout Examples (continued)

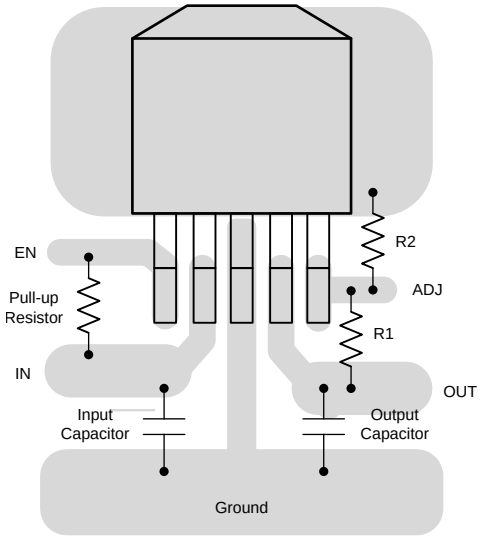


Figure 23. LP38502-ADJ TO-263 Layout

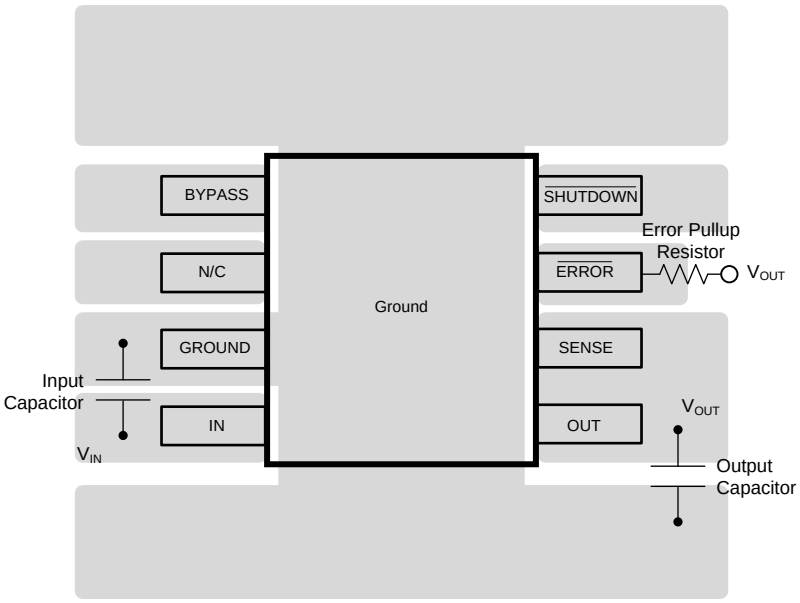


Figure 24. LP3850x WSON Layout

10.2.1 Heatsinking WSON Package

The junction-to-ambient thermal resistance for the WSON package is dependent on how much PCB copper is present to conduct heat away from the device. The LP38502SD-ADJ evaluation board (980600046-100) was tested and gave a result of about 52.5°C/W with a power dissipation of 1 W and no external airflow. This evaluation board is a two layer board using two ounce copper, and the copper area on topside for heatsinking is approximately two square inches. Multiple vias under the DAP also thermally connect to the backside layer which has about three square inches of copper dedicated to heatsinking.

With four thermal vias directly under the DAP to the first copper plane, the modeling predicts a $R_{\theta JA}$ of 52.5°C/W.

Adding a dog-bone copper area with four additional thermal vias in the dog-bone area to the first copper plane can improve $R_{\theta JA}$ to 45°C/W.

Layout Examples (continued)

See Application Note *AN-1520 A Guide to Board Layout for Best Thermal Resistance for Exposed Packages* (SNVA183) for additional thermal considerations for printed circuit board layouts.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

Application Note *AN-1520 A Guide to Board Layout for Best Thermal Resistance for Exposed Packages* (SNVA183).

11.1.2 Related Links

Table 2 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LP38500-ADJ	Click here	Click here	Click here	Click here	Click here
LP38502-ADJ	Click here	Click here	Click here	Click here	Click here

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP38500ASD-ADJ/NOPB	ACTIVE	WSON	NGS	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM		LKUA	Samples
LP38500ASDX-ADJ/NOPB	ACTIVE	WSON	NGS	8	4500	RoHS & Green	SN	Level-1-260C-UNLIM		LKUA	Samples
LP38500ATJ-ADJ/NOPB	ACTIVE	TO-263	NDQ	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM		LP38500 ATJ-ADJ	Samples
LP38500SD-ADJ/NOPB	ACTIVE	WSON	NGS	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LKUB	Samples
LP38500SDE-ADJ/NOPB	ACTIVE	WSON	NGS	8	250	RoHS & Green	SN	Level-1-260C-UNLIM		LKUB	Samples
LP38500SDX-ADJ/NOPB	ACTIVE	WSON	NGS	8	4500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LKUB	Samples
LP38500TJ-ADJ/NOPB	ACTIVE	TO-263	NDQ	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LP38500 TJ-ADJ	Samples
LP38500TS-ADJ/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	-40 to 125	LP38500 TS-ADJ	Samples
LP38500TSX-ADJ/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	-40 to 125	LP38500 TS-ADJ	Samples
LP38502ASD-ADJ/NOPB	ACTIVE	WSON	NGS	8	1000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LKVA	Samples
LP38502ASDX-ADJ/NOPB	ACTIVE	WSON	NGS	8	4500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LKVA	Samples
LP38502ATJ-ADJ/NOPB	ACTIVE	TO-263	NDQ	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LP38502A TJ-ADJ	Samples
LP38502SD-ADJ/NOPB	ACTIVE	WSON	NGS	8	1000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	LKVB	Samples
LP38502SDE-ADJ/NOPB	ACTIVE	WSON	NGS	8	250	RoHS & Green	SN	Level-1-260C-UNLIM		LKVB	Samples
LP38502SDX-ADJ/NOPB	ACTIVE	WSON	NGS	8	4500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LKVB	Samples
LP38502TJ-ADJ/NOPB	ACTIVE	TO-263	NDQ	5	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LP38502 TJ-ADJ	Samples
LP38502TS-ADJ/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	-40 to 125	LP38502 TS-ADJ	Samples
LP38502TSX-ADJ/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	RoHS-Exempt & Green	SN	Level-3-245C-168 HR	-40 to 125	LP38502 TS-ADJ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

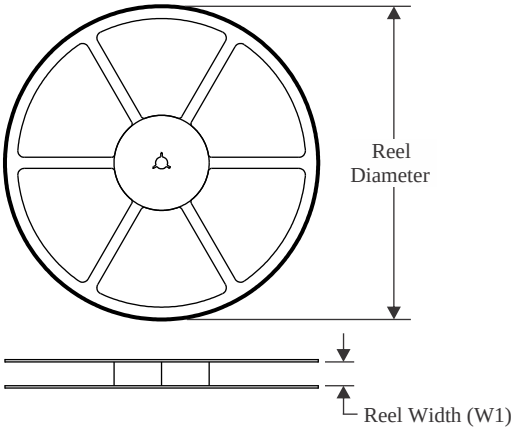
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

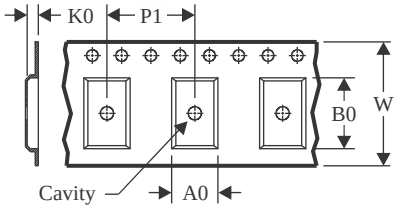
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

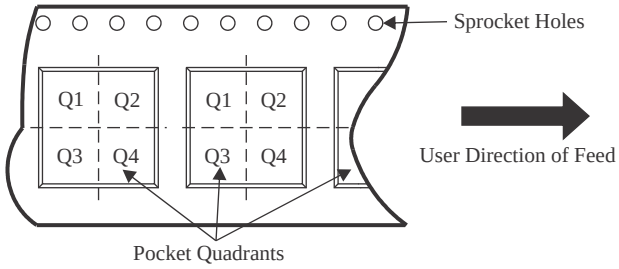


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

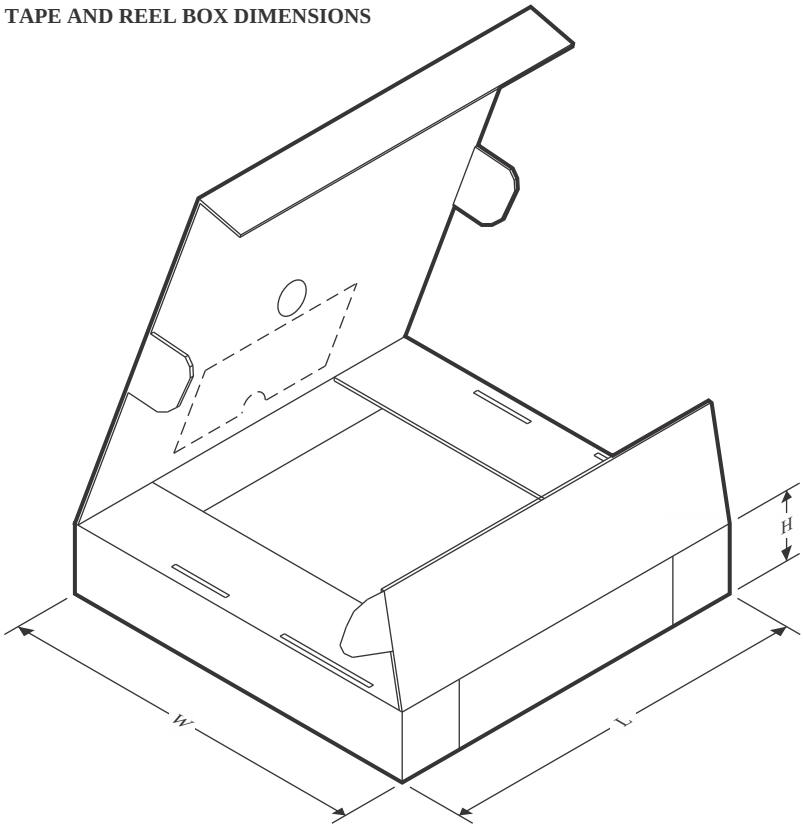


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP38500ASD-ADJ/NOPB	WSON	NGS	8	1000	178.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LP38500ASDX-ADJ/NOPB	WSON	NGS	8	4500	330.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LP38500ATJ-ADJ/NOPB	TO-263	NDQ	5	1000	330.0	24.4	10.6	15.4	2.45	12.0	24.0	Q2
LP38500SD-ADJ/NOPB	WSON	NGS	8	1000	178.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LP38500SDE-ADJ/NOPB	WSON	NGS	8	250	178.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LP38500SDX-ADJ/NOPB	WSON	NGS	8	4500	330.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LP38500TJ-ADJ/NOPB	TO-263	NDQ	5	1000	330.0	24.4	10.6	15.4	2.45	12.0	24.0	Q2
LP38500TSX-ADJ/NOPB	DDPAK/TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LP38502ASD-ADJ/NOPB	WSON	NGS	8	1000	178.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LP38502ASDX-ADJ/NOPB	WSON	NGS	8	4500	330.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LP38502ATJ-ADJ/NOPB	TO-263	NDQ	5	1000	330.0	24.4	10.6	15.4	2.45	12.0	24.0	Q2
LP38502SD-ADJ/NOPB	WSON	NGS	8	1000	178.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LP38502SDE-ADJ/NOPB	WSON	NGS	8	250	178.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1
LP38502SDX-ADJ/NOPB	WSON	NGS	8	4500	330.0	12.4	3.3	2.8	1.0	8.0	12.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP38502TJ-ADJ/NOPB	TO-263	NDQ	5	1000	330.0	24.4	10.6	15.4	2.45	12.0	24.0	Q2
LP38502TSX-ADJ/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2

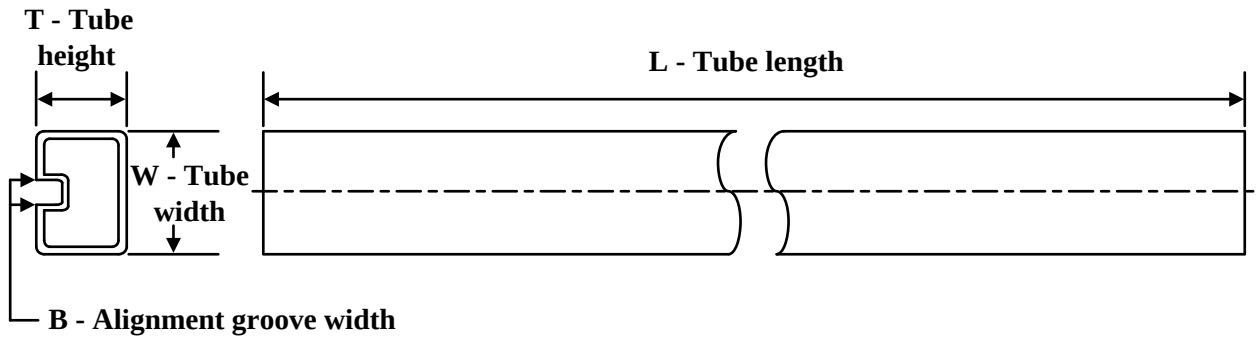
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP38500ASD-ADJ/NOPB	WSON	NGS	8	1000	208.0	191.0	35.0
LP38500ASDX-ADJ/NOPB	WSON	NGS	8	4500	367.0	367.0	35.0
LP38500ATJ-ADJ/NOPB	TO-263	NDQ	5	1000	367.0	367.0	35.0
LP38500SD-ADJ/NOPB	WSON	NGS	8	1000	208.0	191.0	35.0
LP38500SDE-ADJ/NOPB	WSON	NGS	8	250	208.0	191.0	35.0
LP38500SDX-ADJ/NOPB	WSON	NGS	8	4500	367.0	367.0	35.0
LP38500TJ-ADJ/NOPB	TO-263	NDQ	5	1000	367.0	367.0	35.0
LP38500TSX-ADJ/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LP38502ASD-ADJ/NOPB	WSON	NGS	8	1000	208.0	191.0	35.0
LP38502ASDX-ADJ/NOPB	WSON	NGS	8	4500	367.0	367.0	35.0
LP38502ATJ-ADJ/NOPB	TO-263	NDQ	5	1000	367.0	367.0	35.0
LP38502SD-ADJ/NOPB	WSON	NGS	8	1000	208.0	191.0	35.0
LP38502SDE-ADJ/NOPB	WSON	NGS	8	250	208.0	191.0	35.0
LP38502SDX-ADJ/NOPB	WSON	NGS	8	4500	367.0	367.0	35.0
LP38502TJ-ADJ/NOPB	TO-263	NDQ	5	1000	367.0	367.0	35.0
LP38502TSX-ADJ/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0

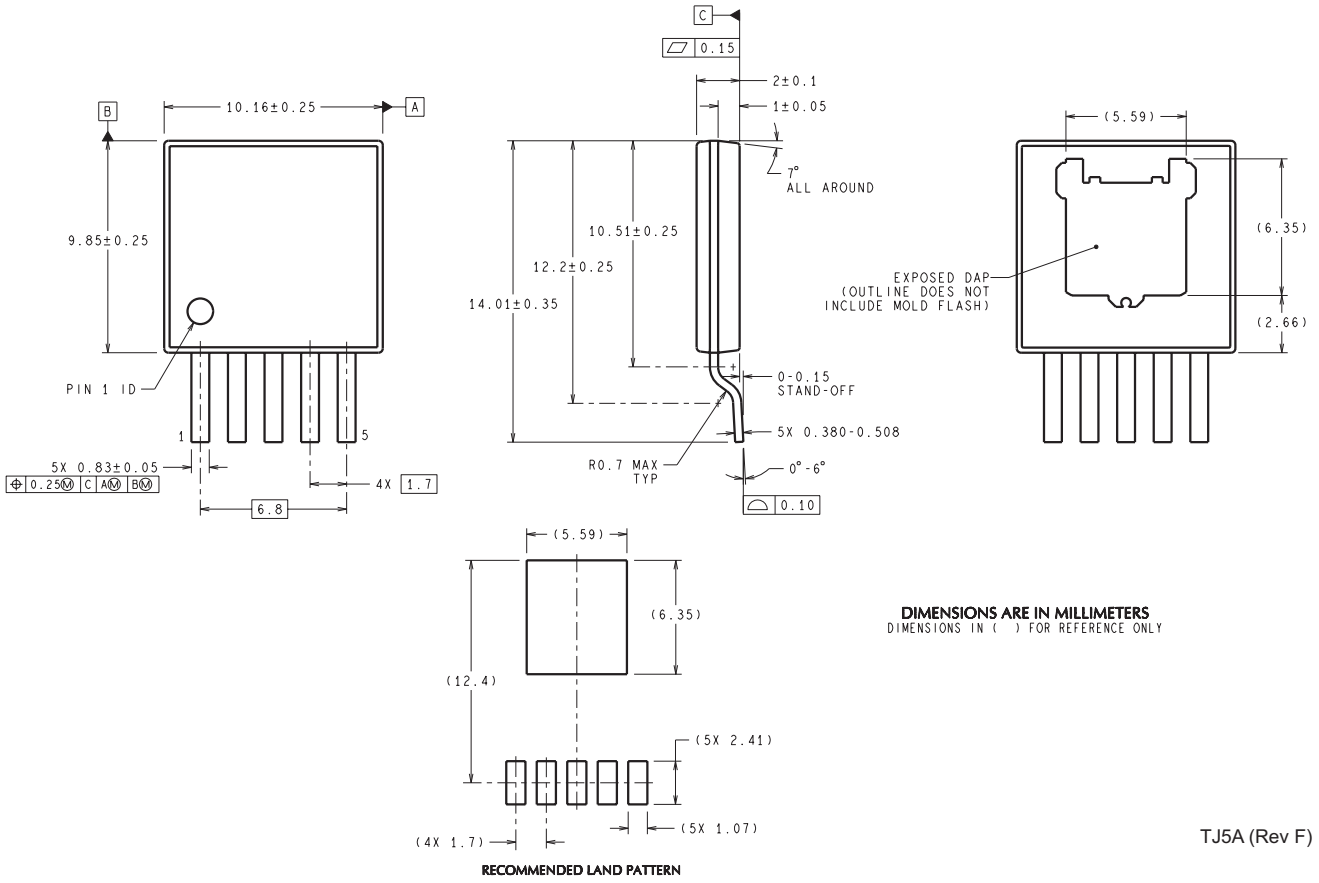
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LP38500TS-ADJ/NOPB	KTT	TO-263	5	45	502	25	8204.2	9.19
LP38502TS-ADJ/NOPB	KTT	TO-263	5	45	502	25	8204.2	9.19

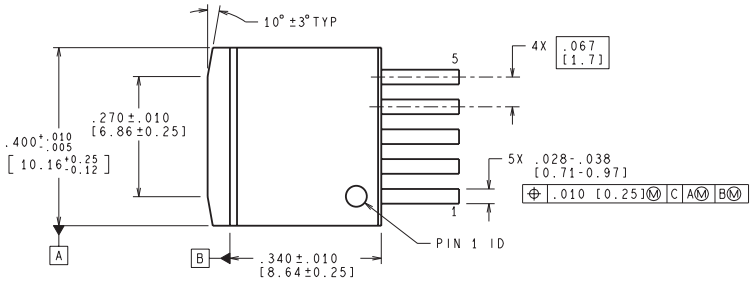
NDQ0005A

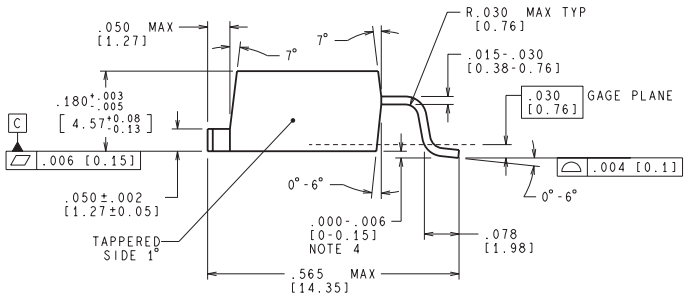


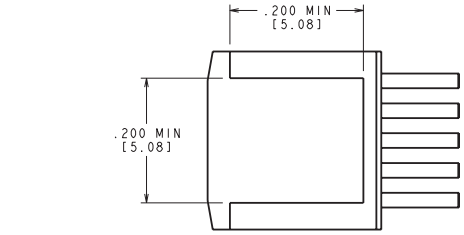
DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

TJ5A (Rev F)

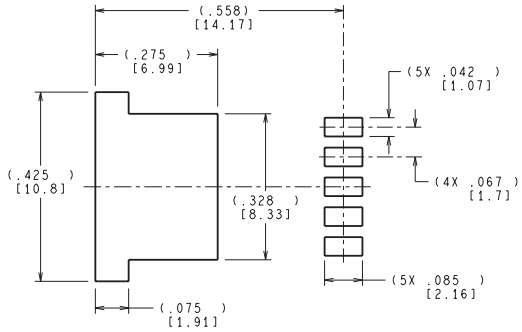
KTT0005B







BOTTOM SIDE OF PACKAGE

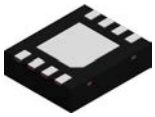


LAND PATTERN RECOMMENDATION

CONTROLLING DIMENSION IS INCH
VALUES IN [ ] ARE MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

TS5B (Rev D)

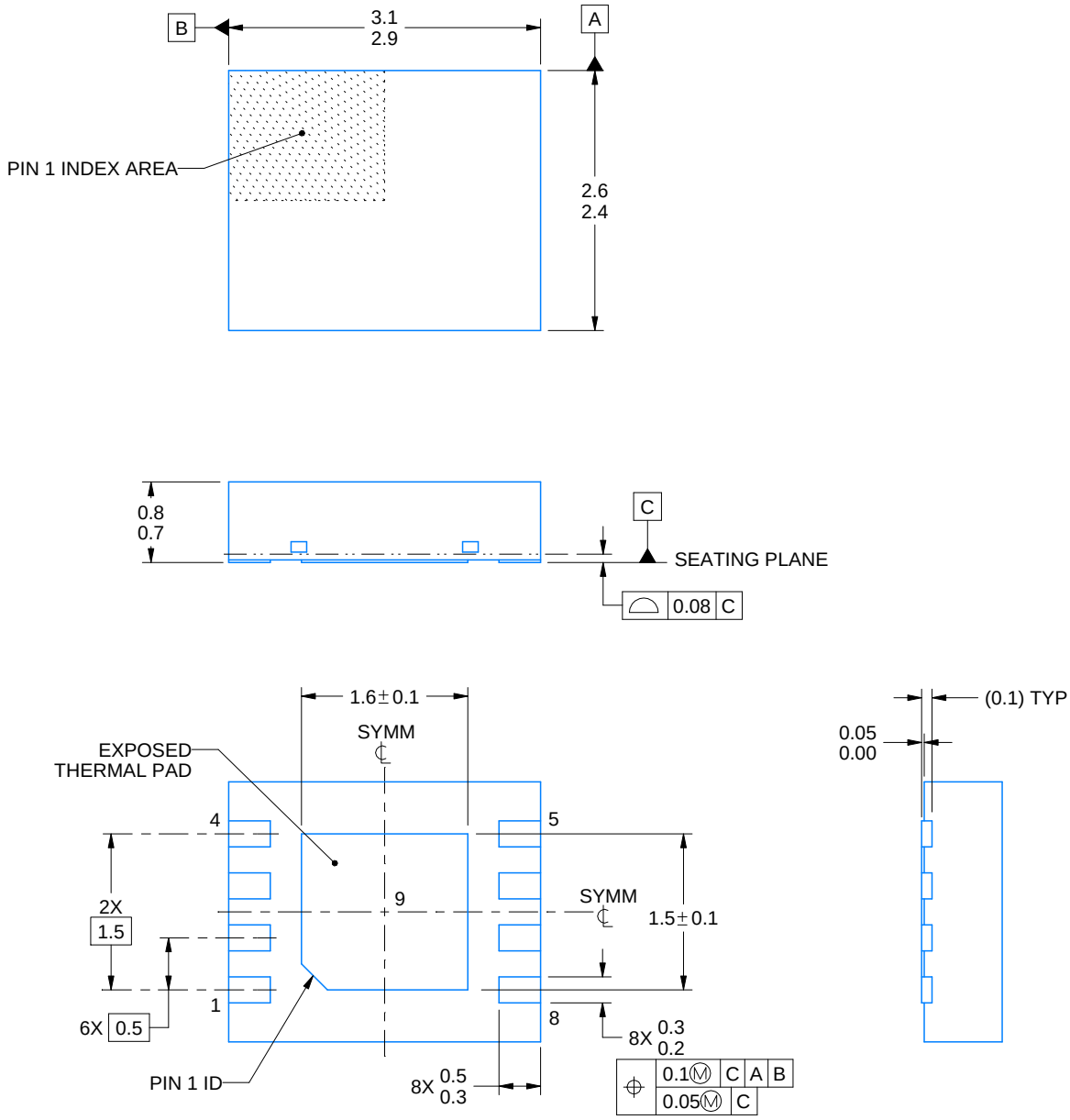
NGS0008C



PACKAGE OUTLINE

WSON - 0.8 mm max height

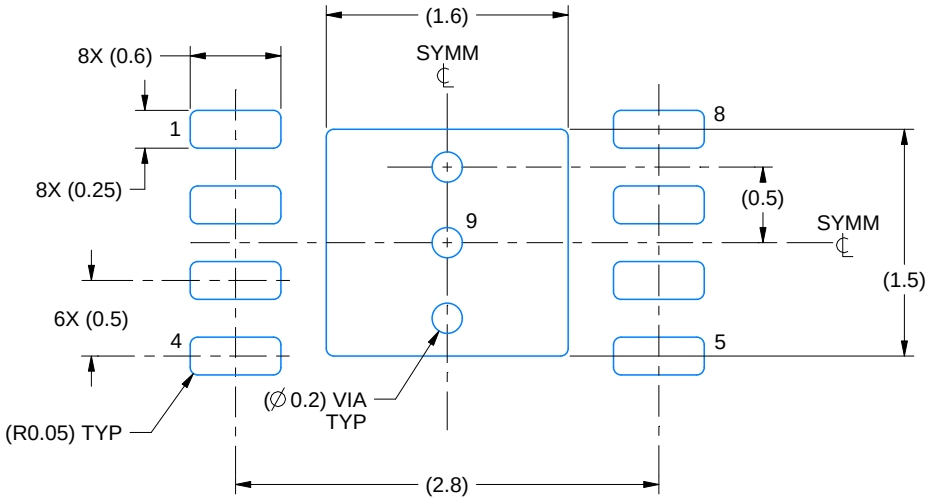
PLASTIC SMALL OUTLINE - NO LEAD



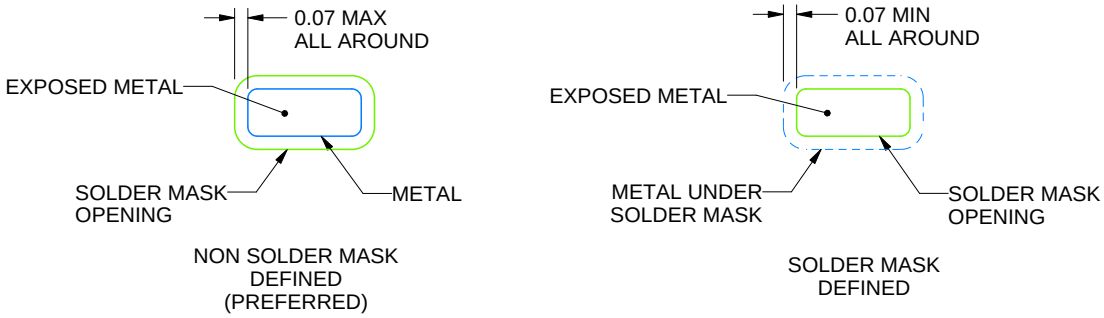
4214924/A 07/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

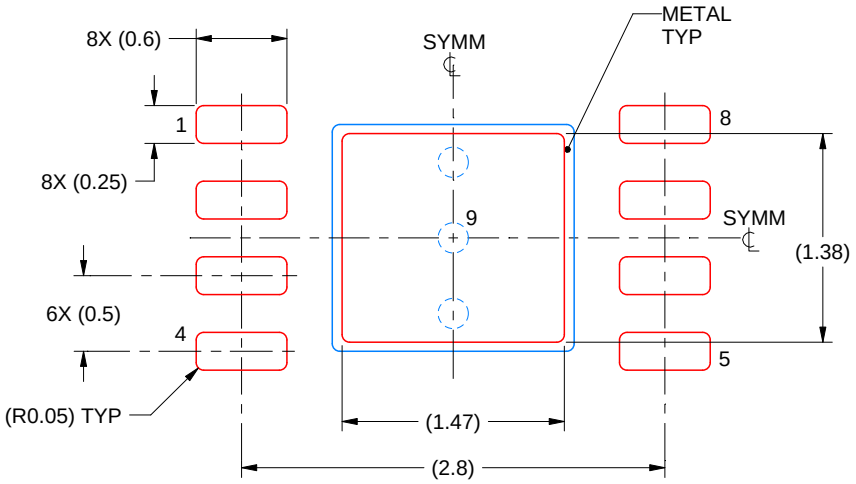


SOLDER MASK DETAILS

4214924/A 07/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 9:
82% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4214924/A 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265