

## 3-V TO 5.5-V MULTICHANNEL RS-232 LINE DRIVER/RECEIVER WITH $\pm 15$ -kV ESD PROTECTION

Check for Samples: [MAX3223E](#)

### FEATURES

- **ESD Protection for RS-232 Bus Pins**
  - $\pm 15$ -kV Human-Body Model (HBM)
  - $\pm 8$ -kV IEC61000-4-2, Contact Discharge
  - $\pm 15$ -kV IEC61000-4-2, Air-Gap Discharge
- **Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU v.28 Standards**
- **Operates With 3-V to 5.5-V  $V_{CC}$  Supply**
- **Operates up to 500 kbit/s**
- **Two Drivers and Two Receivers**
- **Low Standby Current . . . 1  $\mu$ A Typ**
- **External Capacitors . . . 4  $\times$  0.1  $\mu$ F**
- **Accepts 5-V Logic Input With 3.3-V Supply**
- **Alternative High-Speed Pin-Compatible Device (1 Mbit/s) for SNx5C3223E**

### APPLICATIONS

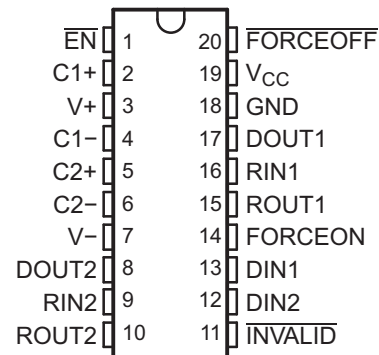
- **Battery-Powered Systems**
- **PDA's**
- **Notebooks**
- **Laptops**
- **Palmtop PCs**
- **Hand-Held Equipment**

### DESCRIPTION/ORDERING INFORMATION

The MAX3223E consists of two line drivers, two line receivers, and a dual charge-pump circuit with  $\pm 15$ -kV ESD protection pin to pin (serial-port connection pins, including GND). The device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The device operates at typical data signaling rates up to 500 kbit/s and a maximum of 30-V/ $\mu$ s driver output slew rate.

Flexible control options for power management are available when the serial port is inactive. The auto-powerdown feature functions when FORCEON is low and FORCEOFF is high. During this mode of operation, if the device does not sense a valid RS-232 signal, the driver outputs are disabled. If FORCEOFF is set low and EN is high, both drivers and receivers are shut off, and the supply current is reduced to 1 mA. Disconnecting the serial port or turning off the peripheral drivers causes auto-powerdown to occur. Auto-powerdown can be disabled when FORCEON and FORCEOFF are high. With auto-powerdown enabled, the device is activated automatically when a valid signal is applied to any receiver input. The INVALID output is used to notify the user if an RS-232 signal is present at any receiver input. INVALID is high (valid data) if any receiver input voltage is greater than 2.7 V or less than  $-2.7$  V, or has been between  $-0.3$  V and 0.3 V for less than 30  $\mu$ s. INVALID is low (invalid data) if the receiver input voltage is between  $-0.3$  V and 0.3 V for more than 30  $\mu$ s. Refer to [Figure 4](#) for receiver input levels.

DB, DW, OR PW PACKAGE  
(TOP VIEW)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

**Table 1. ORDERING INFORMATION**

T <sub>A</sub>	PACKAGE <sup>(1)</sup> <sup>(2)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–0°C to 70°C	SOIC – DW	Tube of 25	MAX3223ECDW
		Reel of 2000	MAX3223ECDWR
	SSOP – DB	Tube of 70	MAX3223ECDB
		Reel of 2000	MAX3223ECDBR
	TSSOP – PW	Tube of 70	MAX3223ECPW
		Reel of 2000	MAX3223ECPWR
–40°C to 85°C	SOIC – DW	Tube of 25	MAX3223EIDW
		Reel of 2000	MAX3223EIDWR
	SSOP – DB	Tube of 70	MAX3223EIDB
		Reel of 2000	MAX3223EIDBR
	TSSOP – PW	Tube of 70	MAX3223EIPW
		Reel of 2000	MAX3223EIPWR

(1) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

**FUNCTION TABLES**
**EACH DRIVER<sup>(1)</sup>**

INPUTS				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	FORCEOFF	VALID RIN RS-232 LEVEL		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-powerdown enabled
H	L	H	Yes	L	
L	L	H	No	Z	Powered off by auto-powerdown feature
H	L	H	No	Z	

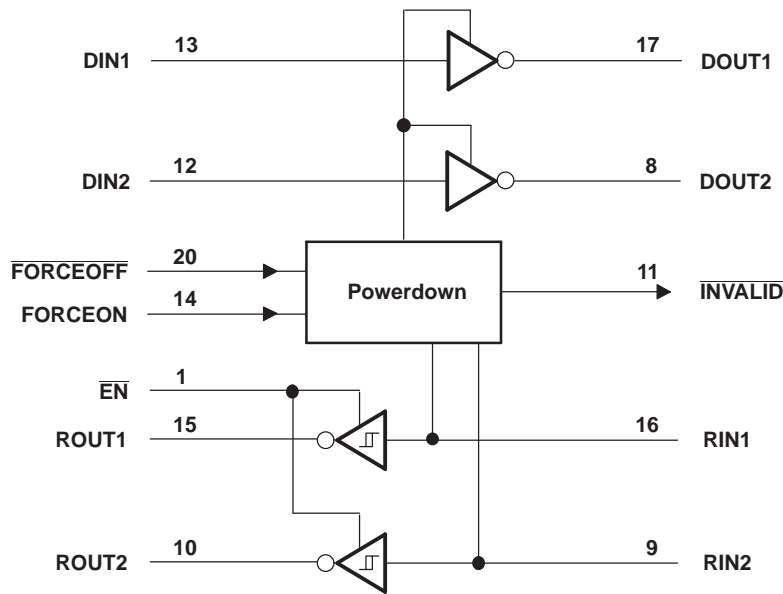
(1) H = high level, L = low level, X = irrelevant, Z = high impedance

**EACH RECEIVER<sup>(1)</sup>**

INPUTS			OUTPUT DOUT
RIN	$\overline{\text{EN}}$	VALID RIN RS-232 LEVEL	
L	L	X	H
H	L	X	L
X	H	X	Z
Open	L	No	H

(1) H = high level, L = low level, X = irrelevant,  
Z = high impedance (off),  
Open = input disconnected or connected driver off

**LOGIC DIAGRAM (POSITIVE LOGIC)**



Pin numbers are for the DB, DW, and PW packages.

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.3	6	V
V <sub>+</sub>	Positive-output supply voltage range <sup>(2)</sup>	-0.3	7	V
V <sub>-</sub>	Negative-output supply voltage range <sup>(2)</sup>	0.3	-7	V
V <sub>+</sub> – V <sub>-</sub>	Supply voltage difference <sup>(2)</sup>		13	V
V <sub>I</sub>	Input voltage range	Driver (FORCEOFF, FORCEON, EN)		V
		Receiver		
V <sub>O</sub>	Output voltage range	Driver		V
		Receiver (INVALID)		
θ <sub>JA</sub>	Package thermal impedance <sup>(3) (4)</sup>	DB package		°C/W
		DW package		
		PW package		
T <sub>J</sub>	Operating virtual junction temperature		150	°C
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.
- (3) Maximum power dissipation is a function of T<sub>J(max)</sub>, θ<sub>JA</sub>, and T<sub>A</sub>. The maximum allowable power dissipation at any allowable ambient temperature is P<sub>D</sub> = (T<sub>J(max)</sub> – T<sub>A</sub>)/θ<sub>JA</sub>. Operating at the absolute maximum T<sub>J</sub> of 150°C can affect reliability.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

**RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>**

 See [Figure 6](#)

			MIN	NOM	MAX	UNIT	
Supply voltage		$V_{CC} = 3.3\text{ V}$	3	3.3	3.6	V	
		$V_{CC} = 5\text{ V}$	4.5	5	5.5		
$V_{IH}$	Driver and control high-level input voltage	DIN, $\overline{EN}$ , $\overline{FORCEOFF}$ , FORCEON	$V_{CC} = 3.3\text{ V}$	2		V	
			$V_{CC} = 5\text{ V}$	2.4			
$V_{IL}$	Driver and control low-level input voltage	DIN, $\overline{EN}$ , $\overline{FORCEOFF}$ , FORCEON			0.8	V	
$V_I$	Driver and control input voltage	DIN, $\overline{EN}$ , $\overline{FORCEOFF}$ , FORCEON	0		5.5	V	
	Receiver input voltage		-25		25	V	
$T_A$	Operating free-air temperature		MAX3223EC	0		70	°C
			MAX3223EI	-40		85	

(1) Test conditions are C1–C4 = 0.1  $\mu\text{F}$  at  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ; C1 = 0.047  $\mu\text{F}$ , C2–C4 = 0.33  $\mu\text{F}$  at  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .

**ELECTRICAL CHARACTERISTICS<sup>(1)</sup>**

 over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT	
$I_i$	Input leakage current	$\overline{EN}$ , $\overline{FORCEOFF}$ , FORCEON		$\pm 0.01$	$\pm 1$	$\mu\text{A}$	
$I_{CC}$	Supply current	Auto-powerdown disabled	$V_{CC} = 3.3\text{ V}$ or $5\text{ V}$ , $T_A = 25^\circ\text{C}$ , No load, $\overline{FORCEOFF}$ and FORCEON at $V_{CC}$		0.3	1	mA
		Powered off	No load, $\overline{FORCEOFF}$ at GND		1	10	$\mu\text{A}$
		Auto-powerdown enabled	No load, $\overline{FORCEOFF}$ at $V_{CC}$ , FORCEON at GND, All RIN are open or grounded		1	10	

(1) Test conditions are C1–C4 = 0.1  $\mu\text{F}$  at  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ ; C1 = 0.047  $\mu\text{F}$ , C2–C4 = 0.33  $\mu\text{F}$  at  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .

(2) All typical values are at  $V_{CC} = 3.3\text{ V}$  or  $V_{CC} = 5\text{ V}$ , and  $T_A = 25^\circ\text{C}$ .

## DRIVER SECTION

### Electrical Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	DOOUT at R <sub>L</sub> = 3 kΩ to GND	5	5.4		V
V <sub>OL</sub>	Low-level output voltage	DOOUT at R <sub>L</sub> = 3 kΩ to GND	–5	–5.4		V
I <sub>IH</sub>	High-level input current	V <sub>I</sub> = V <sub>CC</sub>		±0.01	±1	μA
I <sub>IL</sub>	Low-level input current	V <sub>I</sub> at GND		±0.01	±1	μA
I <sub>OS</sub>	Short-circuit output current <sup>(3)</sup>	V <sub>CC</sub> = 3.6 V, V <sub>O</sub> = 0 V		±35	±60	mA
		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0 V				
r <sub>o</sub>	Output resistance	V <sub>CC</sub> , V <sub>+</sub> , and V <sub>–</sub> = 0 V, V <sub>O</sub> = ±2 V	300	10M		Ω
I <sub>oZ</sub>	Output leakage current	FORCEOFF = GND, V <sub>CC</sub> = 3 V to 3.6 V, V <sub>O</sub> = ±12 V			±25	μA
		FORCEOFF = GND, V <sub>CC</sub> = 4.5 V to 5.5 V, V <sub>O</sub> = ±12 V			±25	

(1) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(3) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

### Switching Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT
	Maximum data rate	C <sub>L</sub> = 1000 pF, One DOOUT switching, R <sub>L</sub> = 3 kΩ, See <a href="#">Figure 1</a>	250	500		kbit/s
t <sub>sk(p)</sub>	Pulse skew <sup>(3)</sup>	C <sub>L</sub> = 150 pF to 2500 pF, See <a href="#">Figure 2</a>		100		ns
SR(tr)	Slew rate, transition region (See <a href="#">Figure 1</a> )	R <sub>L</sub> = 3 kΩ to 7 kΩ, V <sub>CC</sub> = 3.3 V	C <sub>L</sub> = 150 pF to 1000 pF	6	30	V/μs
			C <sub>L</sub> = 150 pF to 2500 pF	4	30	

(1) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(3) Pulse skew is defined as |t<sub>PLH</sub> – t<sub>PHL</sub>| of each channel of the same device.

### ESD Protection

		TYP	UNIT
Driver outputs (DOOUTx)	Human-Body Model (HBM)	±15	kV
	IEC61000-4-2, Air-Gap Discharge	±15	
	IEC61000-4-2, Contact Discharge	±8	

## RECEIVER SECTION

### Electrical Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 6](#))

PARAMETER	TEST CONDITIONS	MIN	TYP <sup>(2)</sup>	MAX	UNIT
V <sub>OH</sub> High-level output voltage	I <sub>OH</sub> = -1 mA	V <sub>CC</sub> - 0.6	V <sub>CC</sub> - 0.1		V
V <sub>OL</sub> Low-level output voltage	I <sub>OL</sub> = 1.6 mA			0.4	V
V <sub>IT+</sub> Positive-going input threshold voltage	V <sub>CC</sub> = 3.3 V		1.6	2.4	V
	V <sub>CC</sub> = 5 V		1.9	2.4	
V <sub>IT-</sub> Negative-going input threshold voltage	V <sub>CC</sub> = 3.3 V	0.6	1.1		V
	V <sub>CC</sub> = 5 V	0.6	1.4		
V <sub>hys</sub> Input hysteresis (V <sub>IT+</sub> - V <sub>IT-</sub> )			0.5		V
I <sub>OZ</sub> Output leakage current	$\overline{EN} = V_{CC}$		±0.05		µA
r <sub>i</sub> Input resistance	V <sub>I</sub> = ±3 V to ±25 V	3	5		kΩ

(1) Test conditions are C1–C4 = 0.1 µF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V<sub>CC</sub> = 5 V ± 0.5 V.

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

### Switching Characteristics<sup>(1)</sup>

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP <sup>(2)</sup>	UNIT
t <sub>PLH</sub> Propagation delay time, low- to high-level output	C <sub>L</sub> = 150 pF, See <a href="#">Figure 3</a>	150	ns
t <sub>PHL</sub> Propagation delay time, high- to low-level output	C <sub>L</sub> = 150 pF, See <a href="#">Figure 3</a>	150	ns
t <sub>en</sub> Output enable time	C <sub>L</sub> = 150 pF, R <sub>L</sub> = 3 kΩ, See <a href="#">Figure 4</a>	200	ns
t <sub>dis</sub> Output disable time	C <sub>L</sub> = 150 pF, R <sub>L</sub> = 3 kΩ, See <a href="#">Figure 4</a>	200	ns
t <sub>sk(p)</sub> Pulse skew <sup>(3)</sup>	See <a href="#">Figure 3</a>	50	ns

(1) Test conditions are C1–C4 = 0.1 µF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V<sub>CC</sub> = 5 V ± 0.5 V.

(2) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(3) Pulse skew is defined as |t<sub>PLH</sub> - t<sub>PHL</sub>| of each channel of the same device.

### ESD Protection

		TYP	UNIT
Receiver inputs (RINx)	Human-Body Model (HBM)	±15	kV
	IEC61000-4-2, Air-Gap Discharge	±15	
	IEC61000-4-2, Contact Discharge	±8	

## AUTO-POWERDOWN SECTION

### Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$V_{T+(valid)}$	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND,	$\overline{FORCEOFF} = V_{CC}$		2.7	V
$V_{T(valid)}$	Receiver input threshold for $\overline{INVALID}$ high-level output voltage	FORCEON = GND,	$\overline{FORCEOFF} = V_{CC}$	-2.7		V
$V_{T(invalid)}$	Receiver input threshold for $\overline{INVALID}$ low-level output voltage	FORCEON = GND,	$\overline{FORCEOFF} = V_{CC}$	-0.3	0.3	V
$V_{OH}$	$\overline{INVALID}$ high-level output voltage	$I_{OH} = 1\text{ mA}$ , $\overline{FORCEOFF} = V_{CC}$	FORCEON = GND,	$V_{CC} - 0.6$		V
$V_{OL}$	$\overline{INVALID}$ low-level output voltage	$I_{OL} = 1.6\text{ mA}$ , $\overline{FORCEOFF} = V_{CC}$	FORCEON = GND,		0.4	V

### Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5](#))

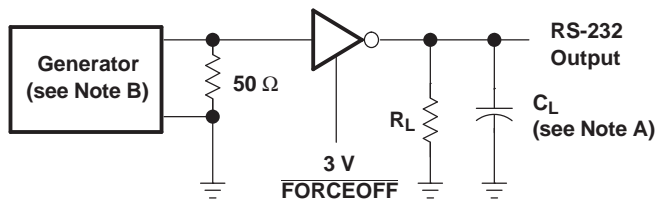
PARAMETER		TYP <sup>(1)</sup>	UNIT
$t_{valid}$	Propagation delay time, low- to high-level output	1	$\mu\text{s}$
$t_{invalid}$	Propagation delay time, high- to low-level output	30	$\mu\text{s}$
$t_{en}$	Supply enable time	100	$\mu\text{s}$

(1) All typical values are at  $V_{CC} = 3.3\text{ V}$  or  $V_{CC} = 5\text{ V}$ , and  $T_A = 25^\circ\text{C}$ .

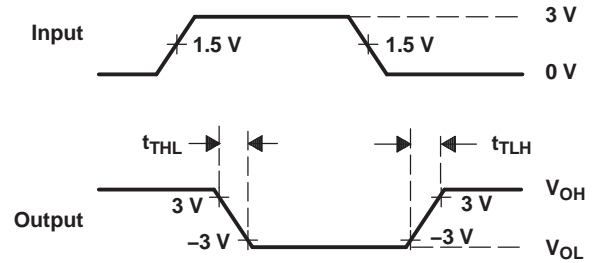


## PARAMETER MEASUREMENT INFORMATION

- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns.



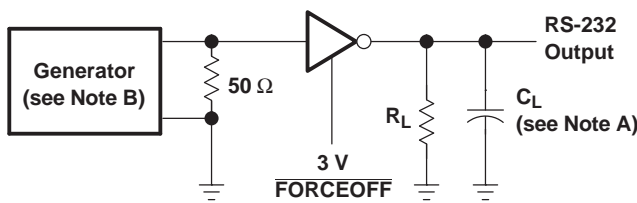
TEST CIRCUIT



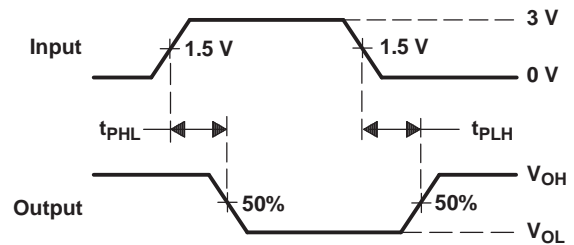
VOLTAGE WAVEFORMS

$$SR(tr) = \frac{6V}{t_{THL} \text{ or } t_{TLH}}$$

- C.  $C_L$  includes probe and jig capacitance.
- D. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns.

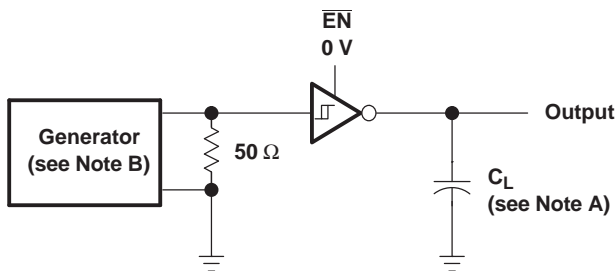


TEST CIRCUIT

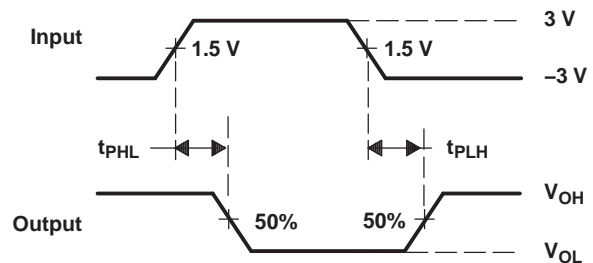


VOLTAGE WAVEFORMS

- E.  $C_L$  includes probe and jig capacitance.
- F. The pulse generator has the following characteristics:  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns.



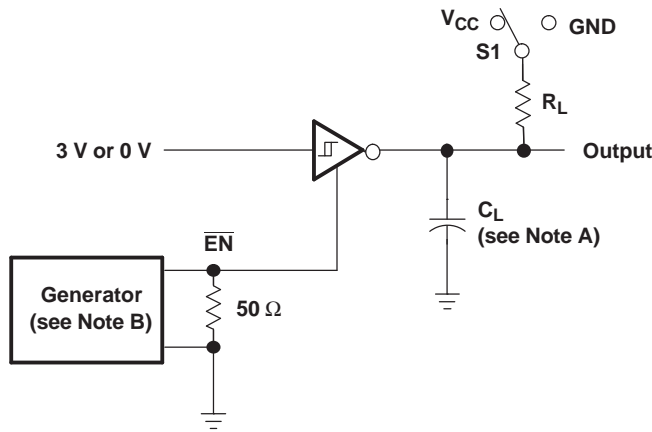
TEST CIRCUIT



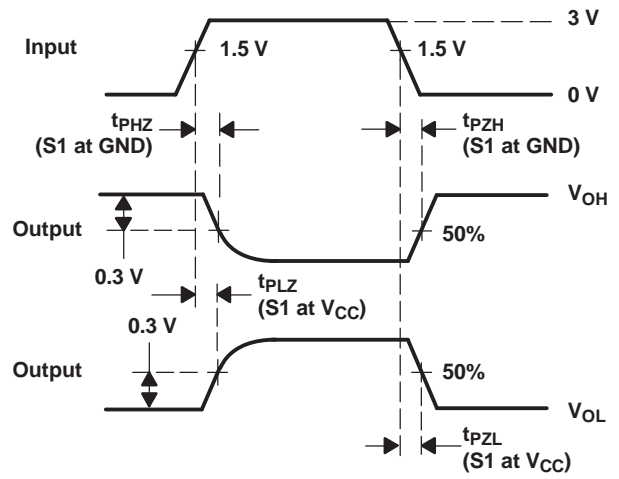
VOLTAGE WAVEFORMS

- G.  $C_L$  includes probe and jig capacitance.
- H. The pulse generator has the following characteristics:  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns.

**PARAMETER MEASUREMENT INFORMATION (continued)**



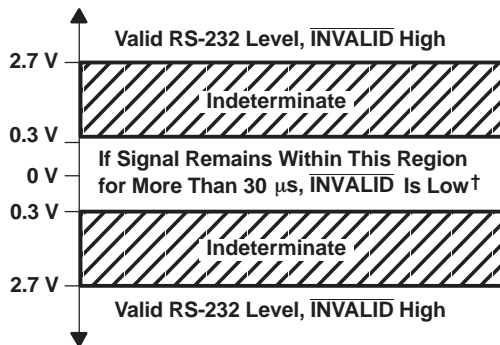
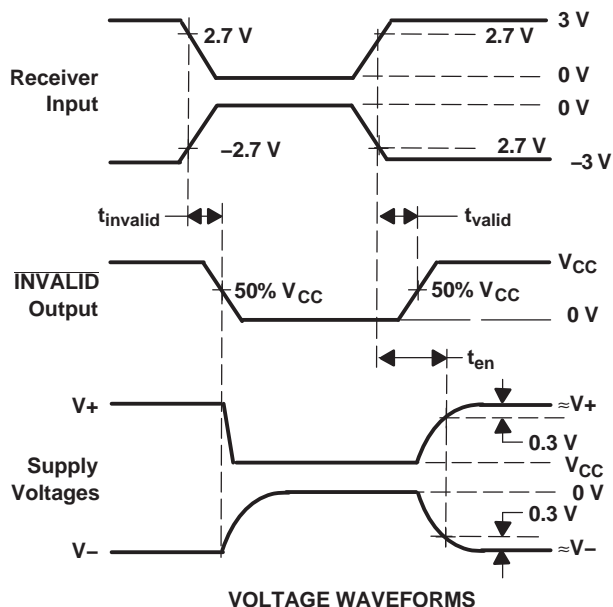
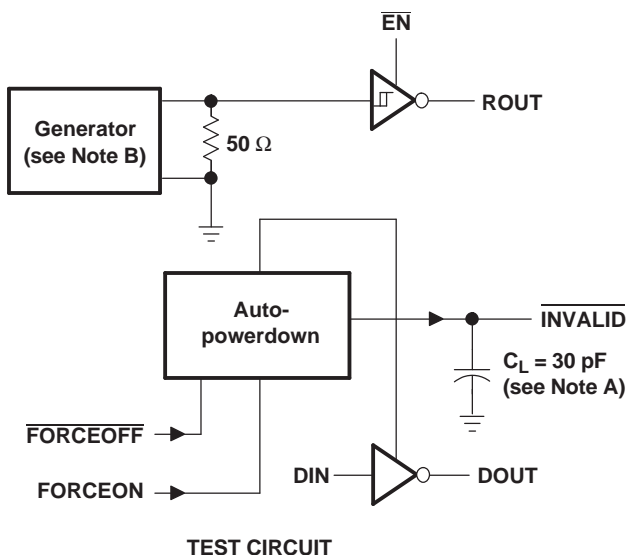
**TEST CIRCUIT**



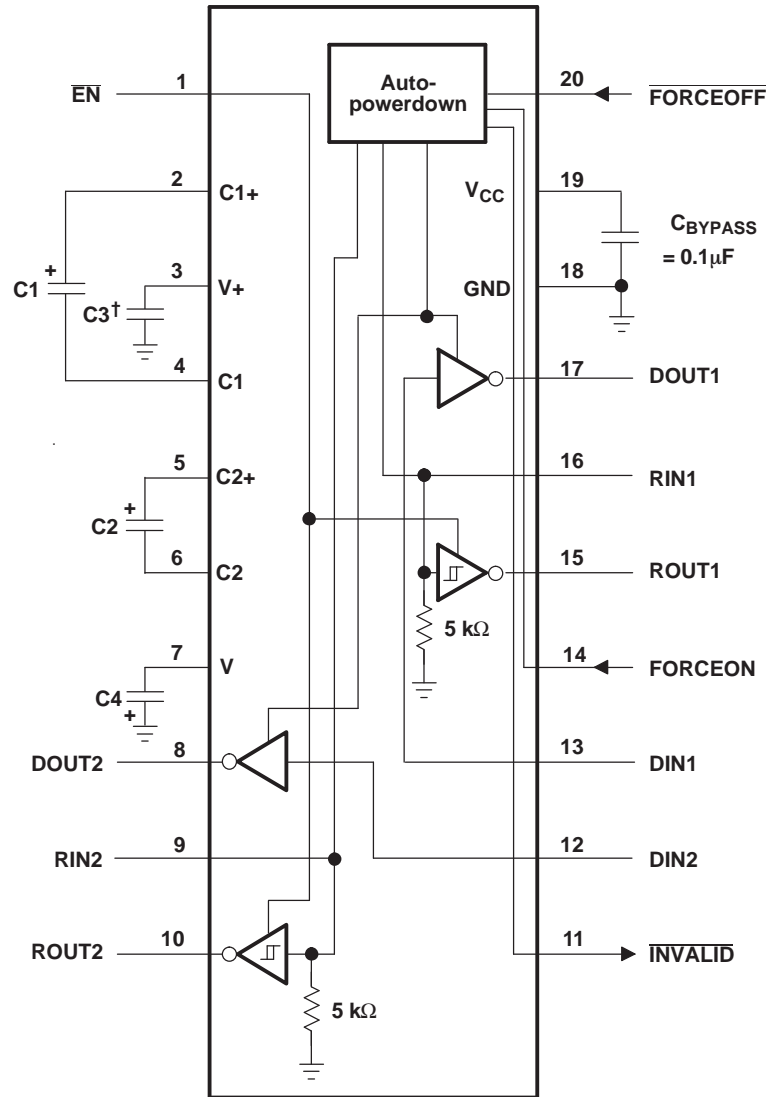
**VOLTAGE WAVEFORMS**

- I.  $C_L$  includes probe and jig capacitance.
- J. The pulse generator has the following characteristics: PRR = 250 kbit/s,  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10$  ns,  $t_f \leq 10$  ns.

PARAMETER MEASUREMENT INFORMATION (continued)



APPLICATION INFORMATION



† C3 can be connected to V<sub>CC</sub> or GND.

NOTES: A. Resistor values shown are nominal.

B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V<sub>CC</sub> vs CAPACITOR VALUES

V <sub>CC</sub>	C1	C2, C3, and C4
3.3 V ± 0.3 V	0.1 μF	0.1 μF
5 V ± 0.5 V	0.047 μF	0.33 μF
3 V to 5.5 V	0.1 μF	0.47 μF

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MAX3223ECDB	LIFEBUY	SSOP	DB	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP223EC	
MAX3223ECDBR	LIFEBUY	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP223EC	
MAX3223ECDW	LIFEBUY	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3223EC	
MAX3223ECDWR	LIFEBUY	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MAX3223EC	
MAX3223ECPW	LIFEBUY	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP223EC	
MAX3223ECPWG4	LIFEBUY	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP223EC	
MAX3223ECPWR	LIFEBUY	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	MP223EC	
MAX3223EIDB	LIFEBUY	SSOP	DB	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP223EI	
MAX3223EIDBG4	LIFEBUY	SSOP	DB	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP223EI	
MAX3223EIDBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP223EI	Samples
MAX3223EIDW	LIFEBUY	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3223EI	
MAX3223EIDWR	LIFEBUY	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MAX3223EI	
MAX3223EIPW	LIFEBUY	TSSOP	PW	20	70	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP223EI	
MAX3223EIPWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	MP223EI	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MAX3223ECDBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
MAX3223ECDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
MAX3223ECPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
MAX3223EIDBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
MAX3223EIDWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
MAX3223EIPWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MAX3223ECDBR	SSOP	DB	20	2000	356.0	356.0	35.0
MAX3223ECDWR	SOIC	DW	20	2000	367.0	367.0	45.0
MAX3223ECPWR	TSSOP	PW	20	2000	356.0	356.0	35.0
MAX3223EIDBR	SSOP	DB	20	2000	356.0	356.0	35.0
MAX3223EIDWR	SOIC	DW	20	2000	367.0	367.0	45.0
MAX3223EIPWR	TSSOP	PW	20	2000	356.0	356.0	35.0



**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
MAX3223ECDB	DB	SSOP	20	70	530	10.5	4000	4.1
MAX3223ECDW	DW	SOIC	20	25	507	12.83	5080	6.6
MAX3223ECPW	PW	TSSOP	20	70	530	10.2	3600	3.5
MAX3223ECPWG4	PW	TSSOP	20	70	530	10.2	3600	3.5
MAX3223EIDB	DB	SSOP	20	70	530	10.5	4000	4.1
MAX3223EIDBG4	DB	SSOP	20	70	530	10.5	4000	4.1
MAX3223EIDW	DW	SOIC	20	25	507	12.83	5080	6.6
MAX3223EIPW	PW	TSSOP	20	70	530	10.2	3600	3.5

# DB0020A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PW0020A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

### NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153.



# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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