OPA1632 高性能、全差分音频运算放大器

1 特性

- 出色音质
- 超低失真：0.000028%
- 低噪声：1.25nV/ √Hz
- 高速：
  - 压摆率：72V/ μs
  - 增益带宽积：180 MHz
- 完全差分架构：
  - 平衡输入和输出将单端输入转换为平衡差分输出
- 宽电源电压范围：±2.5V 至 ±15V
- 关断电流：0.85mA (V_S = ± 5V)
- 温度范围：–40°C 至 +85°C

2 应用

- 专业音频混合器或控制平面
- 专业麦克风和无线系统
- 专业扬声器系统
- 专业音频放大器
- 条形音箱
- 转盘
- 专业摄像机
- 吉他和其他乐器放大器
- 数据采集 (DAQ)

3 说明

OPA1632 是一款全差分放大器，旨在驱动高性能音频模数转换器 (ADC) 或用作 D 类放大器的前置驱动器。它可实现卓越的音频质量、极低的噪声、大输出电压摆幅和高电流驱动。OPA1632 具有 180MHz 的出色增益带宽以及 72V/ μs 的超快压摆率，可实现极低的失真。非常低的输入电压噪声 1.25nV/ √Hz 可进一步确保更大信噪比和动态范围。

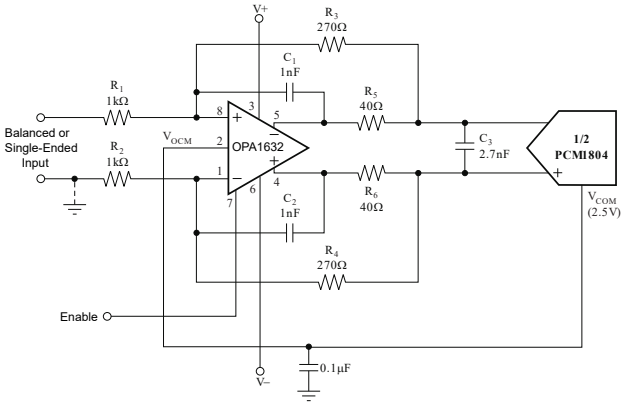
全差分架构的灵活性有助于轻松实现单端到全差分输出转换。差分输出可减少偶次谐波并最大限度地减少共模噪声干扰。OPA1632 在用于驱动高性能音频 ADC（如 PCM1804）时可提供卓越的性能。添加了关断功能以在器件未使用时节省电量。

OPA1632 可在 –40°C 至 +85°C 的温度范围内正常运行，采用 SO-8 封装和散热增强型 MSOP-8 PowerPAD™ 封装。

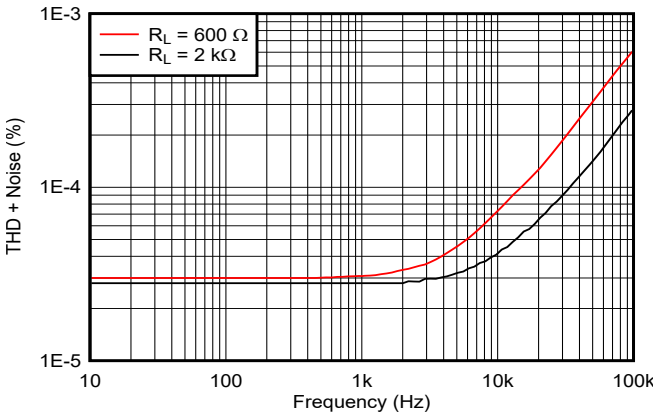
器件信息(1)

器件型号	封装	封装尺寸（标称值）
OPA1632	SOIC (8)	4.90mm × 3.91mm
	MSOP-PowerPAD (8)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



应用示意图



THD+N 与频率间的关系

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

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• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• 更新了*特性* 部分	1
• 更新了*应用* 部分	1
• 更新了*说明* 部分	1
• 更改了*说明* 部分中 SOIC 和 MSOP-PowerPAD 封装的标称封装尺寸	1
• Updated *Pin Configuration and Functions* section	5
• Added Supply turn-on/off dV/dT specification to *Absolute Maximum Ratings* table	6
• Added continuous input current specification to *Absolute Maximum Ratings* table	6
• Changed differential input voltage in *Absolute Maximum Ratings* table from ±3V to ±1.5V	6
• Changed charged-device model (CDM) reference from JESD22-C101 to JS-002 in *ESD Ratings* table	6
• Changed minimum temperature range from 0.4℃ to -40℃ in *Recommended Operating Conditions* table	6
• Updated thermal specifications for D package in *Thermal Information* table	7
• Changed typical offset voltage vs temperature from ±5 μV°C to ± 2.5 μV°C in *Electrical Characteristics: OPA1632D* table	8
• Changed PSRR minimum limit of 316 μV/V to maximum limit in *Electrical Characteristics: OPA1632D table*	8
• Changed typical input bias current limit from 2μA to 7.9μA in *Electrical Characteristics: OPA1632D* table	8
• Changed Max input bias current limit from 6μA to 14μA in *Electrical Characteristics: OPA1632D* table	8
• Changed typical input voltage noise from 1.3nV/ √Hz to 1.25nV/ √Hz in Electrical Characteristics: OPA1632D table	8
• Changed typical input current noise from 0.4 pA/ √Hz to 1.7 pA/ √Hz in *Electrical Characteristics: OPA1632D* table	8
• Changed input impedance spec to show both common-mode and differential impedances in *Electrical Characteristics: OPA1632D* table	8
• Changed SSBW at G = +2, R_F = 602 Ω from 90 MHz to 104 MHz in *Electrical Characteristics: OPA1632D* table	8

- Changed SSBW at G = +5, R_F = 1.5 kΩ from 36 MHz to 46 MHz in *Electrical Characteristics: OPA1632D* table....8
- Changed SSBW at G = +5, R_F = 1.5 kΩ from 18 MHz to 24 MHz in *Electrical Characteristics: OPA1632D* table....8
- Changed typical Large-Signal Bandwidth from 800 kHz to 1.8 MHz in *Electrical Characteristics: OPA1632D* table....8
- Changed typical slew rate from 50 V/μs to 72 V/μs in *Electrical Characteristics: OPA1632D* table....8
- Changed typical rise/fall time from 100 ns to 69 ns in *Electrical Characteristics: OPA1632D* table....8
- Changed typical settling time to 0.1% from 75 ns to 36 ns in *Electrical Characteristics: OPA1632D* table....8
- Changed typical settling time to 0.01% from 200 ns to 49ns in *Electrical Characteristics: OPA1632D* table....8
- Changed typical THD+N with Differential Input/Output and R_L = 600 Ω from 0.0003% to 0.00003% in *Electrical Characteristics: OPA1632D* table....8
- Changed typical THD+N with Differential Input/Output and R_L = 2kΩ from 0.000022% to 0.000028% *in Electrical Characteristics: OPA1632D* table....8
- Changed typical THD+N with single-ended Input/Output and RL = 600Ω from 0.000059% to 0.000036% in *Electrical Characteristics: OPA1632D* table....8
- Changed typical THD+N with single-ended Input/Output and RL = 2kΩ from 0.000043% to 0.000031% in *Electrical Characteristics: OPA1632D* table....8
- Changed IMD at diferrential input/output and R_L= 600Ω from 0.00008% to 0.000061% in *Electrical Characteristics: OPA1632D* table....8
- Changed IMD at diferrential input/output and R_L= 2kΩ from 0.00005% to 0.000061% in *Electrical Characteristics: OPA1632D* table....8
- Changed IMD at single-ended input/output and R_L= 600Ω from 0.0001% to 0.00007% in *Electrical Characteristics: OPA1632D* table....8
- Changed IMD at single-ended input/output and R_L= 2kΩ from 0.0007% to 0.000073% in *Electrical Characteristics: OPA1632D* table....8
- Removed specified operating voltage specifications from *Electrical Characteristics: OPA1632D* table....8
- Changed typical I_Q from 14mA to 13mA in *Electrical Characteristics: OPA1632D* table....8
- Changed title of Electrical Characteristics table to Electrical Characteristics: OPA1632DGN....10
- Changed test condition of power-down shutdown current from V_{ENABLE} = -15 V to V_S = ±5 V, V_{ENABLE} = −5 V for *Electrical Characteristics: OPA1632DGN* Package....10
- Added power-down shutdown current spec at V_{ENABLE} = -15 V for *Electrical Characteristics: OPA1632DGN* table....10
- Changed max specified operating voltage from ±16 V to ±15 V on *Electrical Characteristics: OPA1632DGN* table to align with recommended operating conditions....10
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- Added new Typical Characteristics section for D package....12
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- Updated *Layout Example* section....23
- Changed list of documentation in *Related Documentation* section....25

Changes from Revision B (January 2010) to Revision C (September 2015) **Page**

- 添加了 *ESD 等级* 表、*特性说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源相关建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分。 1

5 Pin Configuration and Functions

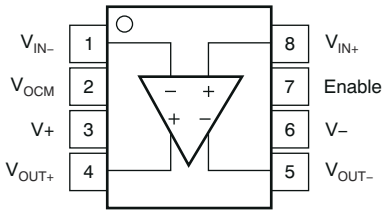


图 5-1. D or DGN(1) Package
8-Pin SOIC or MSOP-PowerPAD
Top View

表 5-1. Pin Functions

PIN		TYPE(2)	DESCRIPTION
NAME	NO.		
Enable	7	I	Active high enable pin
V+	3	I/O	Positive supply voltage pin
V-	6	I/O	Negative supply voltage pin
V_{IN+}	8	I	Positive input voltage pin
V_{IN-}	1	I	Negative input voltage pin
V_{OCM}	2	I	Output common-mode control voltage pin
V_{OUT+}	4	O	Positive output voltage pin
V_{OUT-}	5	O	Negative output voltage pin

(1) Solder the exposed DGN package thermal pad to a heat-spreading power or ground plane. This pad is electrically isolated from the die, but must be connected to a power or ground plane and not floated.
(2) I = input, O = output.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
$\pm V_S$	Supply Voltage		±16.5	V
	Supply turn-on/off dV/dT(3)		1.7	V/µs
V_I	Input Voltage		$\pm V_S$	V
I_O	Output Current		150	mA
I_{IN}	Continuous Input Current		10	mA
V_{ID}	Differential Input Voltage		±1.5	V
T_J	Maximum Junction Temperature		150	°C
	Operating Free-Air Temperature Range	–40	85	°C
T_{STG}	Storage Temperature Range	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The OPA1632 MSOP-8 package version incorporates a PowerPAD on the underside of the chip. This acts as a heatsink and must be connected to a thermally-dissipative plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature, which can permanently damage the device. See TI technical brief SLMA002 for more information about using the PowerPAD thermally-enhanced package.
(3) Staying below this specification ensures that the edge-triggered ESD absorption devices across the supply pins remain off.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), ANSI/ESDA/JEDEC JS-002(2)	±500	V
		Machine Model	±200	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage (V+ – V-)	Dual	±2.5	±15	V
	Single	5	30	
T_A	C-suffix	0	70	°C
	I-suffix	-40	85	

6.4 Thermal Information

THERMAL METRIC(1)	OPA1632		UNIT
	D (SOIC)	DGN (MSOP-PowerPAD)	
	8 PINS	8 PINS	
$R_{\theta JA}$	126.3	59.8	°C/W
$R_{\theta JC(top)}$	67.3	57.7	°C/W
$R_{\theta JB}$	69.8	38.7	°C/W
ψ_{JT}	19.5	2.7	°C/W
ψ_{JB}	69.0	38.4	°C/W
$R_{\theta JC(bot)}$	n/a	8.4	°C/W

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

6.5 Electrical Characteristics: OPA1632D

V_S = ±15 V; R_F = 390 Ω, R_L = 800 Ω, and G = +1 (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
Offset Voltage								
Input Offset Voltage						±0.5	±3	mV
	vs temperature, dc	dV_{OS}/dT				±2.5		µV/°C
	vs Power Supply, dc	PSRR				13	316	µV/V
Input Bias Current								
Input Bias Current	I_B					7.9	14	µA
Input Offset Current	I_{OS}					±100	±500	nA
Noise								
Input Voltage Noise			f = 10 kHz			1.25		nV/√Hz
Input Current Noise			f = 10 kHz			1.7		pA/√Hz
Input Voltage								
Common-Mode Input Range					(V−) + 1.5		(V+) − 1	V
Common-Mode Rejection Ratio, dc					74	90		dB
Input Impedance								
Input Impedance			Measured into each input terminal, common-mode			215 || 1.4		MΩ || pF
			Measured into each input terminal, differential			10 || 3.1		kΩ || pF
Open-Loop Gain								
Open-Loop Gain, dc					66	78		dB
Frequency Response								
Small-Signal Bandwidth			G = +1, R_F= 348 Ω			180		MHz
	(V_O = 100mV$_{PP}$, Peaking < 0.5 dB)		G = +2, R_F = 602 Ω			104		
			G = +5, R_F = 1.5 kΩ			46		
			G = +10, R_F = 3.01 kΩ			24		
Bandwidth for 0.1dB Flatness			G = +1, V_O = 100 mV$_{PP}$			40		MHz
Peaking at a Gain of 1			V_O = 100 mV$_{PP}$			0.5		dB
Large-Signal Bandwidth			G = +2, V_O = 20 V$_{PP}$			1.8		MHz
Slew Rate (25% to 75%)			G = +1			72		V/µs
Rise and Fall Time			G = +1, V_O = 5-V Step			69		ns
Settling Time to	0.1%		G = +1, V_O = 2-V Step			36		ns
	0.01%					49		ns
Total Harmonic Distortion + Noise	Differential Input/Output		G = +1, f = 1 kHz, V_O = 3 V_{RMS}	R_L = 600 Ω		0.00003%		
				R_L = 2 kΩ		0.000028%		
	Single-Ended In/Differential Out			R_L = 600 Ω		0.000036%		
				R_L = 2 kΩ		0.000031%		
Intermodulation Distortion	Differential Input/Output		G = +1, SMPTE/DIN, V_O = 2 V_{PP}	R_L = 600 Ω		0.000061%		
				R_L = 2 kΩ		0.000061%		
	Single-Ended In/Differential Out			R_L = 600 Ω		0.000073%		
				R_L = 2 kΩ		0.00007%		
Headroom			THD < 0.01%, R_L = 2 kΩ			20		V_{PP}

6.5 Electrical Characteristics: OPA1632D (continued)

V_S = ±15 V; R_F = 390 Ω, R_L = 800 Ω, and G = +1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output						
Voltage Output Swing Low		R_L = 2 kΩ		(V−) + 1.6		V
		R_L = 1 kΩ			(V−) + 3.5	V
Voltage Output Swing High		R_L = 2 kΩ		(V+) - 1.6		V
		R_L = 1 kΩ	(V+) − 3.5			V
Short-Circuit Current	I_{SC}	Sourcing	50	85		mA
		Sinking	−60	– 85		
Closed-Loop Output Impedance		G = +1, f = 100 kHz		0.22		Ω
Power-Down(1)						
Enable Voltage Threshold				(V−) + 1.45		V
Disable Voltage Threshold				(V−) + 1.4		V
Shutdown Current		V_S = ±5V, V_{ENABLE} = −5 V		0.85		mA
		V_{ENABLE} = −15 V		1.7		mA
Turn-On Delay		Time for I_Q to Reach 50%		2		µs
Turn-Off Delay				2		µs
Power Supply						
Quiescent Current	I_Q			13	17.1	mA

(1) Amplifier has internal 250-kΩ pull-up resistor to V+ pin. This enables the amplifier with no connection to shutdown pin.

6.6 Electrical Characteristics: OPA1632DGN

V_S = ±15 V; R_F = 390 Ω, R_L = 800 Ω, and G = +1 (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Offset Voltage							
Input Offset Voltage					±0.5	±3	mV
	vs Power Supply, dc dV_{OS}/dT				±5		µV/°C
	vs Power Supply, dc PSRR			316	13		µV/V
Input Bias Current							
Input Bias Current	I_B				2	6	µA
Input Offset Current	I_{OS}				±100	±500	nA
Noise							
Input Voltage Noise		f = 10 kHz			1.3		nV/√Hz
Input Current Noise		f = 10 kHz			0.4		pA/√Hz
Input Voltage							
Common-Mode Input Range				(V−) + 1.5		(V+) − 1	V
Common-Mode Rejection Ratio, dc				74	90		dB
Input Impedance							
Input Impedance (each input pin)					34 || 4		MΩ || pF
Open-Loop Gain							
Open-Loop Gain, dc				66	78		dB
Frequency Response							
Small-Signal Bandwidth		G = +1, R_F= 348 Ω			180		MHz
	(V_O = 100mV$_{PP}$, Peaking < 0.5 dB)	G = +2, R_F = 602 Ω			90		MHz
		G = +5, R_F = 1.5 kΩ			36		MHz
		G = +10, R_F = 3.01 kΩ			18		MHz
Bandwidth for 0.1dB Flatness		G = +1, V_O = 100 mV$_{PP}$			40		MHz
Peaking at a Gain of 1		V_O = 100 mV$_{PP}$			0.5		dB
Large-Signal Bandwidth		G = +2, V_O = 20 V$_{PP}$			800		kHz
Slew Rate (25% to 75%)		G = +1			50		V/µs
Rise and Fall Time		G = +1, V_O = 5-V Step			100		ns
Settling Time to	0.1%	G = +1, V_O = 2-V Step			75		ns
	0.01%	G = +1, V_O = 2-V Step			200		ns
Total Harmonic Distortion + Noise	Differential Input/Output	G = +1, f = 1 kHz, V_O = 3 V_{RMS}	R_L = 600 Ω		0.0003%		
	Differential Input/Output		R_L = 2 kΩ		0.000022%		
	Single-Ended In/Differential Out		R_L = 600 Ω		0.000059%		
	Single-Ended In/Differential Out		R_L = 2 kΩ		0.000043%		
Intermodulation Distortion	Differential Input/Output	G = +1, SMPTE/DIN, V_O = 2 V_{PP}	R_L = 600 Ω		0.00008%		
	Differential Input/Output		R_L = 2 kΩ		0.00005%		
	Single-Ended In/Differential Out		R_L = 600 Ω		0.0001%		
	Single-Ended In/Differential Out		R_L = 2 kΩ		0.0007%		
Headroom		THD < 0.01%, R_L = 2 kΩ			20.0		V_{PP}
Output							
Voltage Output Swing		R_L = 2 kΩ		(V+) − 1.9		(V−) + 1.9	V
		R_L = 800 Ω		(V+) − 4.5		(V−) + 4.5	V
Short-Circuit Current	I_{SC}	Sourcing		+50	85		mA
		Sinking		−60	-85		
Closed-Loop Output Impedance		G = +1, f = 100 kHz			0.3		Ω

6.6 Electrical Characteristics: OPA1632DGN (continued)

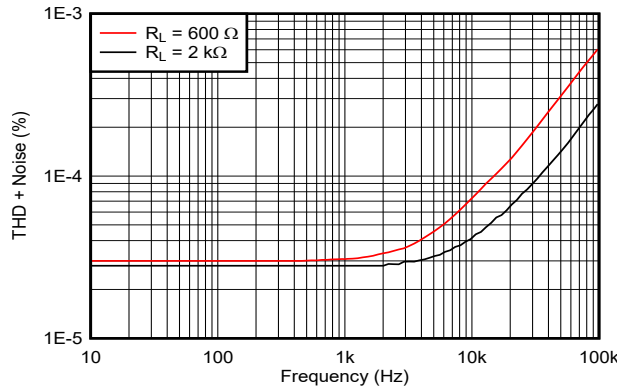
V_S = ±15 V; R_F = 390 Ω, R_L = 800 Ω, and G = +1 (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power-Down(1)					
Enable Voltage Threshold			(V−) + 2		V
Disable Voltage Threshold			(V−) + 0.8		V
Shutdown Current	V_{ENABLE} = −15 V		1.7		mA
Shutdown Current	V_S = ±5 V, V_{ENABLE} = −5 V		0.85		mA
Turn-On Delay	Time for I_Q to Reach 50%		2		µs
Turn-Off Delay	Time for I_Q to Reach 50%		2		µs
Power Supply					
Specified Operating Voltage				±15	V
Operating Voltage		±2.5			V
Quiescent Current I_Q	Per Channel		14	17.1	mA
Temperature Range					
Specified Range		−40		+85	°C
Operating Range		−40		+125	°C
Storage Range		−65		+150	°C

(1) Amplifier has internal 50-kΩ pull-up resistor to V+ pin. This enables the amplifier with no connection to shutdown pin.

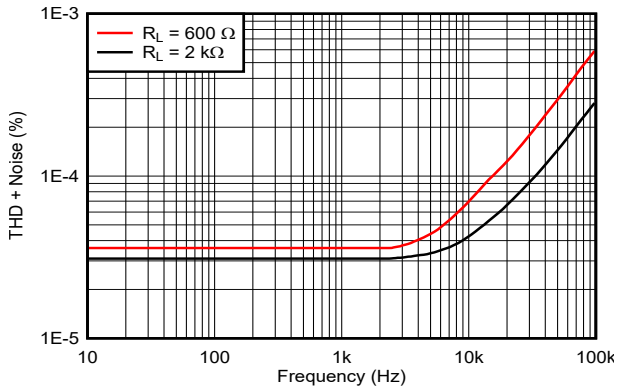
6.7 Typical Characteristics: OPA1632D

at T_A = 25°C, V_S = ±15 V, R_F = 348 Ω, G = +1 and R_L = 2 kΩ (unless otherwise noted)



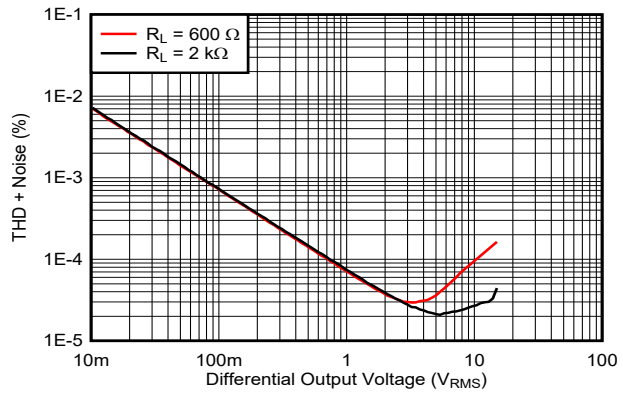
V_O = 3V_{RMS}; Differential Input and Output

图 6-1. THD + Noise vs Frequency



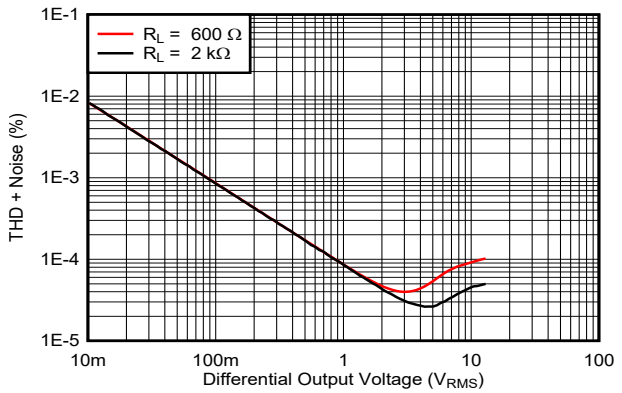
V_O = 3V_{RMS}; Single-ended Input to Differential Output

图 6-2. THD + Noise vs Frequency



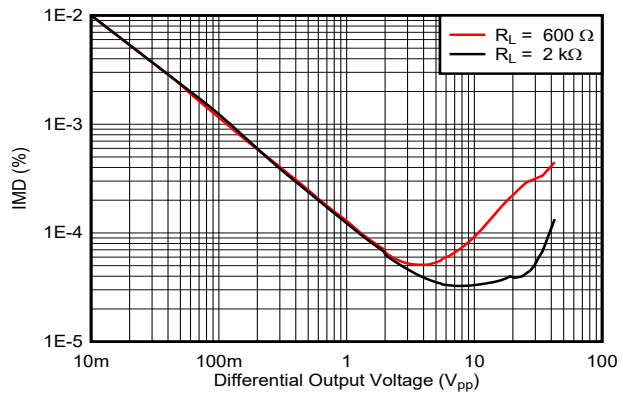
f = 1 kHz; Differential Input and Output

图 6-3. THD + Noise vs Output Voltage



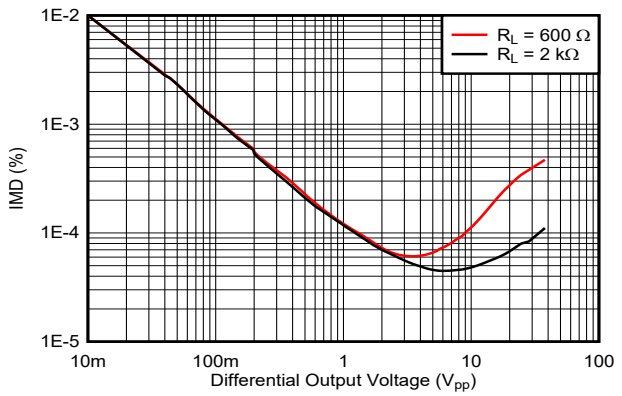
f = 1 kHz; Single-ended Input to Differential Output

图 6-4. THD + Noise vs Output Voltage



SMPTE 4:1: 60Hz, 7kHz; DIN 4:1: 250Hz, 8kHz; Differential Input and Output

图 6-5. Intermodulation Distortion vs Output Voltage



SMPTE 4:1: 60Hz, 7kHz; DIN 4:1: 250Hz, 8kHz; Differential Input and Output

图 6-6. Intermodulation Distortion vs Output Voltage

6.7 Typical Characteristics: OPA1632D (continued)

at T_A = 25°C, V_S = ±15 V, R_F = 348 Ω, G = +1 and R_L = 2 kΩ (unless otherwise noted)

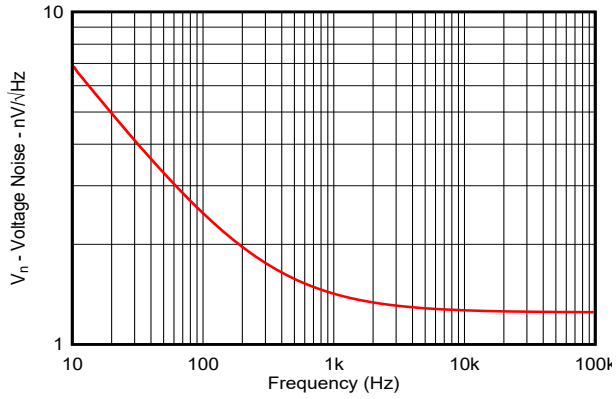


图 6-7. Voltage Noise vs Frequency

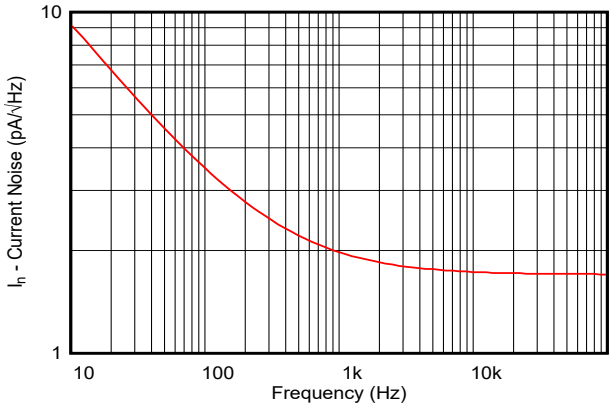
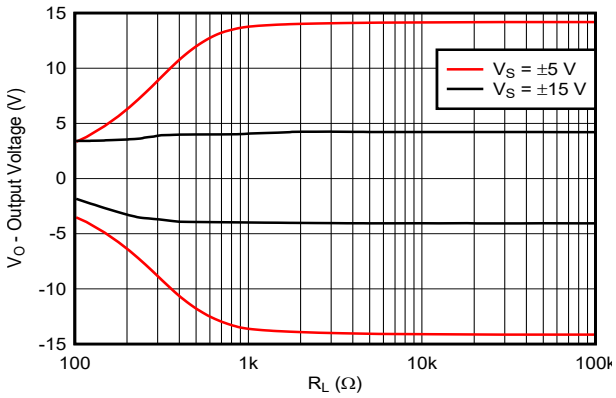


图 6-8. Current Noise vs Frequency



R_F= 1kΩ ; G = +2

图 6-9. Output Voltage vs Differential Load Resistance

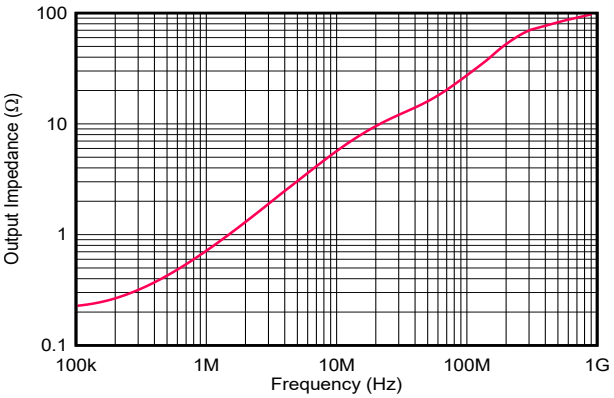


图 6-10. Output Impedance vs Frequency

6.8 Typical Characteristics: OPA1632DGN

at T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ (unless otherwise noted)

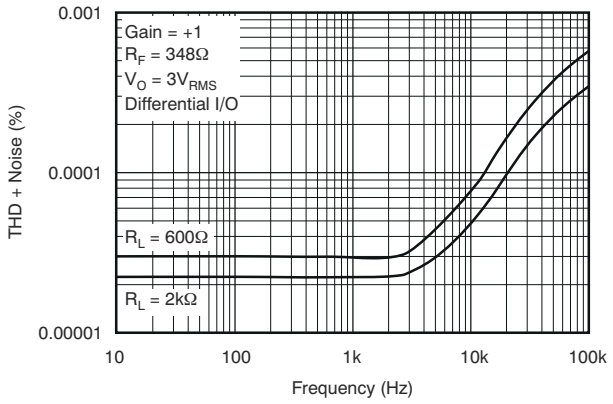


图 6-11. THD + Noise vs Frequency

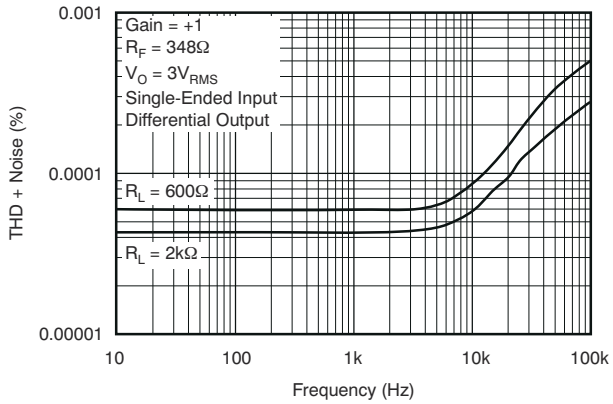


图 6-12. THD + Noise vs Frequency

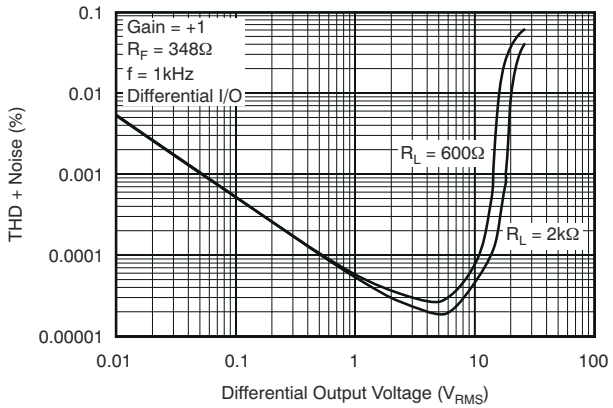


图 6-13. THD + Noise vs Output Voltage

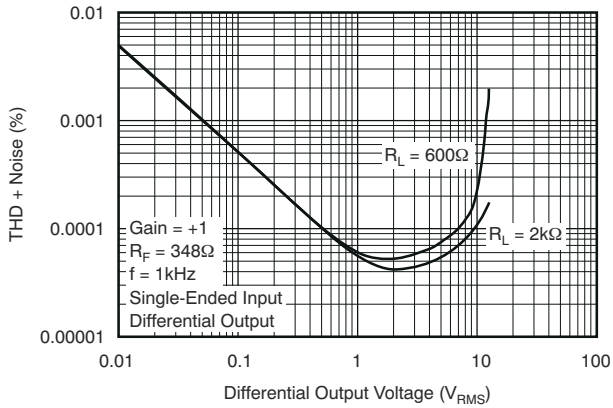


图 6-14. THD + Noise vs Output Voltage

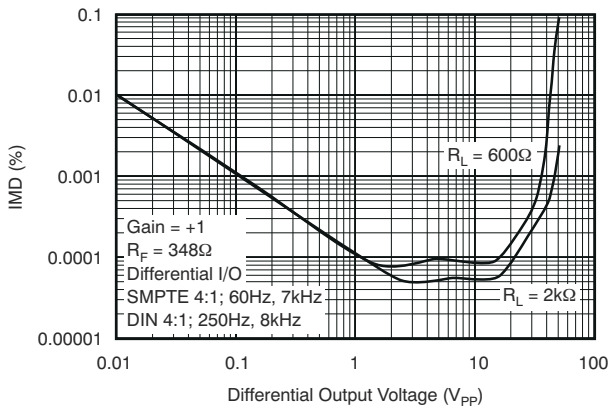


图 6-15. Intermodulation Distortion vs Output Voltage

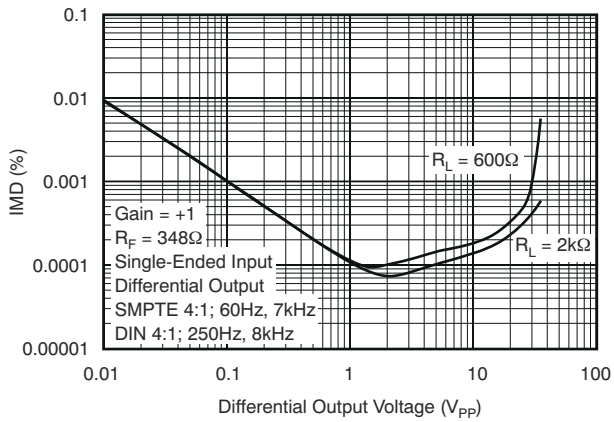


图 6-16. Intermodulation Distortion vs Output Voltage

6.8 Typical Characteristics: OPA1632DGN (continued)

at T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ (unless otherwise noted)

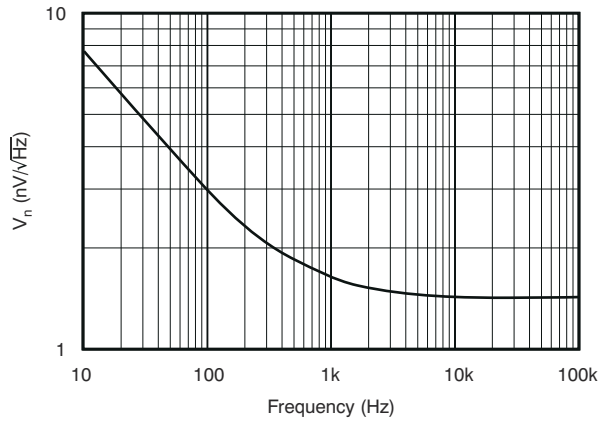


图 6-17. Voltage Noise vs Frequency

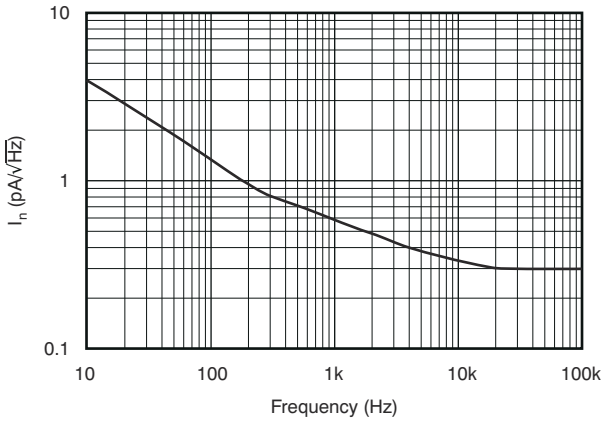


图 6-18. Current Noise vs Frequency

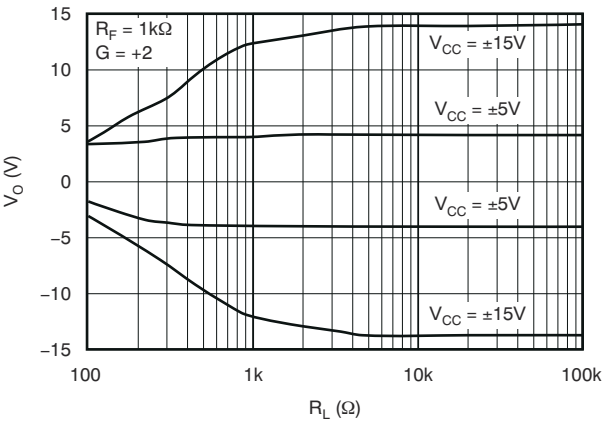


图 6-19. Output Voltage vs Differential Load Resistance

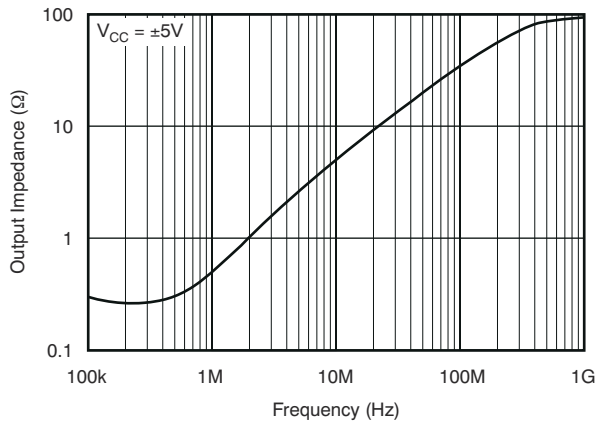


图 6-20. Output Impedance vs Frequency

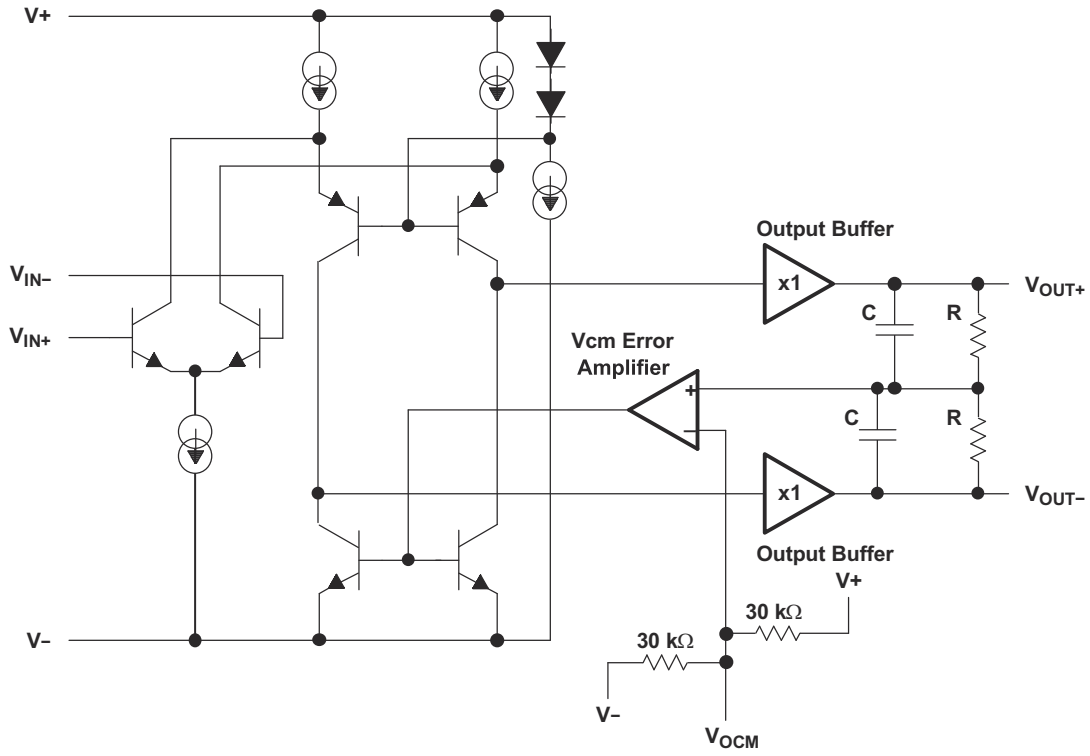
7 Detailed Description

7.1 Overview

7.1.1 Fully-Differential Amplifiers

The OPA1632 is a fully differential amplifier (FDA). Differential signal processing offers a number of performance advantages in high-speed analog signal processing systems, including immunity to external common-mode noise, suppression of even-order non-linearities, and increased dynamic range. FDAs not only serve as the primary means of providing gain to a differential signal chain, but also provide a monolithic solution for converting single-ended signals into differential signals allowing for easy, high-performance processing. For more information on the basic theory of operation for FDAs, refer to the *Fully Differential Amplifiers* application note.

7.2 Functional Block Diagram



7.3 Feature Description

图 7-1 and 图 7-2 depict the differences between the operation of the OPA1632 in two different modes. FDAs can work with differential input or can be implemented as single in/differential out.

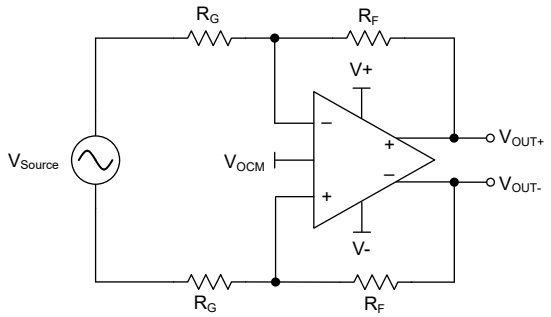


图 7-1. Amplifying Differential Input Signals

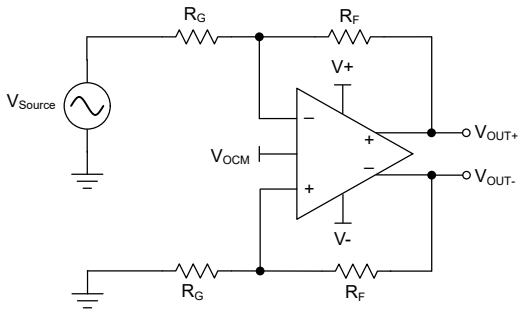


图 7-2. Amplifying Single-ended Input Signals

7.4 Device Functional Modes

7.4.1 Shutdown Function

The shutdown (enable) function of the OPA1632 is referenced to the negative supply of the operational amplifier. A valid logic low (< 0.8 V above negative supply) applied to the enable pin (pin 7) disables the amplifier output. Voltages applied to pin 7 that are greater than 2 V above the negative supply place the amplifier output in an active state, and the device is enabled. If pin 7 is left disconnected, an internal pull-up resistor enables the device. Turn-on and turn-off times are approximately 2 μs each.

Quiescent current is reduced to approximately 0.85 mA when the amplifier is disabled. When disabled, the output stage is *not* in a high-impedance state. Thus, the shutdown function cannot be used to create a multiplexed switching function in series with multiple amplifiers.

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

8.1.1 Output Common-Mode Voltage

The output common-mode voltage pin sets the dc output voltage of the OPA1632. A voltage applied to the V_{OCM} pin from a low-impedance source can be used to directly set the output common-mode voltage. If the V_{OCM} pin is left floating it defaults to the mid-rail voltage, defined as:

$$\frac{(V_+) + (V_-)}{2} \tag{1}$$

To minimize common-mode noise, connect a 0.1-uF bypass capacitor to the V_{OCM} pin. Output common-mode voltage causes additional current to flow in the feedback resistor network. Since this current is supplied by the output stage of the amplifier, this creates additional power dissipation. For commonly-used feedback resistance values, this current is easily supplied by the amplifier. The additional internal power dissipation created by this current may be significant in some applications and may dictate use of the MSOP PowerPAD package to effectively control self-heating.

8.1.1.1 Resistor Matching

Resistor matching is important in FDAs to maintain good output balance. An ideal differential output signal implies the two outputs of the FDA should be exactly equal in amplitude and shifted 180° in phase. Any imbalance in amplitude or phase between the two output signals results in an undesirable common-mode signal at the output. The output balance error is a measure of how well the outputs are balanced and is defined as the ratio of the output common-mode voltage to the output differential signal.

$$Output\ Balance\ Error = \frac{\left(\frac{V_{OUT+} - V_{OUT-}}{2}\right)}{V_{OUT+} - V_{OUT-}} \tag{2}$$

At low frequencies, resistor mismatch is the primary contributor to output balance errors. Additionally CMRR, PSRR, and HD2 performance diminish if resistor mismatch occurs. Therefore, it is recommended to use 1% tolerance resistors or better to optimize performance. See 表 8-1 for recommended resistor values to use for a particular gain.

表 8-1. Recommended Resistor Values

Gain (V/V)	R_G (Ω)	R_F (Ω)
1	390	390
2	374	750
5	402	2010
10	402	4020

8.2 Typical Application

图 8-1 shows the OPA1632 used as a differential-output driver for the PCM1804 high-performance audio ADC.

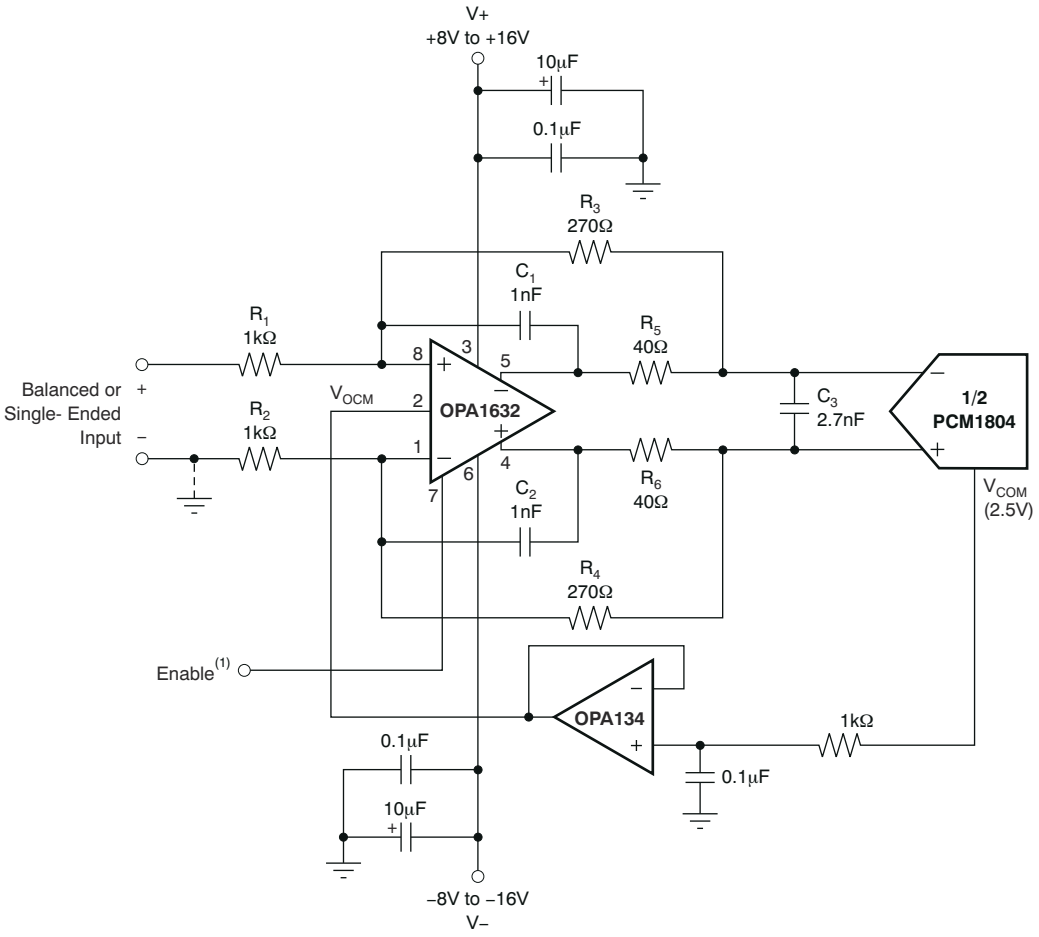


图 8-1. ADC Driver for Professional Audio

8.2.1 Design Requirements

表 8-2 shows example design parameters and values for the typical application design example in 图 7-1.

表 8-2. Design Parameters

DESIGN PARAMETERS	VALUE
Supply voltage	±2.5 V to ±15 V
Amplifier topology	Voltage feedback
Output control	DC coupled with output common mode control capability
Filter requirement	500 kHz, Multiple feedback low pass filter

8.2.2 Detailed Design Procedure

Supply voltages of ±15 V are commonly used for the OPA1632. The relatively low input voltage swing required by the ADC allows use of lower power-supply voltage, if desired. Power supplies as low as ±8 V can be used in this application with excellent performance. This reduces power dissipation and heat rise. Power supplies should be bypassed with 10-μF tantalum capacitors in parallel with 0.1-μF ceramic capacitors to avoid possible oscillations and instability.

The V_{COM} reference voltage output on the PCM1804 ADC provides the proper input common-mode reference voltage (2.5 V). This V_{COM} voltage is buffered with op amp A_2 and drives the output common-mode voltage pin of the OPA1632. This biases the average output voltage of the OPA1632 to 2.5 V.

The signal gain of the circuit is generally set to approximately 0.25 to be compatible with commonly-used audio line levels. Gain can be adjusted, if necessary, by changing the values of R_1 and R_2. The feedback resistor values (R_3 and R_4) should be kept relatively low, as indicated, for best noise performance.

R_5, R_6, and C_3 provide an input filter and charge glitch reservoir for the ADC. The values shown are generally satisfactory. Some adjustment of the values may help optimize performance with different ADCs.

It is important to maintain accurate resistor matching on R_1/R_2 and R_3/R_4 to achieve good differential signal balance. Use 1% resistors for highest performance. When connected for single-ended inputs (inverting input grounded, as shown in 图 8-1), the source impedance must be low. Differential input sources must have well-balanced or low source impedance.

Capacitors C_1, C_2, and C_3 should be chosen carefully for good distortion performance. Polystyrene, polypropylene, NPO ceramic, and mica types are generally excellent. Polyester and high-K ceramic types such as Z5U can create distortion.

8.2.3 Application Curves

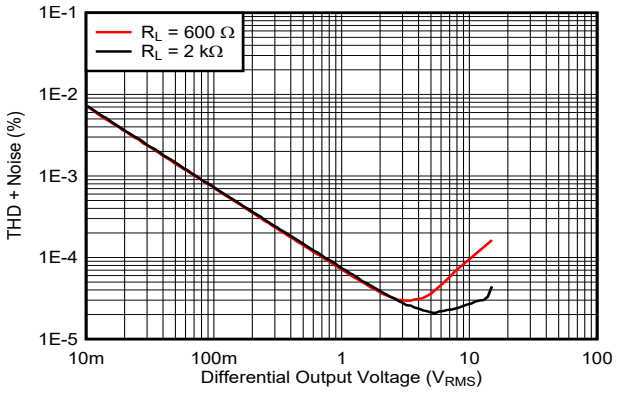


图 8-2. THD + Noise vs Output Voltage

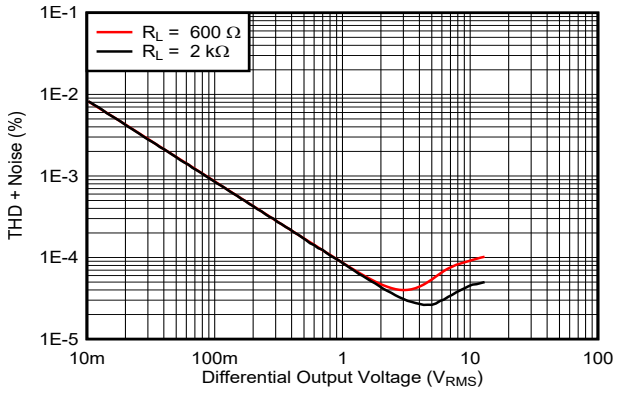


图 8-3. THD + Noise vs Output Voltage

9 Power Supply Recommendations

The OPA1632 device was designed to be operated on power supplies ranging from ±2.5 V to ±15 V. Single power supplies ranging from 5 V to 30 V can also be used. TI recommends using a power-supply accuracy of 5%, or better. When operated on a board with high-speed digital signals, it is important to provide isolation between digital signal noise and the analog input pins. The OPA1632 is connected to power supplies through pin 3 (V_+) and pin 6 (V_-). Each supply pin should be decoupled to GND as close to the device as possible with a low-inductance, surface-mount ceramic capacitor of approximately 10 nF. When vias are used to connect the bypass capacitors to a ground plane the vias should be configured for minimal parasitic inductance. One method of reducing via inductance is to use multiple vias. For broadband systems, two capacitors per supply pin are advised.

To avoid undesirable signal transients, the OPA1632 device should not be powered on with large inputs signals present. Careful planning of system power on sequencing is especially important to avoid damage to ADC inputs when an ADC is used in the application.

10 Layout

10.1 Layout Guidelines

1. The PowerPAD is electrically isolated from the silicon and all leads. Connecting the PowerPAD to any potential voltage between the power-supply voltages is acceptable, but it is recommended to tie to ground because it is generally the largest conductive plane.
2. Prepare the PCB with a top-side etch pattern, as shown in 图 10-1. There should be etch for the leads as well as etch for the thermal pad.
3. Place five holes in the area of the thermal pad. These holes should be 13 mils (0,03302 cm) in diameter. Keep them small so that solder wicking through the holes is not a problem during reflow.
4. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. These vias help dissipate the heat generated by the OPA1632 IC, and may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered so that wicking is not a problem.
5. Connect all holes to the internal ground plane.
6. When connecting these holes to the plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the OPA1632 PowerPAD package should make their connection to the internal plane with a complete connection around the entire circumference of the plated-through hole.
7. The top-side solder mask should leave the terminals of the package and the thermal pad area with its five holes exposed. The bottom-side solder mask should cover the five holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
8. Apply solder paste to the exposed thermal pad area and all of the IC terminals.

   With these preparatory steps in place, the IC is simply placed in position and runs through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

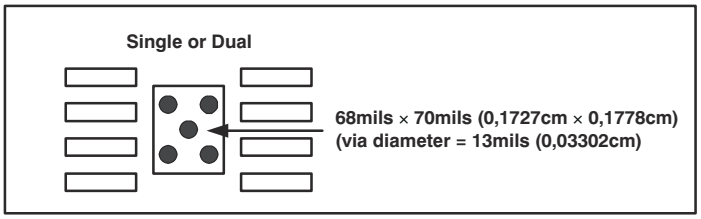


图 10-1. PowerPAD PCB Etch and Via Pattern

10.1.1 PowerPAD Design Considerations

The OPA1632 is available in a thermally-enhanced PowerPAD family of packages. These packages are constructed using a downset leadframe upon which the die is mounted (see 图 10-2(a) and 图 10-2(b)). This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package (see 图 10-2(c)). Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

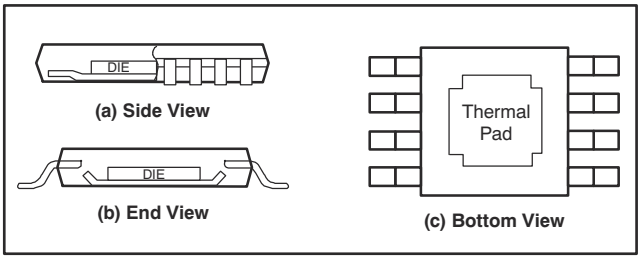


图 10-2. Views of the Thermally-Enhanced Package

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad must be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device. Soldering the PowerPAD to the printed circuit board (PCB) is always required, even with applications that have low power dissipation. It provides the necessary thermal and mechanical connection between the lead frame die pad and the PCB.

10.1.2 Power Dissipation and Thermal Considerations

The OPA1632 does not have thermal shutdown protection. Take care to assure that the maximum junction temperature is not exceeded. Excessive junction temperature can degrade performance or cause permanent damage. For best performance and reliability, assure that the junction temperature does not exceed 125°C.

The thermal characteristics of the device are dictated by the package and the circuit board. Maximum power dissipation for a given package can be calculated using the following formula:

$$P_{DMax} = \frac{T_{Max} - T_A}{\theta_{JA}}$$

where:

- P_{DMax} is the maximum power dissipation in the amplifier (W)
- T_{Max} is the absolute maximum junction temperature (°C)
- T_A is the ambient temperature (°C)
- $\theta_{JA} = \theta_{JC} + \theta_{CA}$
- θ_{JC} is the thermal coefficient from the silicon junctions to the case (°C/W)
- θ_{CA} is the thermal coefficient from the case to ambient air (°C/W)

For systems where heat dissipation is more critical, the OPA1632 is offered in an MSOP-8 with PowerPAD. The thermal coefficient for the MSOP PowerPAD (DGN) package is substantially improved over the traditional SO package. Maximum power dissipation levels are depicted in 图 10-3 for the two packages. The data for the DGN package assume a board layout that follows the PowerPAD layout guidelines.

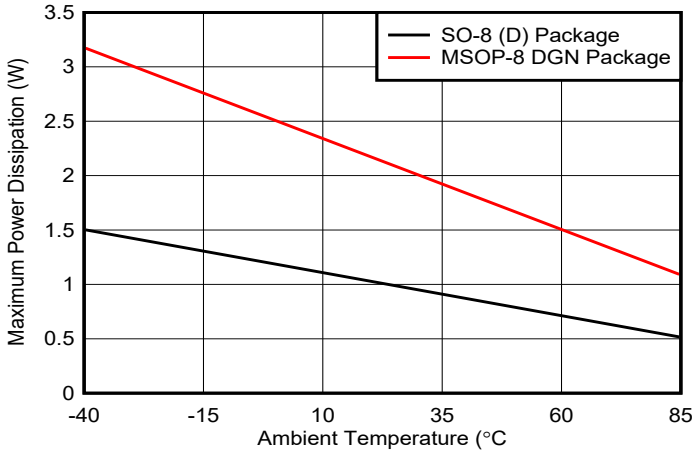


图 10-3. Maximum Power Dissipation vs Ambient Temperature

10.2 Layout Example

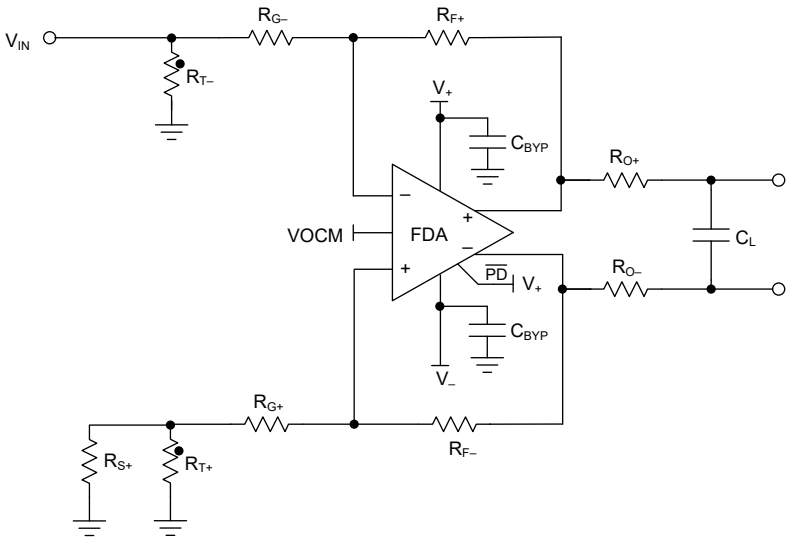


图 10-4. Representative Schematic for Example Layout

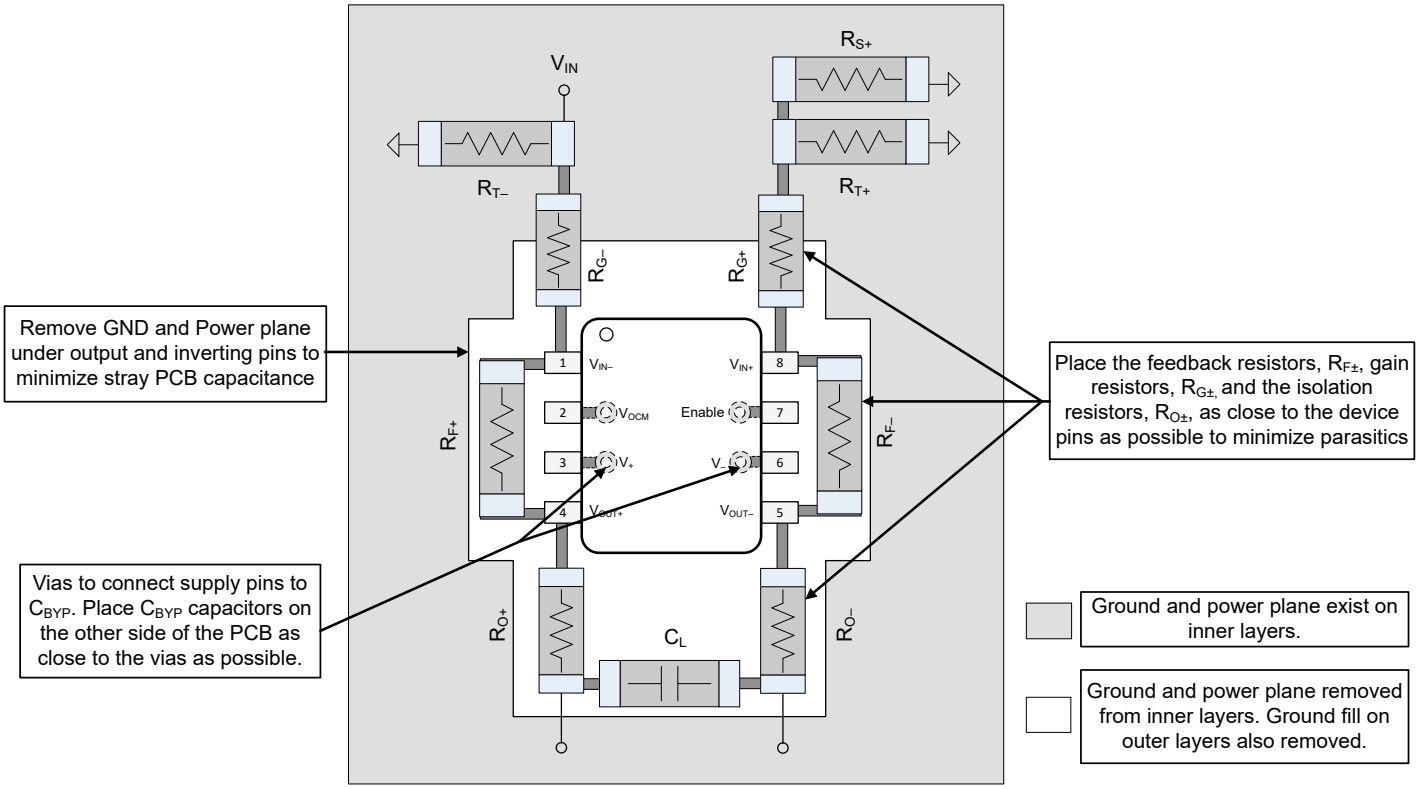


图 10-5. Example Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Fully Differential Amplifiers* application note
- Texas Instruments, *TI Precision Labs - Fully Differential Amplifiers* video series
- Texas Instruments, *Maximizing Signal Chain Distortion Performance Using High Speed Amplifiers* application note
- Texas Instruments, *Analog Audio Amplifier Front-end Reference Design with Improved Noise and Distortion*
- Texas Instruments, *Public Announcement Audio Reference Design utilizing best in class Boost Controller*
- Texas Instruments, *Motherboard/controller for the AMC1210* reference design
- Texas Instruments, TPA6120A2 Stereo, 9.0 to 33.0-V, analog input headphone amplifier with 128 dB dynamic range
- Texas Instruments, OPA2863 Dual, low-power, 110-MHz, 12-V, RRIO voltage feedback amplifier
- Texas Instruments, OPA2834 Ultra-low power, 50MHz rail-to-rail out, negative rail in, voltage-feedback op amp

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ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

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TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA1632D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OPA 1632	Samples
OPA1632DG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OPA 1632	Samples
OPA1632DGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	1632	Samples
OPA1632DGNG4	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	1632	Samples
OPA1632DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	1632	Samples
OPA1632DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OPA 1632	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

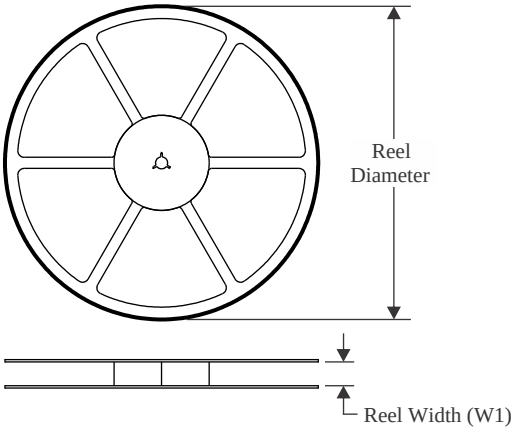
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

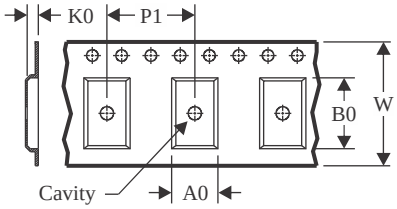
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

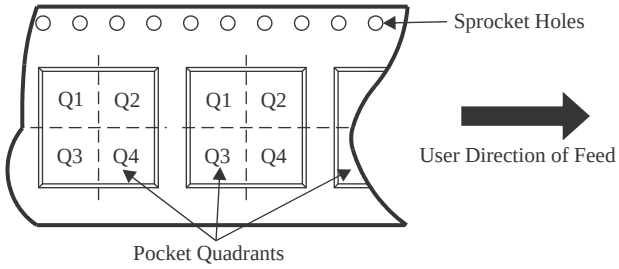


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

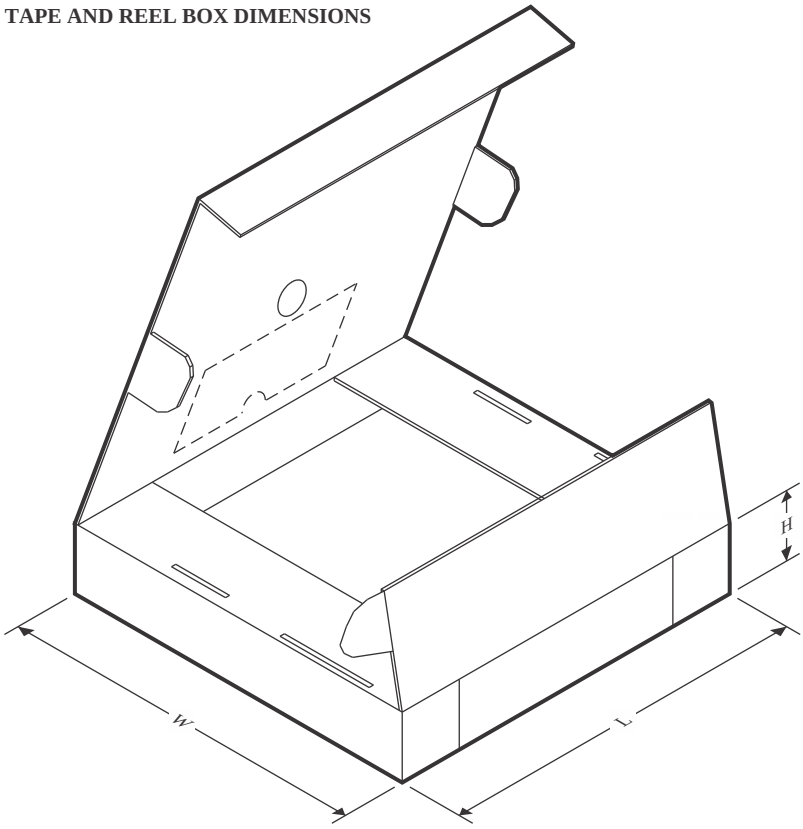
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA1632DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA1632DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

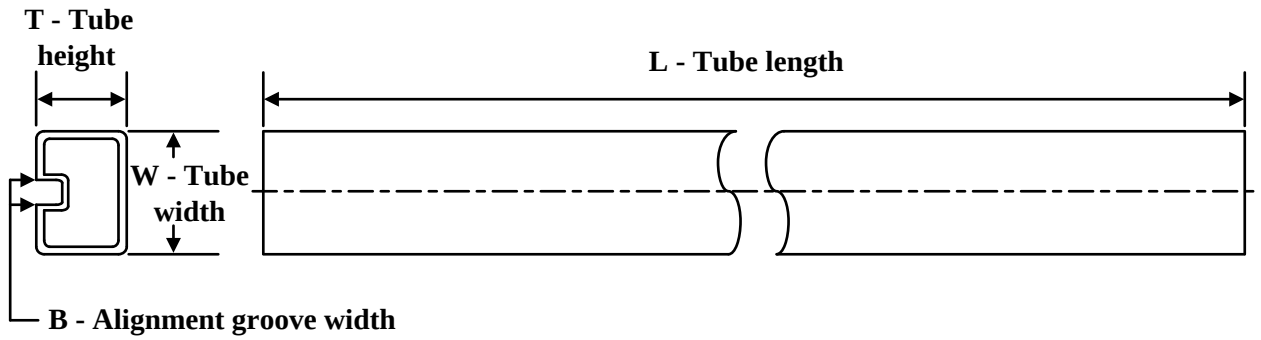
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA1632DGNR	HVSSOP	DGN	8	2500	358.0	335.0	35.0
OPA1632DR	SOIC	D	8	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA1632D	D	SOIC	8	75	505.46	6.76	3810	4
OPA1632DG4	D	SOIC	8	75	505.46	6.76	3810	4

GENERIC PACKAGE VIEW

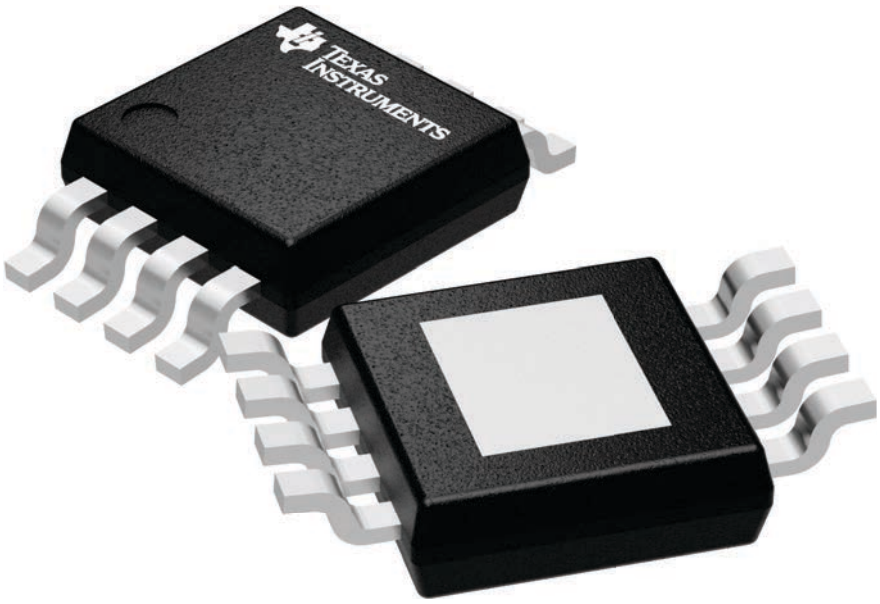
DGN 8

PowerPAD VSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

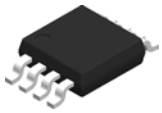
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/A

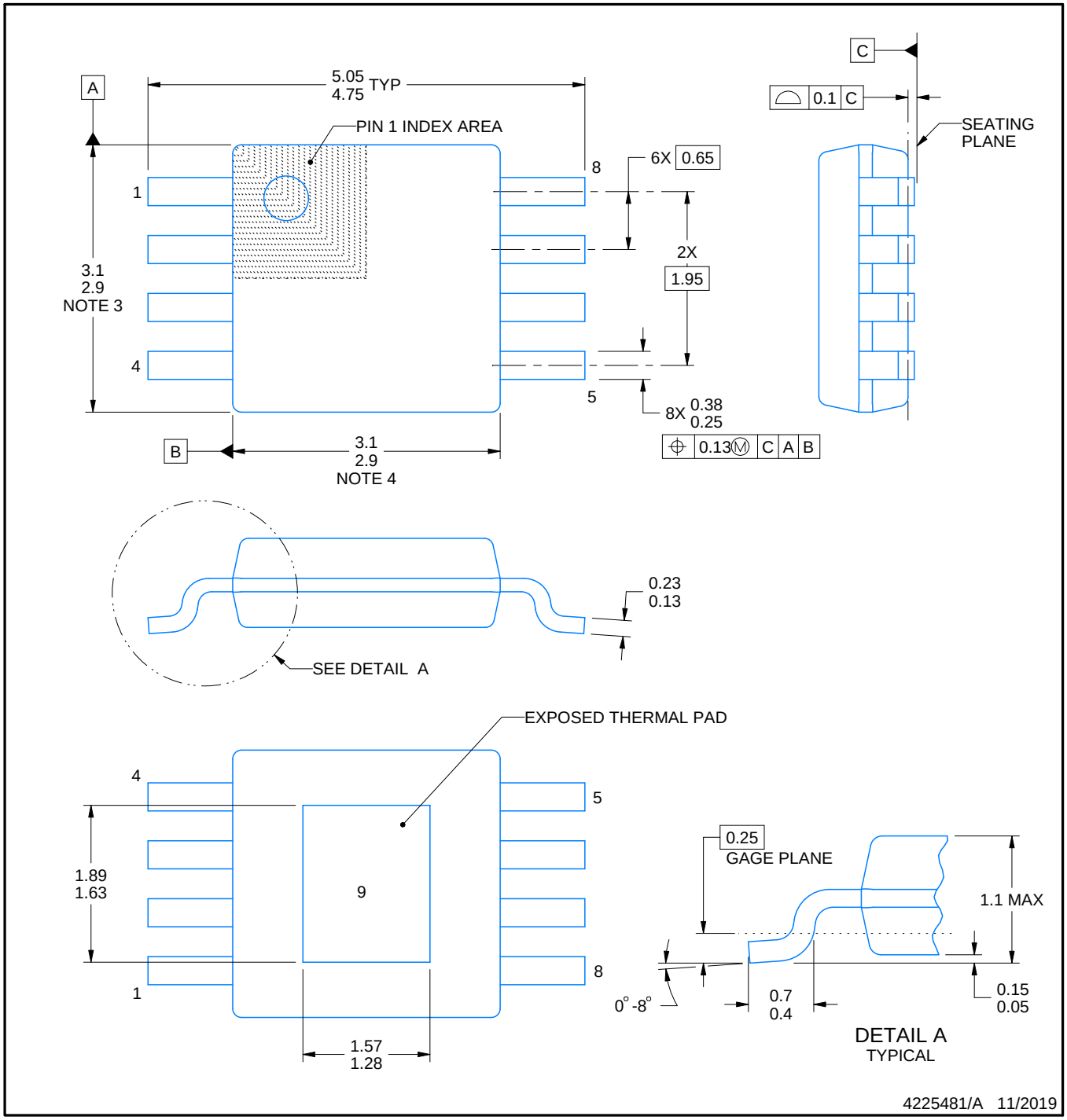
PACKAGE OUTLINE

DGN0008D



PowerPAD™ VSSOP - 1.1 mm max height

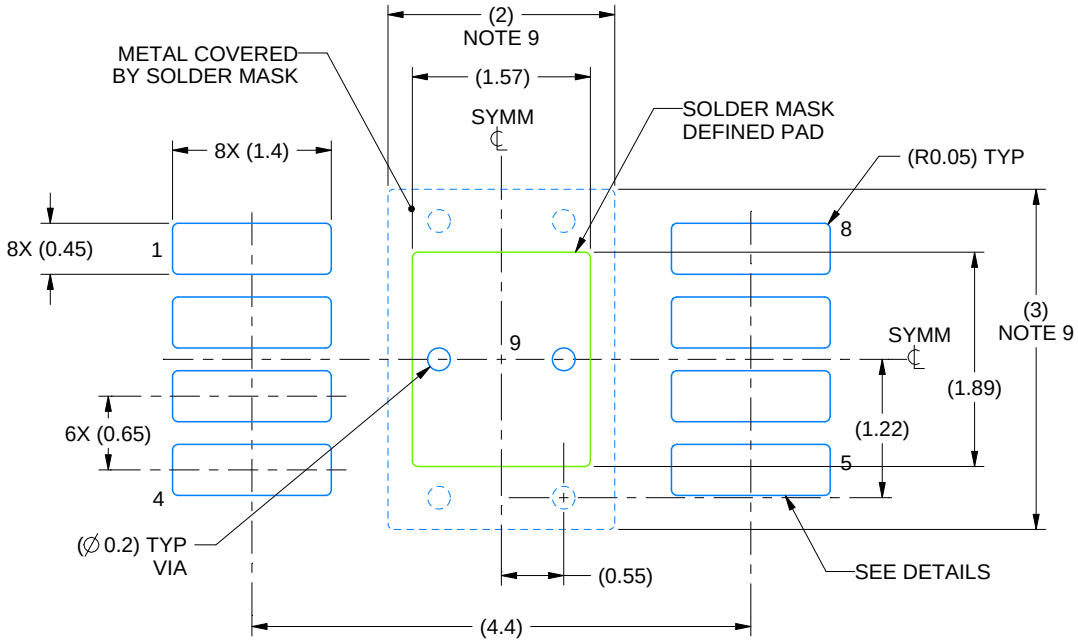
SMALL OUTLINE PACKAGE



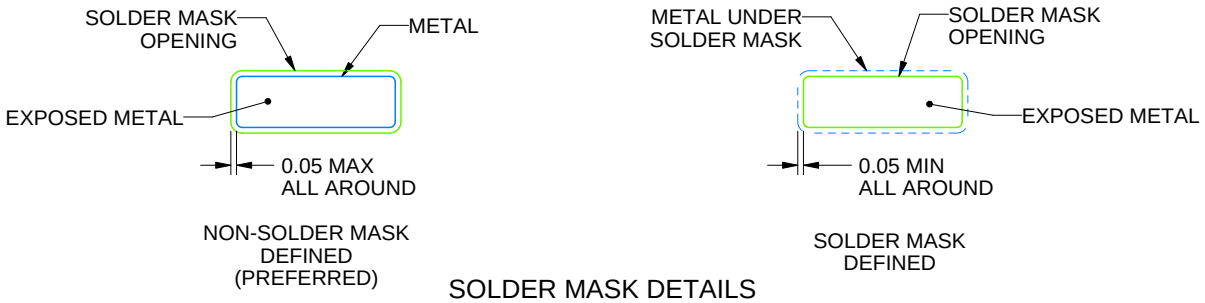
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

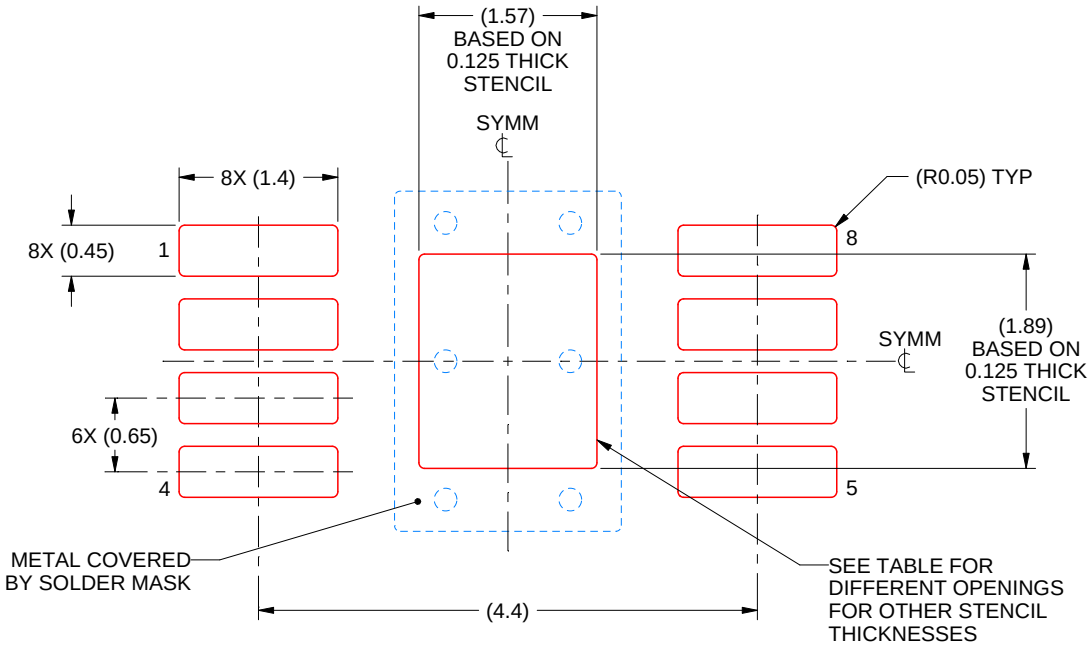


SOLDER MASK DETAILS

4225481/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



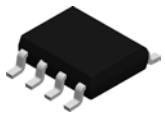
SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225481/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

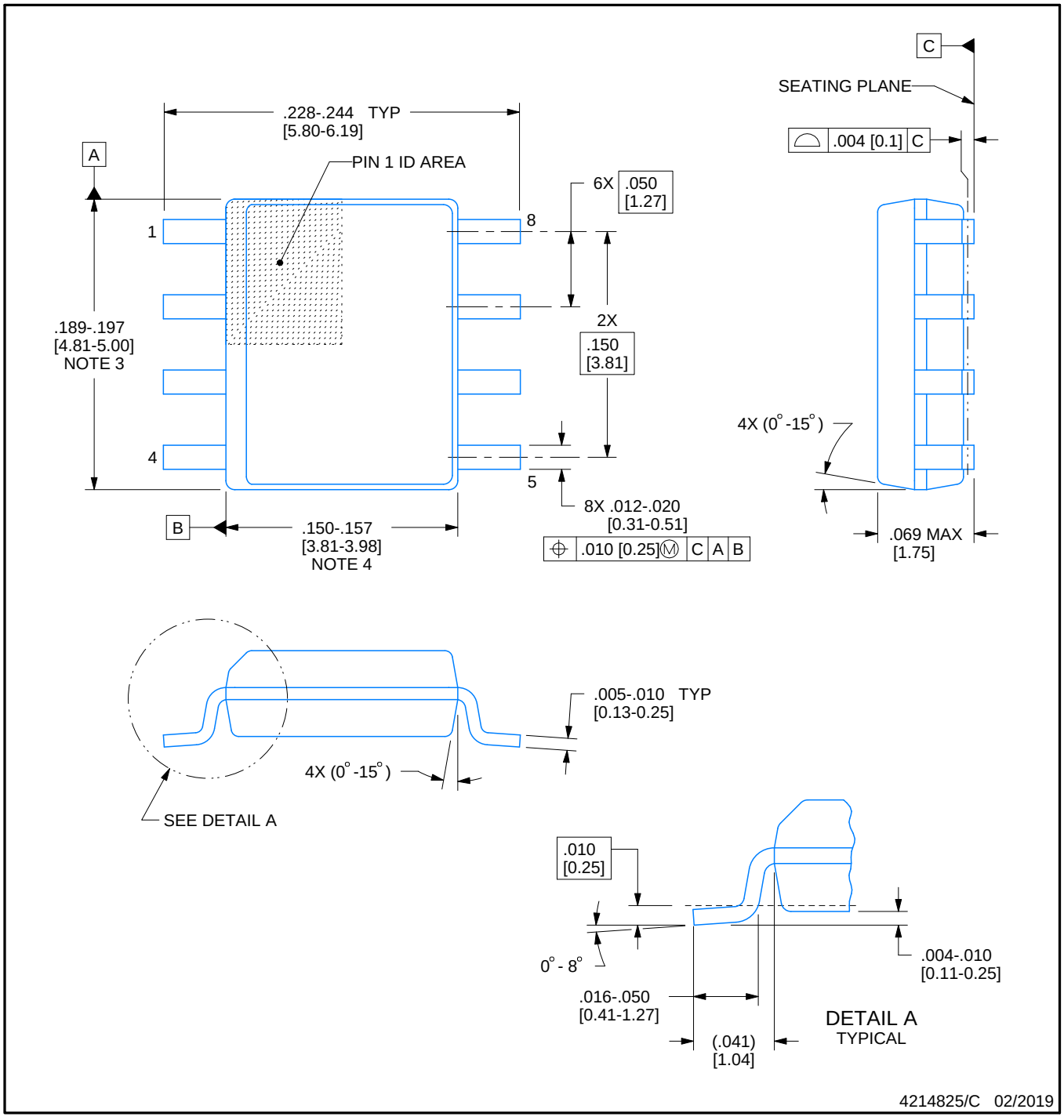


PACKAGE OUTLINE

D0008A

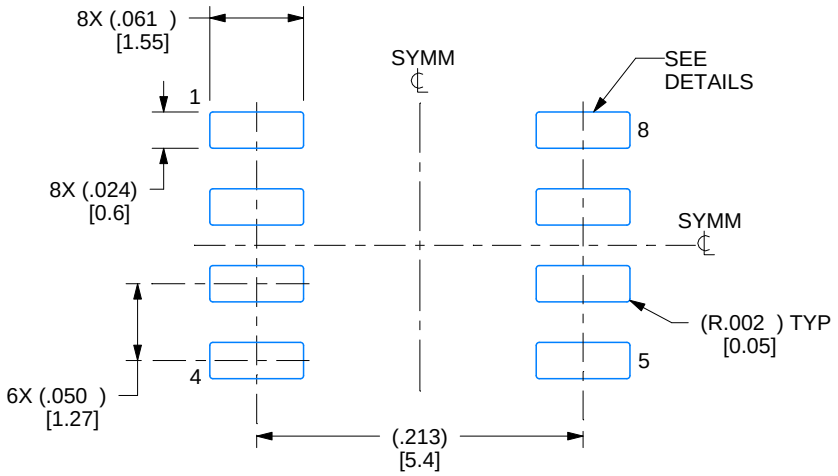
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

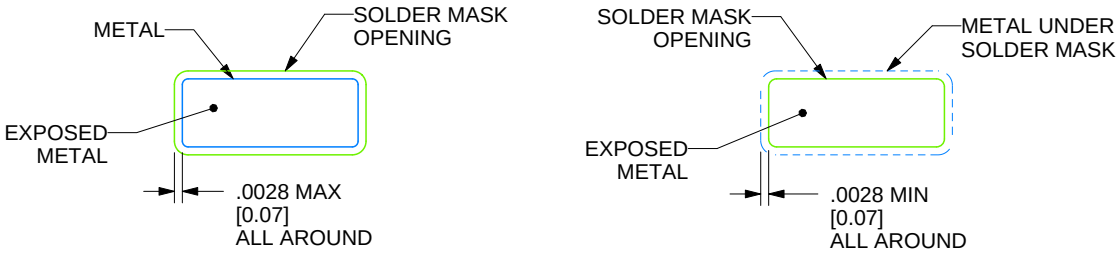


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

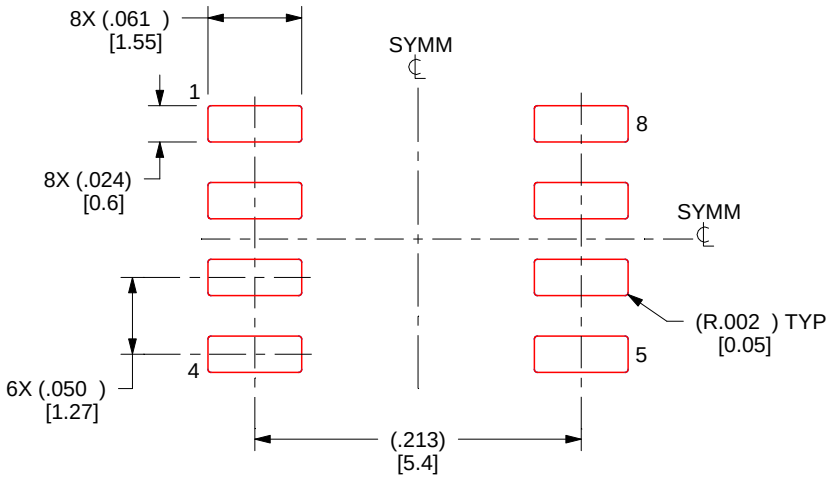
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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