4:1 High-Speed Multiplexer

Check for Samples: OPA4872

FEATURES

- 500MHz SMALL-SIGNAL BANDWIDTH
- 500MHz, $2V_{PP}$ BANDWIDTH
- 0.1dB GAIN FLATNESS to 120MHz
- 10ns CHANNEL SWITCHING TIME
- LOW SWITCHING GLITCH: $40mV_{PP}$
- 2300V/μs SLEW RATE
- 0.035%/0.005° DIFFERENTIAL GAIN, PHASE
- QUIESCENT CURRENT = 10.6mA
- 1.1mA QUIESCENT CURRENT IN SHUTDOWN MODE
- 88dB OFF ISOLATION IN DISABLE OR SHUTDOWN (10MHz)

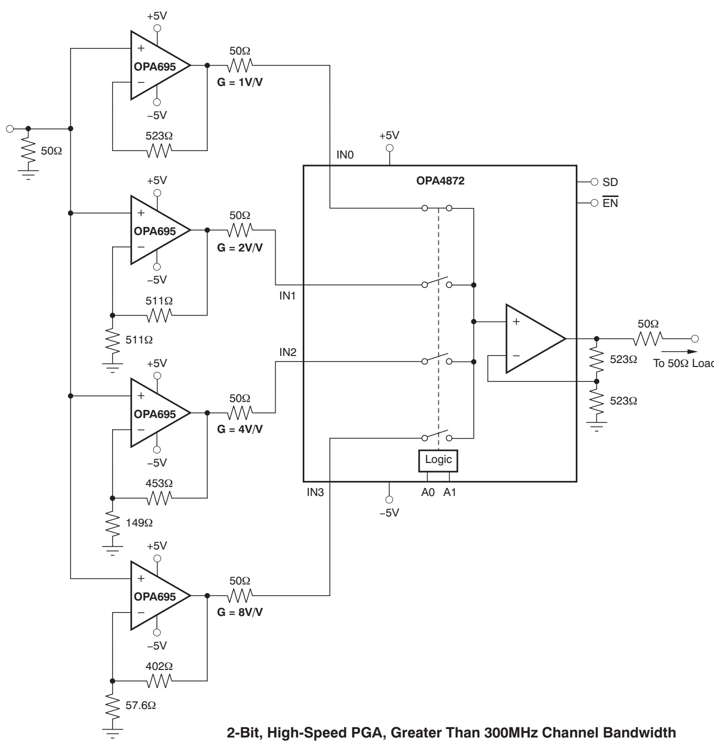
APPLICATIONS

- VIDEO ROUTER
- LCD AND PLASMA DISPLAY
- HIGH SPEED PGA
- DROP-IN UPGRADE TO AD8174

DESCRIPTION

The OPA4872 offers a very wideband 4:1 multiplexer in an SO-14 package. Using only 10.6mA, the OPA4872 provides a user-settable output amplifier gain with greater than 500MHz large-signal bandwidth ($2V_{PP}$). The switching glitch is improved over earlier solutions using a new (patented) input stage switching approach. This technique uses current steering as the input switch while maintaining an overall closed-loop design. The OPA4872 exhibits an off isolation of 88dB in either Disable or Shutdown mode. With greater than 500MHz small-signal bandwidth at a gain of 2, the OPA4872 gives a typical 0.1dB gain flatness to greater than 120MHz.

System power may be optimized using the chip enable feature for the OPA4872. Taking the chip enable ($\overline{EN}$) line high powers down the OPA4872 to less than 3.4mA total supply current. Further power reduction to 1.1mA quiescent current can be achieved by bringing the shutdown (SD) line high. Muxing multiple OPA4872s outputs together, then using the chip enable to select which channels are active, increases the number of possible inputs.



2-Bit, High-Speed PGA, Greater Than 300MHz Channel Bandwidth

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Table 1. ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
OPA4872	SO-14	D	–40°C to +85°C	OPA4872	OPA4872ID	Rails, 50
					OPA4872IDR	Tape and Reel, 2500

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

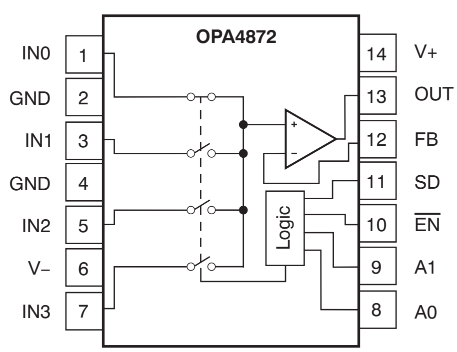
Over operating free-air temperature range, unless otherwise noted.

		OPA4872	UNIT
Power supply		±6.5	V
Internal power dissipation		See Thermal Characteristics	
Input voltage range		$\pm V_S$	V
Storage temperature range		–65 to +125	°C
Junction temperature (T_J)		+150	°C
Junction temperature: continuous operation, long-term reliability		+140	°C
ESD rating	Human body model (HBM)	1300	V
	Charged device model (CDM)	1000	V
	Machine model (MM)	200	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

PIN CONFIGURATION

D PACKAGE
SO-14
(TOP VIEW)



ELECTRICAL CHARACTERISTICS: V_S = ±5V

At T_A = +25°C, G = +2V/V, R_F = 523Ω, and R_L = 150Ω, unless otherwise noted.

		OPA4872						
		TYP	MIN/MAX OVER TEMPERATURE					
PARAMETER	CONDITIONS	+25°C	+25°C[2]	0°C to +70°C[3]	–40°C to +85°C[3]	UNITS	MIN/ MAX	TEST LEVEL[1]
AC PERFORMANCE								
Small-signal bandwidth	V_O = 500mV$_{PP}$, R_L = 150Ω	500	375	360	355	MHz	min	B
Bandwidth for 0.1dB flatness	V_O = 500mV$_{PP}$, R_L = 150Ω	120				MHz	typ	C
Large-signal bandwidth	V_O = 2V$_{PP}$, R_L = 150Ω	500	400	370	350	MHz	min	B
Slew rate	4V step	2300	2150	2025	2000	V/μs	min	B
Rise time and fall time	4V step	1.25	1.4	1.45	1.5	ns	max	B
Settling time to 0.05%	2V step	15				ns	typ	C
to 0.1%	2V step	14	17	17.5	18	ns	max	B
Channel switching time		10	12	12.5	13	ns	max	B
Harmonic distortion	G = +2V/V, f = 10MHz, V_O = 2V$_{PP}$							
2nd-harmonic	R_L = 150Ω	–60	–56	–52	–50	dBc	max	B
3rd-harmonic	R_L = 150Ω	–78	–75	–72	–70	dBc	max	B
Input voltage noise	f > 100kHz	4.5	5.4	5.8	6.2	nV/√Hz	max	B
Noninverting input current noise	f > 100kHz	4.0	4.8	5.0	5.2	pA/√Hz	max	B
Inverting input current noise	f > 100kHz	19	22	23	24	pA/√Hz	max	B
Differential gain	G = +2V/V, PAL, V_O = 1.4V_P	0.035				%	typ	C
Differential phase	G = +2V/V, PAL, V_O = 1.4V_P	0.005				°	typ	C
All hostile crosstalk, input-referred	Three channels driven at 5MHz, 1V$_{PP}$	–80				dB	typ	C
	Three channels driven at 30MHz, 1V$_{PP}$	–66				dB	typ	C
DC PERFORMANCE								
Open-loop transimpedance (Z_{OL})	V_O = 0V, R_L = 100Ω	103	**92**	90	86	kΩ	min	A
Input offset voltage	V_{CM} = 0V	±1	**±5**	±5.7	±6.3	mV	max	A
Average Input offset voltage drift	V_{CM} = 0V			±15	±20	μV/°C	max	B
Input offset voltage matching	V_{CM} = 0V	±1	**±5**	±5.5	±6	mV	max	A
Noninverting input bias current	V_{CM} = 0V	±4	**±14**	±14.7	±15.3	μA	max	A
Average noninverting input bias current	V_{CM} = 0V			±15	±20	nA/°C	max	B
Inverting bias current	V_{CM} = 0V	±4	**±18**	±21.4	±22.9	μA	max	A
Average inverting input bias current	V_{CM} = 0V			±75	±75	nA/°C	max	B
INPUT								
Common-mode input range (CMIR)	Each noninverting input	±2.7	**±2.55**	±2.5	±2.45	V	min	A
Common-mode rejection ratio (CMRR)	V_{CM} = 0V, input-referred, noninverting input	56	**50**	49	48	dB	min	A
Input resistance								
Noninverting	Channel enabled	2.5				MΩ	typ	C
Inverting	open loop	70				Ω	typ	C
Input capacitance								
Noninverting	Channel selected	0.9				pF	typ	C
	Channel deselected	0.9				pF	typ	C
	Chip disabled	0.9				pF	typ	C
OUTPUT								
Output voltage swing	R_L ≥ 1kΩ	±4	**±3.9**	±3.85	±3.8	V	min	A
	R_L = 150Ω	±3.7	**±3.55**	±3.5	±3.45	V	min	A
Output current	V_O = 0V	±75	**±48**	±47	±45	mA	min	A
Short-circuit output current	Output shorted to ground	±100				mA	typ	C
Closed-Loop output impedance	G = +2V/V, f ≤ 100kHz	0.03				Ω	typ	C

(1) Test levels: (A) 100% tested at +25°C. Over temperature limits set by characterization and simulation. (B) Limits set by characterization and simulation. (C) Typical value only for information.
(2) Junction temperature = ambient for +25°C tested specifications.
(3) Junction temperature = ambient at low temperature limit; junction temperature = ambient +9°C at high temperature limit for over temperature specifications.

ELECTRICAL CHARACTERISTICS: V_S = ±5V (continued)

At T_A = +25°C, G = +2V/V, R_F = 523Ω, and R_L = 150Ω, unless otherwise noted.

		OPA4872						
		TYP	MIN/MAX OVER TEMPERATURE					
PARAMETER	CONDITIONS	+25°C	+25°C[2]	0°C to +70°C[3]	–40°C to +85°C[3]	UNITS	MIN/ MAX	TEST LEVEL[1]
ENABLE (EN̄)								
Power-down supply current	$V_{\overline{EN}}$ = 0V	3.4	**3.6**	3.8	3.9	mA	max	A
Disable time	V_{IN} = ±0.25V_{DC}	25				ns	typ	C
Enable time	V_{IN} = ±0.25V_{DC}	6				ns	typ	C
Off isolation	G = +2V/V, f = 10MHz	88				dB	typ	C
Output resistance in disable		14				MΩ	typ	C
Output capacitance in disable		2.5				pF	typ	C
DIGITAL INPUTS								
Maximum logic 0	A0, A1, EN̄, SD		0.8	0.8	0.8	V	max	B
Minimum logic 1	A0, A1, EN̄, SD		2.0	2.0	2.0	V	min	B
Logic input current	A0 , A1, EN̄, SD, input = 0V each line	32	**40**	45	50	µA	max	A
Output switching glitch	Channel selection, at matched load	±20				mV	typ	C
	Channel disable, at matched load	±40				mV	typ	C
	Shutdown, at matched load	±40				mV	typ	C
SHUTDOWN								
Shutdown supply current	V_{SD} = 0V	1.1	**1.3**	1.4	1.5	mA	max	A
Shutdown time	V_{IN} = ±0.25V_{DC}	75				ns	typ	C
Enable time	V_{IN} = ±0.25V_{DC}	15				ns	typ	C
Off isolation	G = +2V/V, f = 10MHz	88				dB	typ	C
Output resistance in shutdown		14				MΩ	typ	C
Output capacitance in shutdown		2.5				pF	typ	C
POWER SUPPLY								
Specified operating voltage		±5				V	typ	C
Minimum operating voltage			±3.5	±3.5	±3.5	V	min	B
Maximum operating voltage			**±6.0**	±6.0	±6.0	V	max	A
Maximum quiescent current	V_S = ±5V	10.6	**11**	11.5	11.7	mA	max	A
Minimum quiescent current	V_S = ±5V	10.6	**10**	9.5	9.3	mA	min	A
Power-supply rejection ratio (+PSRR)	Input-referred	–56	**–50**	–49	–48	dB	min	A
Power-supply rejection ratio (–PSRR)	Input-referred	–57	**–51**	–50	–49	dB	min	A
THERMAL CHARACTERISTICS								
Specified operating range, D package		–40 to +85				°C	typ	C
Thermal resistance, θ_{JA}	Junction-to-ambient							
D SO-14		80				°C/W	typ	C

TYPICAL CHARACTERISTICS

At T_A = +25°C, G = +2V/V, R_F = 523Ω, and R_L = 150Ω, unless otherwise noted.

SMALL-SIGNAL FREQUENCY RESPONSE

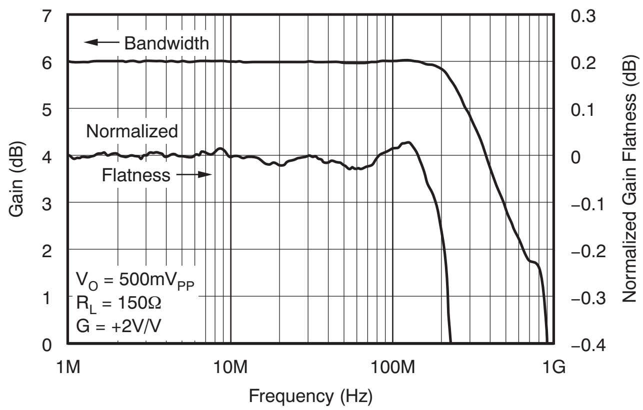


Figure 1.

SMALL-SIGNAL FREQUENCY RESPONSE

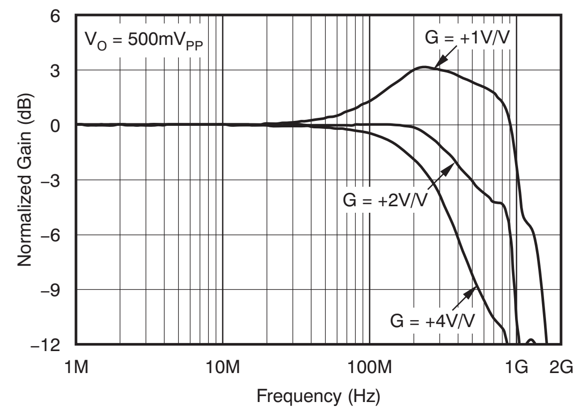


Figure 2.

LARGE-SIGNAL FREQUENCY RESPONSE

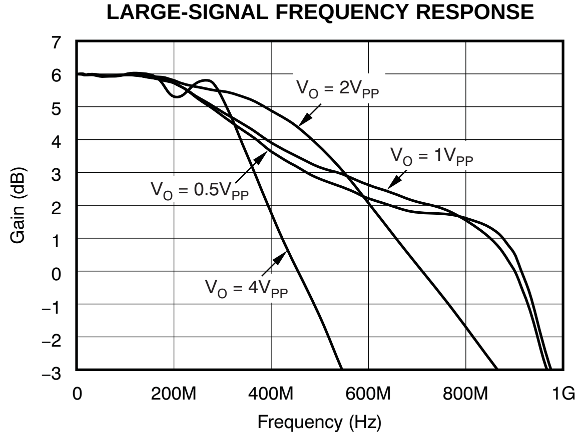


Figure 3.

NONINVERTING PULSE RESPONSE

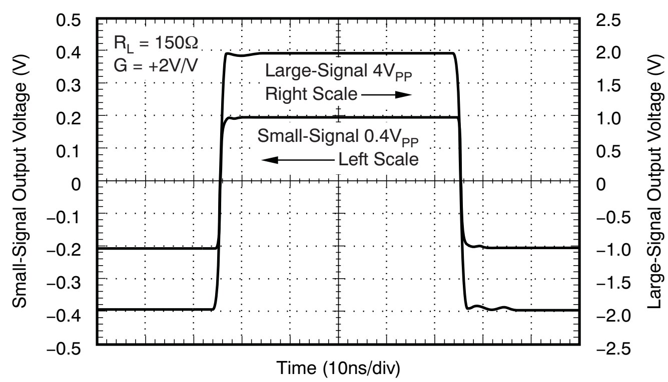


Figure 4.

RECOMMENDED R_S vs CAPACITIVE LOAD

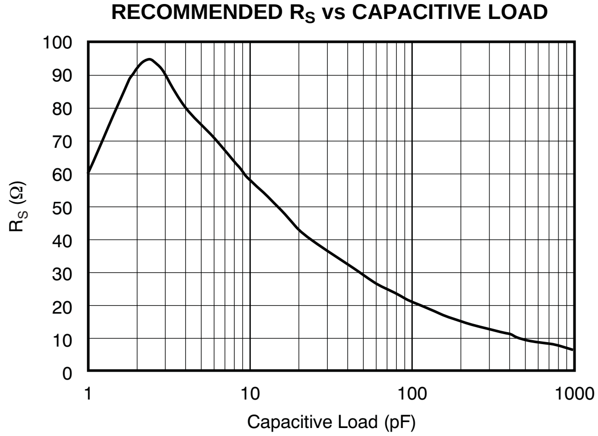


Figure 5.

FREQUENCY RESPONSE vs CAPACITIVE LOAD

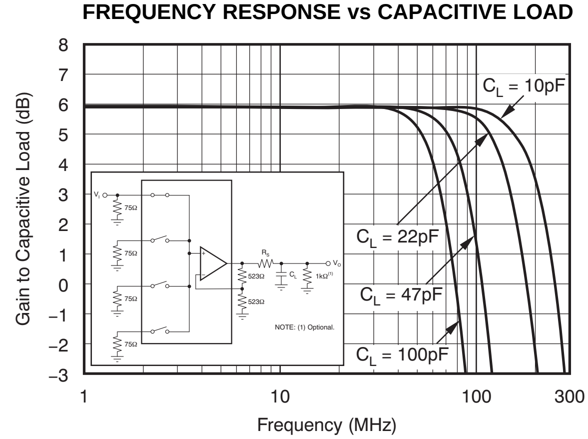


Figure 6.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, G = +2V/V, R_F = 523Ω, and R_L = 150Ω, unless otherwise noted.

HARMONIC DISTORTION vs LOAD RESISTANCE

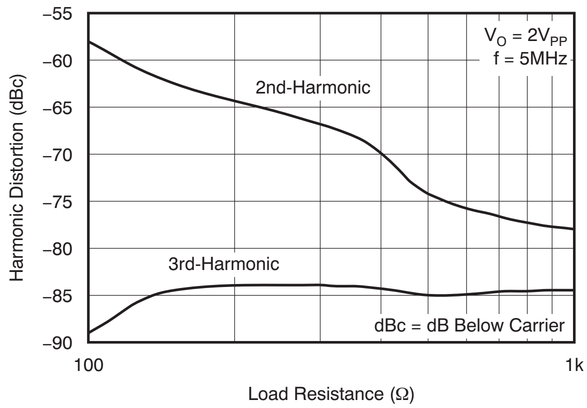


Figure 7.

HARMONIC DISTORTION vs SUPPLY VOLTAGE

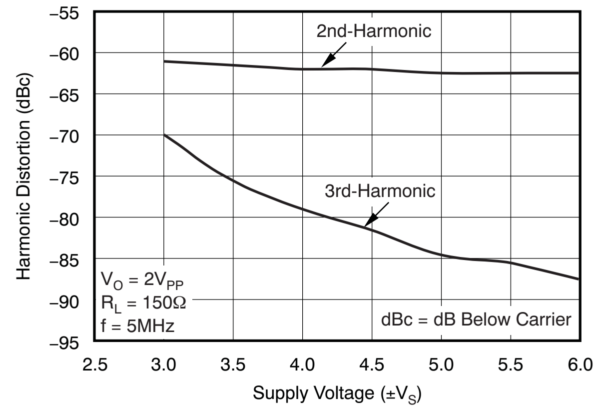


Figure 8.

HARMONIC DISTORTION vs FREQUENCY

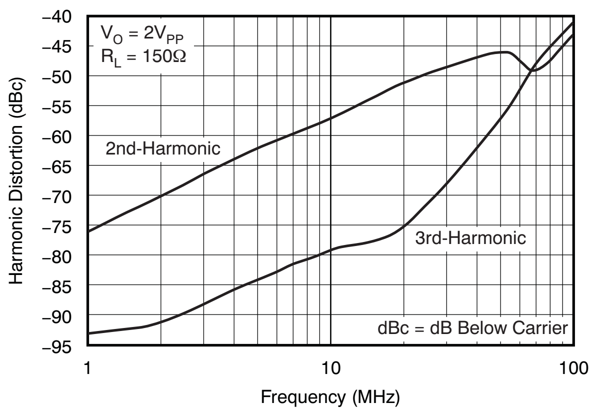


Figure 9.

HARMONIC DISTORTION vs OUTPUT VOLTAGE

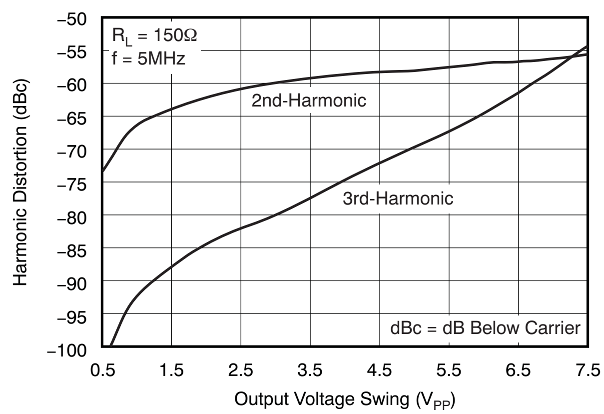


Figure 10.

OUTPUT VOLTAGE AND CURRENT LIMITATIONS

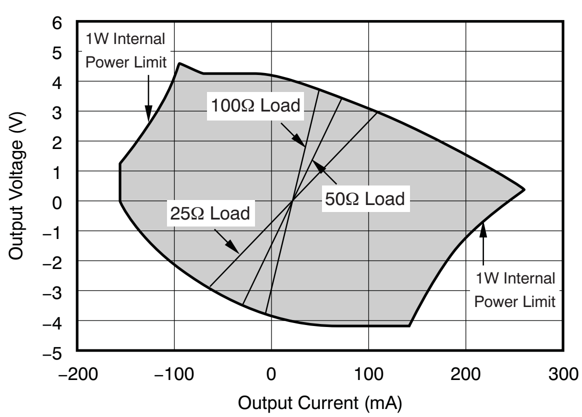


Figure 11.

DISABLE AND SHUTDOWN FEEDTHROUGH vs FREQUENCY

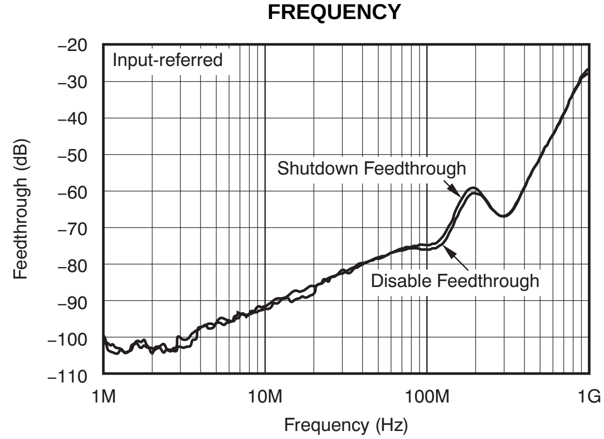


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, G = +2V/V, R_F = 523Ω, and R_L = 150Ω, unless otherwise noted.

CHANNEL-TO-CHANNEL SWITCHING

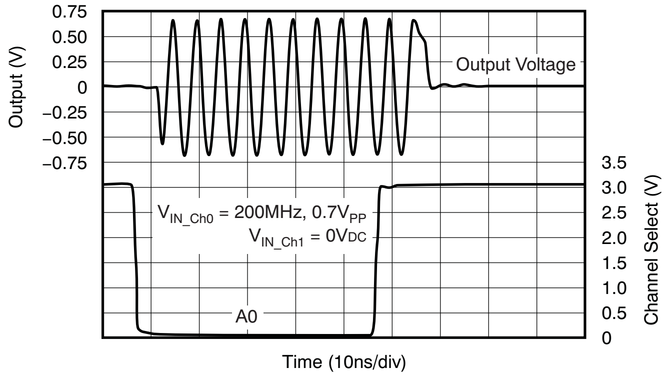


Figure 13.

CHANNEL-TO-CHANNEL SWITCHING GLITCH

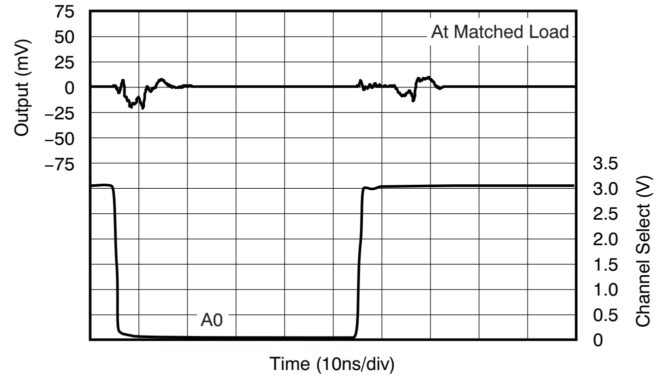


Figure 14.

DISABLE/ENABLE TIME

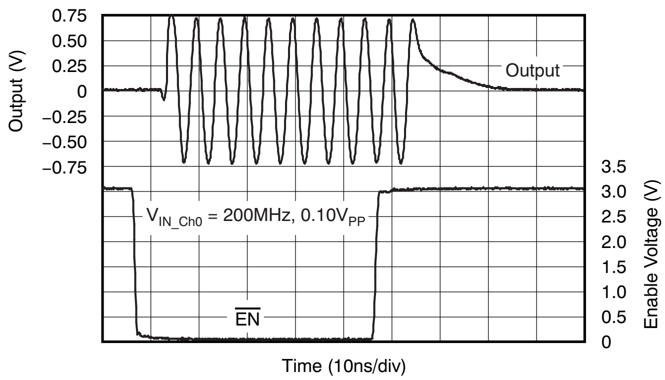


Figure 15.

DISABLE/ENABLE SWITCHING GLITCH

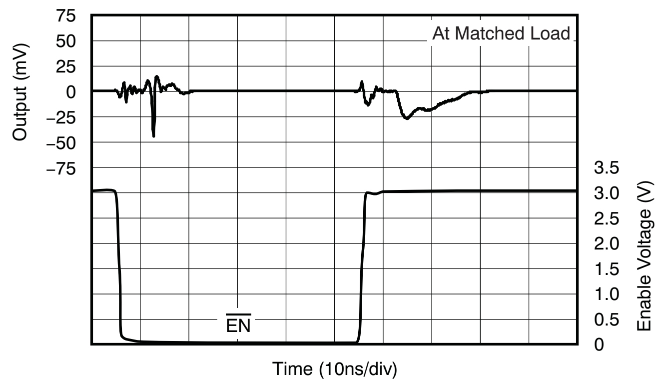


Figure 16.

SHUTDOWN/START-UP TIME

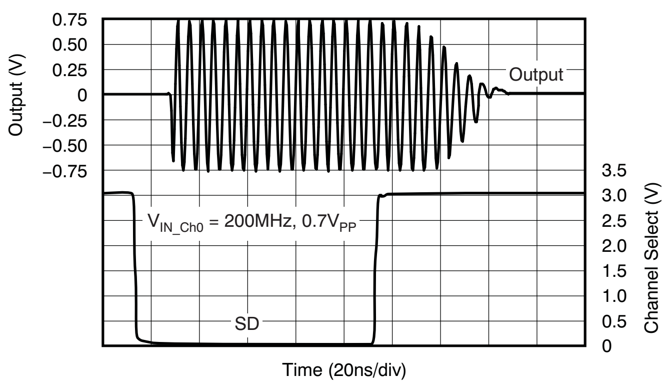


Figure 17.

SHUTDOWN GLITCH

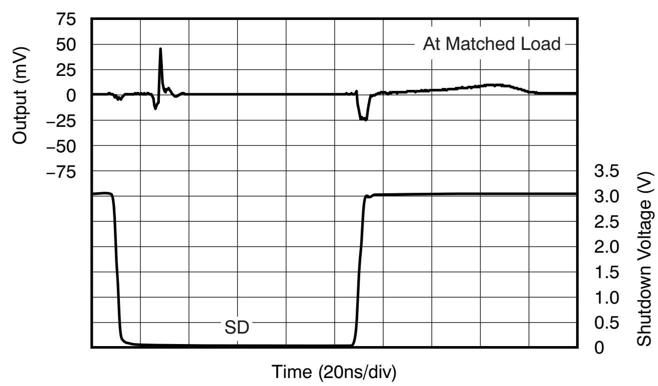


Figure 18.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, G = +2V/V, R_F = 523Ω, and R_L = 150Ω, unless otherwise noted.

ALL HOSTILE CROSSTALK vs FREQUENCY

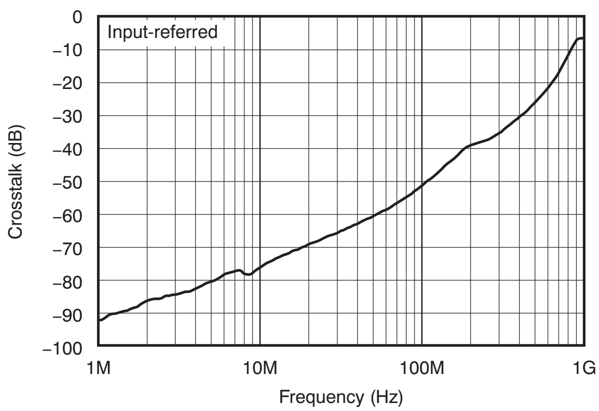


Figure 19.

OPEN-LOOP TRANSIMPEDANCE GAIN AND PHASE vs FREQUENCY

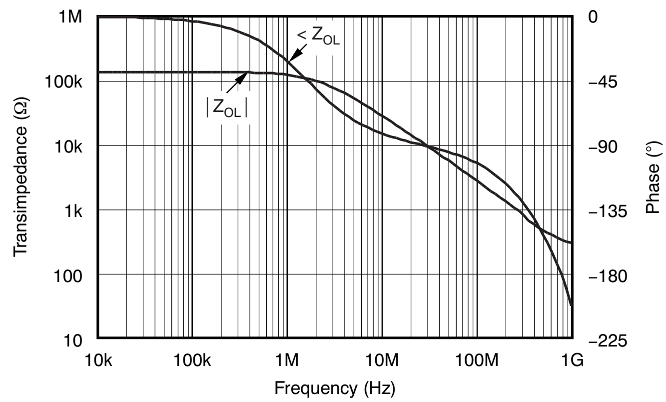


Figure 20.

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

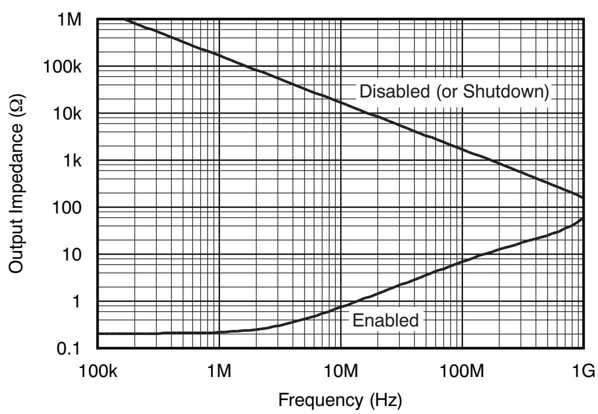


Figure 21.

INPUT IMPEDANCE vs FREQUENCY

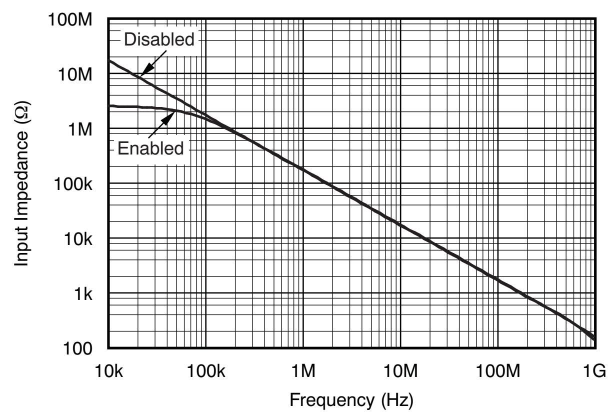


Figure 22.

PSRR vs FREQUENCY

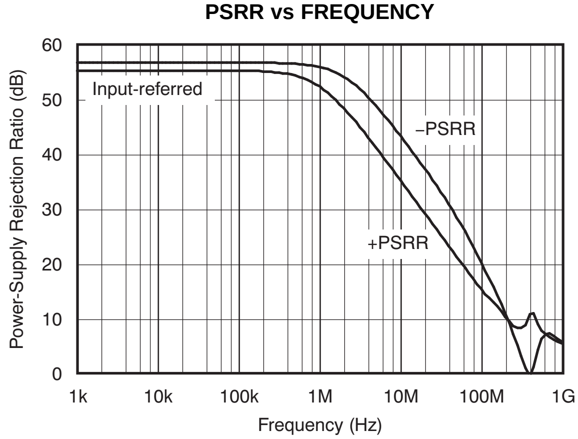


Figure 23.

OUTPUT AND SUPPLY CURRENT vs TEMPERATURE

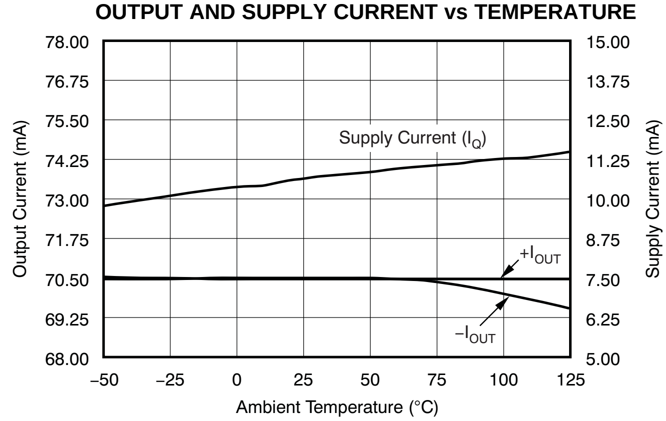


Figure 24.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, G = +2V/V, R_F = 523Ω, and R_L = 150Ω, unless otherwise noted.

TYPICAL DC DRIFT OVER TEMPERATURE

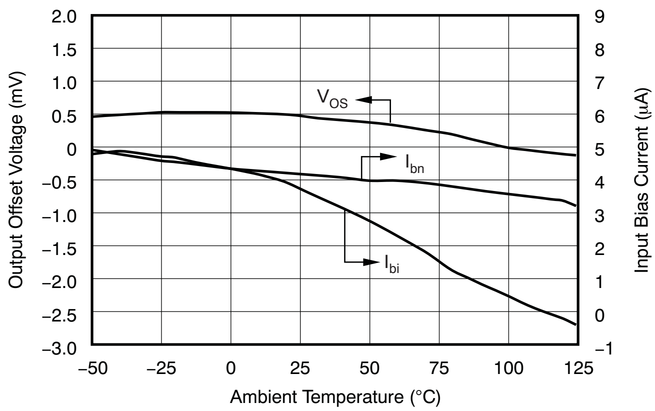


Figure 25.

INPUT VOLTAGE AND CURRENT NOISE

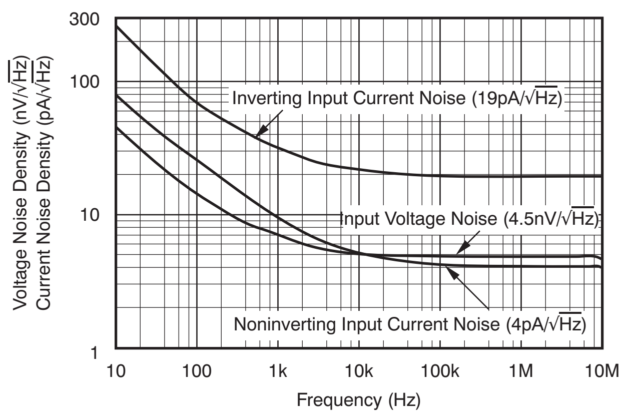


Figure 26.

APPLICATION INFORMATION

WIDEBAND MULTIPLEXER OPERATION

The OPA4872 gives a new level of performance in wideband multiplexers. Figure 27 shows the dc-coupled, gain of +2V/V, dual power-supply circuit used as the basis of the ±5V Electrical Characteristics and Typical Characteristic curves. For test purposes, the input impedance is set to 75Ω with a resistor to ground and the output impedance is set to 75Ω with a series output resistor. Voltage swings reported in the specifications are taken directly at the input and output pins while load powers (in dBm) are defined at a matched 75Ω load. For the circuit of Figure 27, the total effective load will be 150Ω || 1046Ω = 131Ω. Logic pins A0 and A1 control which of the four inputs is selected while $\overline{EN}$ and SD allow for power reduction. One optional component is included in Figure 27. In addition to the usual power-supply decoupling capacitors to ground, a 0.01μF capacitor is included between the two power-supply pins. In practical printed circuit board (PCB) layouts, this optional added capacitor typically improves the 2nd-harmonic distortion performance by 3dB to 6dB for bipolar supply operation.

Even though the internal architecture of the OPA4872 includes current steering, it is advantageous to look at it as four switches looking into the noninverting input of a current feedback amplifier. Depending on the logic applied to channel control pins A0 and A1, one switch is on at all times. Figure 27 represents the OPA4872 in this configuration. The truth table for channel selection is shown in Table 2.

Table 2. TRUTH TABLE

A0	A1	$\overline{EN}$	SD	V_{OUT}
0	0	0	0	IN0
1	0	0	0	IN1
0	1	0	0	IN2
1	1	0	0	IN3
X	X	1	0	High-Z, I_Q = 3.4mA
X	X	X	1	High-Z, I_Q = 1.1mA

The OPA4872 is in disable mode, with a quiescent current of 3.4mA typical, when the $\overline{EN}$ pin is set to 0V. After being placed in disable mode, the OPA4872 is fully enabled in 6ns. For further power savings, the SD pin can be used. Setting the SD pin to 5V places the device in shutdown mode with a standing quiescent current of 1.1mA. Note that in this shutdown mode, the OPA4872 requires 15ns to be fully powered again. The truth table for disable and shutdown modes can be found in Table 2.

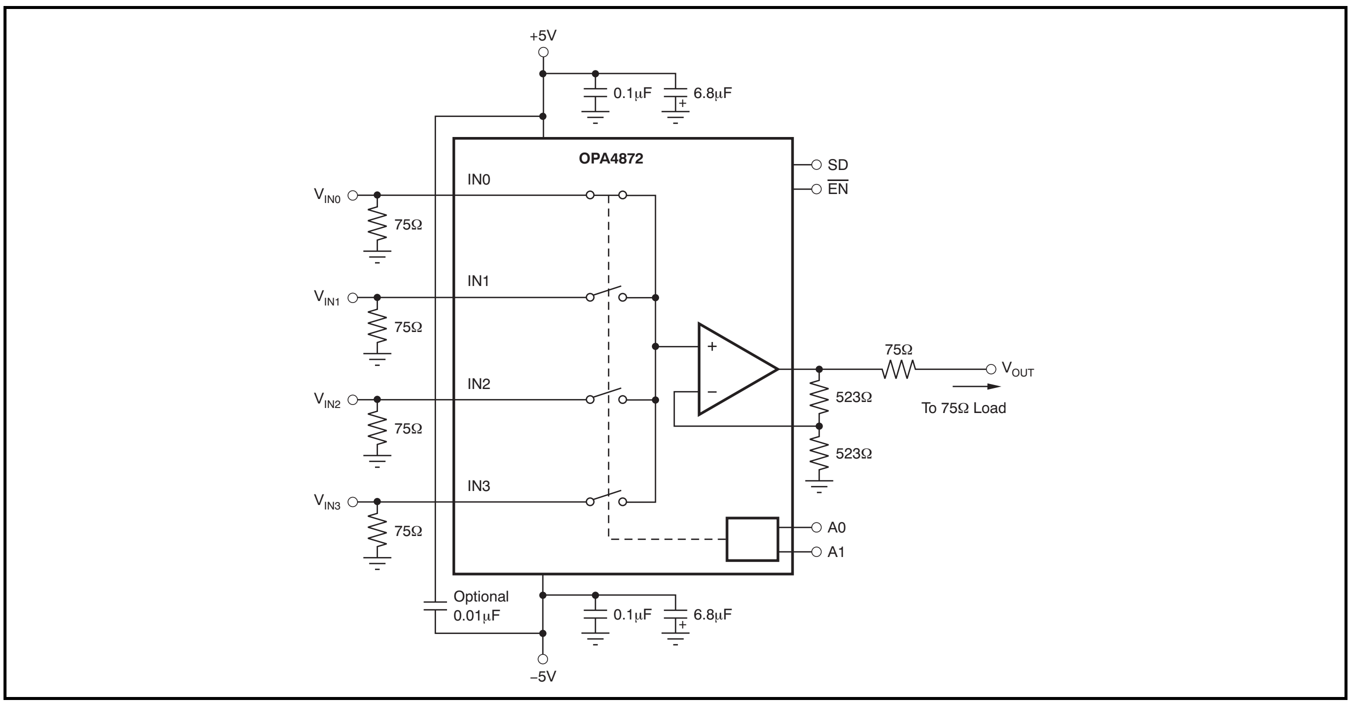


Figure 27. DC-Coupled, G = +2V/V Bipolar Specification and Test Circuit (Channel 0 Selected)

2-BIT HIGH-SPEED PGA

The OPA4872 can be used as a 2-bit, high-speed programmable gain amplifier (PGA) when used in conjunction with another amplifier. Figure 28 shows one OPA695 used in series with each OPA4876 input and configured with gains of +1V/V, +2V/V, +4V/V, and +8V/V, respectively.

When channel 0 is selected, the overall gain to the matched load of the OPA4872 is 0dB. When channel 1 is selected, this circuit delivers 6dB of gain to the matched load. When channel 2 is selected, this circuit delivers 12dB of gain to the matched load. When channel 3 is selected, this circuit delivers 18dB of gain to the matched load.

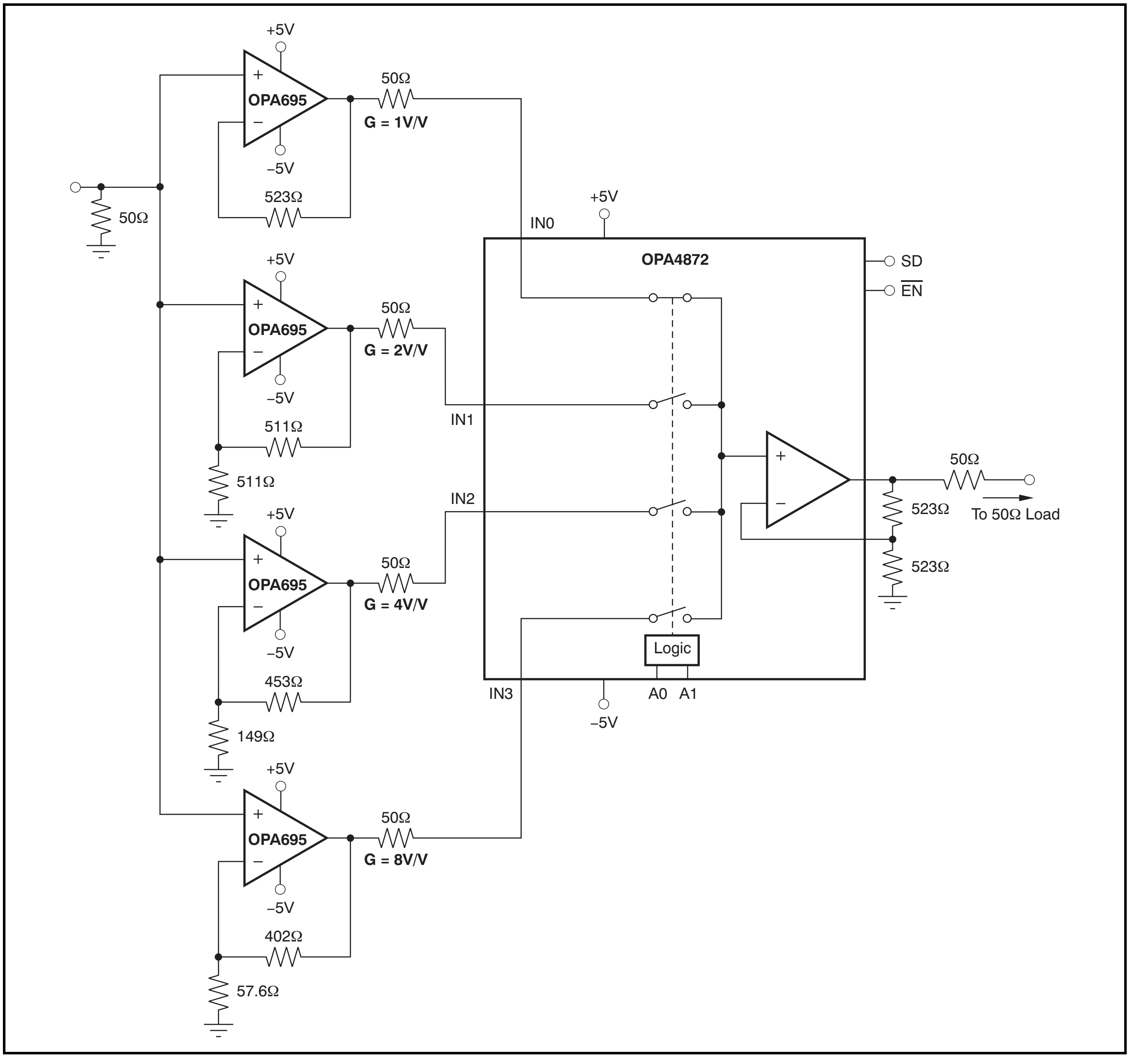


Figure 28. 2-Bit, High-Speed PGA, Greater Than 300MHz Channel Bandwidth

2-BIT, HIGH-SPEED ATTENUATOR

In contrast to the PGA, a two-bit high-speed attenuator can be implemented by using an R-2R ladder together with the OPA4872. Figure 29 shows such an implementation.

Channel 0 sees the full input signal amplitude, where as channel 1 sees 1/2 V_{IN}, channel 2 see 1/4 V_{IN} and channel 3 sees 1/8 V_{IN}.

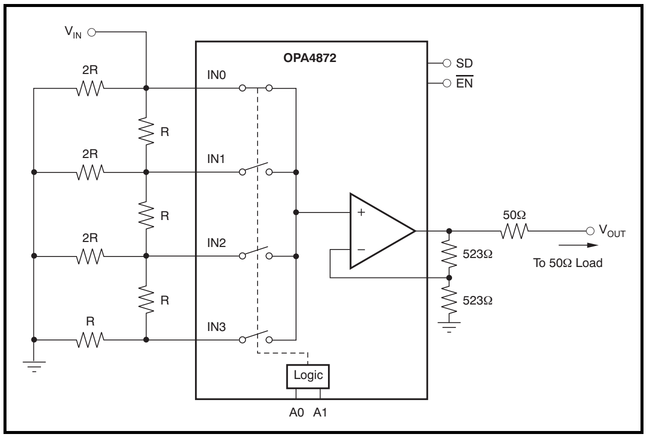


Figure 29. 2-Bit, High-Speed Attenuator, 500MHz Channel Bandwidth

4-INPUT RGB ROUTER

Three OPA4872s can be used together to form a four-input RGB router. The router for the red component is shown in Figure 30. Identical stages would be used for the green and blue channels.

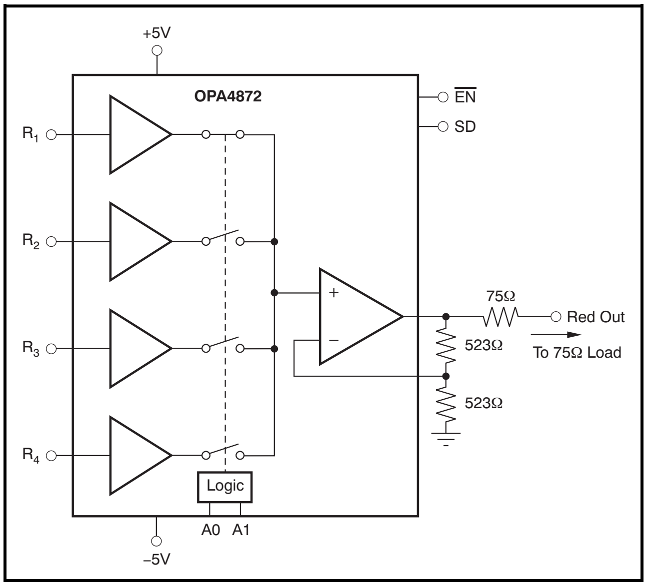


Figure 30. 4-Input RGB Router (Red Channel Shown)

8-TO-1 VIDEO MULTIPLEXER

Two OPA4872s can be used together to form an 8-input video multiplexer. The multiplexer is shown in Figure 31.

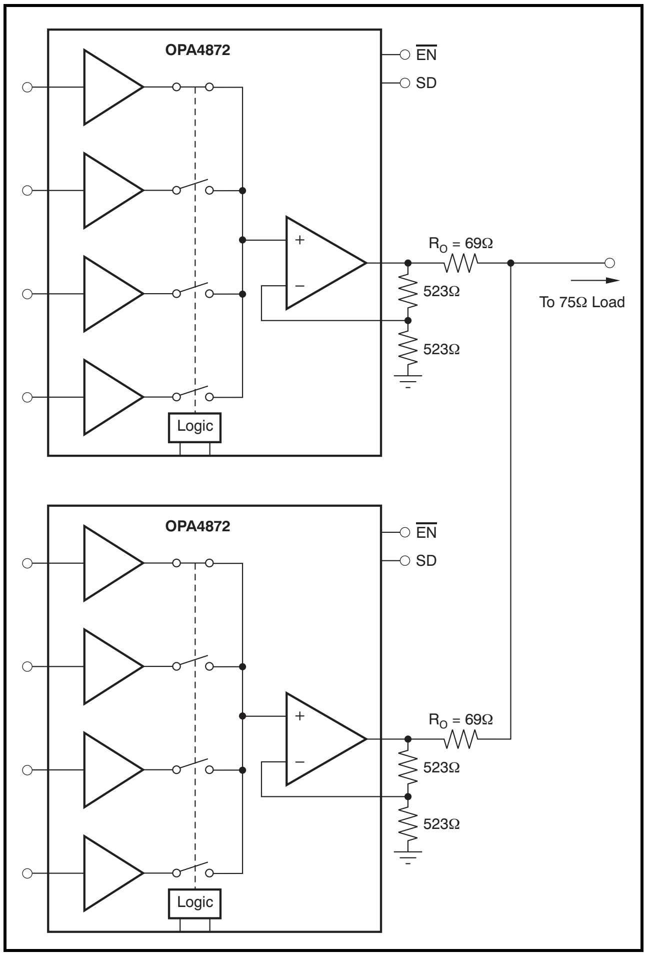


Figure 31. 8-to-1 Video Multiplexer

When connecting OPA4872 outputs together, maintain a gain of +1V/V at the load. The OPA4872 configuration shown is a gain of +6dB; thus, the matching resistance must be selected to achieve –6dB.

The set of equations to solve are shown in Equation 1 and Equation 2. Here, the impedance of interest is 75Ω.

$$\begin{cases} R_O = Z_O \parallel (R_O + R_F + R_G) \\ 1 + \dfrac{R_F}{R_G} = 2 \end{cases} \quad (1)$$

$$\begin{cases} R_F + R_G = 1046\Omega \\ R_F = R_G \end{cases} \quad (2)$$

Solving for R_O, with *n* devices connected together, results in Equation 3:

$$R_O = \frac{75 \times (n-1) + 804}{2} \times \left(\sqrt{1 + \frac{241200}{[75 \times (n-1) + 804]^2}} - 1 \right) \quad (3)$$

Results for *n* varying from 2 to 6 are given in Table 3.

Table 3. Series Resistance versus Number of Parallel Outputs

NUMBER OF OPA4872s	R_O (Ω)
2	69
3	63.94
4	59.49
5	55.59
6	52.15

The two major limitations of this circuit are the device requirements for each OPA4872 and the acceptable return loss resulting from the mismatch between the load and the matching resistor.

DESIGN-IN TOOLS

DEMONSTRATION FIXTURE

A printed circuit board (PCB) is available to assist in the initial evaluation of circuit performance using the OPA4872. The fixture is offered free of charge as an unpopulated PCB, delivered with a user's guide. The summary information for this fixture is shown in Table 4.

Table 4. OPA4872 Demonstration Fixture

PRODUCT	PACKAGE	ORDERING NUMBER	LITERATURE NUMBER
OPA4872	SO-14	DEM-OPA-SO-1E	SBOU045

The demonstration fixture can be requested at the Texas Instruments web site at (www.ti.com) through the OPA4872 product folder.

MACROMODELS AND APPLICATIONS SUPPORT

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. This practice is particularly true for video and RF amplifier circuits, where parasitic capacitance and inductance can have a major effect on circuit performance. A SPICE model for the OPA4872 is available through the Texas Instruments web site at www.ti.com. This model does a good job of predicting small-signal ac and transient performance under a wide variety of operating conditions. It does not do as well in predicting the harmonic distortion or dG/dP characteristics.

OPERATING SUGGESTIONS

SETTING RESISTOR VALUES TO OPTIMIZE BANDWIDTH

The output stage of the OPA4872 is a current-feedback op amp, meaning it can hold an almost constant bandwidth over signal gain settings with the proper adjustment of the external resistor values. This performance is shown in the Typical Characteristic curves; the small-signal bandwidth decreases only slightly with increasing gain. These curves also show that the feedback resistor has been changed for each gain setting. The resistor values on the feedback path can be treated as frequency response compensation elements while the ratio sets the signal gain of the feedback resistor divided by the gain resistor. Figure 32 shows the small-signal frequency response analysis circuit for a current feedback amplifier.

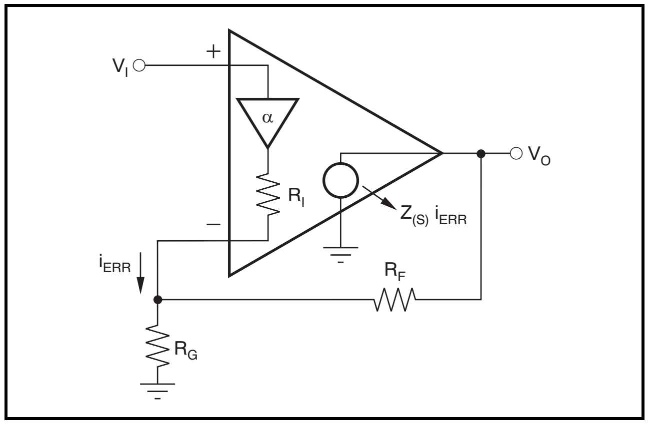


Figure 32. Recommended Feedback Resistor versus Noise Gain

The key elements of this current-feedback op amp model are:

α → Buffer gain from the noninverting input to the inverting input

R_I → Buffer output impedance

i_{ERR} → Feedback error current signal

$Z_{(s)}$ → Frequency-dependent open-loop transimpedance gain from i_{ERR} to V_O

The buffer gain is typically very close to 1.00 and is normally neglected from signal gain considerations. It will, however, set the CMRR for a single op amp differential amplifier configuration. For a buffer gain α < 1.0, the CMRR = –20 × log (1 – α) dB.

R_I, the buffer output impedance, is a critical portion of the bandwidth control equation. R_I for the OPA4872 is typically about 30Ω. A current-feedback op amp senses an error current in the inverting node (as opposed to a differential input error voltage for a voltage-feedback op amp) and passes this on to the output through an internal frequency dependent transimpedance gain. The Typical Characteristics show this open-loop transimpedance response. This open-loop response is analogous to the open-loop voltage gain curve for a voltage-feedback op amp. Developing the transfer function for the circuit of Figure 32 gives Equation 4:

$$\frac{V_O}{V_I} = \frac{\alpha\left(1+\frac{R_F}{R_G}\right)}{1+\frac{R_F+R_I\left(1+\frac{R_F}{R_G}\right)}{Z_{(S)}}} = \frac{\alpha NG}{1+\frac{R_F+R_I NG}{Z_{(S)}}}$$

where:

$$NG = \left(1+\frac{R_F}{R_G}\right) \quad (4)$$

This formula is written in a loop-gain analysis format, where the errors arising from a noninfinite open-loop gain are shown in the denominator. If $Z_{(S)}$ were infinite over all frequencies, the denominator of Equation 4 would reduce to 1 and the ideal desired signal gain shown in the numerator would be achieved. The fraction in the denominator of Equation 4 determines the frequency response. Equation 5 shows this as the loop-gain equation:

$$\frac{Z_{(S)}}{R_F + R_I\,NG} = \text{Loop Gain} \quad (5)$$

If 20 × log(R_F + NG × R_I) were drawn on top of the open-loop transimpedance plot, the difference between the two calculations would be the loop gain at a given frequency. Eventually, $Z_{(S)}$ rolls off to equal the denominator of Equation 5, at which point the loop gain reduces to 1 (and the curves intersect). This point of equality is where the amplifier closed-loop frequency response given by Equation 4 starts to roll off, and is exactly analogous to the frequency at which the noise gain equals the open-loop voltage gain for a voltage-feedback op amp. The difference here is that the total impedance in the denominator of Equation 5 may be controlled somewhat separately from the desired signal gain (or NG).

The OPA4872 is internally compensated to give a maximally flat frequency response for R_F = 523Ω at NG = 2 on ±5V supplies. Evaluating the denominator of Equation 5 (which is the feedback transimpedance) gives an optimal target of 663Ω. As the signal gain changes, the contribution of the NG × R_I term in the feedback transimpedance will change, but the total can be held constant by adjusting R_F. Equation 6 gives an approximate equation for optimum R_F over signal gain:

$$R_F = 663\Omega - NG \times R_I \quad (6)$$

As the desired signal gain increases, this equation will eventually predict a negative R_F. A somewhat subjective limit to this adjustment can also be set by holding R_G to a minimum value of 20Ω. Lower values load both the buffer stage at the input and the output stage, if R_F gets too low, actually decreasing the bandwidth. Figure 33 shows the recommended R_F versus NG for ±5V operation. The values for R_F versus gain shown here are approximately equal to the values used to generate the Typical Characteristics. They differ in that the optimized values used in the Typical Characteristics are also correcting for board parasitics not considered in the simplified analysis leading to Equation 5. The values shown in Figure 33 give a good starting point for design where bandwidth optimization is desired.

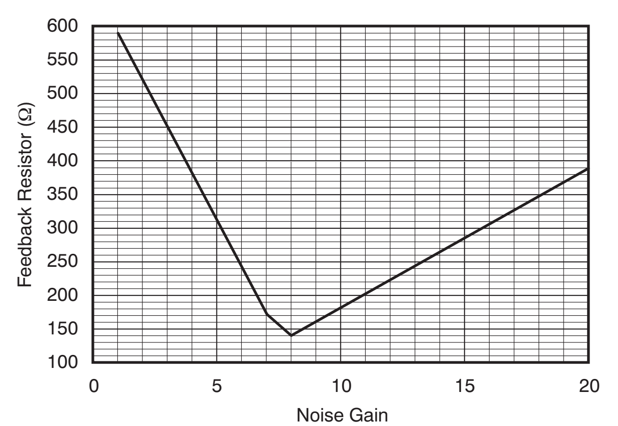


Figure 33. Feedback Resistor vs Noise Gain

The total impedance going into the inverting input may be used to adjust the closed-loop signal bandwidth. Inserting a series resistor between the inverting input and the summing junction increases the feedback impedance (denominator of Equation 4), decreasing the bandwidth.

DRIVING CAPACITIVE LOADS

One of the most demanding, yet very common load conditions, is capacitive loading. Often, the capacitive load is the input of an analog-to-digital converter (ADC)—including additional external capacitance that may be recommended to improve ADC linearity. A high-speed device such as the OPA4872 can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the device open-loop output resistance is considered, this capacitive load introduces an additional pole in the signal path that can decrease the phase margin. Several external solutions to this problem have been suggested. When the primary considerations are frequency response flatness, pulse response fidelity, and/or distortion, the simplest and most effective solution is to isolate the capacitive load from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This isolation resistor does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero acts to cancel the phase lag from the capacitive load pole, thus increasing the phase margin and improving stability.

The Typical Characteristics show the recommended R_S versus capacitive load and the resulting frequency response at the load; see Figure 5. Parasitic capacitive loads greater than 2pF can begin to degrade the performance of the OPA4872. Long PCB traces, unmatched cables, and connections to multiple devices can easily cause this value to be exceeded. Always consider this effect carefully, and add the recommended series resistor as close as possible to the OPA4872 output pin (see the *Board Layout Guidelines* section).

DC ACCURACY

The OPA4872 offers excellent dc signal accuracy. Parameters that influence the output dc offset voltage are:

- Output offset voltage
- Input bias current
- Gain error
- Power-supply rejection ratio
- Temperature

Leaving both temperature and gain error parameters aside, the output offset voltage envelope can be described as shown in Equation 7:

$$V_{OSO\_envelope} = V_{OS} \times G \pm I_{bi} \times R_F \pm (R_S \times I_b) \times G \pm \left|5 - (V_{S+})\right| \times 10^{-\frac{PSRR+}{20}} \pm \left|-5 - (V_{S-})\right| \times 10^{-\frac{PSRR-}{20}} \quad (7)$$

Where:

R_S: Input resistance seen by R0, R1, G0, G1, B0, or B1.

I_b: Noninverting input bias current

I_{bi}: Inverting input bias current

G: Gain

V_{S+}: Positive supply voltage

V_{S-}: Negative supply voltage

PSRR+: Positive supply PSRR

PSRR–: Negative supply PSRR

V_{OS} : Input Offset Voltage

Evaluating the front-page schematic, using a worst-case, +25°C offset voltage, bias current and PSRR specifications and operating at ±6V, gives a worst-case output equal to Equation 8:

$$\pm 10mV + 75\Omega \times \pm 14\mu A \times 2 + 523\Omega \times \pm 18\mu A \pm \left|5 - 6\right| \times 10^{-\frac{50}{20}} \pm \left|-5 - (-6)\right| \times 10^{-\frac{51}{20}} = \pm 29.2mV \quad (8)$$

DISTORTION PERFORMANCE

The OPA4872 provides good distortion performance into a 150Ω load on ±5V supplies. Relative to alternative solutions, it provides exceptional performance into lighter loads. Generally, until the fundamental signal reaches very high frequency or power levels, the 2nd harmonic dominates the distortion with a negligible 3rd harmonic component. Focusing then on the 2nd harmonic, increasing the load impedance directly improves distortion. Also, providing an additional supply decoupling capacitor (0.01µF) between the supply pins (for bipolar operation) improves the 2nd-order distortion slightly (3dB to 6dB).

In most op amps, increasing the output voltage swing increases harmonic distortion directly. The Typical Characteristics show the 2nd harmonic increasing at a little less than the expected 2X rate while the 3rd harmonic increases at a little less than the expected 3X rate. Where the test power doubles, the 2nd harmonic increases only by less than the expected 6dB, whereas the 3rd harmonic increases by less than the expected 12dB.

NOISE PERFORMANCE

The OPA4872 offers an excellent balance between voltage and current noise terms to achieve low output noise. The inverting current noise ($19pA/\sqrt{Hz}$) is significantly lower than earlier solutions, while the input voltage noise ($4.5nV/\sqrt{Hz}$) is lower than most unity-gain stable, wideband, voltage-feedback op amps. As long as the ac source impedance looking out of the noninverting node is less than 100Ω, this current noise will not contribute significantly to the total output noise. The op amp input voltage noise and the two input current noise terms combine to give low output noise under a wide variety of operating conditions. Figure 34 shows the OPA4872 noise analysis model with all the noise terms included. In this model, all noise terms are taken to be noise voltage or current density terms in either $nV/\sqrt{Hz}$ or $pA/\sqrt{Hz}$.

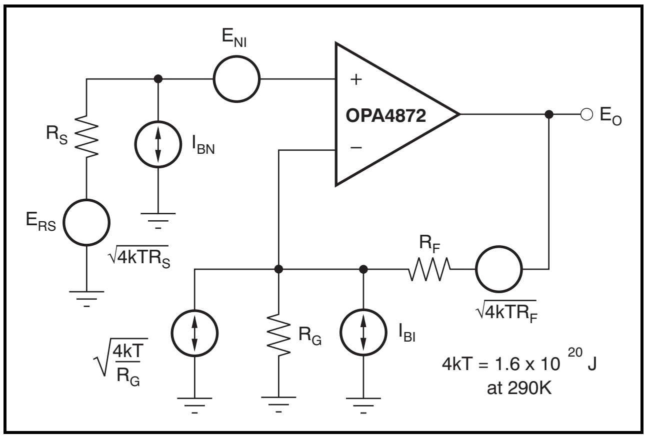


Figure 34. Op Amp Noise Analysis Model

The total output spot noise voltage can be computed as the square root of the sum of all squared output noise voltage contributors. Equation 9 shows the general form for the output noise voltage using the terms shown in Figure 35.

$$E_O = \sqrt{\left(E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S\right)NG^2 + (I_{BI}R_F)^2 + 4kTR_FNG} \tag{9}$$

Dividing this expression by the noise gain ($NG = (1 + R_F/R_G)$) gives the equivalent input-referred spot noise voltage at the noninverting input, as shown in Equation 10.

$$E_O = \sqrt{E_{NI}^2 + (I_{BN}R_S)^2 + 4kTR_S + \left(\frac{I_{BI}R_F}{NG}\right)^2 + \frac{4kTR_F}{NG}} \tag{10}$$

Evaluating these two equations for the OPA4872 circuit and component values (see Figure 27) gives a total output spot noise voltage of $14.2nV/\sqrt{Hz}$ and a total equivalent input spot noise voltage of $7.1nV/\sqrt{Hz}$. This total input-referred spot noise voltage is higher than the $4.5nV/\sqrt{Hz}$ specification for the OPA4872 voltage noise alone. This voltage reflects the noise added to the output by the inverting current noise times the feedback resistor. If the feedback resistor is reduced in high-gain configurations, the total input-referred voltage noise given by Equation 10 approaches only the $4.5nV/\sqrt{Hz}$ of the op amp itself. For example, going to a gain of +10 using R_F = 178Ω gives a total input-referred noise of $4.7nV/\sqrt{Hz}$.

THERMAL ANALYSIS

Heatsinking or forced airflow may be required under extreme operating conditions. Maximum desired junction temperature sets the maximum allowed internal power dissipation as discussed in this document. In no case should the maximum junction temperature be allowed to exceed +150°C.

Operating junction temperature (T_J) is given by $T_A + P_D \times \theta_{JA}$. The total internal power dissipation (P_D) is the sum of quiescent power (P_{DQ}) and additional power dissipated in the output stage (P_{DL}) to deliver load power. Quiescent power is simply the specified no-load supply current times the total supply voltage across the part. P_{DL} depends on the required output signal and load; for a grounded resistive load, P_{DL} is at a maximum when the output is fixed at a voltage equal to 1/2 of either supply voltage (for equal bipolar supplies). Under this condition $P_{DL} = V_S{}^2/(4 \times R_L)$, where R_L includes feedback network loading.

Note that it is the power in the output stage and not in the load that determines internal power dissipation.

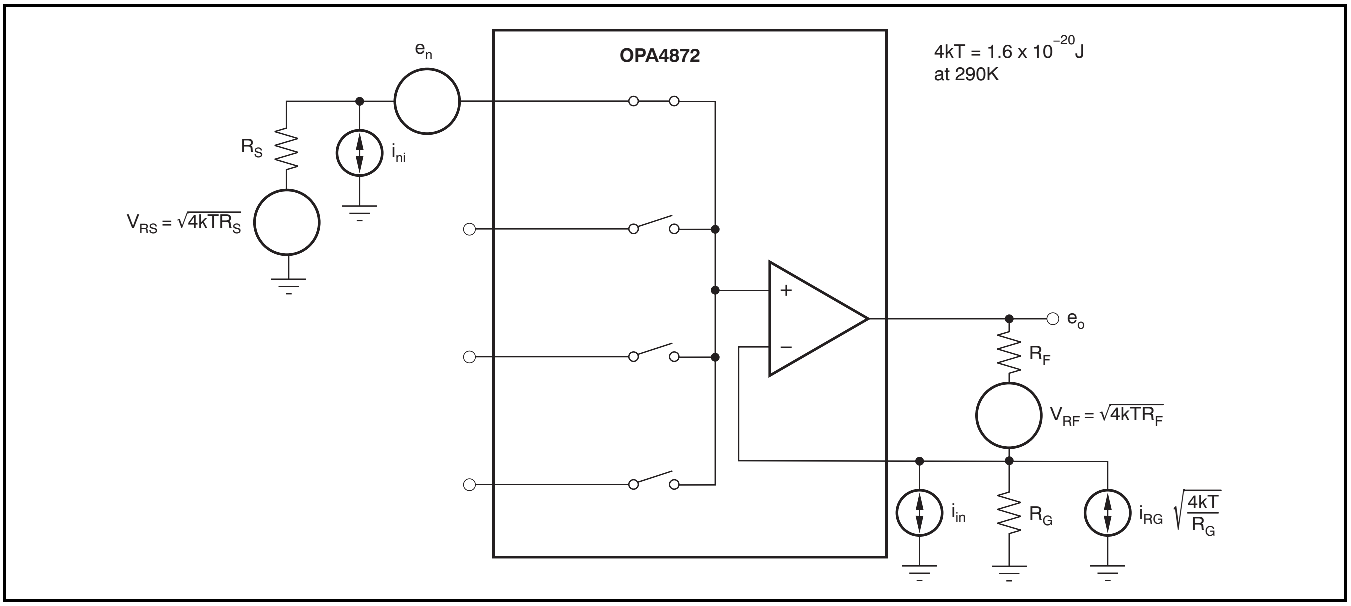


Figure 35. OPA4872 Noise Analysis Model

As a worst-case example, compute the maximum T_J using an OPA4872ID in the circuit of Figure 27 operating at the maximum specified ambient temperature of +85°C with its output driving a grounded 100Ω load to +2.5V:

$$P_D = 10V \times 11.7mA + \left(5^2/[4 \times (150\Omega \parallel 1046\Omega)]\right) = 165mW$$

$$\text{Maximum } T_J = +85°C + (165mW \times 80°C/W) = 98°C$$

This worst-case condition does not exceed the maximum junction temperature. Normally, this extreme case is not encountered.

BOARD LAYOUT GUIDELINES

Achieving optimum performance with a high-frequency amplifier such as the OPA4872 requires careful attention to board layout parasitics and external component types. Recommendations to optimize performance include:

a) Minimize parasitic capacitance to any ac ground for all of the signal I/O pins. Parasitic capacitance on the output pin can cause instability; on the noninverting input, it can react with the source impedance to cause unintentional bandlimiting. To reduce unwanted capacitance, a window around the signal I/O pins should be opened in all of the ground and power planes around those pins. Otherwise, ground and power planes should be unbroken elsewhere on the board.

b) Minimize the distance (< 0.25") from the power-supply pins to high frequency 0.1μF decoupling capacitors. At the device pins, the ground and power plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power-supply connections (on pins 9, 11, 13, and 15) should always be decoupled with these capacitors. An optional supply decoupling capacitor across the two power supplies (for bipolar operation) improves 2nd harmonic distortion performance. Larger (2.2μF to 6.8μF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These capacitors may be placed somewhat farther from the device and may be shared among several devices in the same area of the PCB.

c) Careful selection and placement of external components will preserve the high-frequency performance of the OPA4872. Resistors should be a very low reactance type. Surface-mount resistors work best and allow a tighter overall layout. Metal-film and carbon composition, axially-leaded resistors can also provide good high-frequency performance. Again, keep their leads and PCB trace length as short as possible. Never use wirewound type resistors in a high-frequency application. Other network components, such as noninverting input termination resistors, should also be placed close to the package.

d) Connections to other wideband devices on the board may be made with short direct traces or through onboard transmission lines. For short connections, consider the trace and the input to the next device as a lumped capacitive load. Relatively wide traces (50mils to 100mils) should be used, preferably with ground and power planes opened up around them.

Estimate the total capacitive load and set R_S from the plot of Figure 5. Low parasitic capacitive loads (greater than 5pF) may not need an R_S because the OPA4872 is nominally compensated to operate with a 2pF parasitic load. If a long trace is required, and the 6dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50Ω environment is normally not necessary on the board, and in fact, a higher impedance environment improves distortion as shown in the Distortion versus Load plot; see Figure 7. With a characteristic board trace impedance defined based on board material and trace dimensions, a matching series resistor into the trace from the output of the OPA4872 is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance will be the parallel combination of the shunt resistor and the input impedance of the destination device; this total effective impedance should be set to match the trace impedance. The high output voltage and current capability of the OPA4872 allows multiple destination devices to be handled as separate transmission lines, each with its own series and shunt terminations. If the 6dB attenuation of a doubly-terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and set the series resistor value as shown in Figure 5. This configuration does not preserve signal integrity as well as a doubly-terminated line. If the input impedance of the destination device is low, there will be some signal attenuation because of the voltage divider formed by the series output into the terminating impedance.

e) Socketing a high-speed part like the OPA4872 is not recommended. The additional lead length and pin-to-pin capacitance introduced by the socket can create an extremely troublesome parasitic network that can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the OPA4872 onto the board.

INPUT AND ESD PROTECTION

The OPA4872 is built using a very high-speed complementary bipolar process. The internal junction breakdown voltages are relatively low for these very small geometry devices. These breakdowns are reflected in the Absolute Maximum Ratings table. All device pins have limited ESD protection using internal diodes to the power supplies as shown in Figure 36.

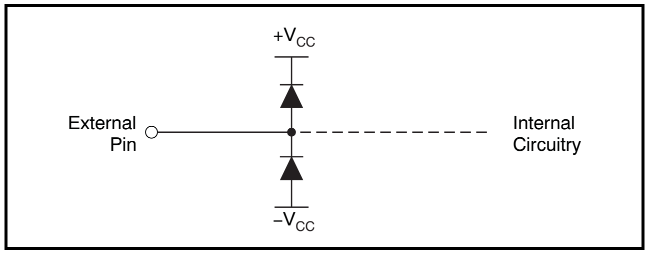


Figure 36. Internal ESD Protection

These diodes provide moderate protection to input overdrive voltages above the supplies as well. The protection diodes can typically support 30mA continuous current. Where higher currents are possible (for example, in systems with ±15V supply parts driving into the OPA4872), current-limiting series resistors should be added into the two inputs. Keep these resistor values as low as possible because high values degrade both noise performance and frequency response.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (August 2008) to Revision C **Page**

- Changed the HBM ESD rating specification in Absolute Maximum Ratings table 2

Changes from Revision A (September 2007) to Revision B **Page**

- Changed storage temperature range rating in *Absolute Maximum Ratings* table from –40°C to +125°C to –65°C to +125°C 2
- Changed 0V to 5V in third paragraph of *Wideband Multiplexer Operation* section 10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA4872ID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA4872	Samples
OPA4872IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	OPA4872	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

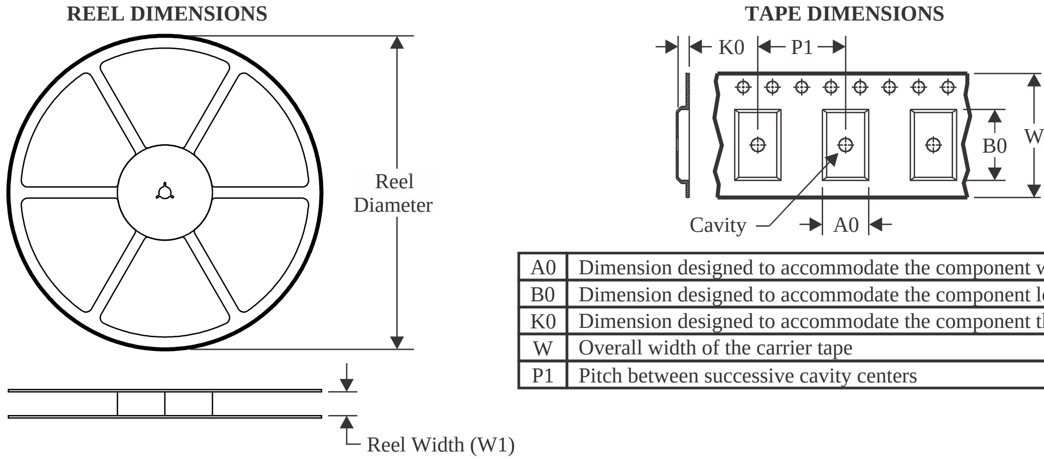
OTHER QUALIFIED VERSIONS OF OPA4872 :

- Enhanced Product : OPA4872-EP

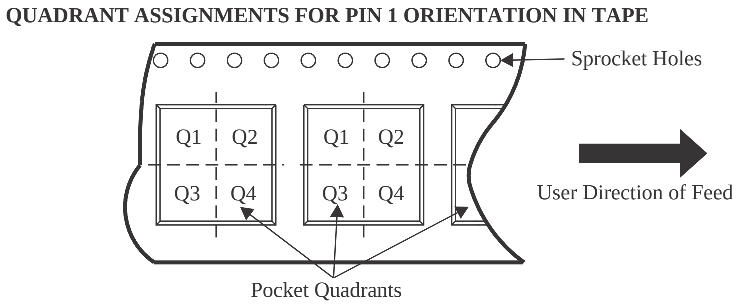
NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



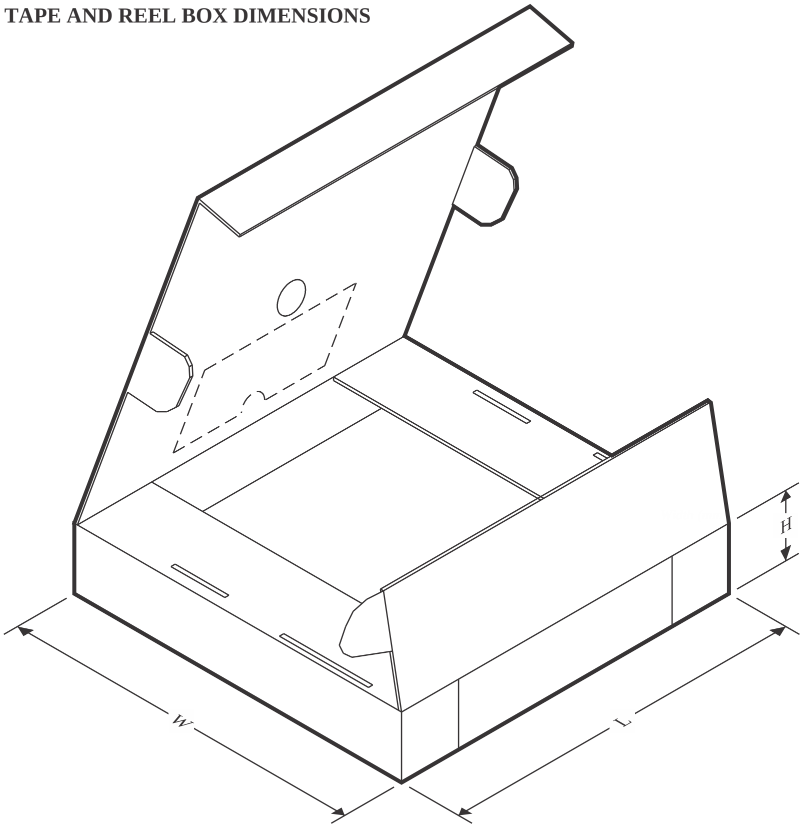
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA4872IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

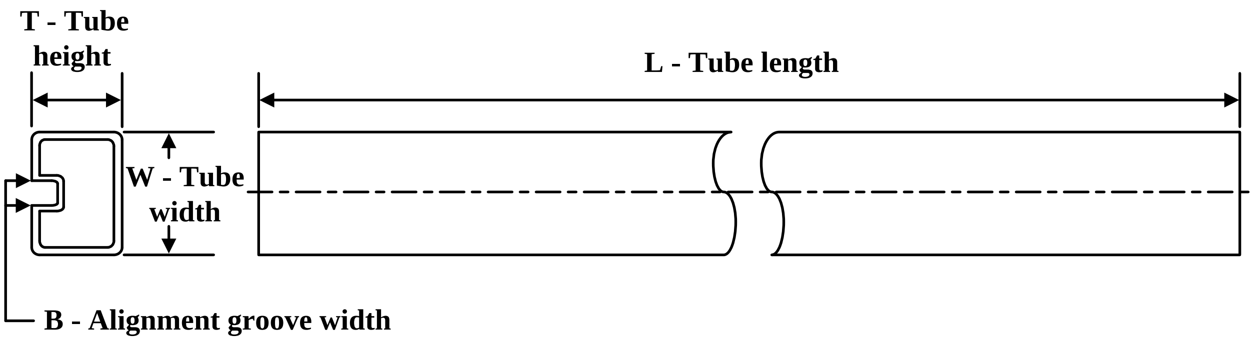
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA4872IDR	SOIC	D	14	2500	356.0	356.0	35.0

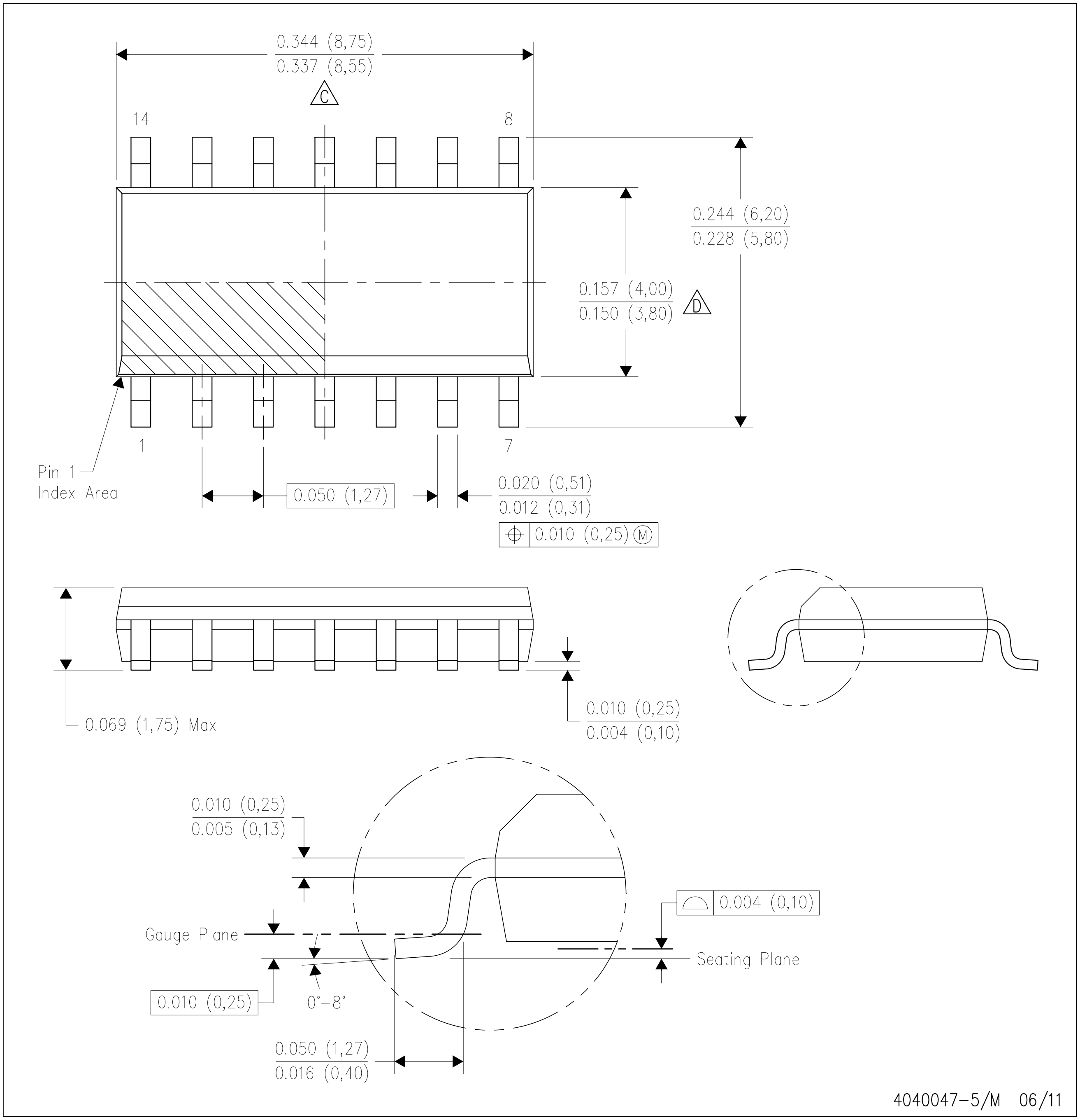
TUBE



*All dimensions are nominal

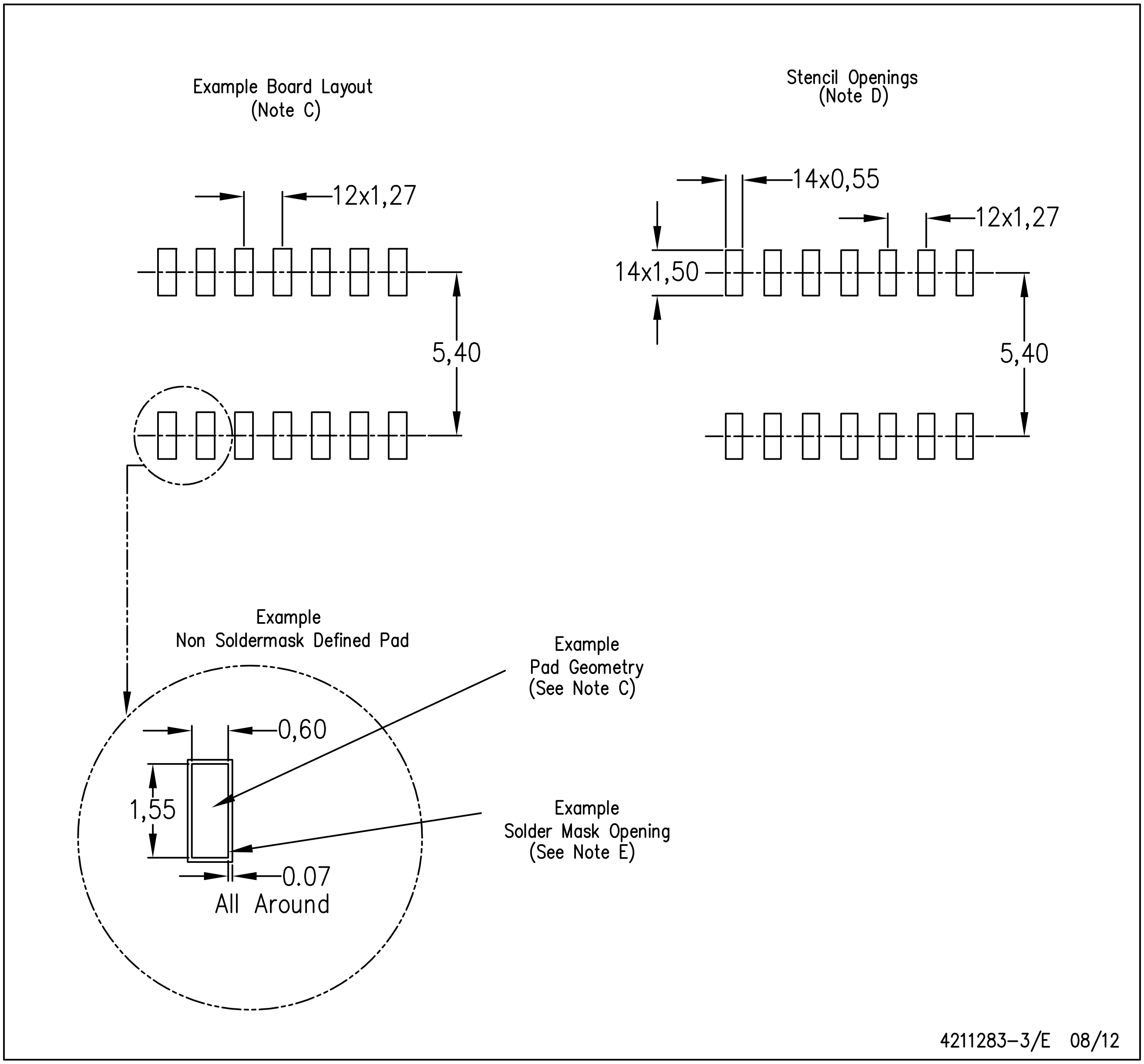
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA4872ID	D	SOIC	14	50	506.6	8	3940	4.32

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Publication IPC-7351 is recommended for alternate designs.

D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.

E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.