OPA548 高电压、大电流运算放大器

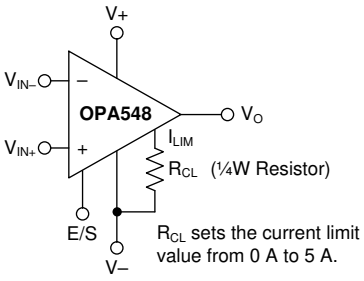
1 特性

- 宽电源电压范围
  - 单电源：8V 至 60V
  - 双电源：±4V 至 ±30V
- 高输出电流：
  - 3A 连续电流
  - 5A 峰值电流
- 宽输出电压摆幅
- 全面保护：
  - 热关断保护
  - 可调电流限制
- 输出禁用选项~
- 热关断指示器
- 高压摆率：10V
- 低静态电流
- 封装：
  - 7 引线 TO-220、锯齿形和直引线
  - 7 引线 DDPAK 表面安装

2 应用

- 半导体制造
- 半导体测试
- 实验室和现场仪表
- LCD 测试
- 模拟输入模块
- 超声波扫描仪

简化电路原理图



3 说明

OPA548 器件是一款低成本、高电压、大电流运算放大器，设计用于驱动各种负载。经过激光修整的单片集成电路可提供出色的低电平信号精度以及高输出电压和电流。

为提高设计灵活性，OPA548 采用单电源或双电源供电。在单电源操作中，输入共模范围可扩展到地电平以下。

OPA548 在过热条件下以及电流过载时会受到内部保护。此外，OPA548 可提供准确的用户自选的电流限制。与其他使用一个与输出电流路径串联的*功率* 电阻器的设计不同，OPA548 间接检测负载。电流限制可通过外部电阻器和电位计在 0A 至 5A 范围内调节，或者通过电压输出或电流输出 DAC 进行数字化控制。

使能/状态 (E/S) 引脚提供两个功能。引脚上的输入不仅可以禁用输出级以有效地断开负载，还可降低静态电流以节省功耗。可对 E/S 引脚输出进行监测，以确定 OPA548 是否处于热关断状态。

OPA548 器件采用业界通用的 7 引线交错和直引线 TO-220 封装以及 7 引线 DDPAK 表面安装塑料电源封装。铜制接线片可轻松安装到散热片或电路板上，从而实现出色的热性能。该器件的扩展工业温度范围为 –40°C 至 85°C。SPICE 宏模型可用于设计分析。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
OPA548	TO-220 (7)	10.17mm x 8.38mm
	TO-263 (7)	10.10mm x 8.89mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。

目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (June 2015) to Revision D **Page**

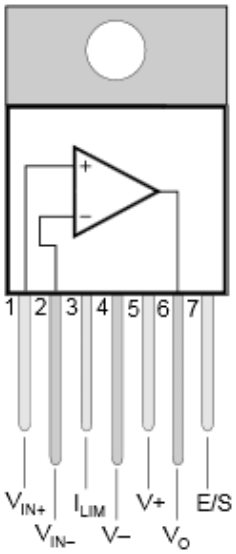
- Changed all INPUT BIAS CURRENT specifications in MIN column to TYP column, and all specifications in TYP column to MAX column (typo) ... 5
- Changed *Quiescent current, shutdown mode* parameter unit typo from nA to mA in *Electrical Characteristics* table ... 6
- Deleted *Temperature Range* section of *Electrical Characteristics* table; content already available in other specifications tables ... 6
- Changed Figure 20 x-axis label from 2 µs/div to 5 µs/div, and y-axis label from 50 mV/div to 10 V/div ... 10

Changes from Revision B (October 2003) to Revision C **Page**

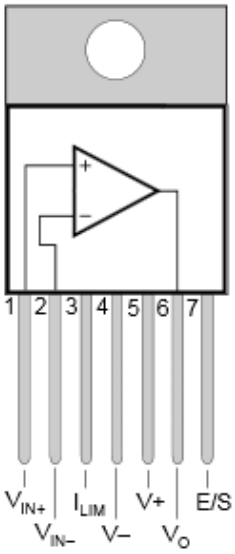
- 已添加 添加了 *ESD 额定值* 表、*特性*、*说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源建议* 部分、*布局* 部分、*器件和文档支持* 部分以及 *机械、封装和可订购信息* 部分 ... 1

5 Pin Configuration and Functions

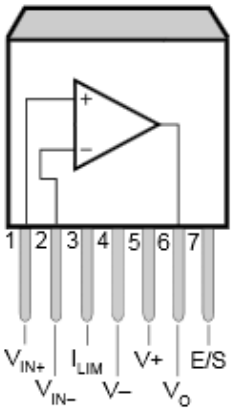
KVT and KC Packages Stagger-Formed
7-Pin TO-220
Top View



KVT and KC Packages Straight-Formed
7-Pin TO-220
Top View



KTW Package Surface-Mount
7-Pin TO-263
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	V_{IN+}	I	Noninverting input
2	V_{IN-}	I	Inverting input
3	I_{LIM}	I	Current limit set
4	V–	I	Negative power supply
5	V+	I	Positive power supply
6	V_O	O	Output
7	E/S	I/O	Enable or disable control input, thermal shutdown status output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
	Output current	See Figure 40		
	Supply voltage, V+ to V–		60	V
	Input voltage	(V–) – 0.5V	(V+) + 0.5	V
	Input shutdown voltage			V+
	Operating temperature	–40	125	°C
	Junction temperature		150	°C
T_{stg}	Storage temperature	–55	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Machine model	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
	Supply voltage (V+ – V–)	8 (±4)		60 (±30)	V
	Specified temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		OPA548		UNIT
		KVT and KC (TO-220)	KTW (DDPAK)	
		7 PINS	7 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.2	30.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.4	37.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.4	14.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.1	5.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.3	14.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.2	0.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
Input offset voltage		V_{CM} = 0 V, I_O = 0 A		±2	±10	mV
Input offset voltage drift		V_{CM} = 0 V, I_O = 0 A, T_A = –40°C to +85°C		±30		µV/°C
Power-supply rejection ratio		V_{CM} = 0 V, I_O = 0 A, V_S = ±4 V to ±30 V		30	100	µV/V
INPUT BIAS CURRENT(1)						
Input bias current(2)		V_{CM} = 0 V		–100	–500	nA
Input bias current drift		V_{CM} = 0 V, T_A = –40°C to +85°C		±0.5		nA/°C
Input offset current		V_{CM} = 0 V		±5	±50	nA
NOISE						
Input voltage noise density		f = 1 kHz		90		nV/√Hz
Current noise density		f = 1 kHz		200		fA/√Hz
INPUT VOLTAGE						
Common-mode voltage	Positive	Linear operation	(V+) – 3	(V+) – 2.3		V
	Negative	Linear operation	(V–) – 0.1	(V–) – 0.2		
Common-mode rejection		V_{CM} = (V–) – 0.1 V to (V+) – 3 V	80	95		dB
INPUT IMPEDANCE						
Differential input impedance				10^7 || 6		Ω || pF
Common-mode input impedance				10^9 || 4		Ω || pF
OPEN-LOOP GAIN						
Open-loop voltage gain		V_O = ±25 V, R_L = 1 kΩ	90	98		dB
		V_O = ±25 V, R_L = 8 Ω		90		dB
FREQUENCY RESPONSE						
Gain-bandwidth product		R_L = 8 Ω		1		MHz
Slew rate		G = 1, V_O = 50 V_{PP}, R_L = 8 Ω		10		V/µs
Full-power bandwidth				See *Typical Characteristics*		kHz
Settling time		To ±0.1%, G = –10, V_O = 50 V_{PP}		15		µs
Total harmonic distortion + noise(3)		f = 1 kHz, R_L = 8 Ω, G = 3, Power = 10 W		0.02%		
OUTPUT						
Voltage output	Positive	I_O = 3 A	(V+) – 4.1	(V+) – 3.7		V
	Negative	I_O = –3 A	(V–) + 3.7	(V–) + 3.3		
	Positive	I_O = 0.6 A	(V+) – 2.4	(V+) – 2.1		
	Negative	I_O = –0.6 A	(V–) + 1.3	(V–) + 1.0		
Maximum continuous current output	DC		±3			A
	AC		3			Arms
Leakage current, output disabled, dc				See *Typical Characteristics*		
Output current limit			–5		5	A
Output current limit equation				I_{LIM} = (15000)(4.75) / (13750 Ω + R_{CL})		A
Output current limit tolerance(1)		R_{CL} = 14.8 kΩ (I_{LIM} = ±2.5 A), R_L = 8 Ω		±100	±250	mA
Capacitive load drive				See Figure 19		

(1) High-speed test at T_J = 25°C.
(2) Positive conventional current flows into the input terminals.
(3) See Figure 12 for additional power levels.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT ENABLE /STATUS (E/S) PIN						
Shutdown input mode	$V_{E/S}$ HIGH (output enabled)	E/S pin open or forced high	(V–) + 2.4			V
	$V_{E/S}$ LOW (output disabled)	E/S pin forced low			(V–) + 0.8	
	$I_{E/S}$ HIGH (output enabled)	E/S pin high		–65		µA
	$I_{E/S}$ LOW (output disabled)	E/S pin low		–70		
Output disable time				1		µs
Output enable time				3		µs
Thermal shutdown status output		Normal operation, sourcing 20 µA	(V–) + 2.4	(V–) + 3.5		V
		Thermally shut down, sinking 5 µA, T_J > 160°C		(V–) + 0.35	(V–) + 0.8	
Thermal protection junction temperature		Shutdown		160		°C
		Reset from shutdown		140		
POWER SUPPLY						
Quiescent current		I_{LIM} connected to V–, I_O = 0 A		±17	±20	mA
Quiescent current, shutdown mode		I_{LIM} connected to V–, I_O = 0 A		±6		mA

6.6 Typical Characteristics

at T_{CASE} = 25°C, V_S = ±30V, and E/S pin open (unless otherwise noted)

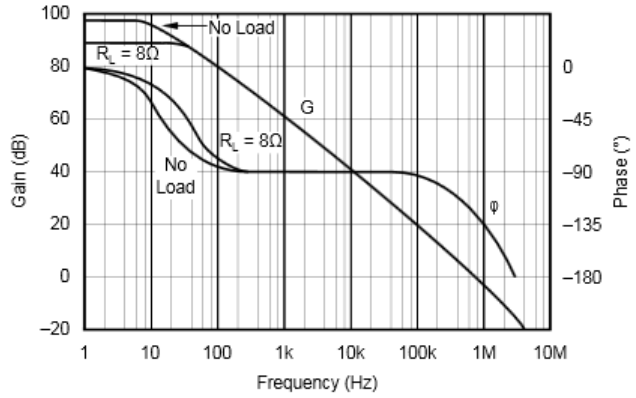


Figure 1. Open-Loop Gain and Phase vs Frequency

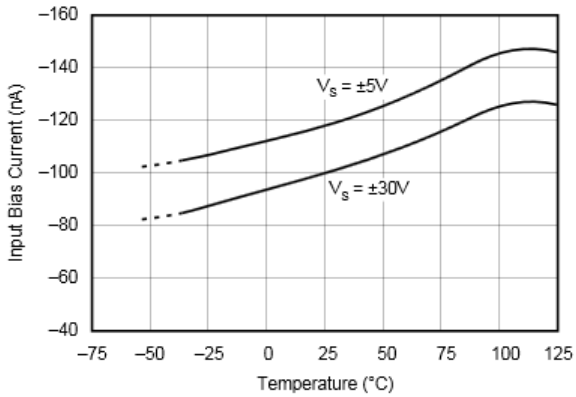


Figure 2. Input Bias Current vs Temperature

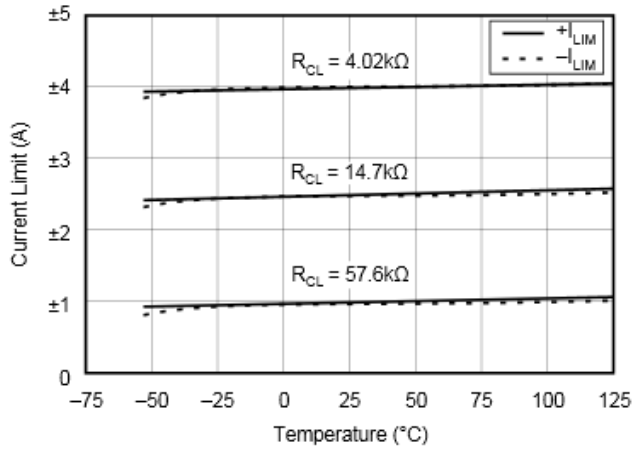


Figure 3. Current Limit vs Temperature

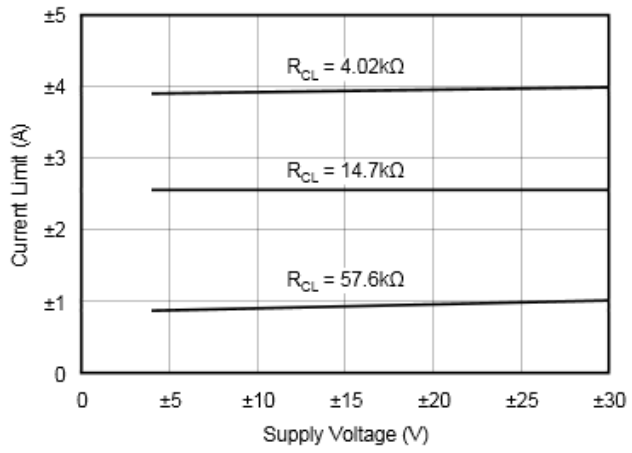


Figure 4. Current Limit vs Supply Voltage

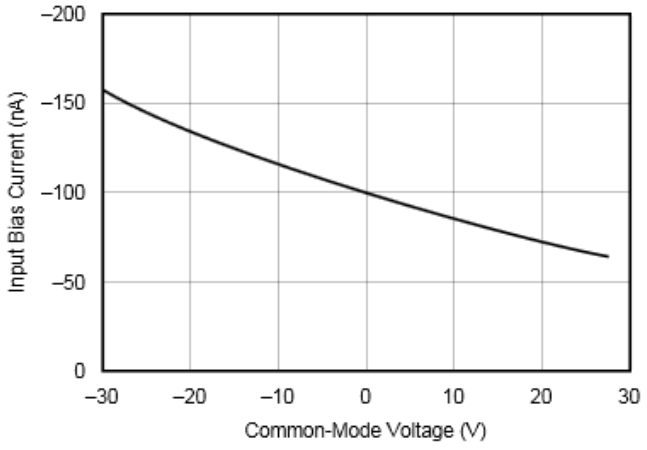


Figure 5. Input Bias Current vs Common-Mode Voltage

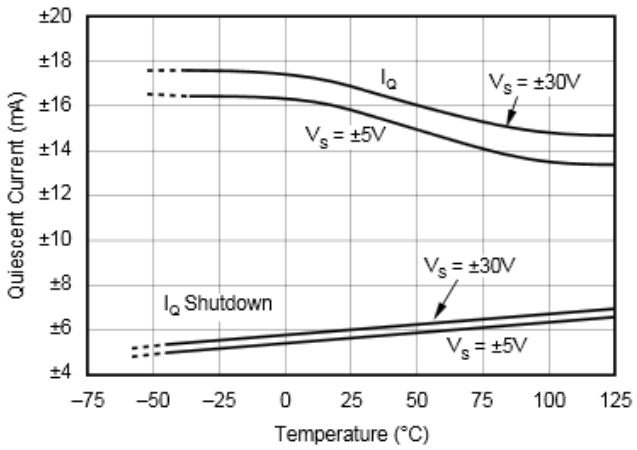


Figure 6. Quiescent Current vs Temperature

Typical Characteristics (continued)

at T_{CASE} = 25°C, V_S = ±30V, and E/S pin open (unless otherwise noted)

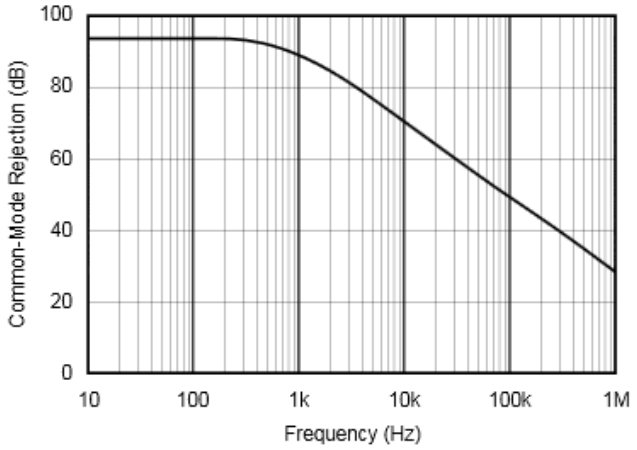


Figure 7. Common-Mode Rejection vs Frequency

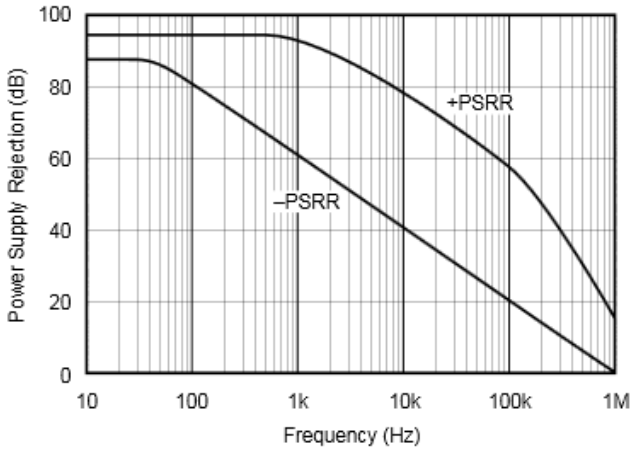


Figure 8. Power-Supply Rejection vs Frequency

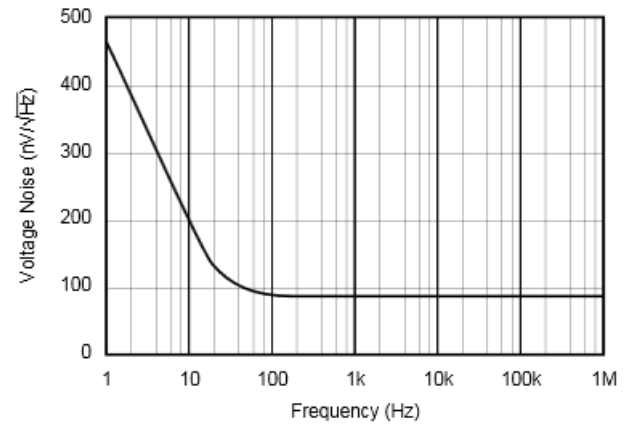


Figure 9. Voltage Noise Density vs Frequency

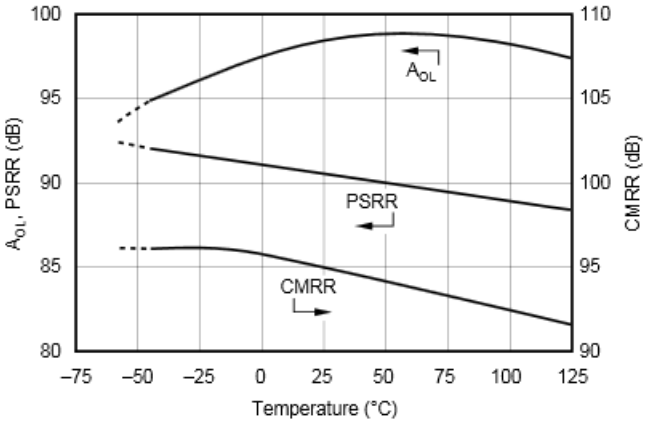


Figure 10. Open-loop Gain, Common-Mode Rejection, and Power-Supply Rejection vs Temperature

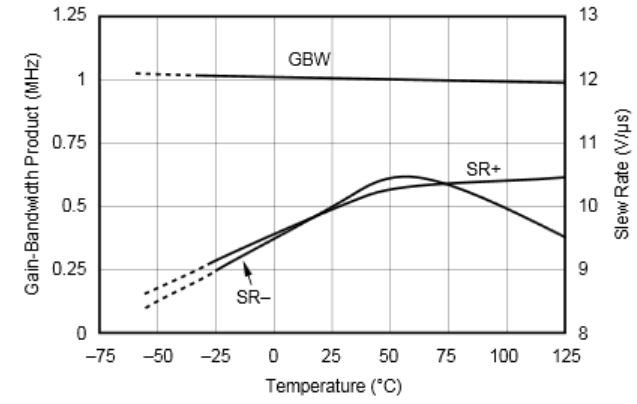


Figure 11. Gain-Bandwidth Product and Slew Rate vs Temperature

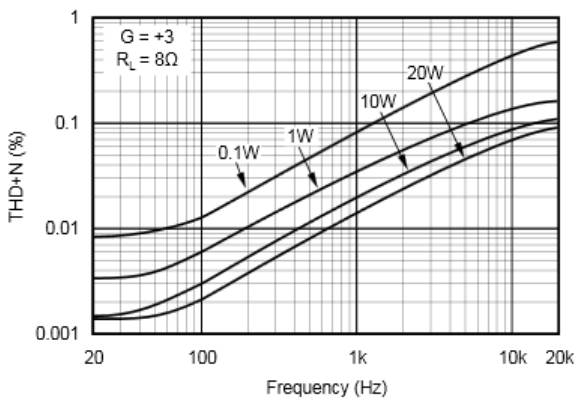


Figure 12. Total Harmonic Distortion+Noise vs Frequency

Typical Characteristics (continued)

at T_{CASE} = 25°C, V_S = ±30V, and E/S pin open (unless otherwise noted)

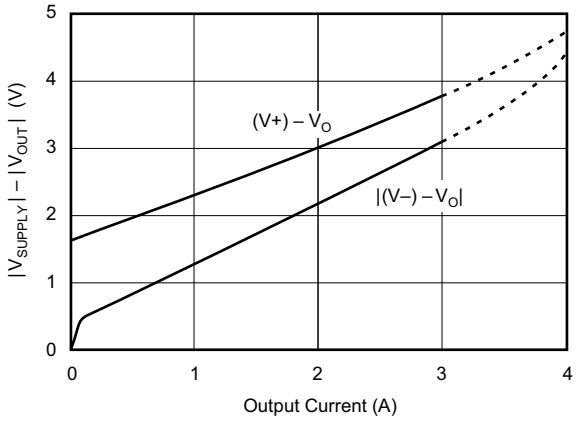


Figure 13. Output Voltage Swing vs Output Current

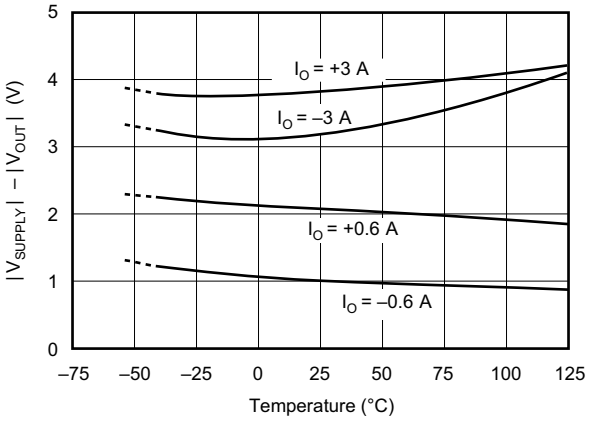


Figure 14. Output Voltage Swing vs Temperature

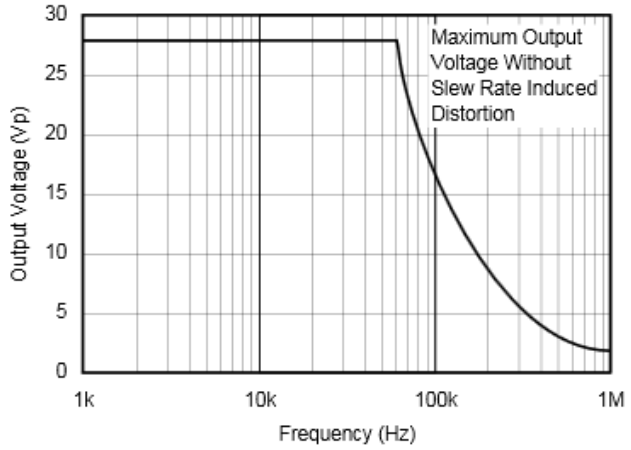


Figure 15. Maximum Output Voltage Swing vs Frequency

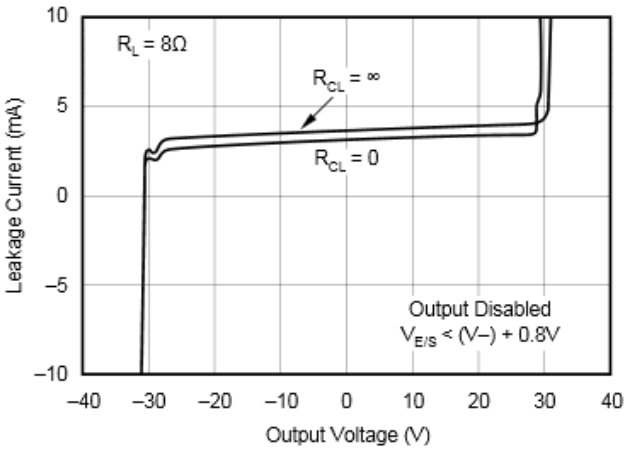


Figure 16. Output Leakage Current vs Applied Output Voltage

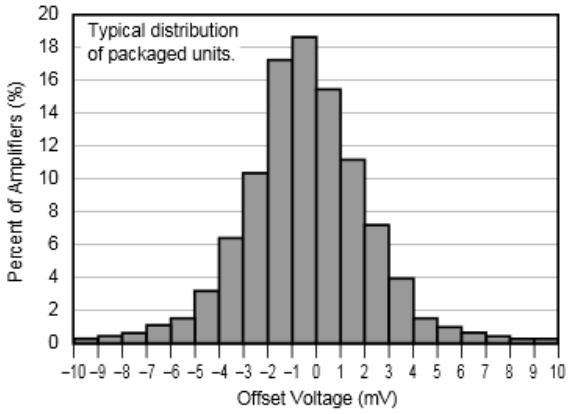


Figure 17. Offset Voltage Production Distribution

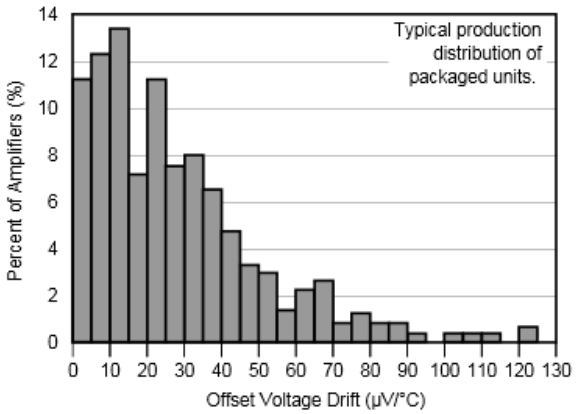


Figure 18. Offset Voltage Drift Production Distribution

Typical Characteristics (continued)

at T_{CASE} = 25°C, V_S = ±30V, and E/S pin open (unless otherwise noted)

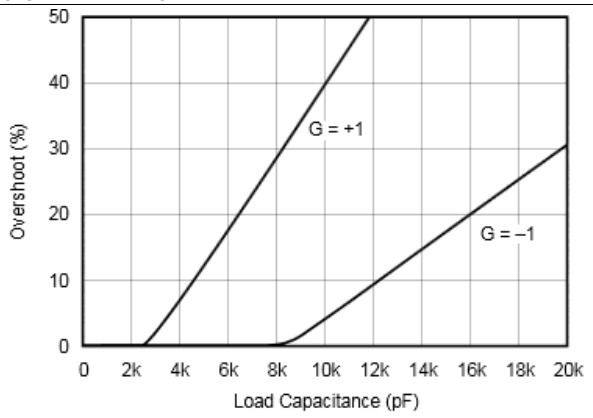
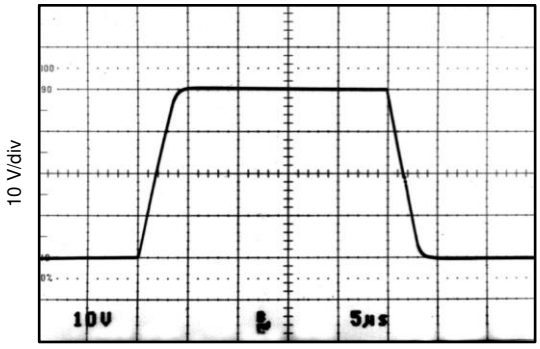


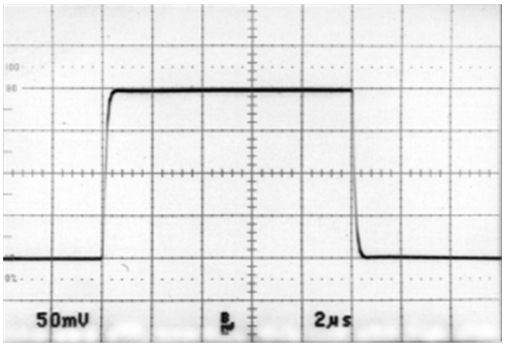
Figure 19. Small-Signal Overshoot vs Load Capacitance



5 µs/div

G = 3 C_L = 1000 pF, R_L = 8 Ω

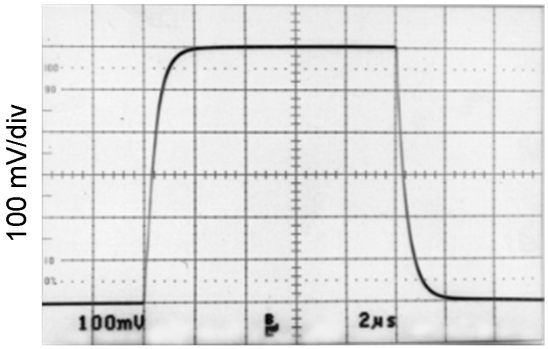
Figure 20. Large-Signal Step Response



2 µs/div

G = 1 C_L = 1000 pF

Figure 21. Small-Signal Step Response



2 µs/div

G = 3 C_L = 1000 pF

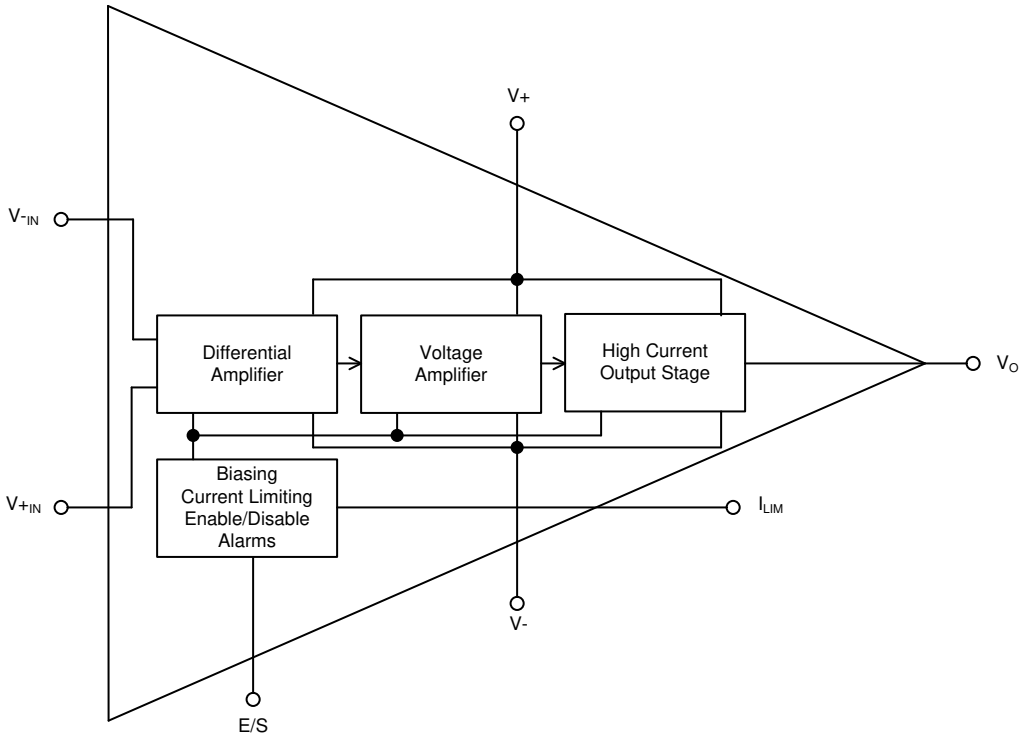
Figure 22. Small-Signal Step Response

7 Detailed Description

7.1 Overview

The OPA548 device uses a PNP input stage (resulting in negative bias currents at each input) without input bias current compensation so matched resistances on the inputs will reduce errors. After the main voltage gain stage is the high current output stage with temperature compensated class A/B biasing to reduce crossover distortion. Local feedback in the output stage may require additional compensation for highly reactive loads (see *Output Stage Compensation*).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Adjustable Current Limit

The OPA548 features an accurate, user-selected current limit. The current limit is set from 0 A to 5 A by controlling the input to the I_{LIM} pin. Unlike other designs, which use a power resistor in series with the output current path, the OPA548 senses the load indirectly. This allows the current limit to be set with a 0-μA to 330-μA control signal. In contrast, other designs require a limiting resistor to handle the full output current (5 A in this case).

With the OPA548, the simplest method for adjusting the current limit uses a resistor or potentiometer connected between the I_{LIM} pin and V– according to the Equation 1:

$$R_{CL} = \frac{(15000)(4.75)}{I_{LIM}} - 13750\ \Omega \quad (1)$$

The low-level control signal (0 μA to 330 μA) also allows the current limit to be digitally controlled.

See Figure 41 for a simplified schematic of the internal circuitry used to set the current limit. Leaving the I_{LIM} pin open programs the output current to zero, while connecting $_{ILIM}$ directly to V– programs the maximum output current limit, typically 5 A.

Feature Description (continued)

7.3.2 Enable/Status (E/S) Pin

The Enable/Status pin provides two functions: forcing this pin LOW disables the output stage, or E/S can be monitored to determine if the OPA548 is in thermal shutdown. One or both of these functions can be used on the same device using single or dual supplies. For normal operation (output enabled), the E/S pin can be left open or pulled HIGH (at least 2.4 V more than the negative rail). A small value capacitor connected between the E/S pin and V– may be required for noisy applications.

7.3.3 Thermal Shutdown Status

Internal thermal shutdown circuitry shuts down the output when the die temperature reaches approximately 160°C, resetting when the die has cooled to 140°C. The E/S pin can be monitored to determine if shutdown has occurred. During normal operation the voltage on the E/S pin is typically 3.5 V more than the negative rail. Once shutdown has occurred, this voltage drops to approximately 350 mV more than the negative rail.

7.4 Device Functional Modes

7.4.1 Output Disable

A unique feature of the OPA548 is its output disable capability. This function not only conserves power during idle periods (quiescent current drops to approximately 6 mA), but also allows multiplexing in low frequency (f < 20 kHz), multichannel applications. Signals greater than 20 kHz may cause leakage current to increase in devices that are shutdown. Figure 33 shows the two OPA548s in a switched amplifier configuration. The ON/OFF state of the two amplifiers is controlled by the voltage on the E/S pin.

To disable the output, the E/S pin is pulled LOW, no greater than 0.8 V more than the negative rail. Typically the output is shutdown in 1 μs. Figure 23 provides an example of how to implement this function using a single supply. Figure 24 gives a circuit for dual-supply applications. To return the output to an enabled state, the E/S pin should be disconnected (open) or pulled to at least (V–) + 2.4 V. It should be noted that pulling the E/S pin HIGH (output enabled) does not disable internal thermal shutdown.

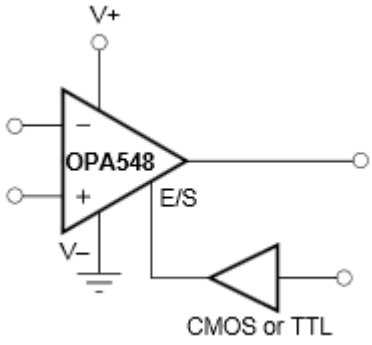
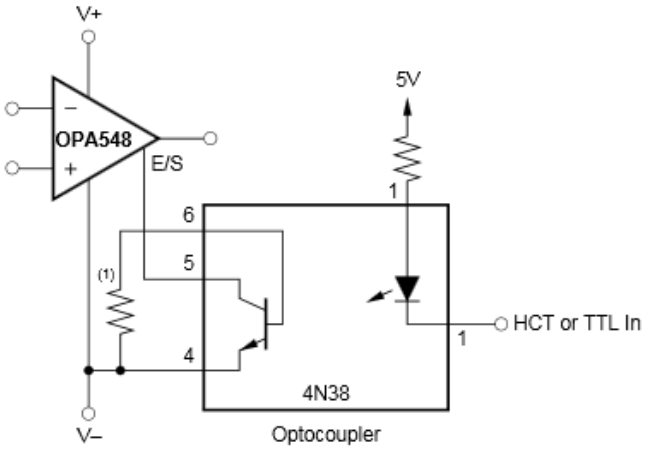


Figure 23. Output Disable With a Single Supply



NOTE: (1) Optional—may be required to limit leakage current of optocoupler at high temperatures.

Figure 24. Output Disable With Dual Supplies

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

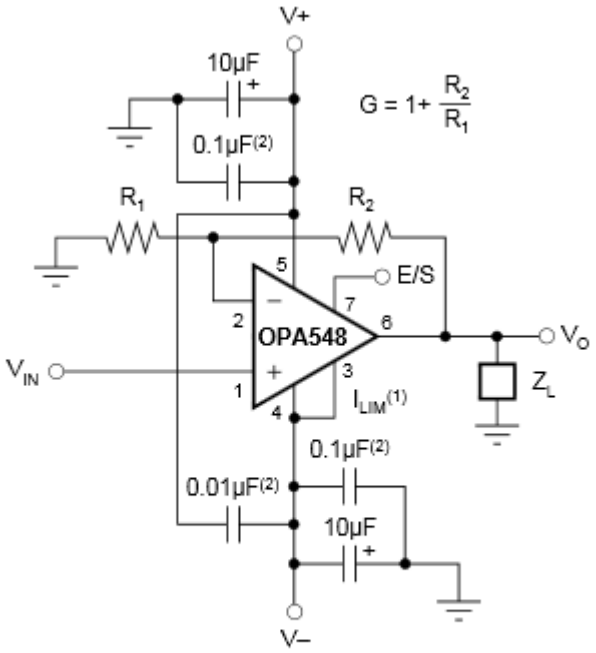
The OPA548 is specified for operation from 8 V to 60 V (±4 V to ±30 V). Specifications apply over the –40°C to 85°C temperature range while the device operates from –40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *Typical Characteristics*.

8.2 Typical Applications

8.2.1 Basic Circuit Connections

Figure 25 shows the OPA548 connected as a basic noninverting amplifier. The OPA548 can be used in virtually any operational amplifier configuration.

Power-supply terminals should be bypassed with low series impedance capacitors. The technique shown in Figure 44, using a ceramic and tantalum type in parallel is recommended. In addition, we recommend a 0.01-µF capacitor between V+ and V– as close to the OPA548 as possible. Power-supply wiring should have low series impedance.



NOTES: (1) I_{LIM} connected to V– gives the maximum current limit, 5A (peak). (2) Connect capacitors directly to package power-supply pins.

Figure 25. Basic Circuit Connections Example

Typical Applications (continued)

8.2.1.1 Design Requirements

To design an example of a noninverting circuit, the following requirements are spelled out:

- Gain: 1
- Output voltage swing: ±10 V
- Maximum Output Current: ±2.5 A
- Load: 4-Ω resistive
- Ambient Temperature: Up to 40°C

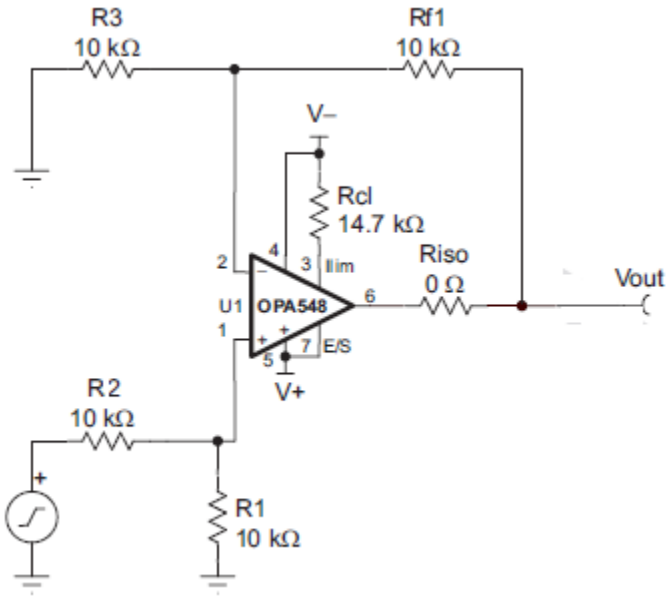


Figure 26. Noninverting Amplifier Configuration Schematic

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Power Supply Requirements

Select the power supply based on the requirement to achieve a ±10-V output with up to a 2.5-A load. The maximum value for output voltage swing at 3-A is approximately within 4 V of either rail, standard 15-V power supplies rated at >2.5 A each will suffice.

8.2.1.2.2 Gain Setting and Input Configuration

A unity gain noninverting application could be provided by simply connecting the output of an operational amplifier back to its input, with the signal applied to the noninverting input. Power operational amplifiers are frequently subject to unpredictable load impedances that can cause instability. Increasing gain can enhance stability. Furthermore, the feedback network provides locations for further opportunities for stability enhancing components if necessary.

In this application two 10-kΩ resistors are used for the input and feedback resistance, which would normally result in a noninverting gain of 2. Adding a voltage divider consisting of R1 and R2 reduces the input signal by half before it is applied to the operational amplifier. In this case the solution just happens to restore us back to the desired overall gain of 1. This solution using an identical pair of resistors before the noninverting input between the signal and ground creates what is known as a difference amplifier.

Typical Applications (continued)

8.2.1.2.3 Current Limit

The OPA548 provides means to limit the maximum output current delivered by the amplifier. A resistor between the negative supply and the amplifier`s Ilim pin, or a DAC can be used to set the current limit. For this circuit a 14.7-kΩ resistor (Rcl) limits the output current to approximately 2.5 A.

8.2.1.2.4 Safe-Operating-Area

Plotting the load on the Safe-Operating-Area (SOA) curve allows the safety of the application to be assessed. Figure 40 depicts the 4-Ω load on the curve. With a resistive load, maximum dissipation occurs at an output voltage one-half of the supply voltage, in this case 7.5 V and 1.875 A for 22.5 W.

Consideration should be given to the condition of a shorted output. In this application this is a stress of 15 V at 2.5 A on the output stage, or 37.5 W which is just within the 50-W SOA of the OPA548. How long the circuit can withstand a short to ground will be determined by the size of the heatsink. Ultimately the thermal shutdown will activate providing short circuit protection, although even this is not recommended as a continuous condition.

8.2.1.2.5 Heat Sinking

From *Safe-Operating-Area* we know we will must support 22.5 W of dissipation up to the 40°C ambient requirements of the application. This indicates the need for a heatsink with a $R_{\theta HA}$ < 2.5°C/W, such as an Aavid Thermalloy 530002B02500G.

8.2.1.3 Application Curve

Figure 27 shows the expected results for the Noninverting Operation of the OPA548. The left picture shows the Noninverting Operation in dual supply mode and the right picture shows the Noninverting Operation in single supply mode. The input signal is a zero-centered sine wave with an amplitude of 10 V p-p and a frequency of 1 kHz. In this trace the OPA548 is delivering a peak current of 1.25 A to the 4-Ω load.

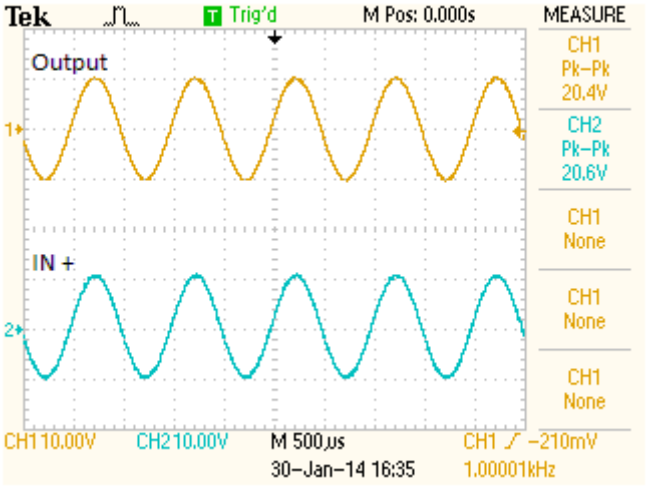


Figure 27. Noninverting Operation, Dual-Supply Waveforms

Typical Applications (continued)

8.2.2 Monitoring Single- and Dual-Supplies

Figure 28 gives an example of monitoring shutdown in a single-supply application. Figure 29 provides a circuit for dual supplies. External logic circuitry or an LED could be used to indicate if the output has been thermally shutdown, see Figure 31.

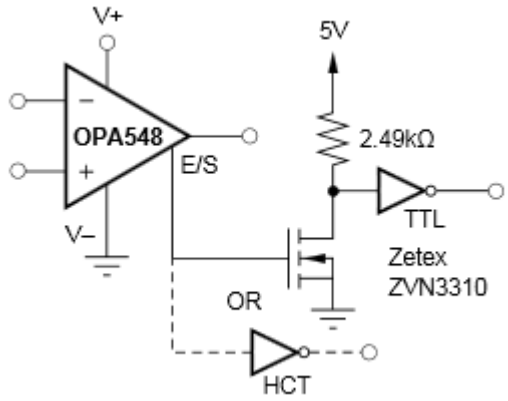


Figure 28. Thermal Shutdown Status With a Single-Supply

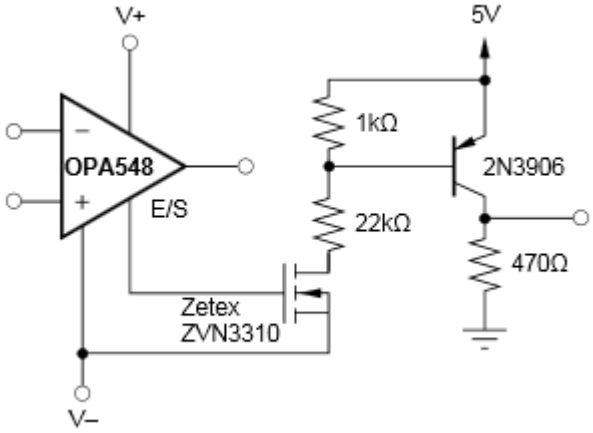


Figure 29. Thermal Shutdown Status With Dual-Supplies

8.2.2.1 Design Requirements

See the previous *Design Requirements*.

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Output Disable and Thermal Shutdown Status

As mentioned earlier, the OPA548's output can be disabled and the disable status can be monitored simultaneously. Figure 28 and Figure 29 provide examples interfacing to the E/S pin while using a single supply and dual supplies, respectively.

Typical Applications (continued)

8.2.3 Programmable Power Supply

A programmable source or sink power supply can easily be built using the OPA548. Both the output voltage and output current are user-controlled. See Figure 30 for a circuit using potentiometers to adjust the output voltage and current while Figure 31 uses DACs. An LED tied to the E/S pin through a logic gate indicates if the OPA548 is in thermal shutdown.

Figure 30 illustrates how to use the OPA548 to provide an accurate voltage source with only three external resistors. First, the current limit resistor, R_{CL}, is chosen according to the desired output current. The resulting voltage at the I_{LIM} pin is constant and stable over temperature. This voltage, V_{CL}, is connected to the noninverting input of the operational amplifier and used as a voltage reference, thus eliminating the need for an external reference. The feedback resistors are selected to gain V_{CL} to the desired output voltage level.

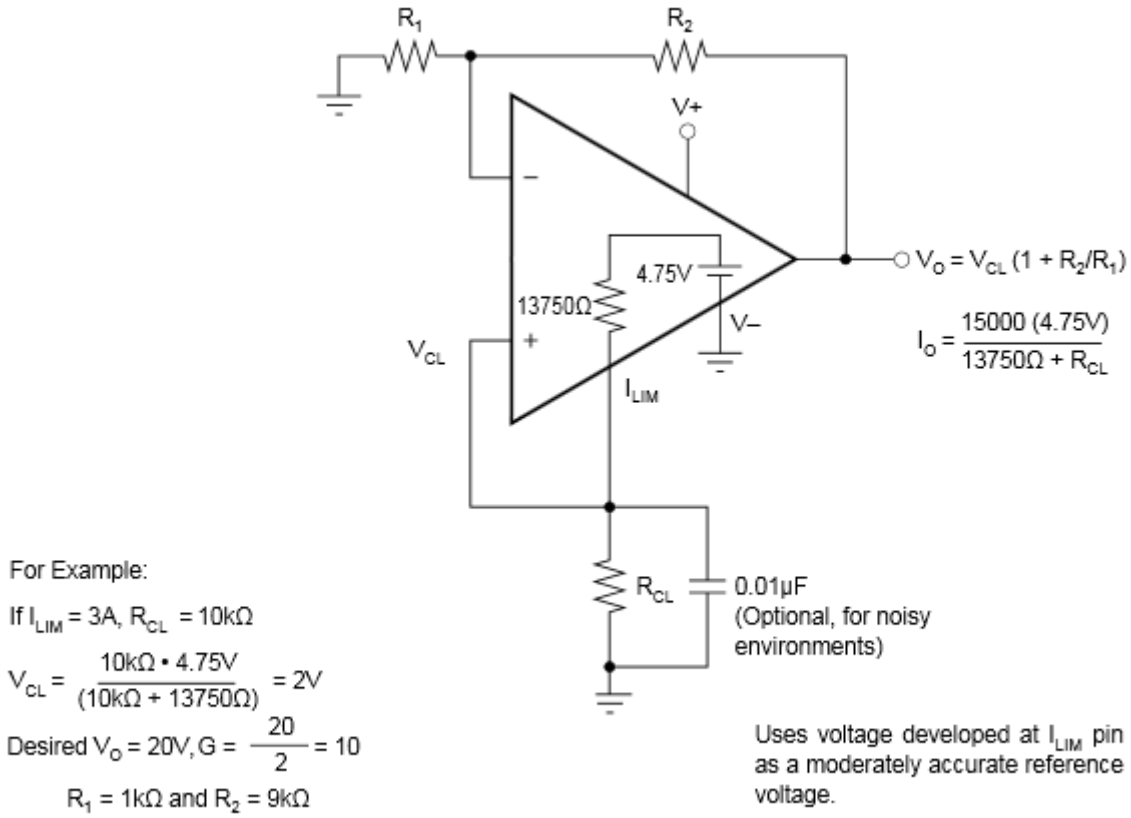


Figure 30. Voltage Source Schematic

Typical Applications (continued)

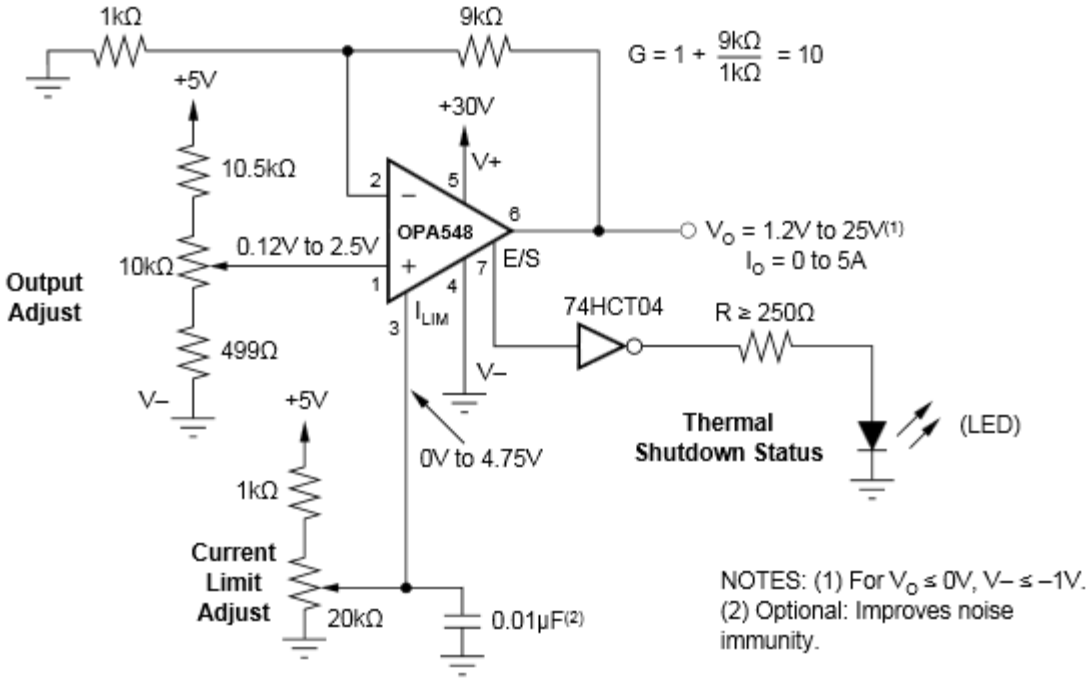
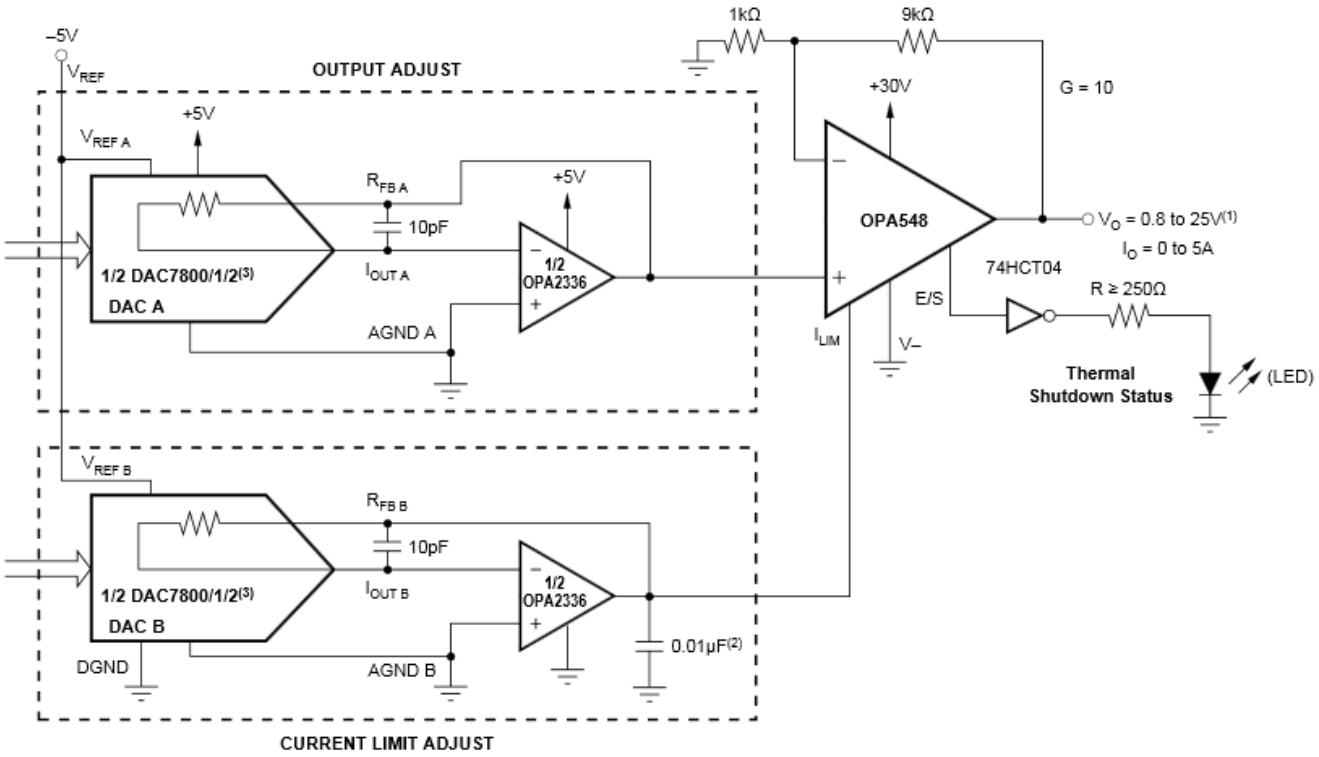


Figure 31. Resistor-Controlled Programmable Power Supply Schematic

Typical Applications (continued)



NOTES: (1) For $V_O \leq 0V$, $V- \leq -1V$. (2) Optional, improves noise immunity. (3) Chose DAC780X based on digital interface: DAC7800—12-bit interface, DAC7801—8-bit interface + 4 bits, DAC7802—serial interface.

Figure 32. Digitally-Controlled Programmable Power Supply Schematic

8.3 System Examples

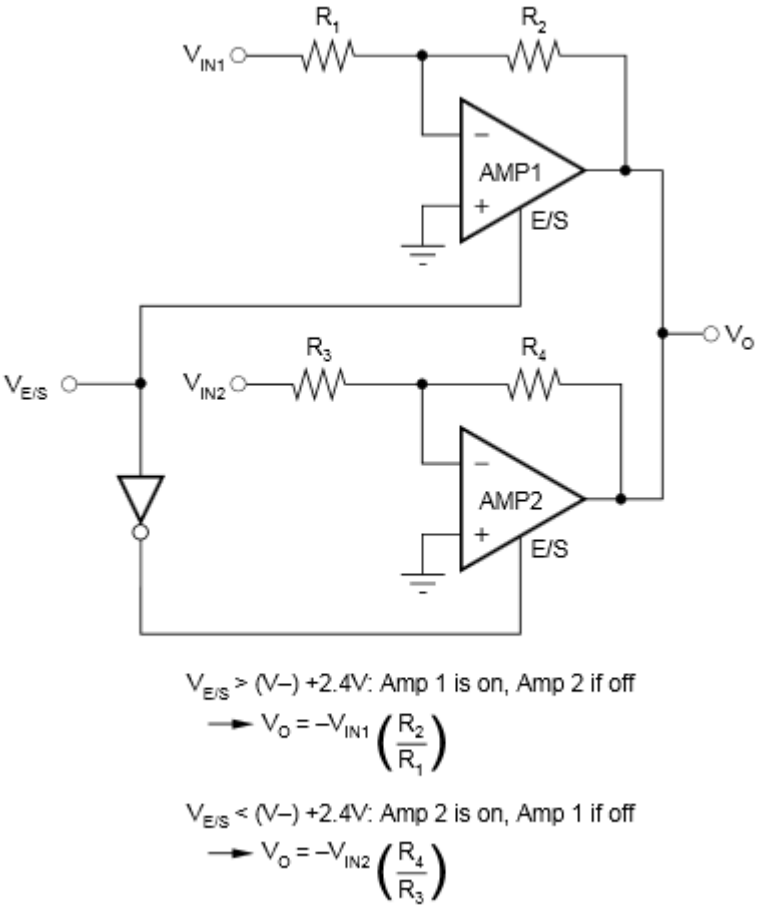


Figure 33. Switched Amplifier Schematic

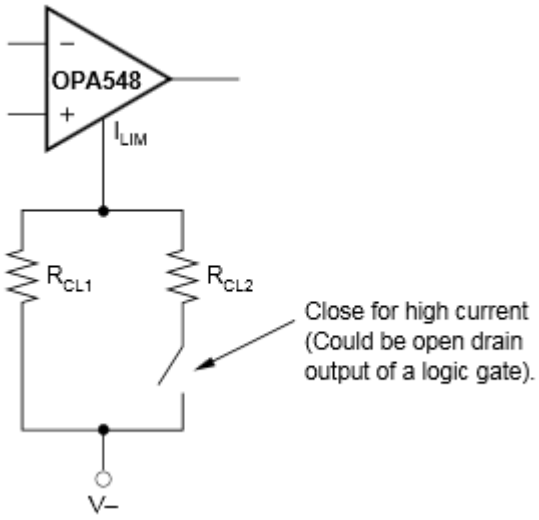


Figure 34. Multiple Current Limit Values Schematic

System Examples (continued)

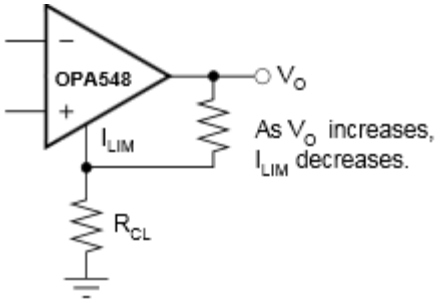
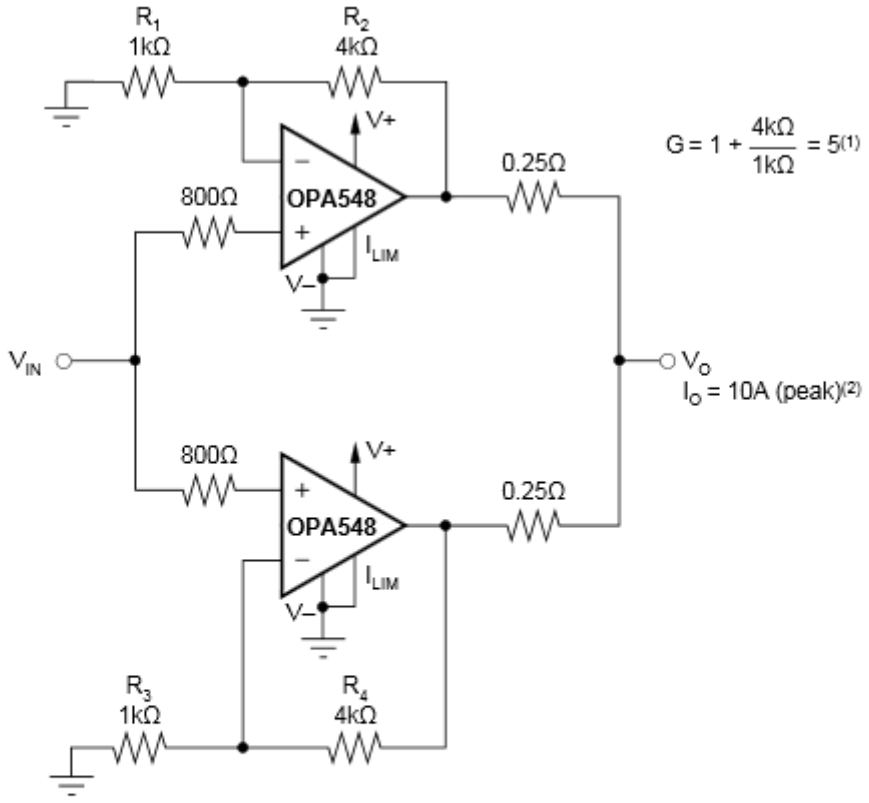


Figure 35. Single Quadrant V × I Limiting



NOTES: (1) Works well for G < 10. Input offset causes output current to flow between amplifiers with G > 10. Gains (resistor ratios) of the two amplifiers should be carefully matched to ensure equal current sharing. (2) As configured (I_{LIM} connected to V–) output current limit is set to 10A (peak). Each amplifier is limited to 5A (peak). Other current limit values may be obtained, see Figure 3, "Adjustable Current Limit".

Figure 36. Parallel Output for Increased Output Current Schematic

9 Power Supply Recommendations

The OPA548 operates from single (8 V to 60 V) or dual (±4 V to ±30 V) supplies with excellent performance. Most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown Typical Characteristics.

Some applications do not require equal positive and negative output voltage swing. Power-supply voltages do not must be equal. The OPA548 can operate with as little as 8 V between the supplies and with up to 60 V between the supplies. For example, the positive supply could be set to 55 V with the negative supply at –5 V, or vice-versa.

9.1 Output Stage Compensation

The complex load impedances common in power operational amplifier applications can cause output stage instability. For normal operation output compensation circuitry is typically not required. However, if the OPA548 is intended to be driven into current limit, an R/C network may be required. See Figure 38 for an output series R/C compensation (snubber) network which generally provides excellent stability.

A snubber circuit may also enhance stability when driving large capacitive loads (> 1000 pF) or inductive loads (motors, loads separated from the amplifier by long cables). Typically 3 Ω to 10 Ω in series with 0.01 μF to 0.1 μF is adequate. Some variations in circuit value may be required with certain loads.

9.2 Output Protection

Reactive and EMF-generating loads can return load current to the amplifier, causing the output voltage to exceed the power-supply voltage. This damaging condition can be avoided with clamp diodes from the output terminal to the power supplies, as shown in Figure 38. Schottky rectifier diodes with a 5 A or greater continuous rating are recommended.

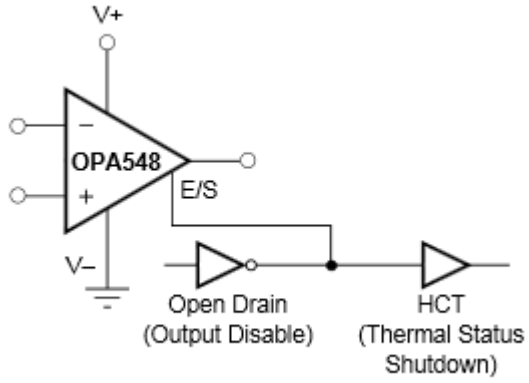


Figure 37. Output Disable and Thermal Shutdown Status With a Single Supply

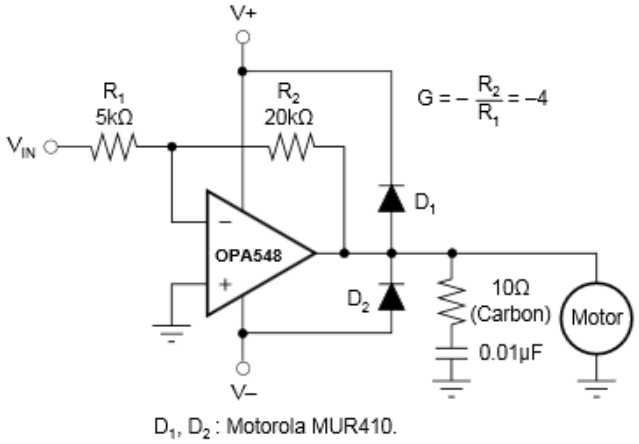
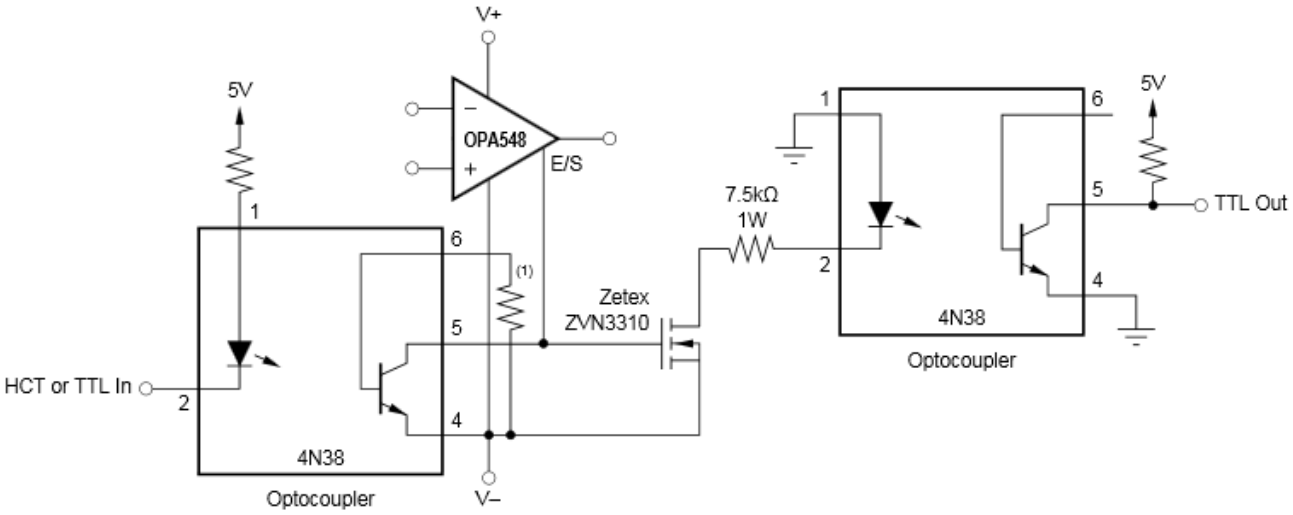


Figure 38. Motor Drive Circuit

Output Protection (continued)



NOTE: (1) Optional—may be required to limit leakage current of optocoupler at high temperatures.

Figure 39. Output Disable and Thermal Shutdown Status With Dual Supplies

10 Layout

10.1 Layout Guidelines

10.1.1 Safe Operating Area

Stress on the output transistors is determined both by the output current and by the output voltage across the conducting output transistor, $V_S – V_O$. The power dissipated by the output transistor is equal to the product of the output current and the voltage across the conducting transistor, $V_S – V_O$. The Safe Operating Area (SOA curve, Figure 40) shows the permissible range of voltage and current.

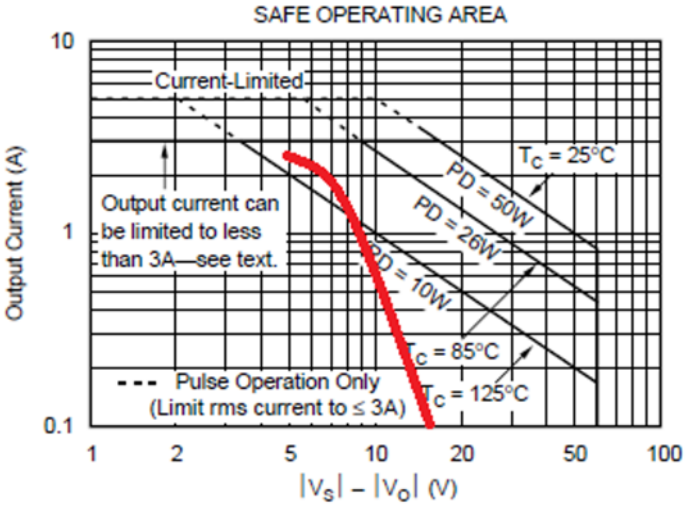


Figure 40. 4-Ω Load Plotted on OPA548 SOA for this Application

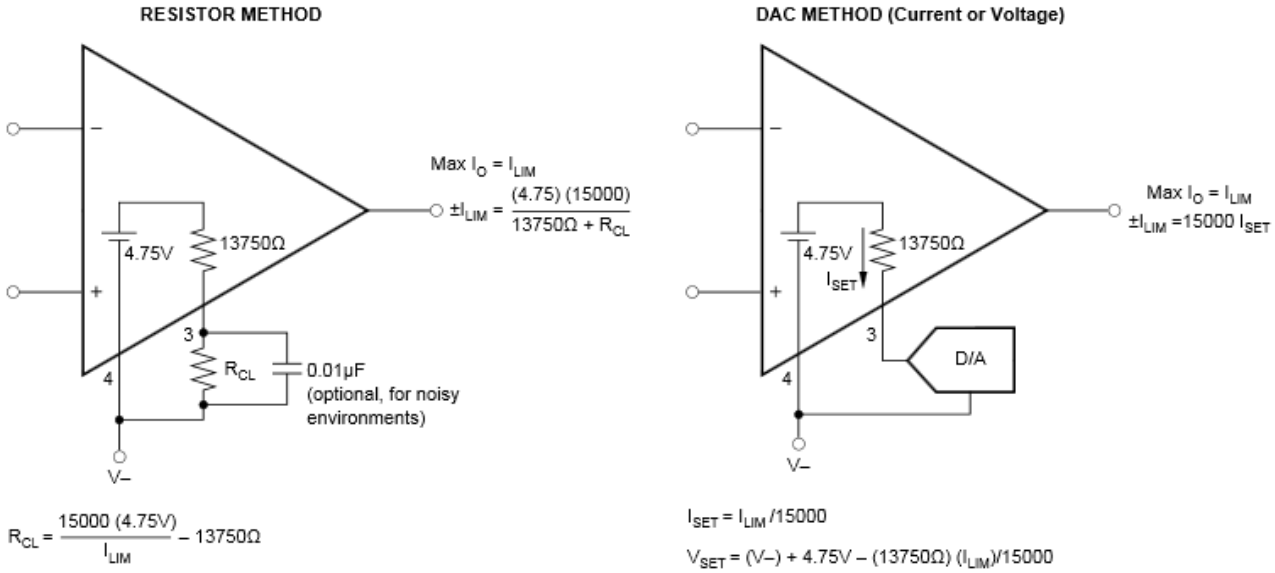
The safe output current decreases as $V_S – V_O$ increases. Output short circuits are a very demanding case for SOA. A short-circuit to ground forces the full power-supply voltage (V+ or V–) across the conducting transistor. Increasing the case temperature reduces the safe output current that can be tolerated without activating the thermal shutdown circuit of the OPA548. For further insight on SOA, consult Application Bulletin SBOA022.

Layout Guidelines (continued)

10.1.2 Amplifier Mounting

图 46 provides recommended solder footprints for both the TO-220 and DDPAK power packages. The tab of both packages is electrically connected to the negative supply, V–. It may be desirable to isolate the tab of the TO-220 package from its mounting surface with a mica (or other film) insulator (see Figure 42). For lowest overall thermal resistance it is best to isolate the entire heat sink/OPA548 structure from the mounting surface rather than to use an insulator between the semiconductor and heat sink.

For best thermal performance, the tab of the DDPAK surface-mount version should be soldered directly to a circuit board copper area. Increasing the copper area improves heat dissipation. See Figure 43 for typical thermal resistance from junction-to-ambient as a function of the copper area.



OPA547 CURRENT LIMIT: 0 to 5A

DESIRED CURRENT LIMIT	RESISTOR(1) (R_{CL})	CURRENT (I_{SET})	VOLTAGE (V_{SET})
0A	I_{LIM} Open	0µA	(V–) + 4.75V
1A	57.6kΩ	67µA	(V–) + 3.8V
2.5A	14.7kΩ	167µA	(V–) + 2.5V
3A	10kΩ	200µA	(V–) + 2V
4A	4.02kΩ	267µA	(V–) + 1.1V
5A	I_{LIM} Connected to V–	333µA	(V–)

NOTE: (1) Resistors are nearest standard 1% values.

Figure 41. Adjustable Current Limit

Layout Guidelines (continued)

10.1.3 Power Dissipation

Power dissipation depends on power supply, signal, and load conditions. For DC signals, power dissipation is equal to the product of output current times the voltage across the conducting output transistor. Power dissipation can be minimized by using the lowest possible power-supply voltage necessary to assure the required output voltage swing.

For resistive loads, the maximum power dissipation occurs at a DC output voltage of one-half the power-supply voltage. Dissipation with AC signals is lower. Application Bulletin SBOA022 explains how to calculate or measure power dissipation with unusual signals and loads.

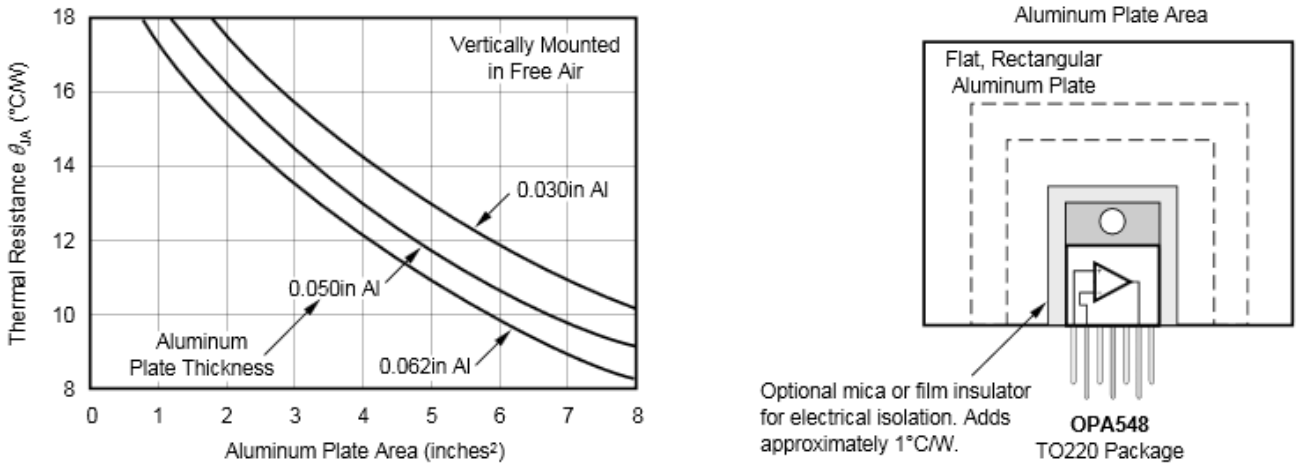


Figure 42. TO-220 Thermal Resistance vs Aluminum Plate Area

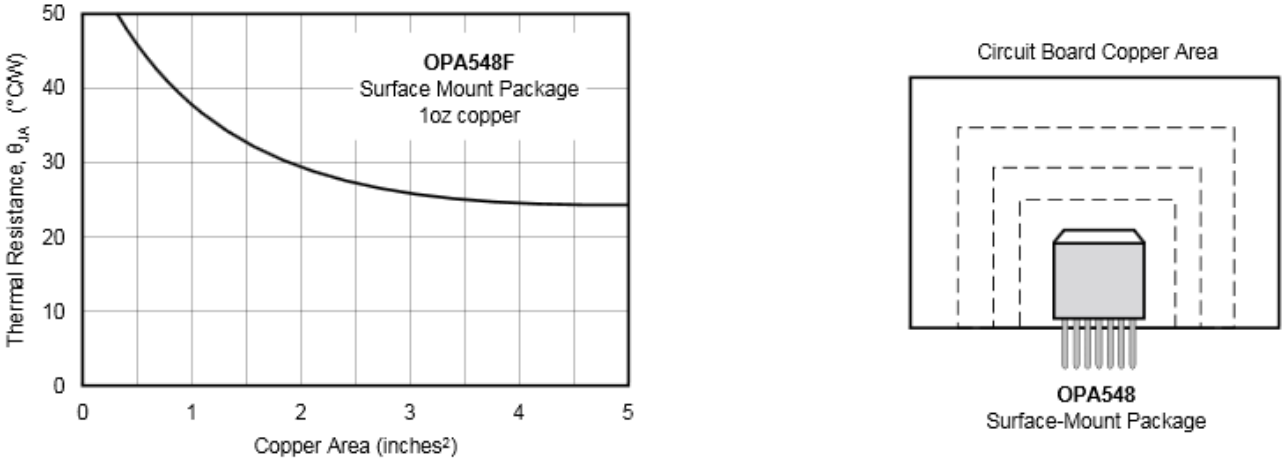


Figure 43. DDPAK Thermal Resistance vs Circuit Board Copper Area

10.1.4 Thermal Considerations

Power dissipated in the OPA548 will cause the junction temperature to rise. The OPA548 has thermal shutdown circuitry that protects the amplifier from damage. The thermal protection circuitry disables the output when the junction temperature reaches approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on load and signal conditions, the thermal protection circuit may cycle on and off. This limits the dissipation of the amplifier but may have an undesirable effect on the load.

Layout Guidelines (continued)

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature should be limited to 125°C, maximum. To estimate the margin of safety in a complete design (including heat sink) increase the ambient temperature until the thermal protection is triggered. Use worst-case load and signal conditions. For good reliability, thermal protection should trigger more than 35°C more than the maximum expected ambient condition of your application. This produces a junction temperature of 125°C at the maximum expected ambient condition.

The internal protection circuitry of the OPA548 was designed to protect against overload conditions. It was not intended to replace proper heat sinking. Continuously running the OPA548 into thermal shutdown will degrade reliability.

10.1.5 Heat Sinking

Most applications require a heat sink to assure that the maximum operating junction temperature (125°C) is not exceeded. In addition, the junction temperature should be kept as low as possible for increased reliability. Junction temperature can be determined according to the equation:

$$T_J = T_A + P_D R_{\theta JA} \quad (2)$$

where

- $R_{\theta JA} = R_{\theta JC} + R_{\theta CH} + R_{\theta HA}$
- T_J = Junction Temperature (°C)
- T_A = Ambient Temperature (°C)
- P_D = Power Dissipated (W)
- $R_{\theta JC}$ = Junction-to-Case Thermal Resistance (°C/W)
- $R_{\theta CH}$ = Case-to-Heat Sink Thermal Resistance (°C/W)
- $R_{\theta HA}$ = Heat Sink-to-Ambient Thermal Resistance (°C/W)
- $R_{\theta JA}$ = Junction-to-Air Thermal Resistance (°C/W)

Figure 44 shows maximum power dissipation versus ambient temperature with and without the use of a heat sink. Using a heat sink significantly increases the maximum power dissipation at a given ambient temperature as shown.

The difficulty in selecting the heat sink required lies in determining the power dissipated by the OPA548. For DC output into a purely resistive load, power dissipation is simply the load current times the voltage developed across the conducting output transistor, $P_D = I_L(V_S – V_O)$. Other loads are not as simple. Consult Application Bulletin SBOA022 for further insight on calculating power dissipation. Once power dissipation for an application is known, the proper heat sink can be selected.

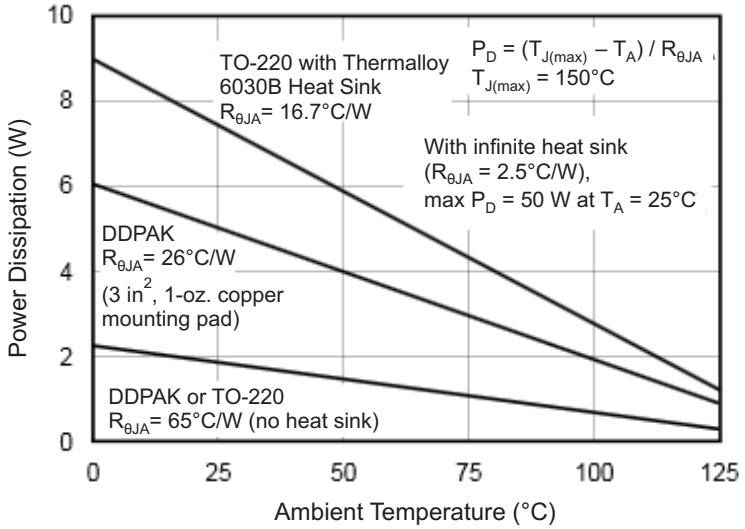


Figure 44. Maximum Power Dissipation vs Ambient Temperature

Layout Guidelines (continued)

10.1.5.1 Heat Sink Selection Example

A TO-220 package is dissipating 5 W. The maximum expected ambient temperature is 40°C. Find the proper heat sink to keep the junction temperature less than 125°C (150°C minus 25°C safety margin).

Combining Equation 2 and Equation 3 gives:

$$T_J = T_A + P_D(R_{\theta JC} + R_{\theta CH} + R_{\theta HA}) \quad (3)$$

T_J, T_A, and P_D are given. $R_{\theta JC}$ is provided in the specification table, 2.5°C/W (DC). $R_{\theta CH}$ can be obtained from the heat sink manufacturer. Its value depends on heat sink size, area, and material used. Semiconductor package type, mounting screw torque, insulating material used (if any), and thermal joint compound used (if any) also affect $R_{\theta CH}$. A typical $R_{\theta CH}$ for a TO-220 mounted package is 1°C/W. Now we can solve for $R_{\theta HA}$:

$$\theta_{HA} = \frac{T_J - T_A}{P_D} - (\theta_{JC} + \theta_{CH})$$

$$\theta_{HA} = \frac{125°C - 40°C}{5W} - (2.5°C/W + 1°C/W) = 13.5°C/W \quad (4)$$

To maintain junction temperature less than 125°C, the heat sink selected must have a $R_{\theta HA}$ less than 14°C/W. In other words, the heat sink temperature rise above ambient must be less than 67.5°C (13.5°C/W × 5 W). For example, at 5-W Thermalloy model number 6030B has a heat sink temperature rise of 66°C more than ambient ($R_{\theta HA}$ = 66°C / 5 W = 13.2°C / W), which is less than the 67.5°C required in this example. Figure 44 shows power dissipation versus ambient temperature for a TO-220 package with a 6030B heat sink.

Another variable to consider is natural convection versus forced convection air flow. Forced-air cooling by a small fan can lower $R_{\theta JCA}$ ($R_{\theta CH}$ + $R_{\theta HA}$) dramatically. Heat sink manufactures provide thermal data for both of these cases. For additional information on determining heat sink requirements, consult Application Bulletin SBOA021.

As mentioned earlier, once a heat sink has been selected, the complete design should be tested under worst-case load and signal conditions to maintain proper thermal protection.

10.2 Layout Example

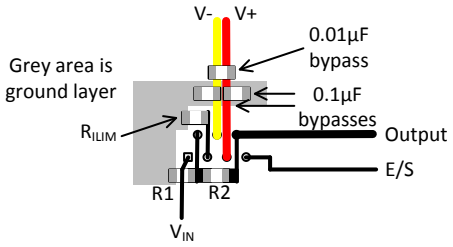


Figure 45. Recommended Layout Example

11 器件和文档支持

11.1 器件支持

11.1.1 第三方产品免责声明

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11.2 文档支持

11.2.1 相关文档

德州仪器 (TI)，*《散热片 - TO-3 热模型 SBOA021》* 应用公告

11.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com.cn 上的器件产品文件夹。单击右上角的*通知我*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 支持资源

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

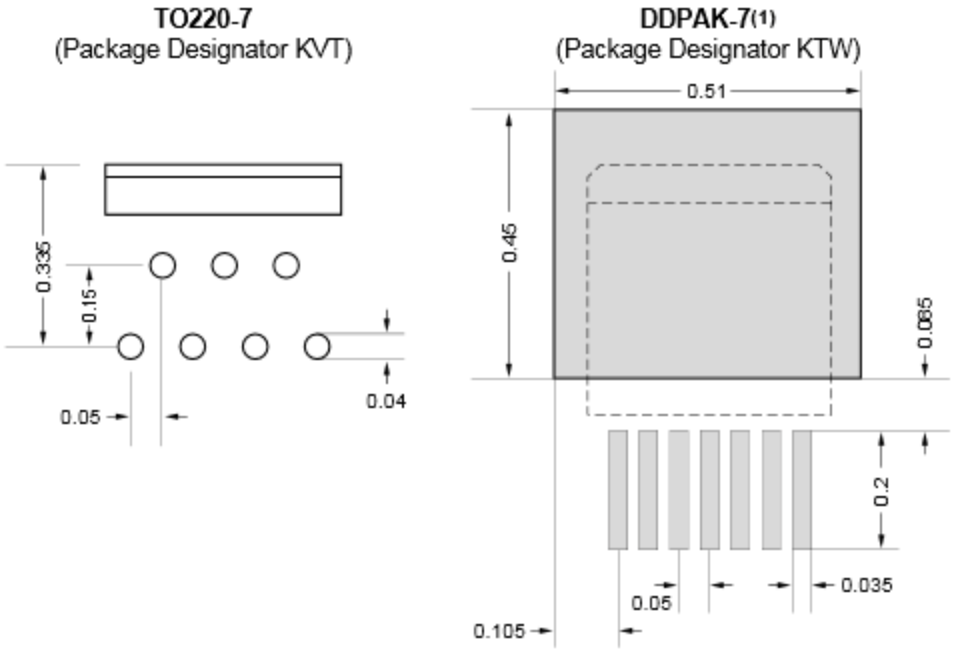
11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。



(1) 为了提高热性能，增加了封装面积。请参阅Figure 43。

(2) 尺寸单位为英寸。有关公差和详细的封装图，请参见机械制图或 www.ti.com.cn。

图 46. TO-220 和 DDPAK 焊盘封装

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA548F/500	ACTIVE	DDPAK/ TO-263	KTW	7	500	RoHS & Green	Call TI | SN	Level-2-260C-1 YEAR	-40 to 85	OPA548F	Samples
OPA548F/500G3	LIFEBUY	DDPAK/ TO-263	KTW	7	500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 85	OPA548F	
OPA548FKTWT	ACTIVE	DDPAK/ TO-263	KTW	7	250	RoHS & Green	Call TI | SN	Level-2-260C-1 YEAR	-40 to 85	OPA548F	Samples
OPA548FKTWTG3	LIFEBUY	DDPAK/ TO-263	KTW	7	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 85	OPA548F	
OPA548T	ACTIVE	TO-220	KVT	7	50	RoHS & Green	Call TI | SN	N / A for Pkg Type	-40 to 85	OPA548T	Samples
OPA548T-1	ACTIVE	TO-220	KC	7	50	RoHS & Green	Call TI | SN	N / A for Pkg Type	-40 to 85	OPA548T	Samples
OPA548T-1G3	LIFEBUY	TO-220	KC	7	50	RoHS & Green	SN	N / A for Pkg Type	-40 to 85	OPA548T	
OPA548TG3	LIFEBUY	TO-220	KVT	7	50	RoHS & Green	SN	N / A for Pkg Type	-40 to 85	OPA548T	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

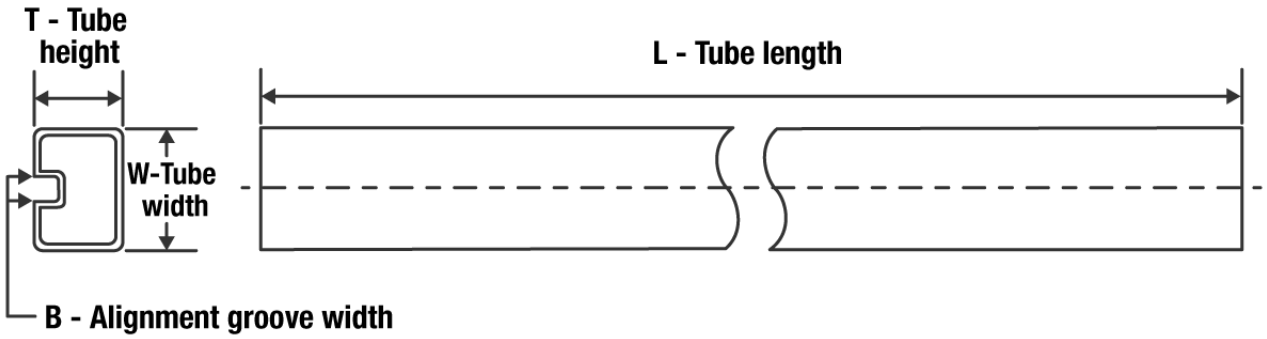
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA548T	KVT	TO-220	7	50	532.13	34.54	13340	NA
OPA548T-1	KC	TO-220	7	50	532.13	34.54	13340	NA
OPA548T-1G3	KC	TO-220	7	50	532.13	34.54	13340	NA
OPA548TG3	KVT	TO-220	7	50	532.13	34.54	13340	NA

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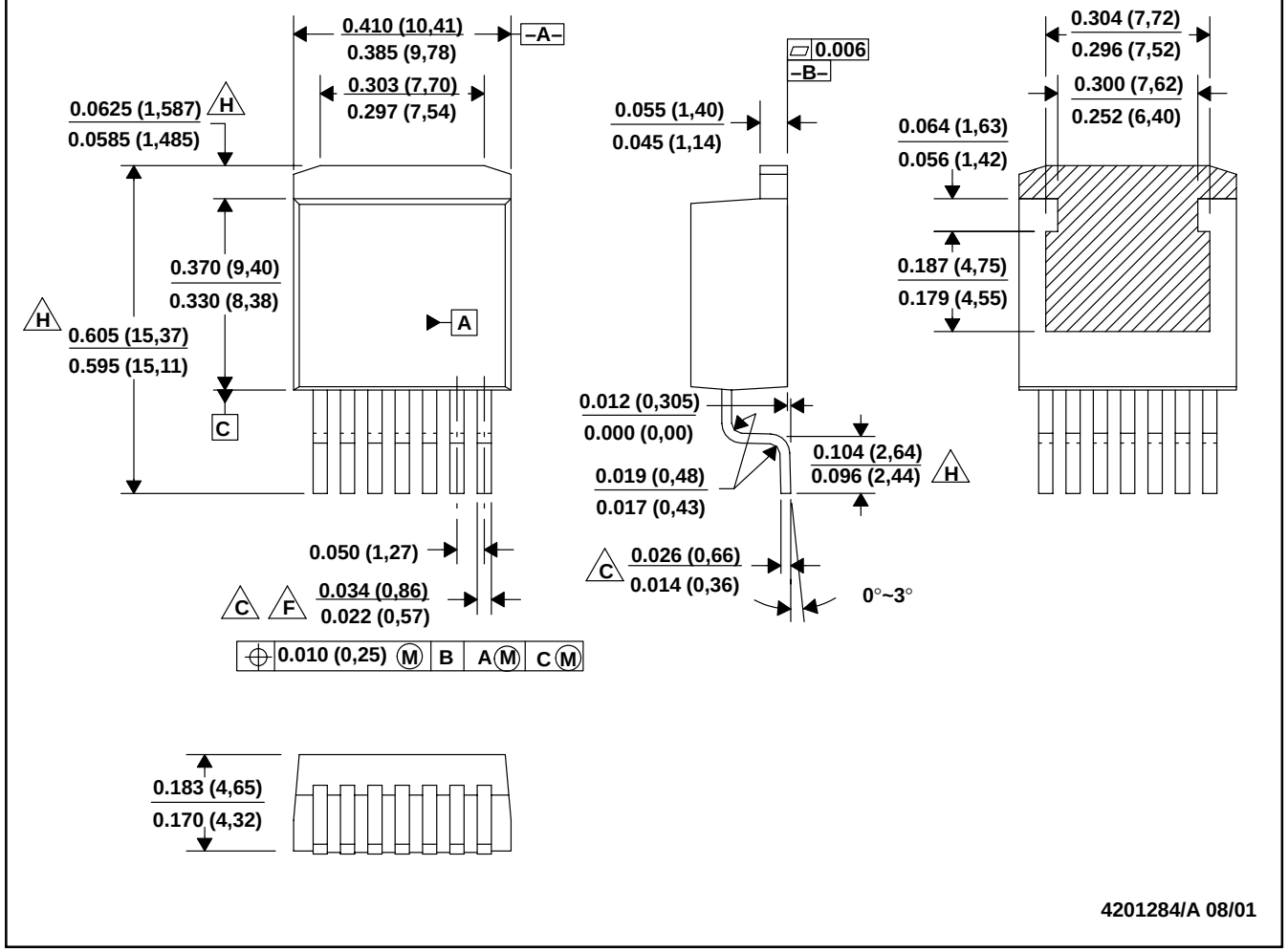
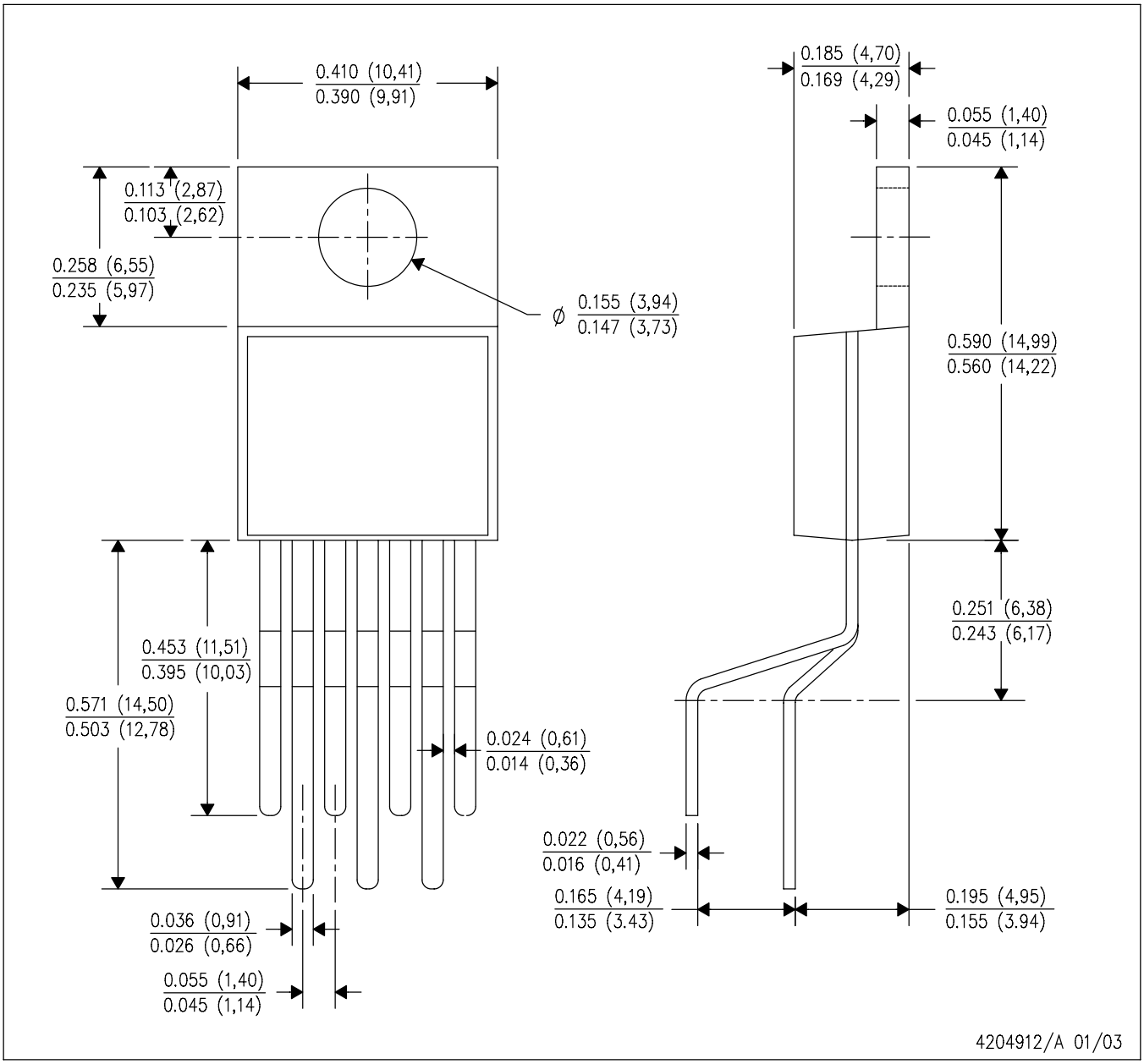
KTW (R-PSFM-G7) **PLASTIC FLANGE-MOUNT**



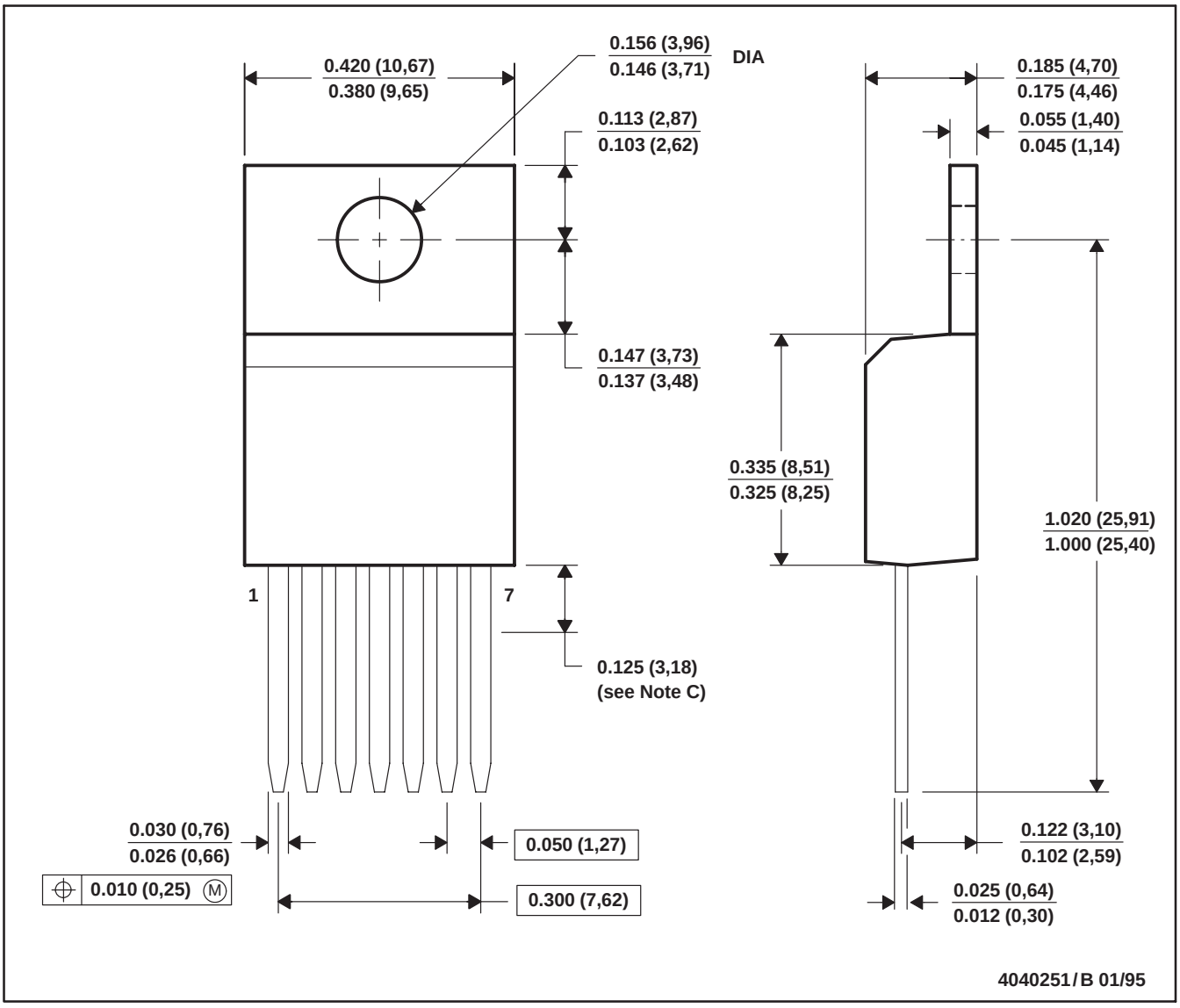
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Lead width and height dimensions apply to the plated lead.
D. Leads are not allowed above the Datum B.
E. Stand–off height is measured from lead tip with reference to Datum B.
F. Lead width dimension does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum dimension by more than 0.003”.
G. Cross–hatch indicates exposed metal surface.
H. Falls within JEDEC MO–169 with the exception of the dimensions indicated.

KVT (R–PZFM–T7) PLASTIC FLANGE MOUNT PACKAGE



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

KC (R-PSFM-T7) **PLASTIC FLANGE-MOUNT PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Lead dimensions are not controlled within this area.
D. All lead dimensions apply before solder dip.
E. The center lead is in electrical contact with the mounting tab.

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