

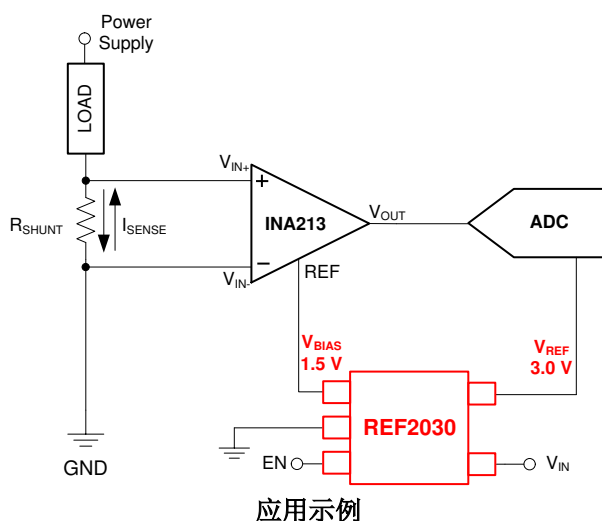
## REF20xx 低漂移、低功率、双路输出、 $V_{REF}$ 和 $V_{REF}/2$ 电压基准

### 1 特性

- 两个输出， $V_{REF}$  和  $V_{REF}/2$ ，方便用于单电源系统
- 出色的温漂性能：
  - -40°C 至 125°C 范围内为 8ppm/°C (最大值)
- 高初始精度： $\pm 0.05\%$  (最大值)
- $V_{REF}$  和  $V_{BIAS}$  跟踪过热：
  - -40°C 至 85°C 范围内为 6ppm/°C (最大值)
  - -40°C 至 125°C 范围内为 7ppm/°C (最大值)
- 微型封装：SOT 23-5
- 低压降：10 mV
- 高输出电流： $\pm 20$  mA
- 低静态电流：360  $\mu$  A
- 线性调节：3ppm/V
- 负载调节：8ppm/mA
- **Matte-Sn** 版本 (REF2025AISDDCR) 在 **Battelle Class III** 和类似严苛环境中的抗腐蚀性得以改进

### 2 应用

- 电表
- 模拟输入模块
- 模拟输出模块
- 伺服驱动器控制模块
- 断路器 (ACB、MCCB、VCB)
- 临床数字温度计
- 实验室和现场仪表
- 电池测试



### 3 说明

仅具有正向电源电压的应用通常需要使用一个处于模数转换器 (ADC) 输入范围中间位置的附加稳定电压来偏置输入双极信号。REF20xx 提供了一个可供 ADC 使用的基准电压 ( $V_{REF}$ ) 和一个可用于偏置输入双极信号的高精度电压 ( $V_{BIAS}$ )。

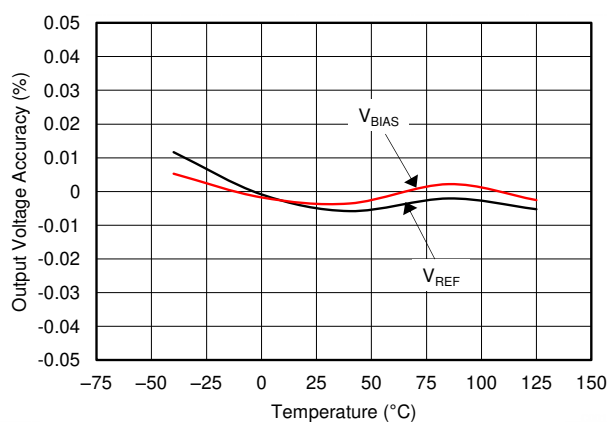
REF20xx 在  $V_{REF}$  和  $V_{BIAS}$  输出端具有出色的温漂 (最大 8ppm/°C) 和初始精度 (0.05%)，同时可保持静态工作电流低于 430  $\mu$  A。此外， $V_{REF}$  和  $V_{BIAS}$  输出端在 -40°C 至 125°C 的温度范围内相互跟踪，精度为 6ppm/°C (最大值)。与分立式解决方案相比，所有这些特性使得 REF20xx 提升了信号链的精度、节省了电路板空间并降低了系统成本。仅 10mV 的超低压降允许器件在极低输入电压条件下工作，这一特性在电池供电系统中非常适用。

$V_{REF}$  和  $V_{BIAS}$  电压具有同样出色的技术规范，而且灌电流和拉电流能力同样强大。这些器件具有优异的长期稳定性和低噪声级别，是高精度工业应用的理想选择。

#### 器件信息

器件名称	封装 (1)	封装尺寸 (标称值)
REF20xx	SOT-23 (5)	2.90mm × 1.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



$V_{REF}$  和  $V_{BIAS}$  与温度间的关系



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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (May 2018) to Revision E (January 2022)	Page
• 更新了“应用”部分.....	1
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• Changed <i>ESD Rating</i> table: changed HBM rating from $\pm 4000$ V to $\pm 2500$ V.....	4
• Updated Long-term stability value.....	5
• Added Long-Term Stability sub-section under Parameter Measurement Information section.....	14

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Changes from Revision C (January 2017) to Revision D (May 2018)	Page
• Changed application information to include corrosion resistance advantages. ....	19

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Changes from Revision B (July 2014) to Revision C (January 2017)	Page
• Added I/O column to <i>Pin Functions</i> table .....	3
• Added <i>Storage temperature</i> parameter to <i>Absolute Maximum Ratings</i> table (moved from <i>ESD Ratings</i> table) .....	4
• Changed <i>ESD Rating</i> table: changed title, updated table format .....	4

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Changes from Revision A (June 2014) to Revision B (July 2014)	Page
• 将器件状态从“量产数据”更改为“混合状态” .....	1
• 删除了“器件信息”表中的脚注 2.....	1
• Deleted footnote from Device Comparison Table .....	3
• Added Thermal Information table.....	4

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Changes from Revision * (May 2014) to Revision A (June 2014)	Page
• 更改了产品预发布数据表.....	1

## 5 Device Comparison Table

PRODUCT	$V_{REF}$	$V_{BIAS}$
REF2025	2.5 V	1.25 V
REF2030	3.0 V	1.5 V
REF2033	3.3 V	1.65 V
REF2041	4.096 V	2.048 V

## 6 Pin Configuration and Functions

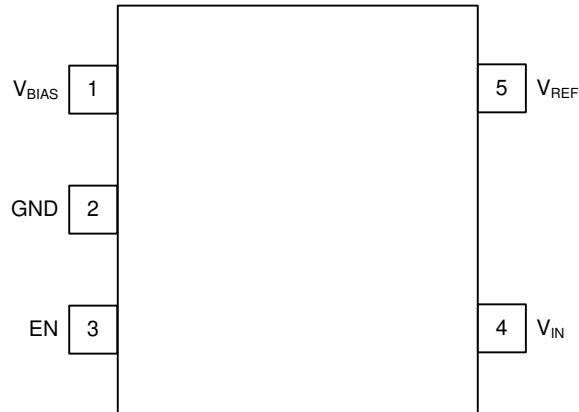


图 6-1. DDC Package SOT23-5 (Top View)

### Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	$V_{BIAS}$	Output	Bias voltage output ( $V_{REF} / 2$ )
2	GND	—	Ground
3	EN	Input	Enable ( $EN \geq V_{IN} - 0.7$ V, device enabled)
4	$V_{IN}$	Input	Input supply voltage
5	$V_{REF}$	Output	Reference voltage output ( $V_{REF}$ )

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Input voltage	V <sub>IN</sub>	- 0.3	6	V
	EN	- 0.3	V <sub>IN</sub> + 0.3	
Temperature	Operating	- 55	150	°C
	Junction, T <sub>j</sub>		150	
	Storage, T <sub>stg</sub>	- 65	170	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2500	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.  
 (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>IN</sub>	Supply input voltage range (I <sub>L</sub> = 0 mA, T <sub>A</sub> = 25°C)	V <sub>REF</sub> + 0.02 <sup>(1)</sup>		5.5	V

- (1) See [图 7-28](#) in [节 7.6](#) for minimum input voltage at different load currents and temperature

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		REF20xx	UNIT
		DDC (SOT23)	
		5 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	193.6	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	40.2	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	34.5	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.9	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	34.3	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Electrical Characteristics

At  $T_A = 25^\circ\text{C}$ ,  $I_L = 0\text{ mA}$ , and  $V_{IN} = 5\text{ V}$ , unless otherwise noted. Both  $V_{REF}$  and  $V_{BIAS}$  have the same specifications.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ACCURACY AND DRIFT</b>						
Output voltage accuracy			-0.05%		0.05%	
Output voltage temperature coefficient <sup>(1)</sup>		$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		$\pm 3$	$\pm 8$	ppm/ $^\circ\text{C}$
$V_{REF}$ and $V_{BIAS}$ tracking over temperature <sup>(2)</sup>		$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$		$\pm 1.5$	$\pm 6$	ppm/ $^\circ\text{C}$
		$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$		$\pm 2$	$\pm 7$	
<b>LINE AND LOAD REGULATION</b>						
$\Delta V_{O(\Delta V)}$ Line regulation		$V_{REF} + 0.02\text{ V} \leq V_{IN} \leq 5.5\text{ V}$		3	35	ppm/V
$\Delta V_{O(\Delta I_L)}$ Load regulation	Sourcing	$0\text{ mA} \leq I_L \leq 20\text{ mA}$ , $V_{REF} + 0.6\text{ V} \leq V_{IN} \leq 5.5\text{ V}$		8	20	ppm/mA
	Sinking	$0\text{ mA} \leq I_L \leq -20\text{ mA}$ , $V_{REF} + 0.02\text{ V} \leq V_{IN} \leq 5.5\text{ V}$		8	20	
<b>POWER SUPPLY</b>						
$I_{CC}$ Supply current	Active mode			360	430	$\mu\text{A}$
		$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$			460	
Shutdown mode				3.3	5	
	$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$				9	
Enable voltage	Device in shutdown mode (EN = 0)		0		0.7	V
	Device in active mode (EN = 1)		$V_{IN} - 0.7$		$V_{IN}$	
Dropout voltage				10	20	mV
	$I_L = 20\text{ mA}$				600	
$I_{SC}$ Short-circuit current				50		mA
$t_{ON}$ Turn-on time	0.1% settling, $C_L = 1\ \mu\text{F}$			500		$\mu\text{s}$
<b>NOISE</b>						
Low-frequency noise <sup>(3)</sup>		$0.1\text{ Hz} \leq f \leq 10\text{ Hz}$		12		ppm <sub>PP</sub>
Output voltage noise density		$f = 100\text{ Hz}$		0.25		ppm/ $\sqrt{\text{Hz}}$
<b>CAPACITIVE LOAD</b>						
Stable output capacitor range			0		10	$\mu\text{F}$
<b>HYSTERESIS AND LONG TERM STABILITY</b>						
Long-term stability <sup>(4)</sup>		0 to 1000 hours		25		ppm
Output voltage hysteresis <sup>(5)</sup>	$25^\circ\text{C}$ , $-40^\circ\text{C}$ , $125^\circ\text{C}$ , $25^\circ\text{C}$		Cycle 1	60		ppm
			Cycle 2	35		

- (1) Temperature drift is specified according to the box method. See the [§ 9.3](#) section for more details.
- (2) The  $V_{REF}$  and  $V_{BIAS}$  tracking over temperature specification is explained in more detail in the [§ 9.3](#) section.
- (3) The peak-to-peak noise measurement procedure is explained in more detail in the [§ 8.4](#) section.
- (4) Long-term stability measurement procedure is explained in more in detail in the [§ 8.2](#) section.
- (5) The thermal hysteresis measurement procedure is explained in more detail in the [§ 8.3](#) section.

## 7.6 Typical Characteristics

At  $T_A = 25^\circ\text{C}$ ,  $I_L = 0\text{ mA}$ ,  $V_{IN} = 5\text{-V}$  power supply,  $C_L = 0\text{ }\mu\text{F}$ , and 2.5-V output, unless otherwise noted.

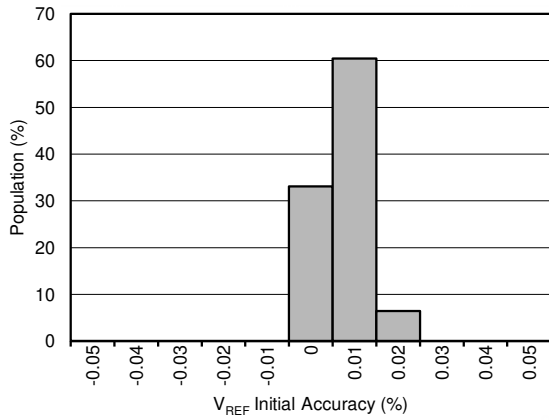
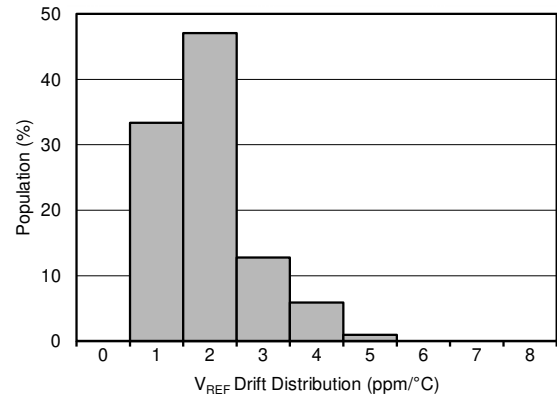


图 7-1. Initial Accuracy Distribution ( $V_{REF}$ )



$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$

图 7-2. Drift Distribution ( $V_{REF}$ )

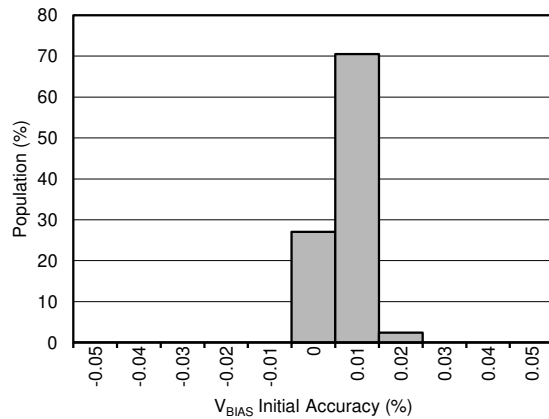
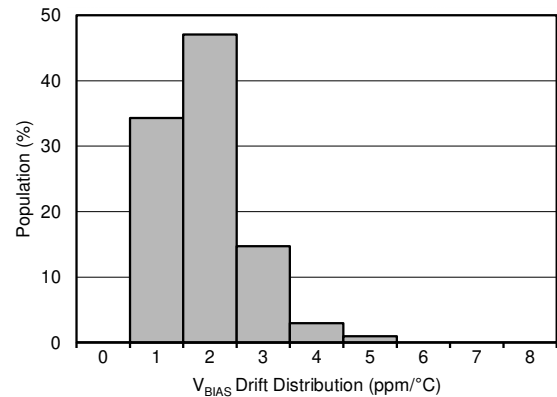


图 7-3. Initial Accuracy Distribution ( $V_{BIAS}$ )



$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$

图 7-4. Drift Distribution ( $V_{BIAS}$ )

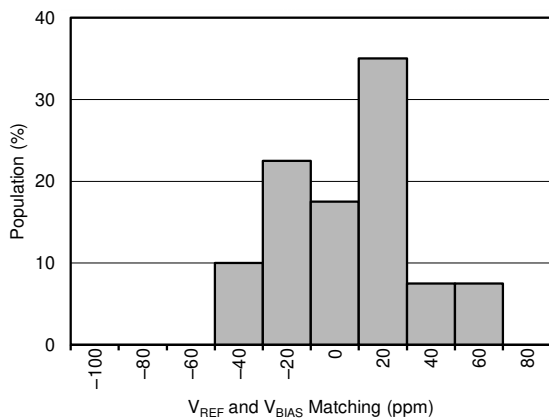
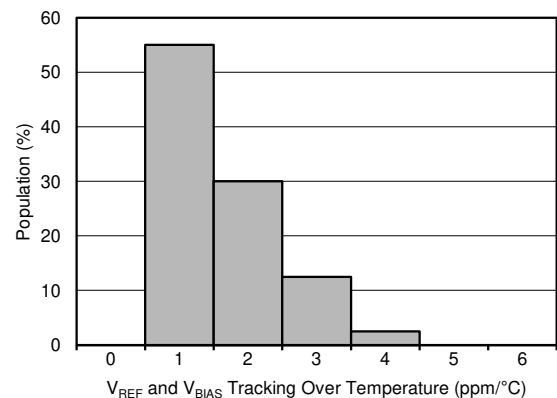


图 7-5.  $V_{REF} - 2 \times V_{BIAS}$  Distribution

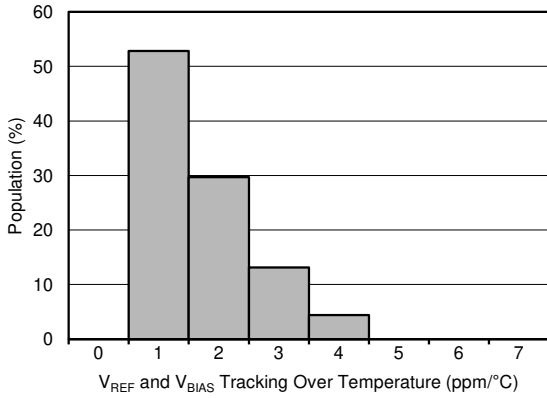


$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$

图 7-6. Distribution of  $V_{REF} - 2 \times V_{BIAS}$  Drift Tracking Over Temperature

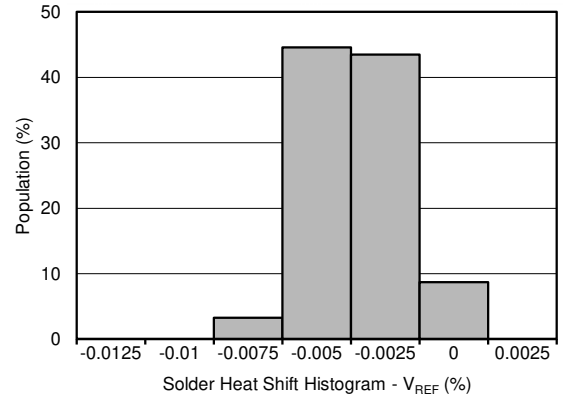
## 7.6 Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $I_L = 0\text{ mA}$ ,  $V_{IN} = 5\text{-V}$  power supply,  $C_L = 0\text{ }\mu\text{F}$ , and  $2.5\text{-V}$  output, unless otherwise noted.



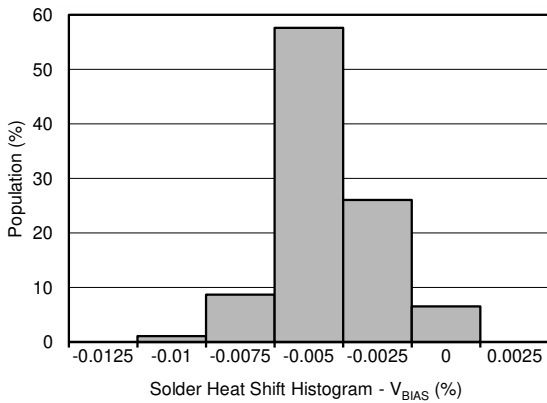
$-40^\circ\text{C} \leq T_A \leq 125^\circ\text{C}$

图 7-7. Distribution of  $V_{REF} - 2 \times V_{BIAS}$  Drift Tracking Over Temperature



Refer to the [§ 8.1](#) section for more information.

图 7-8. Solder Heat Shift Distribution ( $V_{REF}$ )



Refer to the [§ 8.1](#) section for more information.

图 7-9. Solder Heat Shift Distribution ( $V_{BIAS}$ )

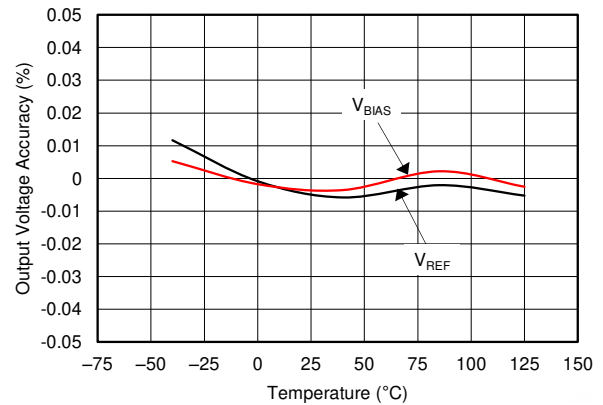


图 7-10. Output Voltage Accuracy ( $V_{REF}$ ) vs Temperature

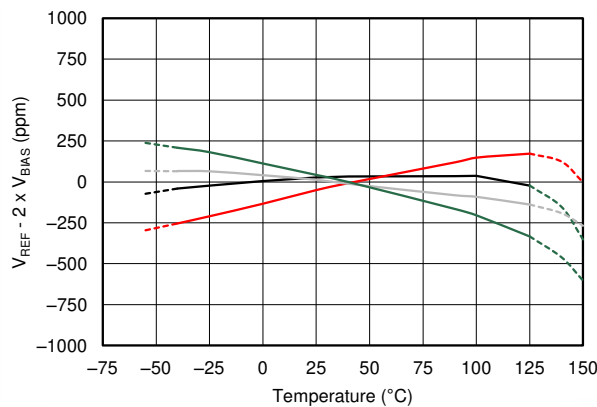


图 7-11.  $V_{REF} - 2 \times V_{BIAS}$  Tracking vs Temperature

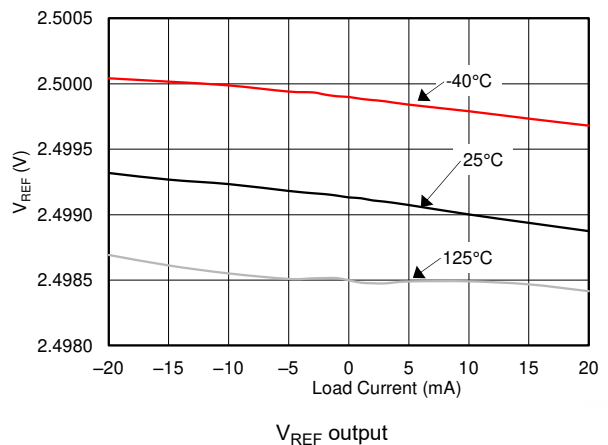


图 7-12. Output Voltage Change vs Load Current ( $V_{REF}$ )

## 7.6 Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $I_L = 0\text{ mA}$ ,  $V_{IN} = 5\text{-V}$  power supply,  $C_L = 0\text{ }\mu\text{F}$ , and  $2.5\text{-V}$  output, unless otherwise noted.

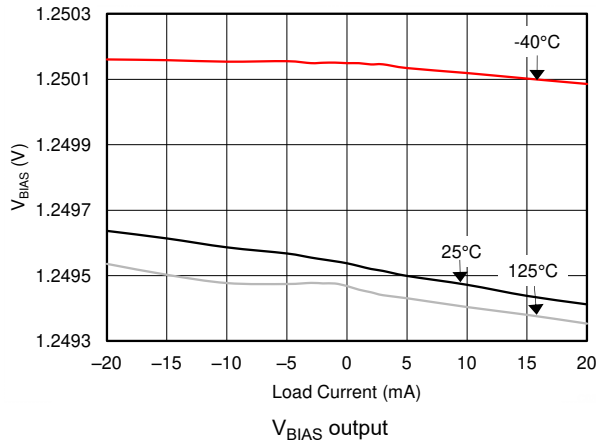


图 7-13. Output Voltage Change vs Load Current ( $V_{BIAS}$ )

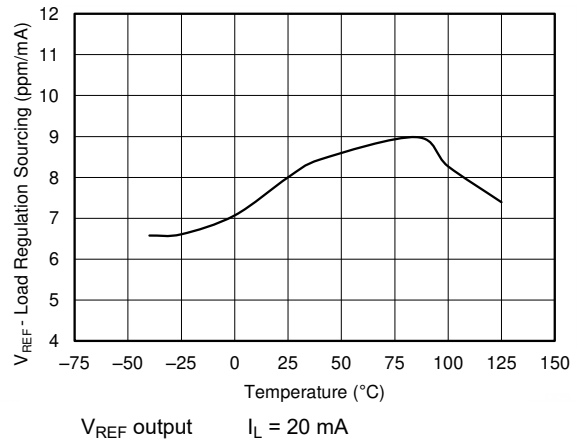


图 7-14. Load Regulation Sourcing vs Temperature ( $V_{REF}$ )

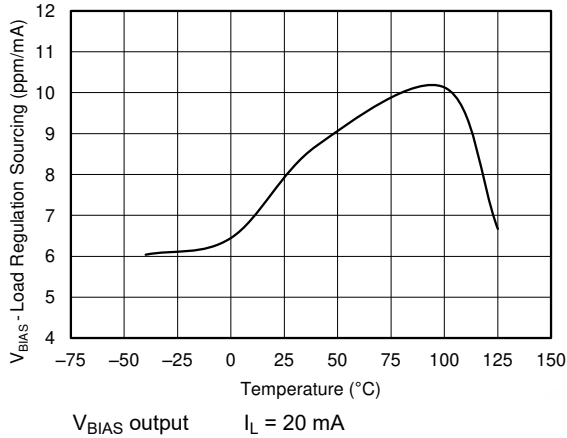


图 7-15. Load Regulation Sourcing vs Temperature ( $V_{BIAS}$ )

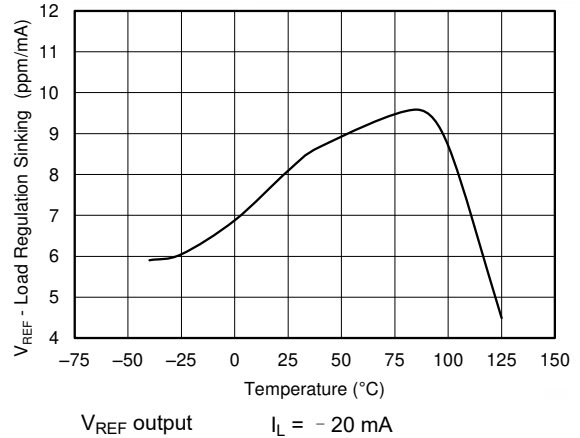


图 7-16. Load Regulation Sinking vs Temperature ( $V_{REF}$ )

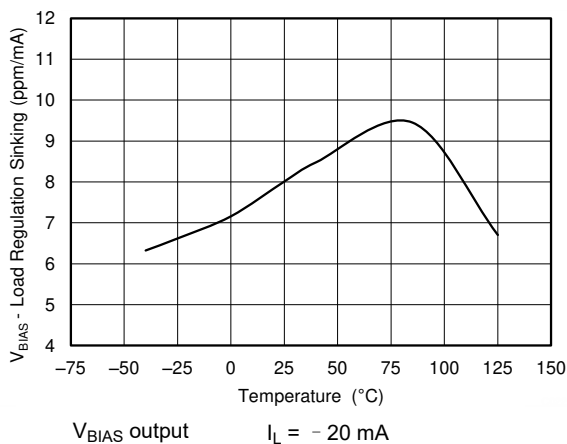


图 7-17. Load Regulation Sinking vs Temperature ( $V_{BIAS}$ )

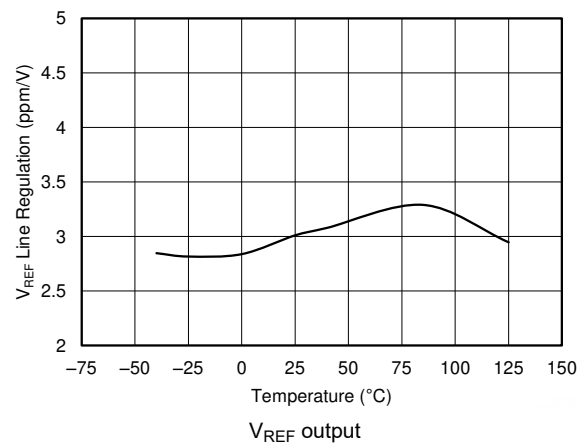


图 7-18. Line Regulation vs Temperature ( $V_{REF}$ )



## 7.6 Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $I_L = 0\text{ mA}$ ,  $V_{IN} = 5\text{-V}$  power supply,  $C_L = 0\text{ }\mu\text{F}$ , and  $2.5\text{-V}$  output, unless otherwise noted.

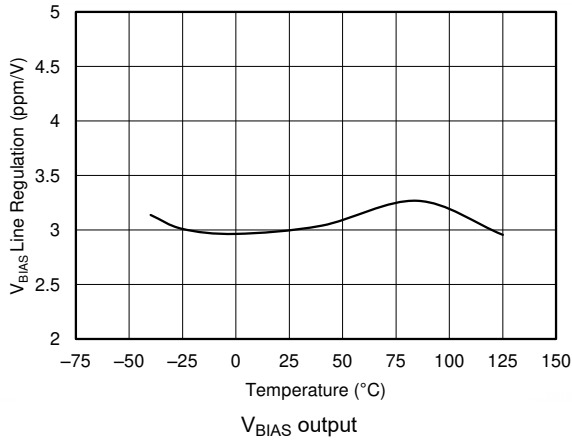


图 7-19. Line Regulation vs Temperature ( $V_{BIAS}$ )

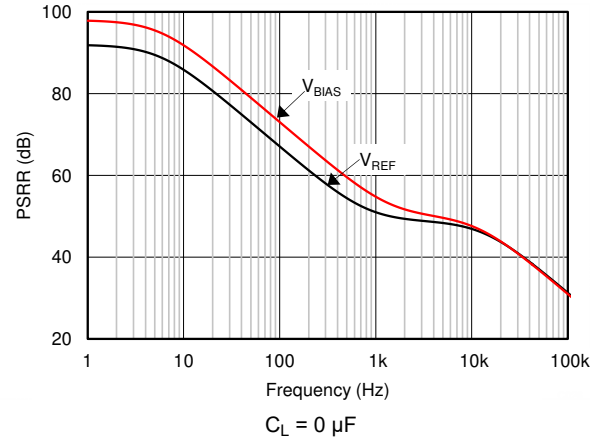


图 7-20. Power-Supply Rejection Ratio vs Frequency

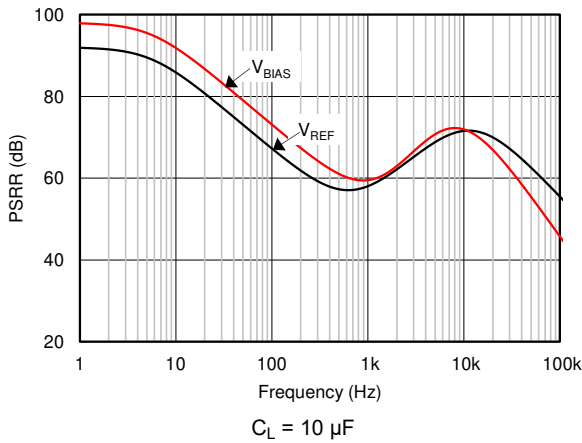


图 7-21. Power-Supply Rejection Ratio vs Frequency

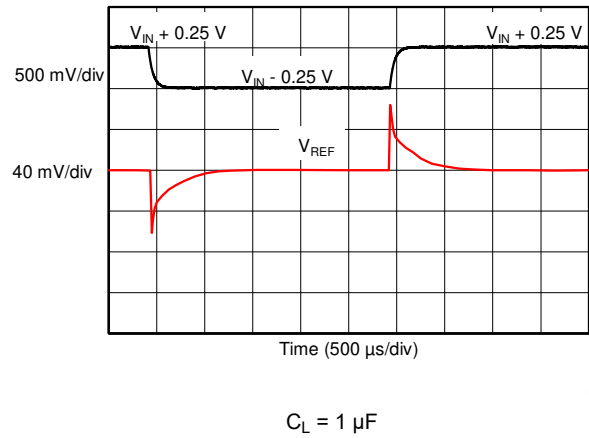


图 7-22. Line Transient Response

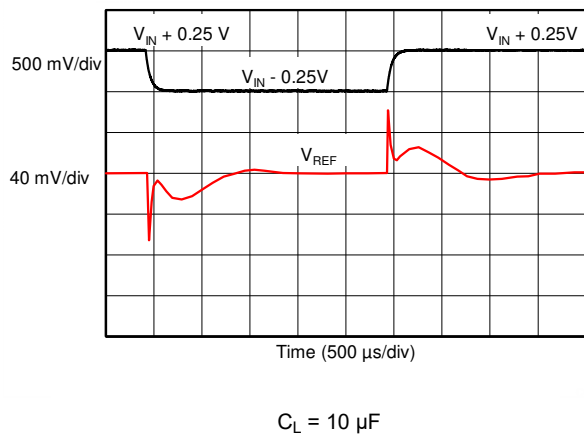


图 7-23. Line Transient Response

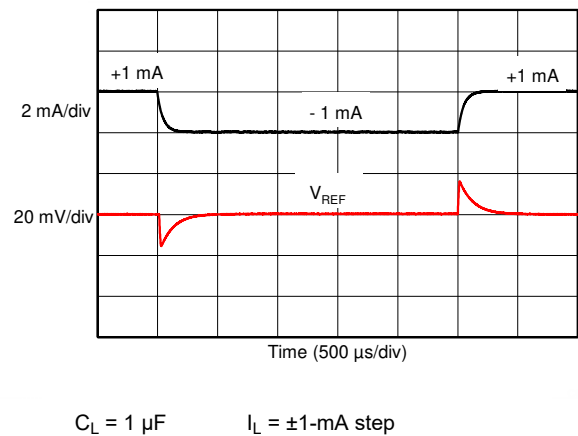
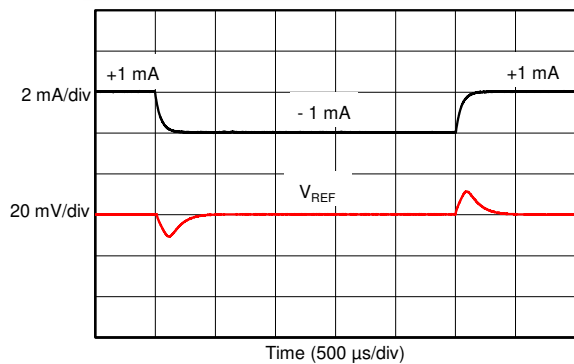


图 7-24. Load Transient Response

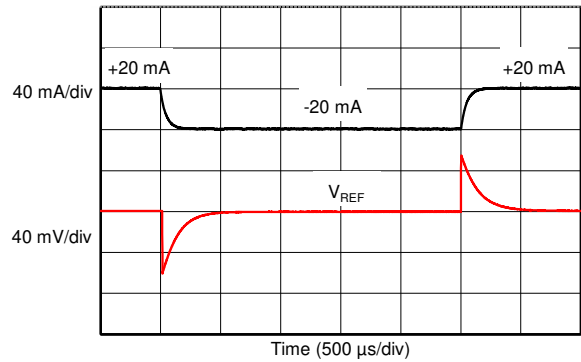
## 7.6 Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $I_L = 0\text{ mA}$ ,  $V_{IN} = 5\text{-V}$  power supply,  $C_L = 0\text{ }\mu\text{F}$ , and 2.5-V output, unless otherwise noted.



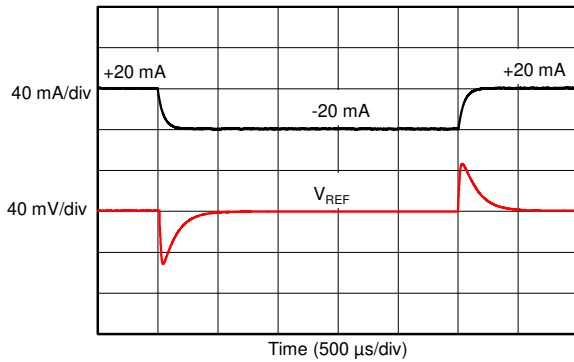
$C_L = 10\text{ }\mu\text{F}$      $I_L = \pm 1\text{-mA}$  step

图 7-25. Load Transient Response



$C_L = 1\text{ }\mu\text{F}$      $I_L = \pm 20\text{-mA}$  step

图 7-26. Load Transient Response



$C_L = 10\text{ }\mu\text{F}$      $I_L = \pm 20\text{-mA}$  step

图 7-27. Load Transient Response

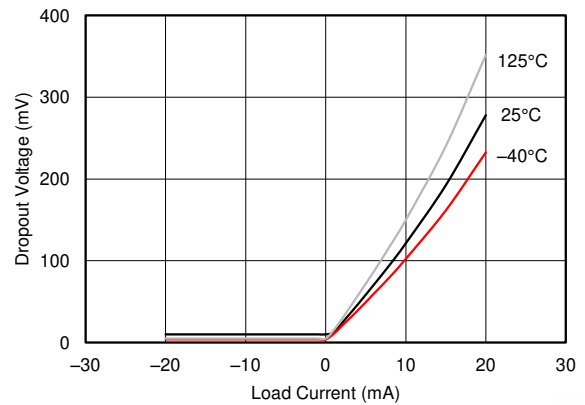
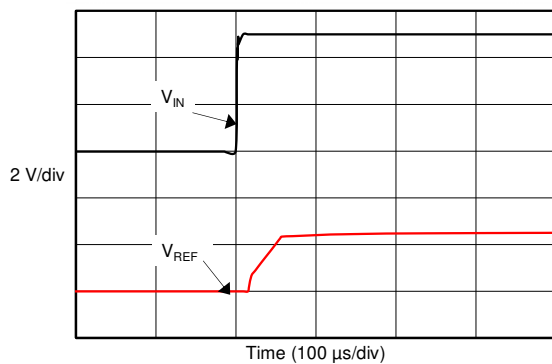
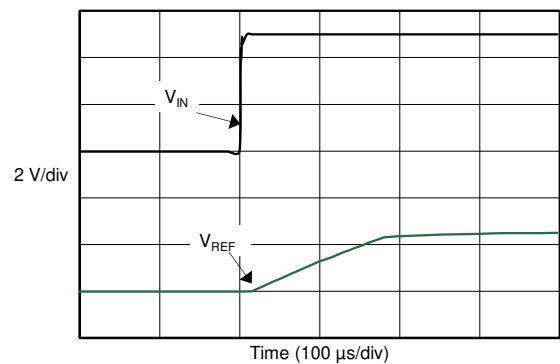


图 7-28. Minimum Dropout Voltage vs Load Current



$C_L = 1\text{ }\mu\text{F}$

图 7-29. Turn-On Settling Time



$C_L = 10\text{ }\mu\text{F}$

图 7-30. Turn-On Settling Time

## 7.6 Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $I_L = 0\text{ mA}$ ,  $V_{IN} = 5\text{-V}$  power supply,  $C_L = 0\ \mu\text{F}$ , and 2.5-V output, unless otherwise noted.

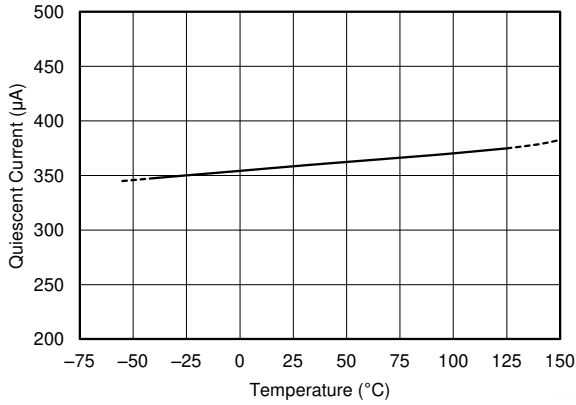


图 7-31. Quiescent Current vs Temperature

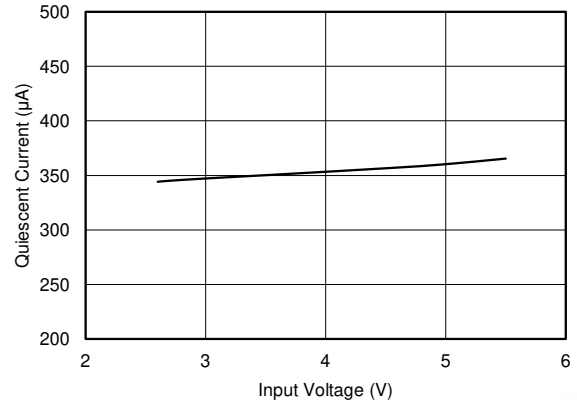
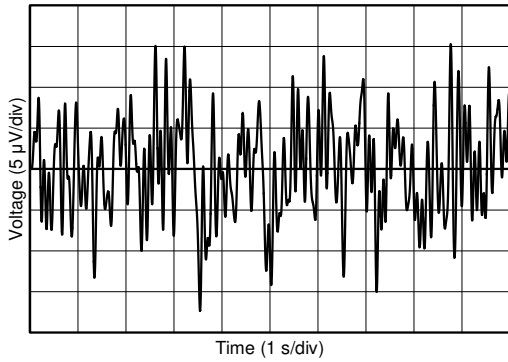
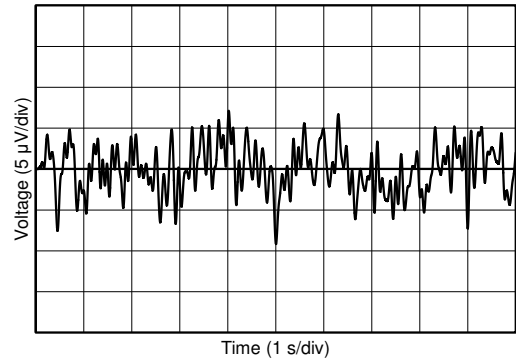


图 7-32. Quiescent Current vs Input Voltage



$V_{REF}$  output

图 7-33. 0.1-Hz to 10-Hz Noise ( $V_{REF}$ )



$V_{BIAS}$  output

图 7-34. 0.1-Hz to 10-Hz Noise ( $V_{BIAS}$ )

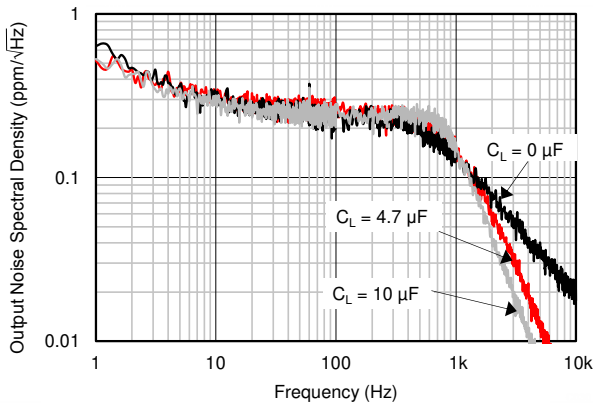
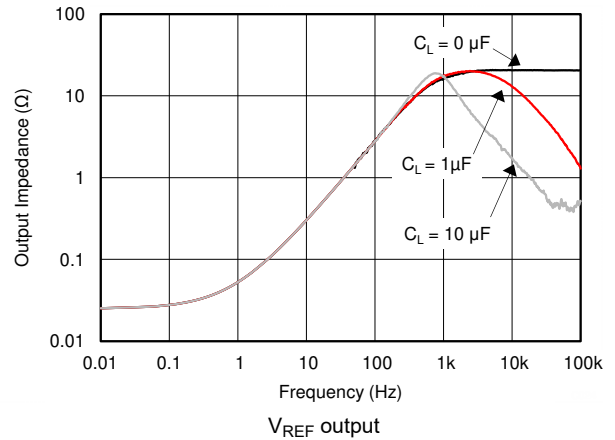


图 7-35. Output Voltage Noise Spectrum



$V_{REF}$  output

图 7-36. Output Impedance vs Frequency ( $V_{REF}$ )

## 7.6 Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $I_L = 0\text{ mA}$ ,  $V_{IN} = 5\text{-V}$  power supply,  $C_L = 0\ \mu\text{F}$ , and 2.5-V output, unless otherwise noted.

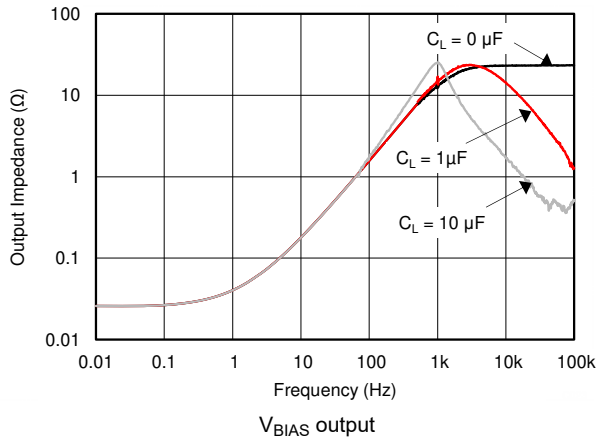


图 7-37. Output Impedance vs Frequency ( $V_{BIAS}$ )

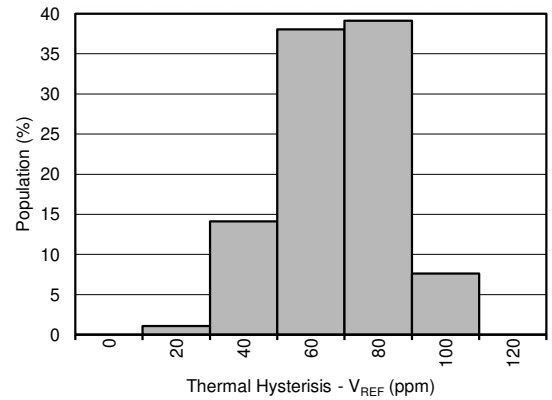


图 7-38. Thermal Hysteresis Distribution ( $V_{REF}$ )

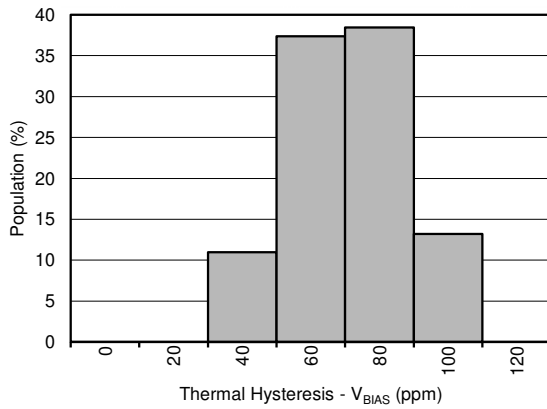


图 7-39. Thermal Hysteresis Distribution ( $V_{BIAS}$ )

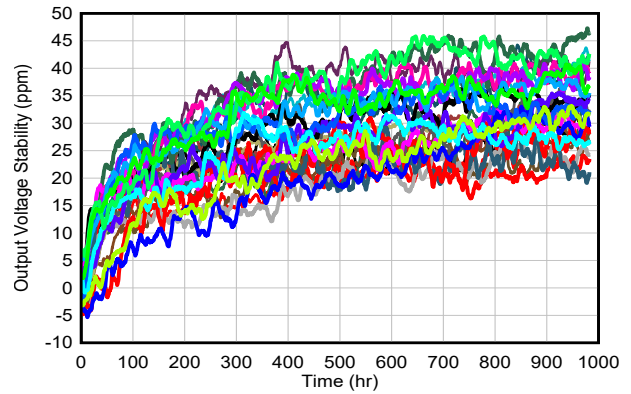


图 7-40. Long-Term Stability (First 1000 hours)

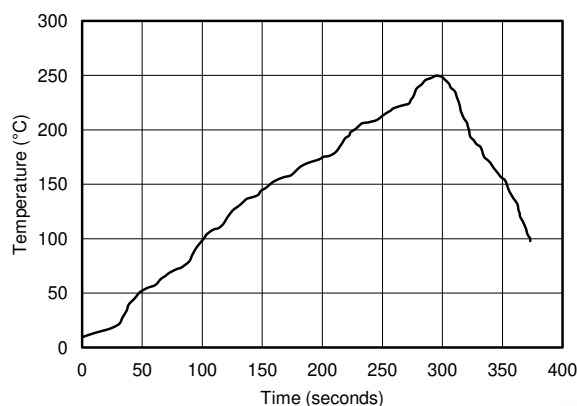
## 8 Parameter Measurement Information

### 8.1 Solder Heat Shift

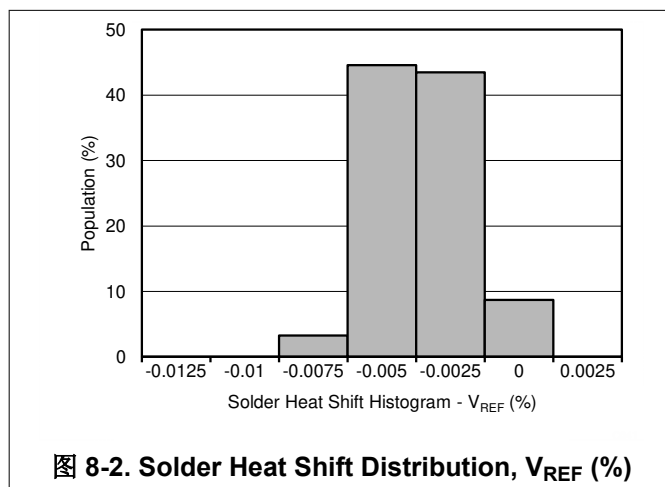
The materials used in the manufacture of the REF20xx have differing coefficients of thermal expansion, resulting in stress on the device die when the part is heated. Mechanical and thermal stress on the device die can cause the output voltages to shift, degrading the initial accuracy specifications of the product. Reflow soldering is a common cause of this error.

In order to illustrate this effect, a total of 92 devices were soldered on four printed circuit boards [23 devices on each printed circuit board (PCB)] using lead-free solder paste and the paste manufacturer suggested reflow profile. The reflow profile is as shown in [图 8-1](#). The printed circuit board is comprised of FR4 material. The board thickness is 1.57 mm and the area is 171.54 mm × 165.1 mm.

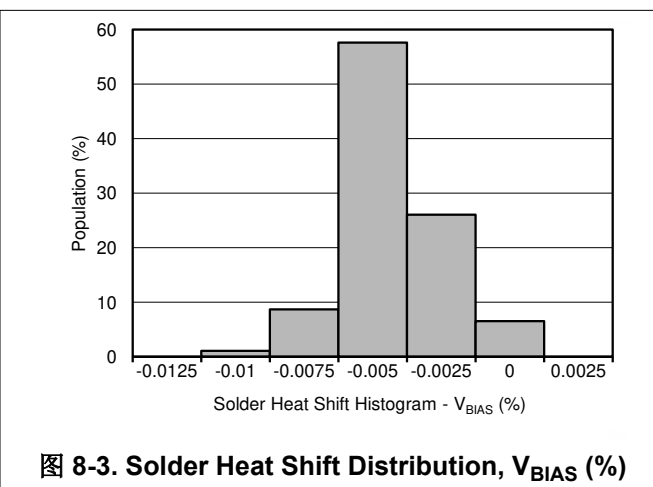
The reference and bias output voltages are measured before and after the reflow process; the typical shift is displayed in [图 8-2](#) and [图 8-3](#). Although all tested units exhibit very low shifts (< 0.01%), higher shifts are also possible depending on the size, thickness, and material of the printed circuit board. An important note is that the histograms display the typical shift for exposure to a single reflow profile. Exposure to multiple reflows, as is common on PCBs with surface-mount components on both sides, causes additional shifts in the output bias voltage. If the PCB is exposed to multiple reflows, the device should be soldered in the second pass to minimize its exposure to thermal stress.



**图 8-1. Reflow Profile**



**图 8-2. Solder Heat Shift Distribution, V<sub>REF</sub> (%)**



**图 8-3. Solder Heat Shift Distribution, V<sub>BIAS</sub> (%)**

## 8.2 Long-Term Stability

The long term stability of the REF20xx was collected on 32 parts that were soldered onto Printed Circuit Boards without any slots or special layout considerations. The boards were then placed into an oven with air temperature maintained at  $T_A = 35^\circ\text{C}$ . The  $V_{\text{REF}}$  output of the 32 parts was measured regularly. Typical long term stability is as shown in [图 8-4](#).

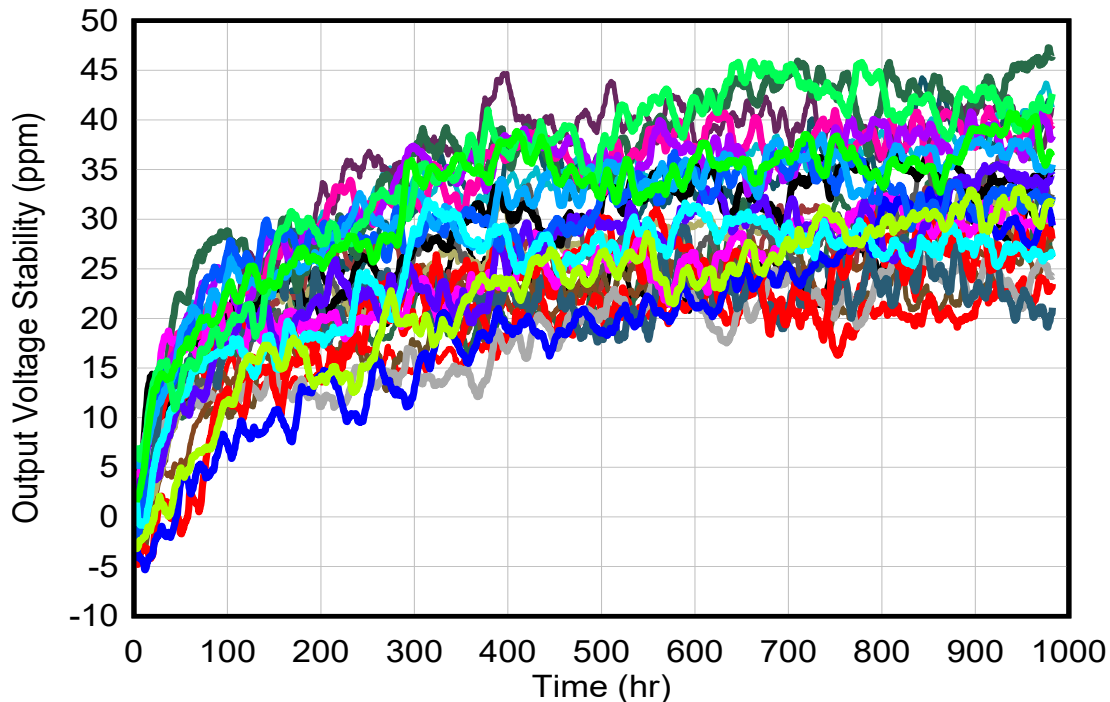


图 8-4. Long Term Stability - 1000 hours ( $V_{\text{REF}}$ )

### 8.3 Thermal Hysteresis

Thermal hysteresis is measured with the REF20xx soldered to a PCB, similar to a real-world application. Thermal hysteresis for the device is defined as the change in output voltage after operating the device at 25°C, cycling the device through the specified temperature range, and returning to 25°C. Hysteresis can be expressed by 方程式 1:

$$V_{\text{HYST}} = \left( \frac{|V_{\text{PRE}} - V_{\text{POST}}|}{V_{\text{NOM}}} \right) \cdot 10^6 \quad (\text{ppm}) \quad (1)$$

where

- $V_{\text{HYST}}$  = thermal hysteresis (in units of ppm),
- $V_{\text{NOM}}$  = the specified output voltage,
- $V_{\text{PRE}}$  = output voltage measured at 25°C pre-temperature cycling, and
- $V_{\text{POST}}$  = output voltage measured after the device has cycled from 25°C through the specified temperature range of - 40°C to 125°C and returns to 25°C.

Typical thermal hysteresis distribution is as shown in 图 8-5 and 图 8-6.

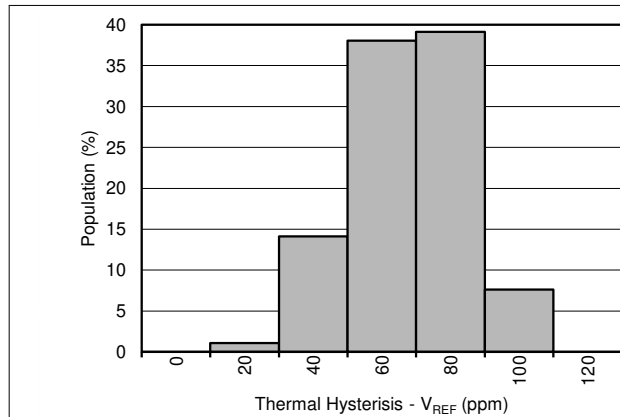


图 8-5. Thermal Hysteresis Distribution (V<sub>REF</sub>)

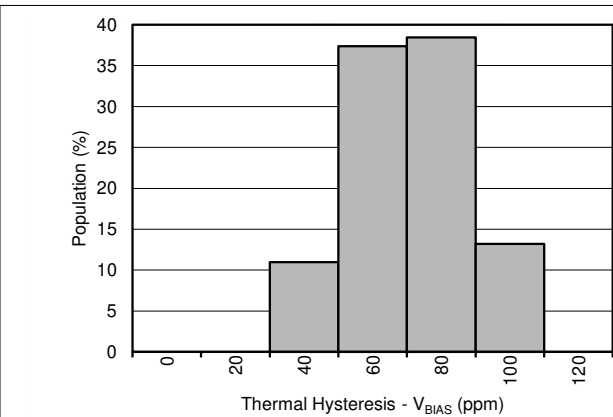
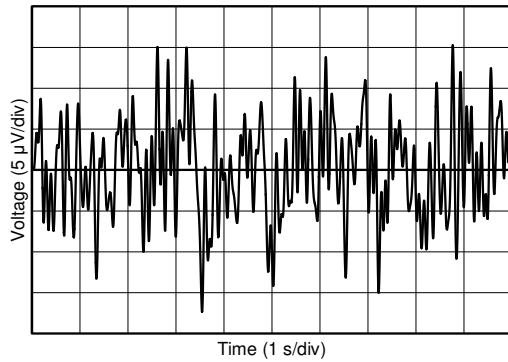


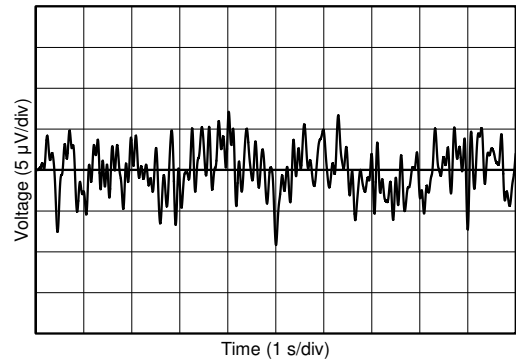
图 8-6. Thermal Hysteresis Distribution (V<sub>BIAS</sub>)

## 8.4 Noise Performance

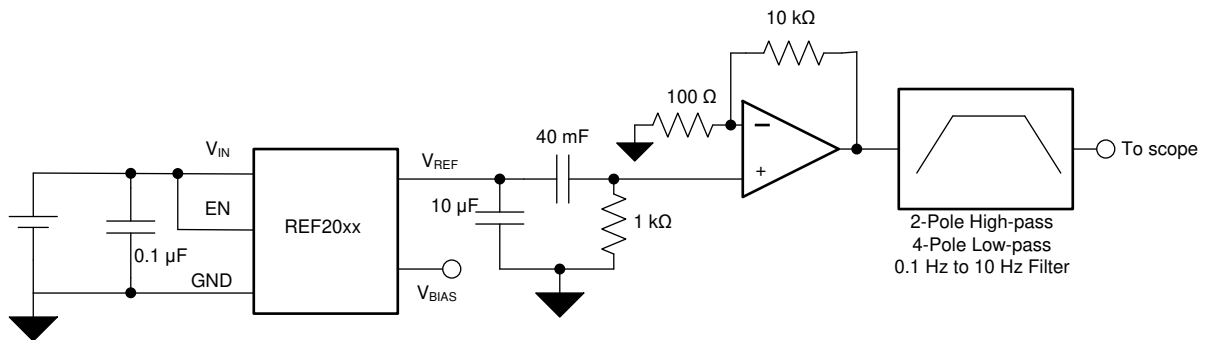
Typical 0.1-Hz to 10-Hz voltage noise can be seen in [图 8-7](#) and [图 8-8](#). Device noise increases with output voltage and operating temperature. Additional filtering can be used to improve output noise levels, although care should be taken to ensure the output impedance does not degrade ac performance. Peak-to-peak noise measurement setup is shown in [图 8-9](#).



**图 8-7. 0.1-Hz to 10-Hz Noise ( $V_{REF}$ )**



**图 8-8. 0.1-Hz to 10-Hz Noise ( $V_{BIAS}$ )**



**图 8-9. 0.1-Hz to 10-Hz Noise Measurement Setup**



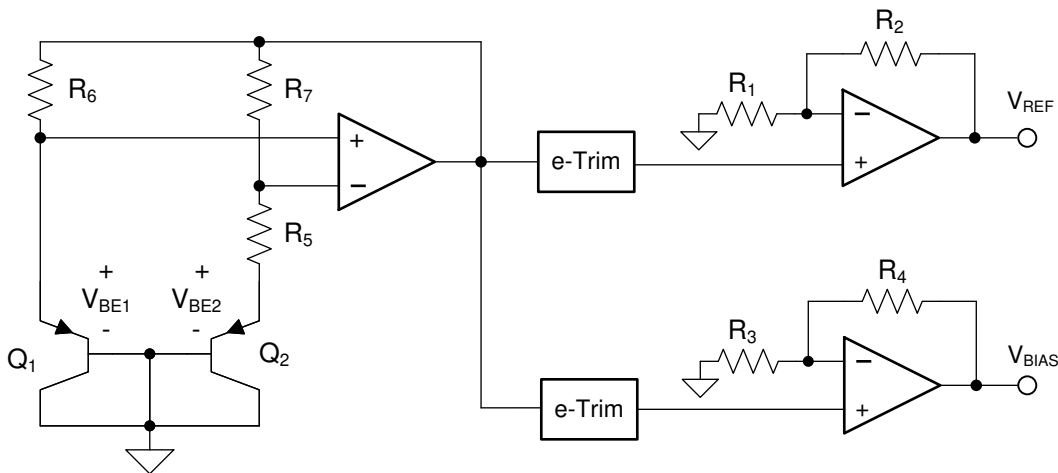
## 9 Detailed Description

### 9.1 Overview

The REF20xx are a family of dual-output,  $V_{REF}$  and  $V_{BIAS}$  ( $V_{REF} / 2$ ) band-gap voltage references. The [# 9.2](#) section provides a block diagram of the basic band-gap topology and the two buffers used to derive the  $V_{REF}$  and  $V_{BIAS}$  outputs. Transistors  $Q_1$  and  $Q_2$  are biased such that the current density of  $Q_1$  is greater than that of  $Q_2$ . The difference of the two base emitter voltages ( $V_{BE1} - V_{BE2}$ ) has a positive temperature coefficient and is forced across resistor  $R_5$ . The voltage is amplified and added to the base emitter voltage of  $Q_2$ , which has a negative temperature coefficient. The resulting band-gap output voltage is almost independent of temperature. Two independent buffers are used to generate  $V_{REF}$  and  $V_{BIAS}$  from the band-gap voltage. The resistors  $R_1$ ,  $R_2$  and  $R_3$ ,  $R_4$  are sized such that  $V_{BIAS} = V_{REF} / 2$ .

e-Trim™ is a method of package-level trim for the initial accuracy and temperature coefficient of  $V_{REF}$  and  $V_{BIAS}$ , implemented during the final steps of manufacturing after the plastic molding process. This method minimizes the influence of inherent transistor mismatch, as well as errors induced during package molding. e-Trim is implemented in the REF20xx to minimize the temperature drift and maximize the initial accuracy of both the  $V_{REF}$  and  $V_{BIAS}$  outputs.

### 9.2 Functional Block Diagram



### 9.3 Feature Description

#### 9.3.1 $V_{REF}$ and $V_{BIAS}$ Tracking

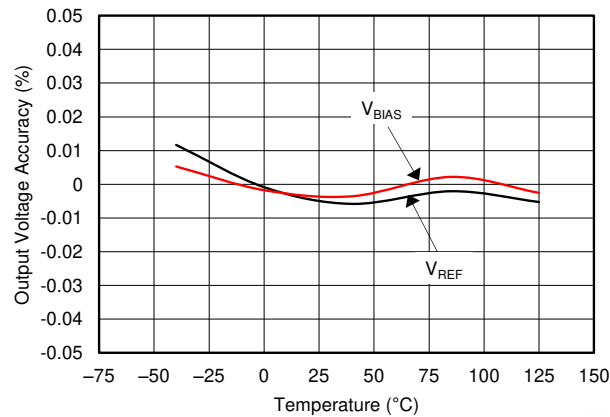
Most single-supply systems require an additional stable voltage in the middle of the analog-to-digital converter (ADC) input range to bias input bipolar signals. The  $V_{REF}$  and  $V_{BIAS}$  outputs of the REF20xx are generated from the same band-gap voltage as shown in the [# 9.2](#) section. Hence, both outputs track each other over the full temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  with an accuracy of 7 ppm/ $^{\circ}\text{C}$  (maximum). The tracking accuracy increases to 6 ppm/ $^{\circ}\text{C}$  (maximum) when the temperature range is limited to  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . The tracking error is calculated using the box method, as described by [方程式 2](#):

$$\text{Tracking Error} = \left( \frac{V_{\text{DIFF(MAX)}} - V_{\text{DIFF(MIN)}}}{V_{\text{REF}} \cdot \text{Temperature Range}} \right) \cdot 10^6 \quad (\text{ppm}) \quad (2)$$

where

- $V_{\text{DIFF}} = V_{\text{REF}} - 2 \cdot V_{\text{BIAS}}$

The tracking accuracy is as shown in [图 9-1](#).



**图 9-1. V<sub>REF</sub> and V<sub>BIAS</sub> Tracking vs Temperature**

### 9.3.2 Low Temperature Drift

The REF20xx is designed for minimal drift error, which is defined as the change in output voltage over temperature. The drift is calculated using the box method, as described by [方程式 3](#):

$$\text{Drift} = \left( \frac{V_{\text{REF(MAX)}} - V_{\text{REF(MIN)}}}{V_{\text{REF}} \cdot \text{Temperature Range}} \right) \cdot 10^6 \quad (\text{ppm}) \quad (3)$$

### 9.3.3 Load Current

The REF20xx family is specified to deliver a current load of  $\pm 20$  mA per output. Both the V<sub>REF</sub> and V<sub>BIAS</sub> outputs of the device are protected from short circuits by limiting the output short-circuit current to 50 mA. The device temperature increases according to [方程式 4](#):

$$T_J = T_A + P_D \cdot R_{\theta JA} \quad (4)$$

where

- T<sub>J</sub> = junction temperature (°C),
- T<sub>A</sub> = ambient temperature (°C),
- P<sub>D</sub> = power dissipated (W), and
- R<sub>θJA</sub> = junction-to-ambient thermal resistance (°C/W)

The REF20xx maximum junction temperature must not exceed the absolute maximum rating of 150°C.

## 9.4 Device Functional Modes

When the EN pin of the REF20xx is pulled high, the device is in active mode. The device should be in active mode for normal operation. The REF20xx can be placed in a low-power mode by pulling the ENABLE pin low. When in shutdown mode, the output of the device becomes high impedance and the quiescent current of the device reduces to 5 μA in shutdown mode. See the [# 7.5](#) for logic high and logic low voltage levels.

## 10 Applications and Implementation

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### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

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### 10.1 Application Information

The low-drift, bidirectional, single-supply, low-side, current-sensing solution, described in this section, can accurately detect load currents from  $-2.5\text{ A}$  to  $2.5\text{ A}$ . The linear range of the output is from  $250\text{ mV}$  to  $2.75\text{ V}$ . Positive current is represented by output voltages from  $1.5\text{ V}$  to  $2.75\text{ V}$ , whereas negative current is represented by output voltages from  $250\text{ mV}$  to  $1.5\text{ V}$ . The difference amplifier is the [INA213](#) current-shunt monitor, whose supply and reference voltages are supplied by the low-drift REF2030.

Industrial applications with electronics in corrosive environments are susceptible to corrosive damage due to the exposure to heat, moisture, and corrosive gases. The combination of the following conditions in a given system lead to higher risk of corrosive damage:

1. Ventilated enclosures exposing underlying PCB.
2. PCBs not conformally coated.
3. Exposed-lead components with plating susceptible to corrosion.
4. Changes in plating techniques for RoHS compliance (e.g. removal of Pb (lead) and certain types of plating).

To improve resistance to corrosion in harsh environments, the REF2025AISDDCR uses Matte-Sn plating with improved assembly process to reduce exposed Cu, leading to improved corrosion resistance in the Battelle Class III and similar harsh environments. The “S” in the part number identifies this special plating option. REF2025 versions that do not have the “S” will continue to be available in industry standard NiPdAu processing technique.

## 10.2 Typical Application

### 10.2.1 Low-Side, Current-Sensing Application

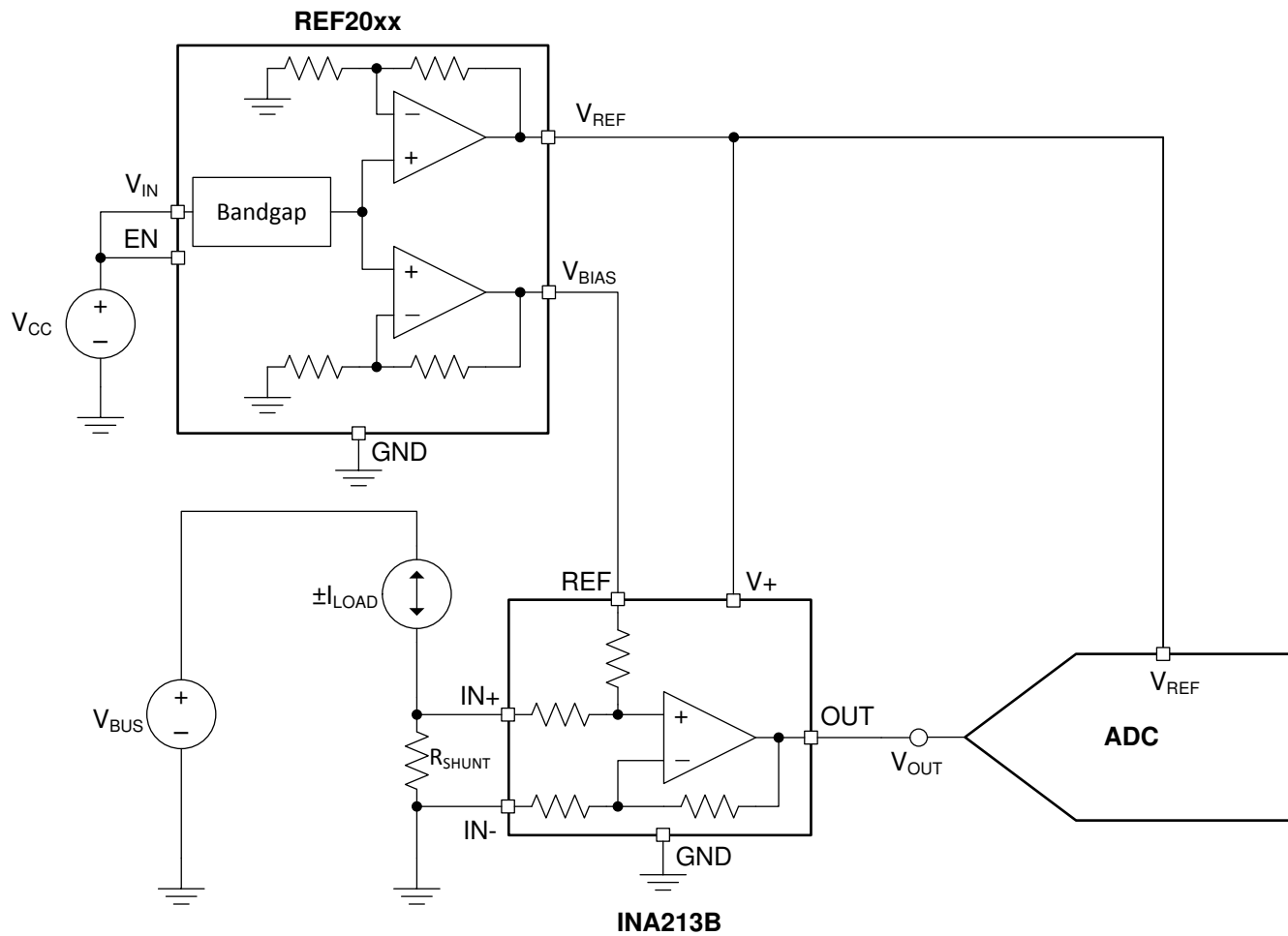


图 10-1. Low-Side, Current-Sensing Application

### 10.2.1.1 Design Requirements

The design requirements are as follows:

1. Supply voltage: 5.0 V
2. Load current:  $\pm 2.5$  A
3. Output: 250 mV to 2.75 V
4. Maximum shunt voltage:  $\pm 25$  mV

### 10.2.1.2 Detailed Design Procedure

Low-side current sensing is desirable because the common-mode voltage is near ground. Therefore, the current-sensing solution is independent of the bus voltage,  $V_{BUS}$ . When sensing bidirectional currents, use a differential amplifier with a reference pin. This procedure allows for the differentiation between positive and negative currents by biasing the output stage such that it can respond to negative input voltages. There are a variety of methods for supplying power ( $V+$ ) and the reference voltage ( $V_{REF}$ , or  $V_{BIAS}$ ) to the differential amplifier. For a low-drift solution, use a monolithic reference that supplies both power and the reference voltage. 图 10-2 shows the general circuit topology for a low-drift, low-side, bidirectional, current-sensing solution. This topology is particularly useful when interfacing with an ADC; see 图 10-1. Not only do  $V_{REF}$  and  $V_{BIAS}$  track over temperature, but their matching is much better than alternate topologies. For a more detailed version of the design procedure, refer to TIDU357.

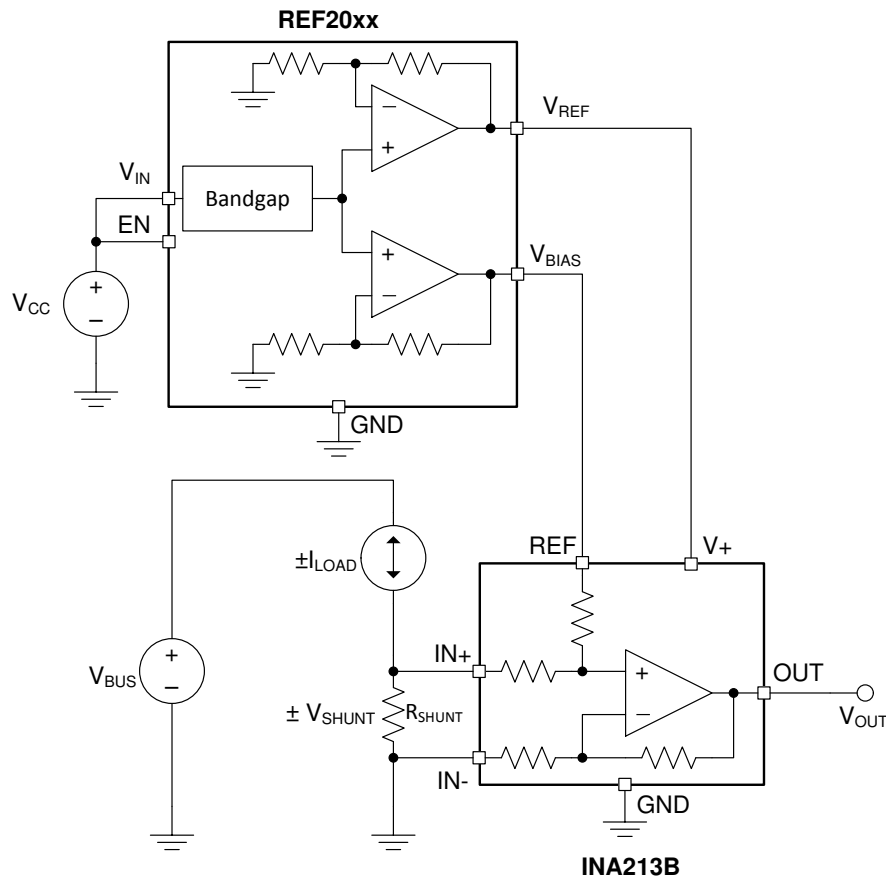


图 10-2. Low-Drift, Low-side, Bidirectional, Current-Sensing Circuit Topology

The transfer function for the circuit given in 图 10-2 is as shown in 方程式 5:

$$\begin{aligned} V_{OUT} &= G \cdot (\pm V_{SHUNT}) + V_{BIAS} \\ &= G \cdot (\pm I_{LOAD} \cdot R_{SHUNT}) + V_{BIAS} \end{aligned} \quad (5)$$

### 10.2.1.2.1 Shunt Resistor

As illustrated in [图 10-2](#), the value of  $V_{SHUNT}$  is the ground potential for the system load. If the value of  $V_{SHUNT}$  is too large, issues may arise when interfacing with systems whose ground potential is actually 0 V. Also, a value of  $V_{SHUNT}$  that is too negative may violate the input common-mode voltage of the differential amplifier in addition to potential interfacing issues. Therefore, limiting the voltage across the shunt resistor is important. [方程式 6](#) can be used to calculate the maximum value of  $R_{SHUNT}$ .

$$R_{SHUNT(max)} = \frac{V_{SHUNT(max)}}{I_{LOAD(max)}} \quad (6)$$

Given that the maximum shunt voltage is  $\pm 25$  mV and the load current range is  $\pm 2.5$  A, the maximum shunt resistance is calculated as shown in [方程式 7](#).

$$R_{SHUNT(max)} = \frac{V_{SHUNT(max)}}{I_{LOAD(max)}} = \frac{25mV}{2.5A} = 10m\Omega \quad (7)$$

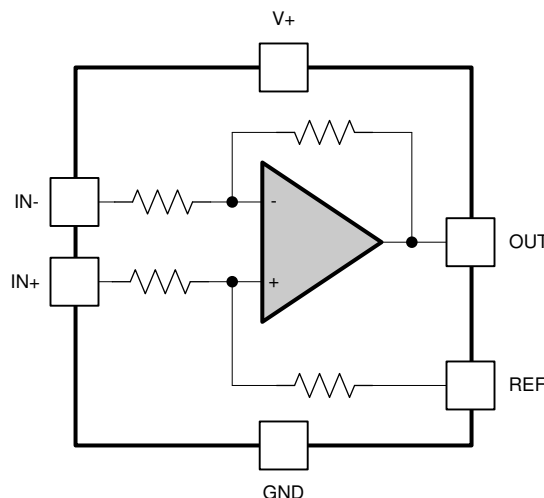
To minimize errors over temperature, select a low-drift shunt resistor. To minimize offset error, select a shunt resistor with the lowest tolerance. For this design, the Y14870R01000B9W resistor is used.

### 10.2.1.2.2 Differential Amplifier

The differential amplifier used for this design should have the following features:

1. Single-supply (3 V),
2. Reference voltage input,
3. Low initial input offset voltage ( $V_{OS}$ ),
4. Low-drift,
5. Fixed gain, and
6. Low-side sensing (input common-mode range below ground).

For this design, a current-shunt monitor (INA213) is used. The INA21x family topology is shown in [图 10-3](#). The INA213B specifications can be found in the [INA213 product data sheet](#).



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**图 10-3. INA21x Current-Shunt Monitor Topology**

The INA213B is an excellent choice for this application because all the required features are included. In general, instrumentation amplifiers (INAs) do not have the input common-mode swing to ground that is essential for this application. In addition, INAs require external resistors to set their gain, which is not desirable for low-drift applications. Difference amplifiers typically have larger input bias currents, which reduce solution accuracy at

small load currents. Difference amplifiers typically have a gain of 1 V/V. When the gain is adjustable, these amplifiers use external resistors that are not conducive to low-drift applications.

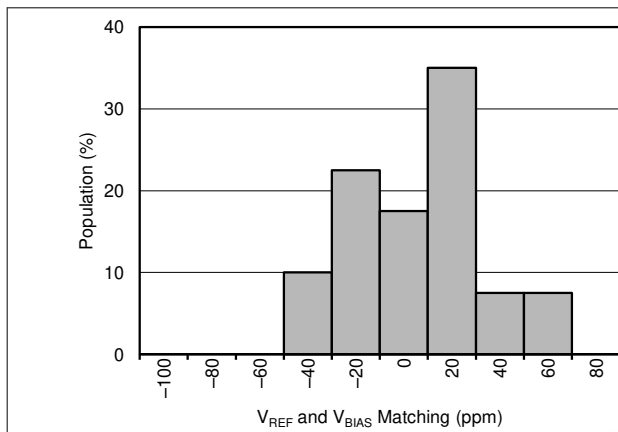
### 10.2.1.2.3 Voltage Reference

The voltage reference for this application should have the following features:

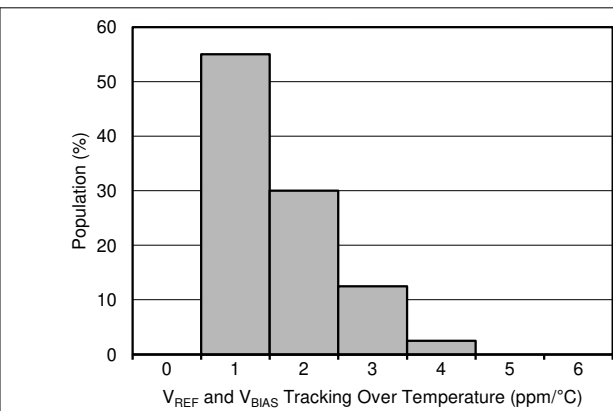
1. Dual output (3.0 V and 1.5 V),
2. Low drift, and
3. Low tracking errors between the two outputs.

For this design, the REF2030 is used. The REF20xx topology is as shown in the [§ 9.2](#) section.

The REF2030 is an excellent choice for this application because of its dual output. The temperature drift of 8 ppm/°C and initial accuracy of 0.05% make the errors resulting from the voltage reference minimal in this application. In addition, there is minimal mismatch between the two outputs and both outputs track very well across temperature, as shown in [图 10-4](#) and [图 10-5](#).



**图 10-4. V<sub>REF</sub> - 2 × V<sub>BIAS</sub> Distribution (At T<sub>A</sub> = 25°C)**



**图 10-5. Distribution of V<sub>REF</sub> - 2 × V<sub>BIAS</sub> Drift Tracking Over Temperature**

### 10.2.1.2.4 Results

[表 10-1](#) summarizes the measured results.

**表 10-1. Measured Results**

ERROR	UNCALIBRATED (%)	CALIBRATED (%)
Error across the full load current range (25°C)	±0.0355	±0.004
Error across the full load current range (-40°C to 125°C)	±0.0522	±0.0606

### 10.2.1.3 Application Curves

Performing a two-point calibration at 25°C removes the errors associated with offset voltage, gain error, and so forth. 图 10-6 to 图 10-8 show the measured error at different conditions. For a more detailed description on measurement procedure, calibration, and calculations, please refer to TIDU357.

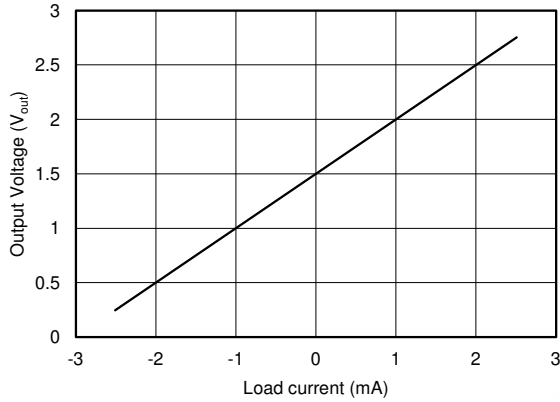


图 10-6. Measured Transfer Function

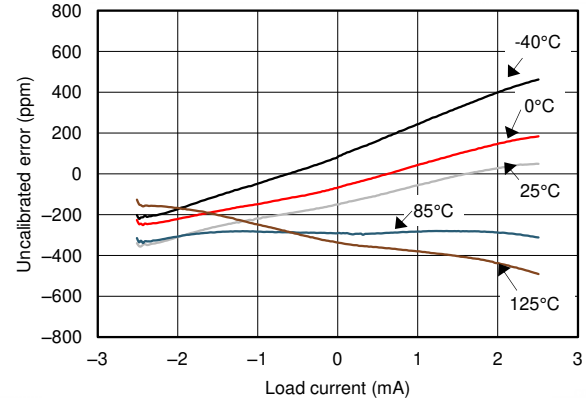


图 10-7. Uncalibrated Error vs Load Current

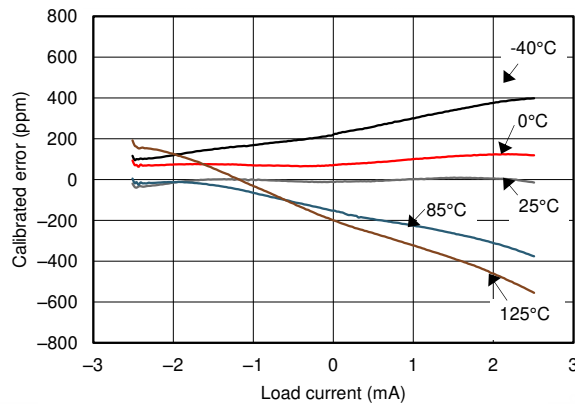
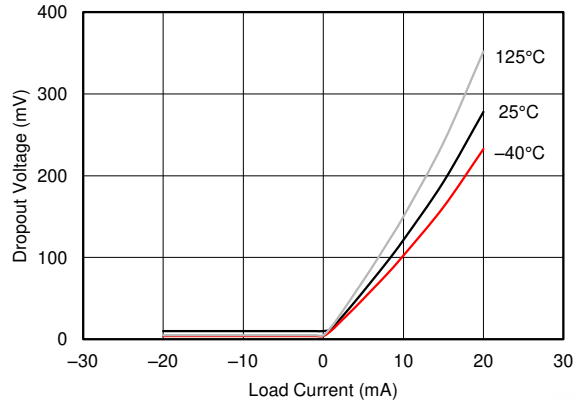


图 10-8. Calibrated Error vs Load Current



## 11 Power-Supply Recommendations

The REF20xx family of references feature an extremely low-dropout voltage. These references can be operated with a supply of only 20 mV above the output voltage. For loaded reference conditions, a typical dropout voltage versus load is shown in [Figure 11-1](#). A supply bypass capacitor ranging between 0.1  $\mu\text{F}$  to 10  $\mu\text{F}$  is recommended.



**图 11-1. Dropout Voltage vs Load Current**

## 12 Layout

### 12.1 Layout Guidelines

图 12-1 shows an example of a PCB layout for a data acquisition system using the REF2030. Some key considerations are:

- Connect low-ESR, 0.1- $\mu$ F ceramic bypass capacitors at  $V_{IN}$ ,  $V_{REF}$ , and  $V_{BIAS}$  of the REF2030.
- Decouple other active devices in the system per the device specifications.
- Using a solid ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup.
- Place the external components as close to the device as possible. This configuration prevents parasitic errors (such as the Seebeck effect) from occurring.
- Minimize trace length between the reference and bias connections to the INA and ADC to reduce noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

### 12.2 Layout Example

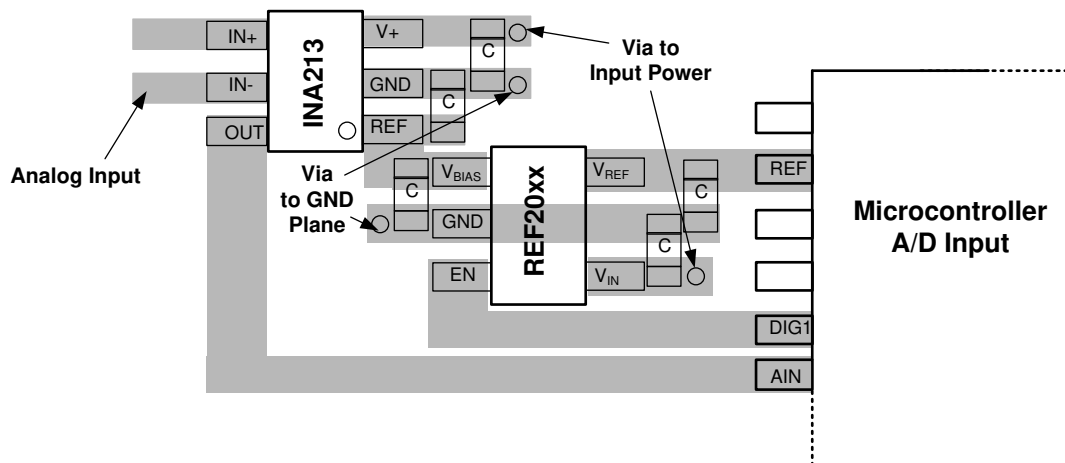


图 12-1. Layout Example

## 13 Device and Documentation Support

### 13.1 Documentation Support

#### 13.1.1 Related Documentation

For related documentation see the following:

- [INA21x Voltage Output, Low- or High-Side Measurement, Bidirectional, Zero-Drift Series, Current-Shunt Monitors](#) (SBOS437)
- [Low-Drift Bidirectional Single-Supply Low-Side Current Sensing Reference Design](#) (TIDU357)

#### 13.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

#### 13.3 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

#### 13.4 Trademarks

e-Trim™ is a trademark of Texas Instruments, Inc.

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

#### 13.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

#### 13.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF2025AIDDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GACM	<a href="#">Samples</a>
REF2025AIDDCT	ACTIVE	SOT-23-THIN	DDC	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GACM	<a href="#">Samples</a>
REF2025AISDDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	Call TI	Level-2-260C-1 YEAR	-40 to 125	1M98	<a href="#">Samples</a>
REF2030AIDDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GADM	<a href="#">Samples</a>
REF2030AIDDCT	ACTIVE	SOT-23-THIN	DDC	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GADM	<a href="#">Samples</a>
REF2033AIDDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAEM	<a href="#">Samples</a>
REF2033AIDDCT	ACTIVE	SOT-23-THIN	DDC	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAEM	<a href="#">Samples</a>
REF2041AIDDCR	ACTIVE	SOT-23-THIN	DDC	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAFM	<a href="#">Samples</a>
REF2041AIDDCT	ACTIVE	SOT-23-THIN	DDC	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	GAFM	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



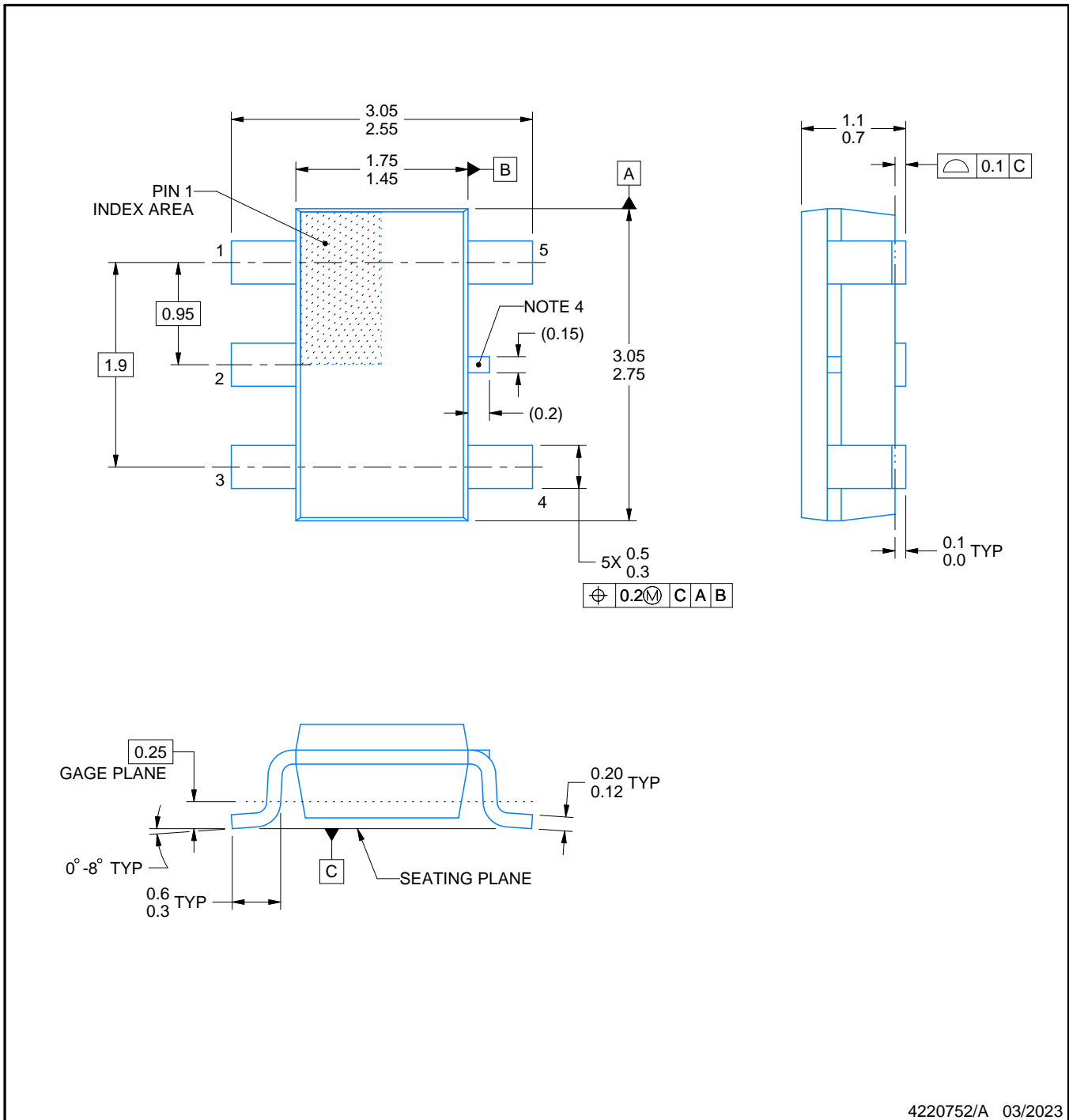
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
REF2025AIDDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2025AIDDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2025AISDDCR	SOT-23-THIN	DDC	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2030AIDDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2030AIDDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2033AIDDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2033AIDDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2041AIDDCR	SOT-23-THIN	DDC	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
REF2041AIDDCT	SOT-23-THIN	DDC	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
REF2025AIDDCR	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
REF2025AIDDCT	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0
REF2025AISDDCR	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
REF2030AIDDCR	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
REF2030AIDDCT	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0
REF2033AIDDCR	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
REF2033AIDDCT	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0
REF2041AIDDCR	SOT-23-THIN	DDC	5	3000	213.0	191.0	35.0
REF2041AIDDCT	SOT-23-THIN	DDC	5	250	213.0	191.0	35.0



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.
4. Support pin may differ or may not be present.

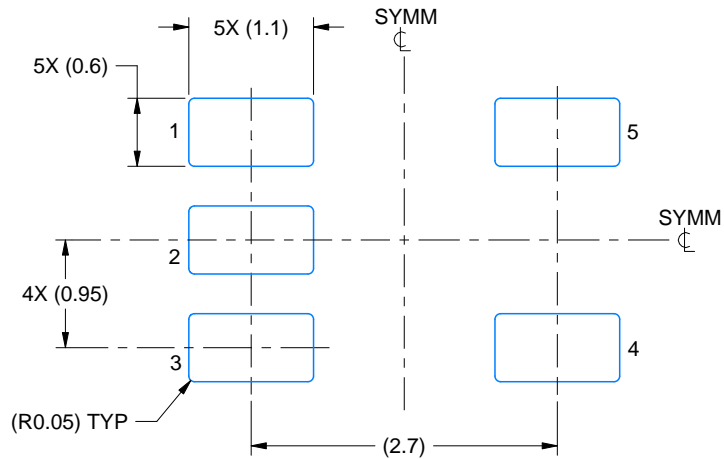


# EXAMPLE BOARD LAYOUT

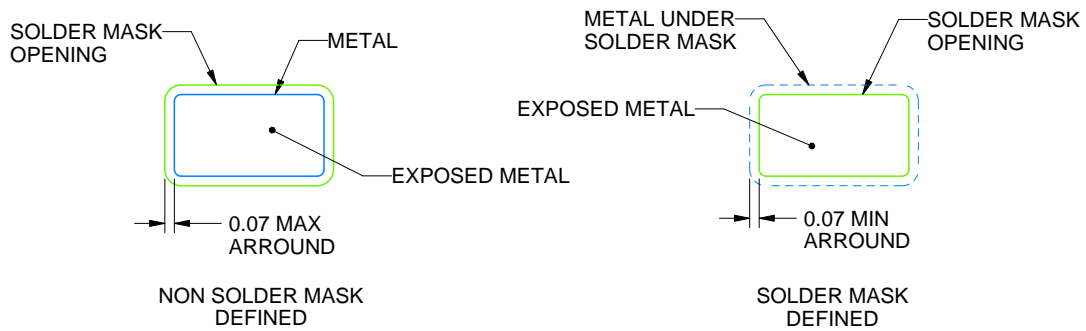
DDC0005A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPLODED METAL SHOWN  
SCALE:15X



SOLDERMASK DETAILS

4220752/A 03/2023

NOTES: (continued)

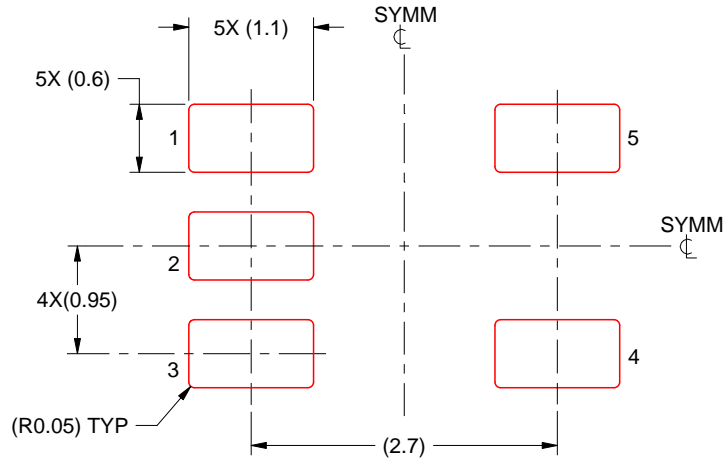
- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DDC0005A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:15X

4220752/A 03/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

## 重要声明和免责声明

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