HIGH-SPEED RAIL-TO-RAIL OUTPUT VIDEO AMPLIFIERS

FEATURES

- **High Speed**
  - **100 MHz Bandwidth (–3 dB, G = 2)**
  - **900 V/s Slew Rate**
- **Excellent Video Performance**
  - **50 MHz Bandwidth (0.1 dB, G = 2)**
  - **0.007% Differential Gain**
  - **0.007 Differential Phase**
- **Rail-to-Rail Output Swing**
  - **V_O = –4.5 / 4.5 (R_L= 150 Ω)**
- **High Output Drive, I_O = 100 mA (typ)**
- **Ultralow Distortion**
  - **HD2 = –78 dBc (f = 5 MHz, R_L = 150 Ω)**
  - **HD3 = –85 dBc (f = 5 MHz, R_L = 150 Ω)**
- **Wide Range of Power Supplies**
  - **V_S = 3 V to 15 V**

APPLICATIONS

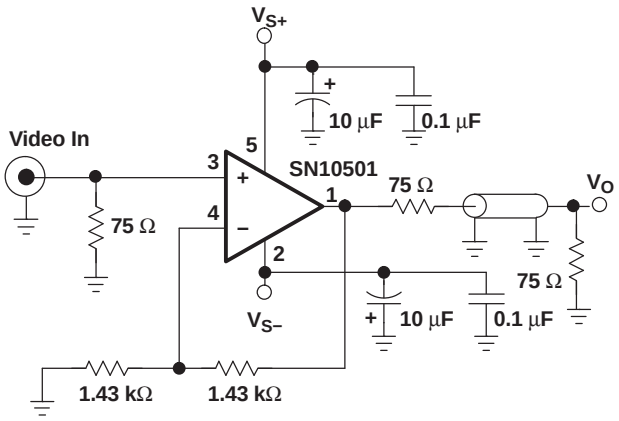
- **Video Line Driver**
- **Imaging**
- **DVD / CD ROM**
- **Active Filtering**
- **General Purpose Signal Chain Conditioning**

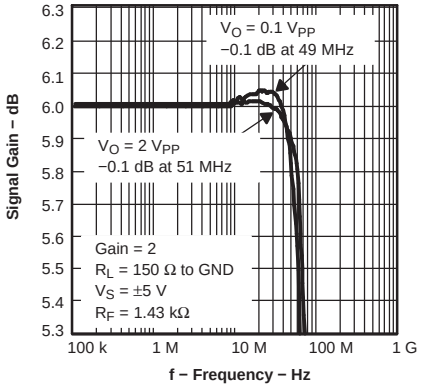
DESCRIPTION

The SN1050x family is a set of rail-to-rail output single, dual, and triple low-voltage, high-output swing, low-distortion high-speed amplifiers ideal for driving data converters, video switching, or low distortion applications. This family of voltage-feedback amplifiers can operate from a single 15-V power supply down to a single 3-V power supply while consuming only 14 mA of quiescent current per channel. In addition, the family offers excellent ac performance with 100-MHz bandwidth, 900-V/µs slew rate and harmonic distortion (THD) at –78 dBc at 5 MHz.

DEVICE	DESCRIPTION
SN10501	Single
SN10502	Dual
SN10503	Triple

VIDEO DRIVE CIRCUIT





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

owerPAD is a trademark of Texas Instruments.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

operating free-air temperature range unless otherwise (1)

	UNIT
Supply voltage, V_S	16.5 V
Input voltage, V_I	$\pm V_S$
Output current, I_O	150 mA
Differential input voltage, V_{ID}	4 V
Continuous power dissipation See Dissipation Rating Table	
Maximum junction temperature, T_J	150°C
Maximum junction temperature, continuous operation, longterm reliability, T_J (2)	125°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	300°C

(1) The absolute maximum ratings under any condition is limited by the constraints of the silicon process. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

PACKAGE DISSIPATION RATINGS

PACKAGE	θ_{JC}(°C/W) (1)	θ_{JA}(°C/W)	POWER RATING (2)	
			$T_A \le 25°C$	$T_A = 85°C$
DBV (5)	55	255.4	391 mW	156 mW
D (8)	38.3	97.5	1.02 W	410 mW
D (14)	26.9	66.6	1.5 W	600 mW
DGK (8)	54.2	260	385 mW	154 mW
DGN (8) (3)	4.7	58.4	1.71 W	685 mW
PWP (14) (3)	2.07	37.5	2.67 W	1.07 W

(1) This data was taken using the JEDEC standard High-K test PCB.
(2) Power rating is determined with a junction temperature of 125°C. This is the point where distortion starts to substantially increase. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and long term reliability.
(3) The SN10501, SN10502, and SN10503 may incorporate a PowerPAD™ on the underside of the chip. This acts as a heatsink and must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in exceeding the maximum junction temperature which could permanently damage the device. See TI Technical Brief SLMA002 for more information about utilizing the PowerPAD™ thermally enhanced package.

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Supply voltage,(V_{S+} and V_{S-})	Dual supply	1.35	8	V
	Single supply	2.7	16	
Input common-mode voltage range		V_{S-} + 1.1	V_{S+} - 1.1	V

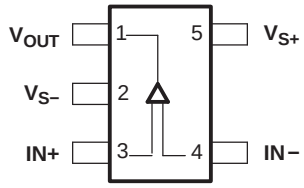
PACKAGE ORDERING INFORMATION

PACKAGED DEVICES			PACKAGE TYPE	TRANSPORT MEDIA, QUANTITY
SINGLE	DUAL	TRIPLE		
SN10501DBVT	—	—	SOT-23-5	Tape and Reel, 250
SN10501DBVR	—	—	SOT-23-5	Tape and Reel, 3000
SN10501DGK	SN10502DGK	—	MSOP-8	Rails, 75
SN10501DGKR	SN10502DGKR	—	MSOP-8	Tape and Reel, 2500
SN10501DGN	SN10502DGN	—	MSOP-8-PP	Rails, 75
SN10501DGNR	SN10502DGNR	—	MSOP-8-PP	Tape and Reel, 2500
SN10501D	SN10502D	SN10503D	SOIC	Rails, 75
SN10501DR	SN10502DR	SN10503DR	SOIC	Tape and Reel, 2500
—	—	SN10503PWP	TSSOP-14-PP	Rails, 75
—	—	SN10503PWPR	TSSOP-14-PP	Tape and Reel, 2000

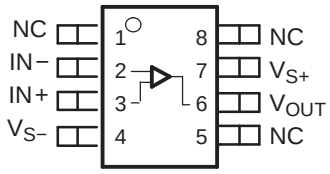
PIN ASSIGNMENTS

PACKAGE DEVICES

SN10501
DBV PACKAGE
(TOP VIEW)

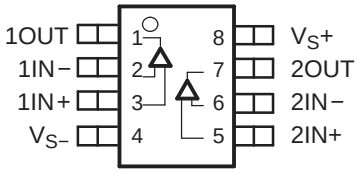


SN10501
D, DGK, DGN PACKAGE
(TOP VIEW)

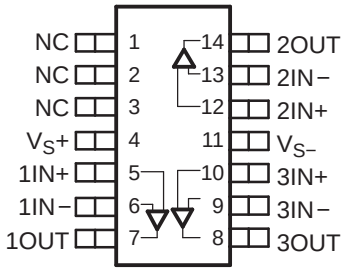


NC – No internal connection

SN10502
D, DGK, DGN PACKAGE
(TOP VIEW)



SN10503
D, PWP PACKAGE
(TOP VIEW)



NC – No internal connection

ELECTRICAL CHARACTERISTICS

V_S = 5 V, R_L = 150 Ω, and G = 2 unless otherwise noted

PARAMETER	TEST CONDITIONS	TYP	OVER TEMPERATURE				
		25°C	25°C	0°C to 70°C	–40°C to 85°C	UNITS	MIN/MAX
AC PERFORMANCE							
Small signal bandwidth	G = 1, V_O = 100 mV_{PP}	170				MHz	Typ
	G = 2, V_O = 100 mV_{PP}, R_f = 1 kΩ	100				MHz	Typ
	G = 10, V_O = 100 mV_{PP}, R_f = 1 kΩ	12				MHz	Typ
0.1 dB flat bandwidth	G = 2, V_O = 100 mV_{PP}, R_f = 1.43 kΩ	50				MHz	Typ
Gain bandwidth product	G > 10, f = 1 MHz, R_f = 1 kΩ	120				MHz	Typ
Full-power bandwidth(1)	G = 2, V_O = ±2.5 V_{PP}	57				MHz	Typ
Slew rate	G = 2, V_O = ±2.5 V_{PP}	900				V/µs	Min
Settling time to 0.1%	G = -2, V_O = ±2 V_{PP}	25				ns	Typ
Settling time to 0.01%		52				ns	Typ
Harmonic distortion							
Second harmonic distortion	G = 2, V_O = 2 V_{PP}, f = 5 MHz, R_L = 150 Ω	–78				dBc	Typ
Third harmonic distortion		–85				dBc	Typ
Differential gain (NTSC, PAL)	G = 2, R = 150 Ω	0.007				%	Typ
Differential phase (NTSC, PAL)		0.007				°	Typ
Input voltage noise	f = 1 MHz	13				nV/√Hz	Typ
Input current noise		0.8				pA/√Hz	Typ
Crosstalk (dual and triple only)	f = 5 MHz Ch-to-Ch	–90				dB	Typ
DC PERFORMANCE							
Open-loop voltage gain (A_{OL})	V_O = ±2 V	100	80	75	75	dB	Min
Input offset voltage	V_{CM} = 0 V	12	25	30	30	mV	Max
Input bias current		0.9	3	5	5	µA	Max
Input offset current		100	500	700	700	nA	Max
INPUT CHARACTERISTICS							
Common-mode input range		–4 / 4	–3.9 / 3.9			V	Min
Common-mode rejection ratio	V_{CM} = 2 V	94	70	65	65	dB	Min
Input resistance		33				MΩ	Typ
Input capacitance	Common-mode / differential	1 / 0.5				pF	Max
OUTPUT CHARACTERISTICS							
Output voltage swing	R_L = 150 Ω	–4.5 / 4.5				V	Typ
	R_L = 499 Ω	–4.7 / 4.7	–4.5 / 4.5	–4.4 / 4.4	-4.4 / 4.4	V	Min
Output current (sourcing)	R_L = 10 Ω	100	92	88	88	mA	Min
Output current (sinking)		-100	-92	-88	-88	mA	Min
Output impedance	f = 1 MHz	0.09				Ω	Typ
POWER SUPPLY							
Specified operating voltage		±5	±8	±8	±8	V	Max
Maximum quiescent current	Per channel	14	18	20	22	mA	Max
Power supply rejection (±PSRR)		75	62	60	60	dB	Min

(1) Full-power bandwidth = SR / 2πVpp

ELECTRICAL CHARACTERISTICS

V_S = 5 V, R_L = 150 Ω, and G = 2 unless otherwise noted

PARAMETER	TEST CONDITIONS	TYP	OVER TEMPERATURE				
		25°C	25°C	0°C to 70C	-40°C to 85C	UNITS	MIN/MAX
AC PERFORMANCE							
Small signal bandwidth	G = 1, V_O = 100 mV_{PP}	170				MHz	Typ
	G = 2, V_O = 100 mV_{PP}, R_f = 1.5 kΩ	100				MHz	Typ
	G = 10, V_O = 100 mV_{PP}, R_f = 1.5 kΩ	12				MHz	Typ
0.1 dB flat bandwidth	G = 2, V_O = 100 mV_{PP}, R_f = 1.24 kΩ	50				MHz	Typ
Gain bandwidth product	G > 10, f = 1 MHz, R_f = 1.5 kΩ	120				MHz	Typ
Full-power bandwidth(1)	G = 2, V_O = 4 V step	60				MHz	Typ
Slew rate		750				V/µs	Min
Settling time to 0.1%	G = -2, V_O = 2 V	27				ns	Typ
Settling time to 0.01%		48				ns	Typ
Harmonic distortion							
Second harmonic distortion	G = 2, V_O = 2 V_{PP}, f = 5 MHz, R_L = 150 Ω	–82				dBc	Typ
Third harmonic distortion		–88				dBc	Typ
Differential gain (NTSC, PAL)	G = 2, R = 150 Ω	0.014				%	Typ
Differential phase (NTSC, PAL)		0.011				°	Typ
Input voltage noise	f = 1 MHz	13				nV/√Hz	Typ
Input current noise		0.8				pA/√Hz	Typ
Crosstalk (dual and triple only)	f = 5 MHz Ch-to-Ch	–90				dB	Typ
DC PERFORMANCE							
Open-loop voltage gain (A_{OL})	V_O = 1.5 V to 3.5 V	100	80	75	75	dB	Min
Input offset voltage	V_{CM} = 2.5 V	12	25	30	30	mV	Max
Input bias current		0.9	3	5	5	µA	Max
Input offset current		100	500	700	700	nA	Max
INPUT CHARACTERISTICS							
Common-mode input range		1 / 4	1.1 / 3.9			V	Min
Common-mode rejection ratio	V_{CM} = 1.5 V to 3.5 V	96	70	65	65	dB	Min
Input resistance		33				MΩ	Typ
Input capacitance	Common-mode / differential	1 / 0.5				pF	Max
OUTPUT CHARACTERISTICS							
Output voltage swing	R_L = 150 Ω	0.5 / 4.5				V	Typ
	R_L = 499 Ω	0.2 / 4.8	0.3 / 4.7	0.4 / 4.6	0.4 / 4.6	V	Min
Output current (sourcing)	R_L = 10 Ω	95	85	80	80	mA	Min
Output current (sinking)		–95	-85	–80	–80	mA	Min
Output impedance	f = 1 MHz	0.09				Ω	Typ
POWER SUPPLY							
Specified operating voltage		5	16	16	16	V	Max
Maximum quiescent current	Per channel	12	15	17	19	mA	Max
Power supply rejection (±PSRR)		70	62	60	60	dB	Min

(1) Full-power bandwidth = SR / 2πVpp

TYPICAL CHARACTERISTICS

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Rejection ratio	vs Case temperature	25
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Output impedance	vs Frequency	28, 29
Crosstalk	vs Frequency	30
Input bias and offset current	vs Case temperature	31, 32

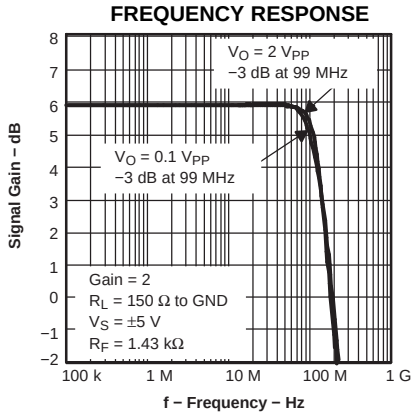


Figure 1.

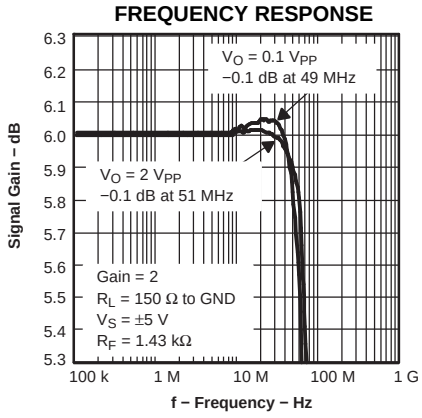


Figure 2.

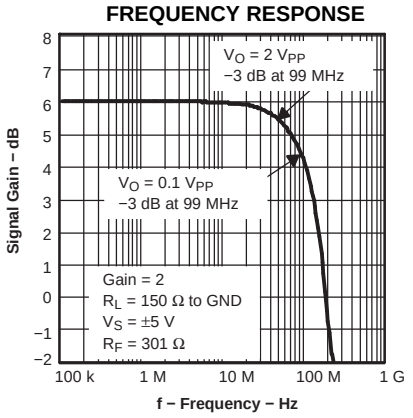


Figure 3.

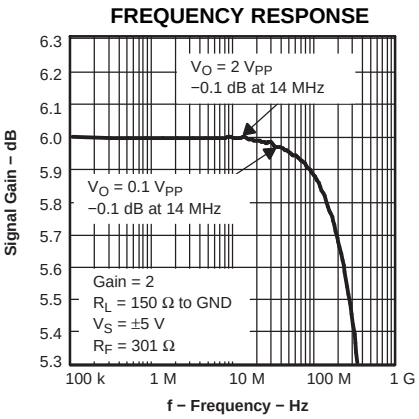


Figure 4.

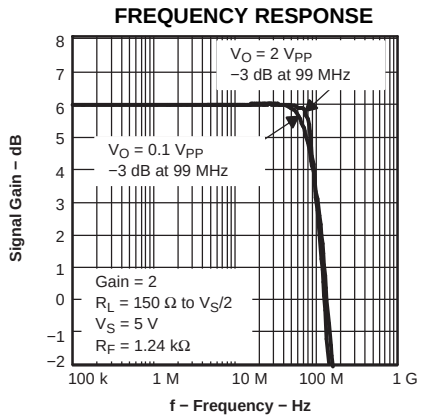


Figure 5.

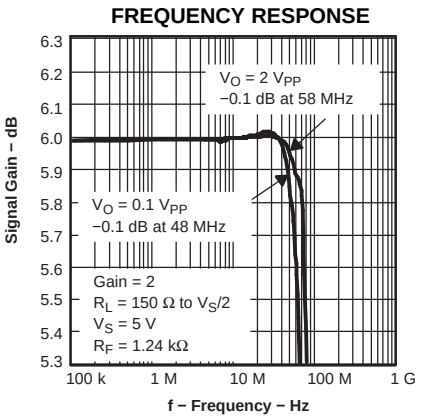
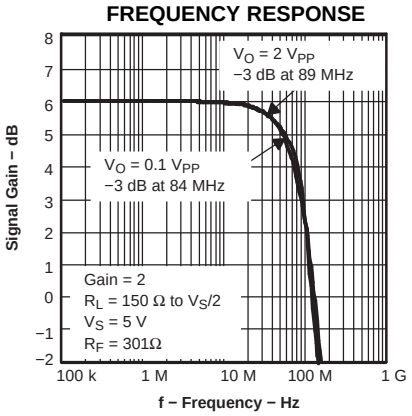


Figure 6.



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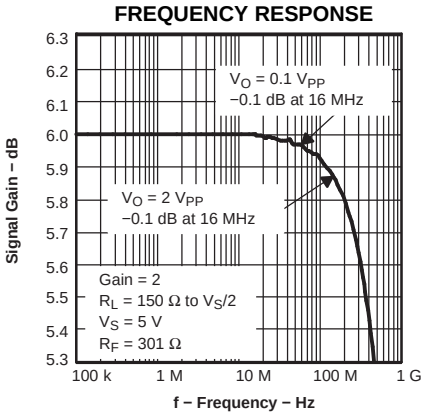


Figure 8.

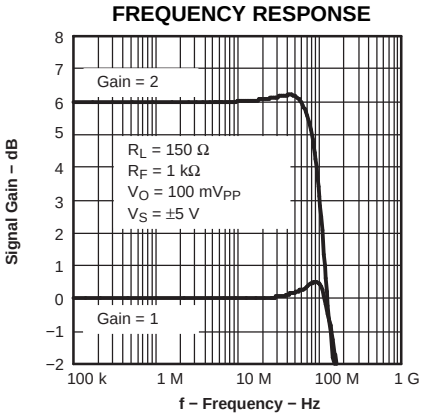


Figure 9.

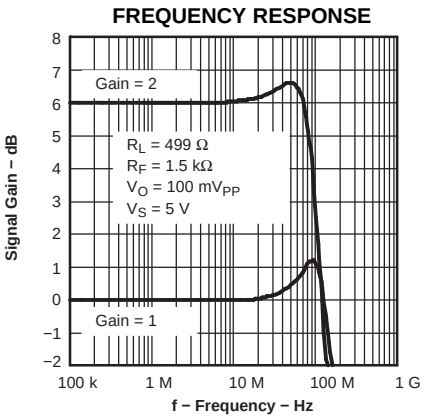


Figure 10.

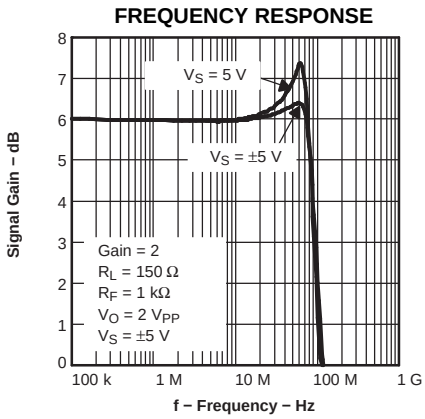


Figure 11.

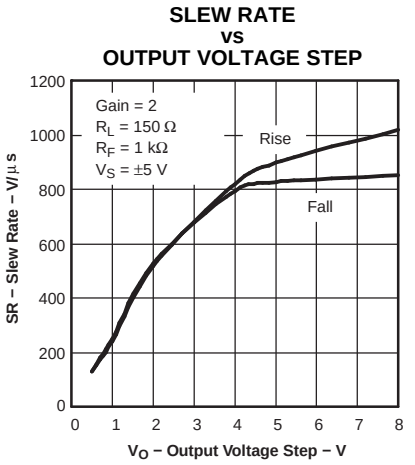


Figure 12.

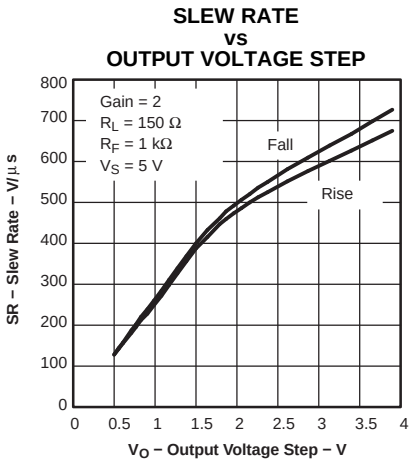


Figure 13.

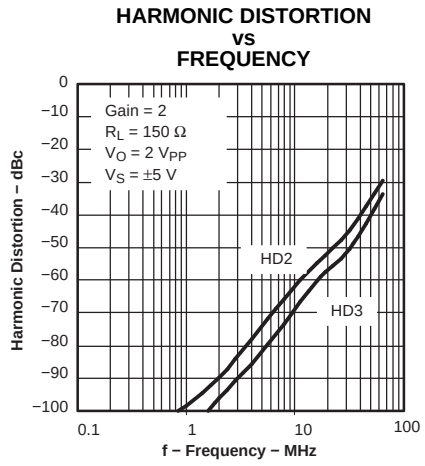


Figure 14.

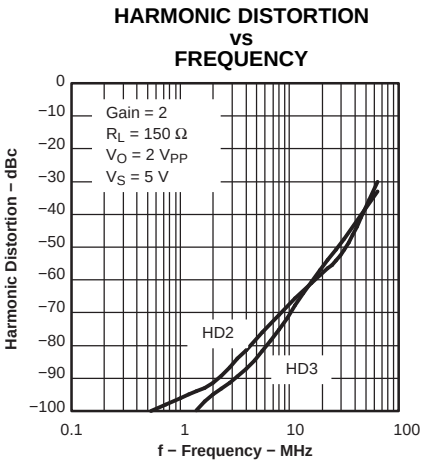


Figure 15.

VOLTAGE AND CURRENT NOISE VS FREQUENCY

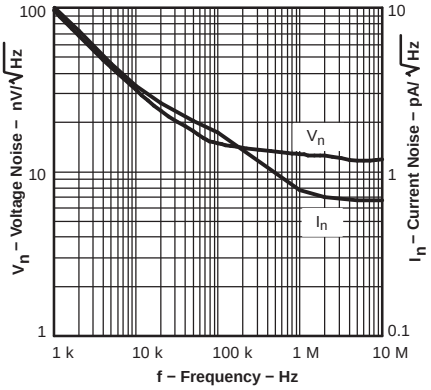


Figure 16.

DIFFERENTIAL GAIN VS NUMBER OF LOADS

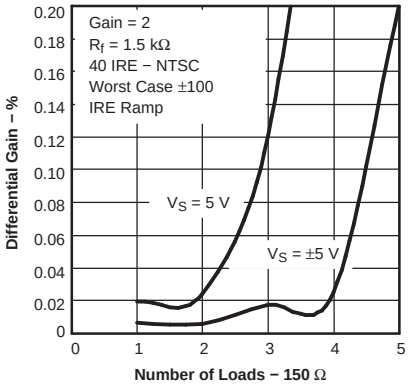


Figure 17.

DIFFERENTIAL PHASE VS NUMBER OF LOADS

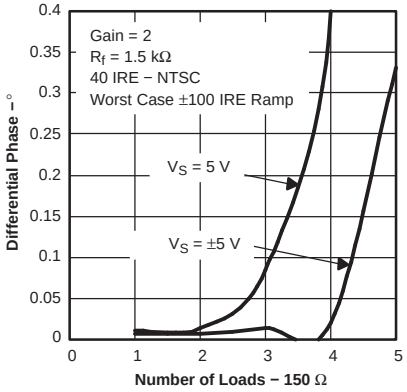


Figure 18.

DIFFERENTIAL GAIN VS NUMBER OF LOADS

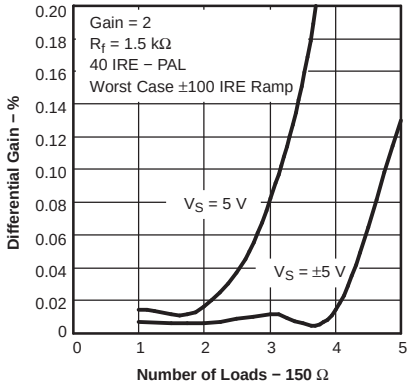


Figure 19.

DIFFERENTIAL PHASE VS NUMBER OF LOADS

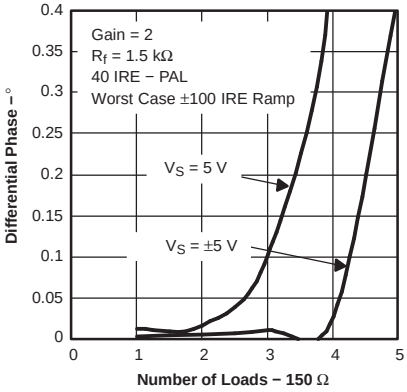


Figure 20.

QUIESCENT CURRENT VS SUPPLY VOLTAGE

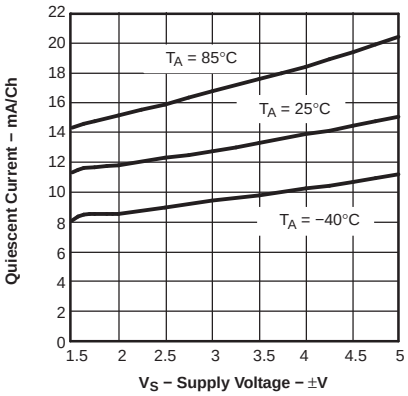


Figure 21.

OUTPUT VOLTAGE VS LOAD RESISTANCE

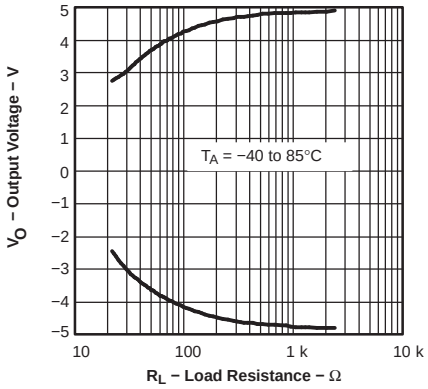


Figure 22.

OPEN-LOOP GAIN AND PHASE VS FREQUENCY

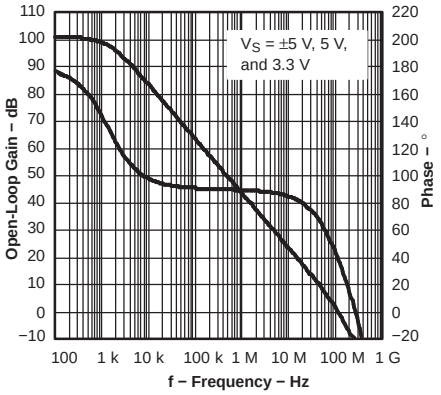


Figure 23.

REJECTION RADIO VS FREQUENCY

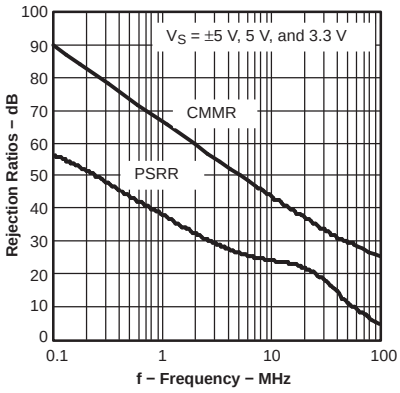


Figure 24.

REJECTION RATIO vs CASE TEMPERATURE

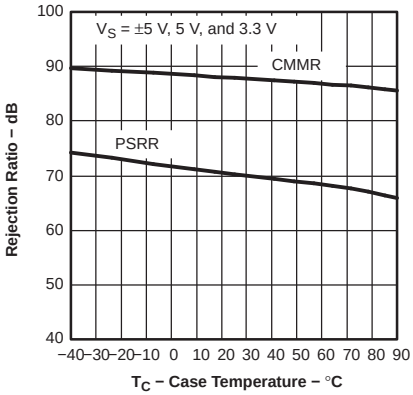


Figure 25.

COMMON-MODE REJECTION RATIO vs INPUT COMMON-MODE RANGE

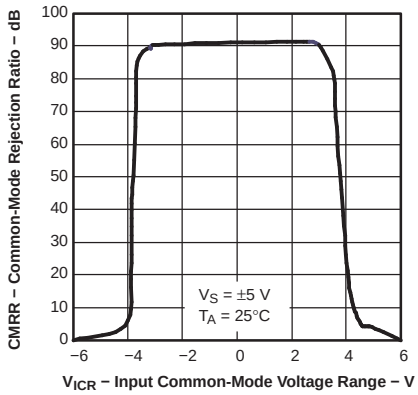


Figure 26.

COMMON-MODE REJECTION RATIO vs INPUT COMMON-MODE RANGE

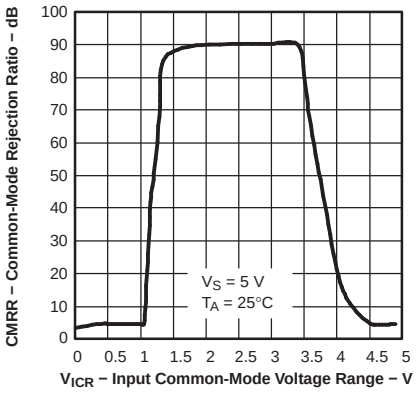


Figure 27.

OUTPUT IMPEDANCE vs FREQUENCY

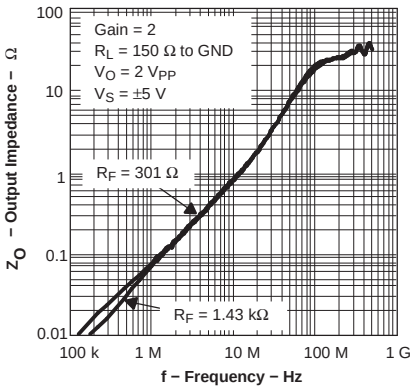


Figure 28.

OUTPUT IMPEDANCE vs FREQUENCY

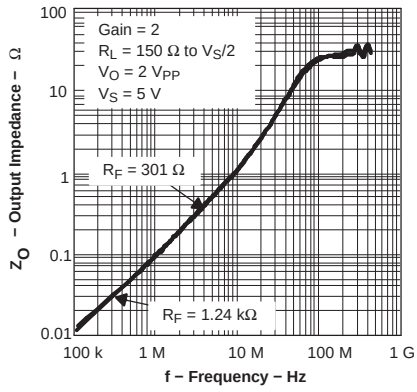


Figure 29.

CROSSTALK vs FREQUENCY

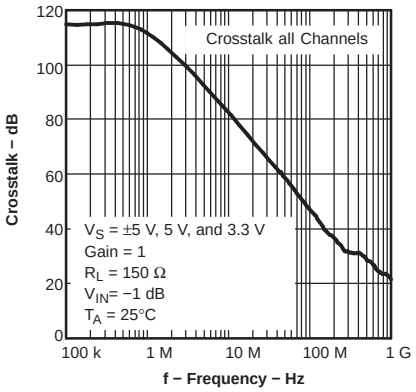


Figure 30.

INPUT BIAS AND OFFSET CURRENT vs CASE TEMPERATURE

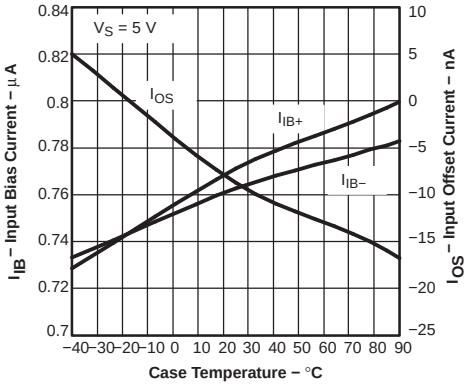


Figure 31.

INPUT BIAS AND OFFSET CURRENT vs CASE TEMPERATURE

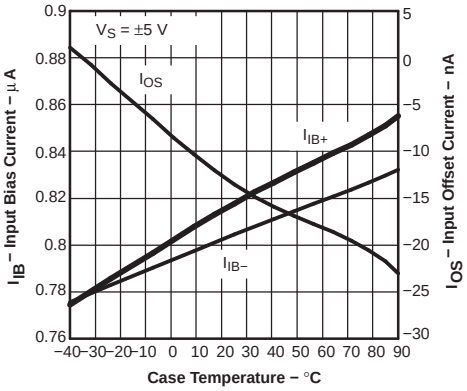


Figure 32.

APPLICATION INFORMATION

HIGH-SPEED OPERATIONAL AMPLIFIERS

The SN1050x operational amplifiers are a family of single, dual, and triple rail-to-rail output voltage feedback amplifiers. The SN1050x family combines both a high slew rate and a rail-to-rail output stage.

Applications Section Contents

- Wideband, Noninverting Operation
- Wideband, Inverting Gain Operation
- Video Drive Circuits
- Single Supply Operation
- Power Supply Decoupling Techniques and Recommendations
- Active Filtering With the SN1050x
- Driving Capacitive Loads
- Board Layout
- Thermal Analysis
- Additional Reference Material
- Mechanical Package Drawings

WIDEBAND, NONINVERTING OPERATION

The SN1050x is a family of unity gain stable rail-to-rail output voltage feedback operational amplifiers designed to operate from a single 3-V to 15-V power supply.

Figure 33 is the noninverting gain configuration of 2V/V used to demonstrate the typical performance curves.

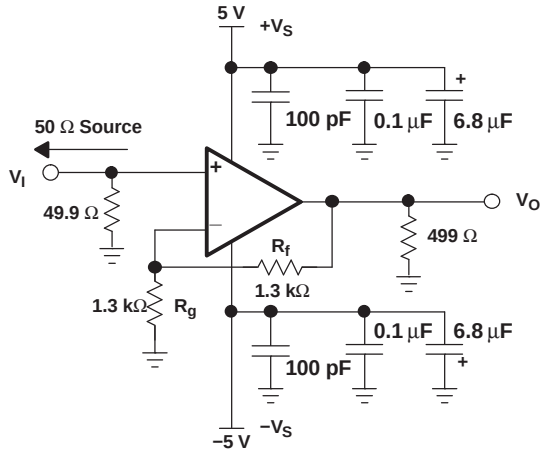


Figure 33. Wideband, Noninverting Gain Configuration

Voltage-feedback amplifiers, unlike current-feedback designs, can use a wide range of resistors values to set their gain with minimal impact on their stability and frequency response. Larger-valued resistors decrease the loading effect of the feedback network on the output of the amplifier, but this enhancement comes at the expense of additional noise and potentially lower bandwidth. Feedback-resistor values between 1 kΩ and 2 kΩ are recommended for most situations.

WIDEBAND, INVERTING OPERATION

Since the SN1050x family are general-purpose, wideband voltage-feedback amplifiers, several familiar operational-amplifier applications circuits are available to the designer. Figure 34 shows a typical inverting configuration where the input and output impedances and noise gain from Figure 33 are retained in an inverting circuit configuration. Inverting operation is one of the more common requirements and offers several performance benefits. The inverting configuration shows improved slew rates and distortion due to the pseudo-static voltage maintained on the inverting input.

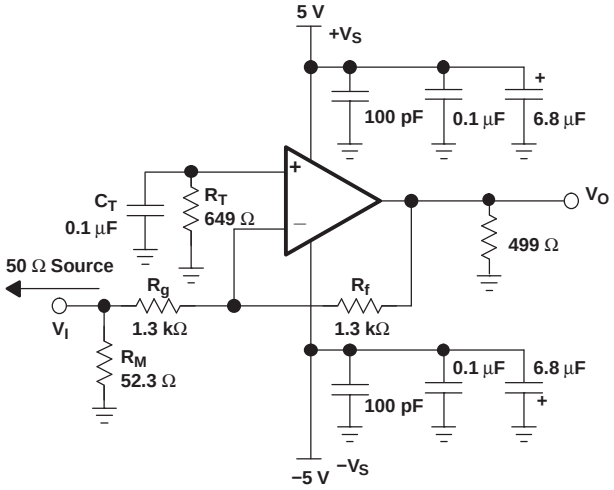


Figure 34. Wideband, Inverting Gain Configuration

In the inverting configuration, some key design considerations must be noted. One is that the gain resistor (R_g) becomes part of the signal channel input impedance. If input impedance matching is desired (beneficial when the signal is coupled through a cable, twisted pair, long PC-board trace, or other transmission-line conductors), R_g may be set equal to the required termination value and R_f adjusted to give the desired gain. However, care must be taken when dealing with low inverting gains, because the resulting feedback-resistor value can present a significant load to the amplifier output. For an inverting gain of 2, setting R_g to 49.9 Ω for input matching eliminates the need for R_M but requires a 100-Ω feedback resistor. This has the advantage that the noise gain becomes equal to 2 for a 50-Ω source impedance—the same

as the noninverting circuit in Figure 33. However, the amplifier output now sees the 100-Ω feedback resistor in parallel with the external load. To eliminate this excessive loading, increase both R_g and R_f, values, as shown in Figure 34, and then provide the input-matching impedance with a third resistor (R_M) to ground. The total input impedance becomes the parallel combination of R_g and R_M.

The last major consideration to discuss in inverting amplifier design is setting the bias-current cancellation resistor on the noninverting input. If the resistance is set equal to the total dc resistance looking out of the inverting terminal, the output dc error, due to the input bias currents, is reduced to the input-offset current multiplied by R_f in Figure 34. The dc source impedance looking out of the inverting terminal is 1.3 kΩ || (1.3 kΩ + 25.6 Ω) = 649 Ω. To reduce the additional high-frequency noise introduced by the resistor at the noninverting input, and power-supply feedback, R_T is bypassed with a capacitor to ground.

SINGLE SUPPLY OPERATION

The SN1050x family is designed to operate from a single 3-V to 15-V power supply. When operating from a single power supply, care must be taken to ensure that the input signal and amplifier are biased appropriately to allow for the maximum output voltage swing. The circuits shown in Figure 35 demonstrate methods to configure an amplifier for single-supply operation.

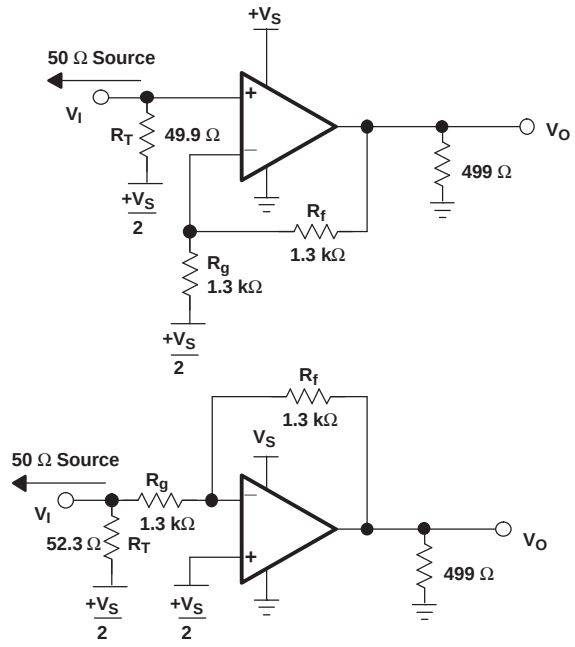


Figure 35. DC-Coupled Single Supply Operation

Video Drive Circuits

Most video-distribution systems are designed with 75-Ω series resistors to drive a matched 75-Ω cable. In order to deliver a net gain of 1 to the 75-Ω matched load, the amplifier is typically set up for a voltage gain of 2, compensating for the 6-dB attenuation of the voltage divider formed by the series and shunt 75-Ω resistors at either end of the cable. The circuit shown in Figure 36 meets this requirement. The SN1050x gain flatness and differential gain/phase performance provide exceptional results in video distribution applications.

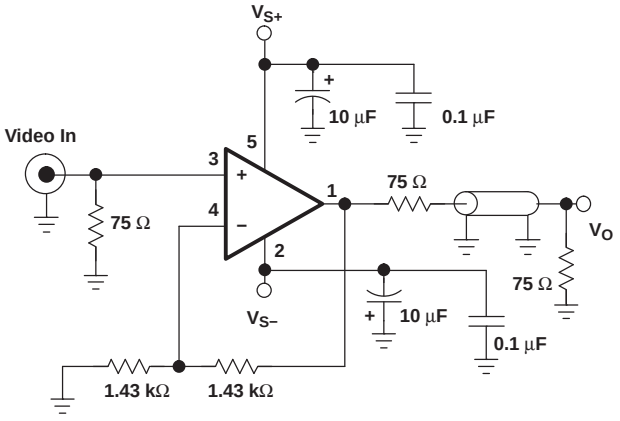


Figure 36. Cable Drive Application

Differential gain and phase measure the change in overall small-signal gain and phase for the color subcarrier frequency (3.58 MHz in NTSC systems) vs changes in the large-signal output level (which represents luminance information in a composite video signal). The SN1050x, with the typical 150-Ω load of a single matched video cable, shows less than 0.007% / 0.007° differential gain/phase errors over the standard luminance range for a positive video (negative sync) signal.

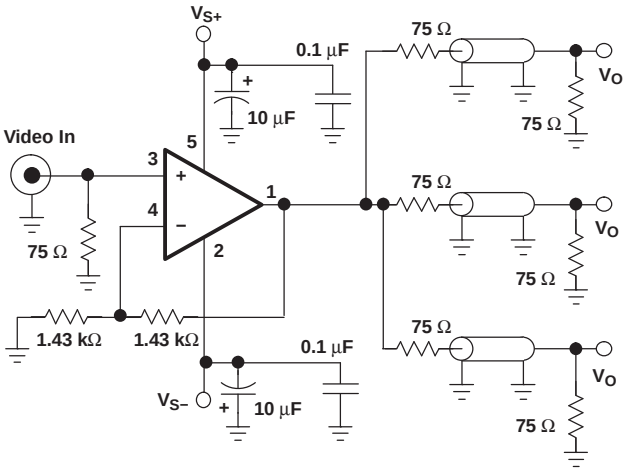


Figure 37. Video Distribution

Similar performance is observed for negative video signals. In practice, similar performance is achieved even with three video loads as shown in Figure 37 due to the linear high-frequency output impedance of the SN1050x. This circuit is suitable for driving video cables, provided that the length does not exceed a few feet. If longer cables are driven, the gain of the SN1050x can be increased to compensate for cable loss.

Configuring the SN1050x for single-supply video applications is easily done, but attention must be given to input and output bias voltages to ensure proper system operation. Unlike some video amplifiers, the SN1050x input common-mode voltage range does not include the negative power supply, but rather it is about 1-V from each power supply. For split supply configurations, this is very beneficial. For single-supply systems, there are some design constraints that must be observed.

Figure 38 shows a single-supply video configuration illustrating the dc bias voltages acceptable for the SN1050x. The lower end of the input common-mode range is specified as 1 V. The upper end is limited to 4 V with the 5-V supply shown, but the output range and gain of 2 limit the highest acceptable input voltage to 4.5 V / 2 = 2.25 V. The 4.5-V output is what is typically expected with a 150-Ω load. It is easily seen that the input and output voltage ranges are limiting factors in the total system. Both specifications must be taken into account when designing a system.

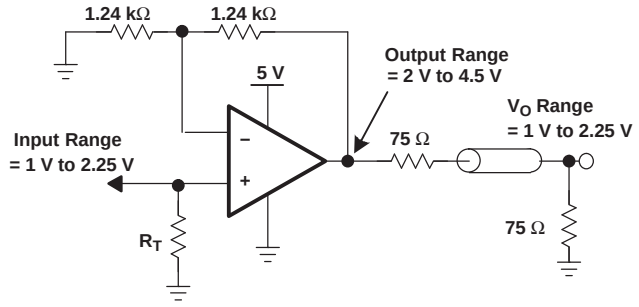


Figure 38. DC-Coupled Single-Supply Video Amplifier

In most systems, this may be acceptable because most receivers are ac-coupled and set the black level to the desired system value, typically 0 V (0-IRE). But, to ensure full compatibility with any system, it is often desirable to place an ac coupling capacitor on the output as shown in Figure 39. This removes the dc-bias voltage appearing at the amplifier output. To minimize field tilt, the size of this capacitor is typically 470 µF, although values as small as 220 µF have been used with acceptable results.

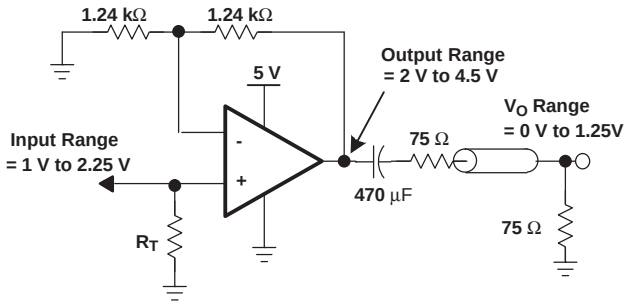


Figure 39. AC-Coupled Output Single-Supply Video Amplifier

In some systems, the physical size and/or cost of a 470-µF capacitor can be prohibitive. One way to circumvent this issue is to use two smaller capacitors in a feedback configuration as shown in Figure 40. This is commonly known as SAG correction. This circuit increases the gain of the amplifier up to 3 V/V at low frequencies to counteract the increased impedance of the capacitor placed at the amplifier output. One issue that must be resolved is that the gain at low frequencies is typically limited by the power-supply voltage and the output swing of the amplifier. Therefore, it is possible to saturate the amplifier at these low frequencies if full analysis is not done on this system which includes both input and output requirements.

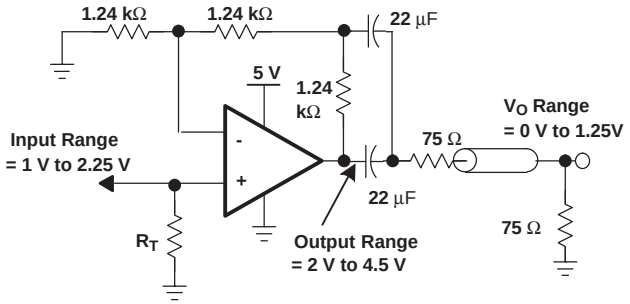


Figure 40. AC-Coupled SAG Corrected Output Single-Supply Video Amplifier

Many times the output of the video encoder or DAC does not have the capability to output the 1-V to 2.25-V range, but rather a 0-V to 1.25-V range. In this instance, the signal must be ac-coupled to the amplifier input as shown in Figure 41. Note that it does not matter what the voltage output of the DAC is, but rather the voltage swing should be kept less than 1.25 V_{PP}.

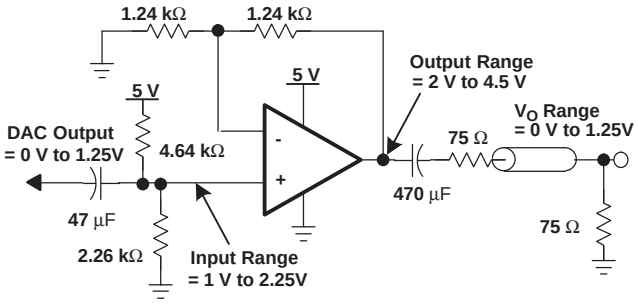


Figure 41. AC-Coupled Input and Output Single-Supply Video Amplifier

To further increase dynamic range at the output, the output dc bias should be centered around 2.5 V for the 5-V system shown. However, a wide output range requires a wide input range, and should be centered around 2.5 V. The best ways to accomplish this are to ac-couple the gain resistor or bias it at 2.5 V with a reference supply as shown in Figure 42 and Figure 43.

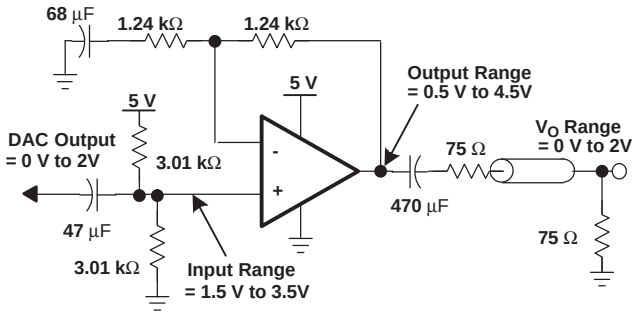


Figure 42. AC-Coupled Wide Output Swing Single-Supply Video Amplifier

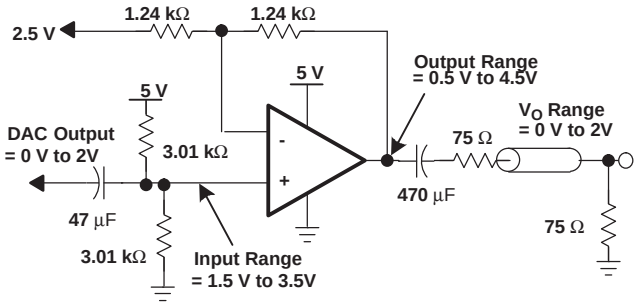


Figure 43. AC-Coupled Wide Output Swing Single-Supply Video Amplifier Using Voltage Reference

Another beneficial configuration is to use the amplifier in an inverting configuration as shown in Figure 44.

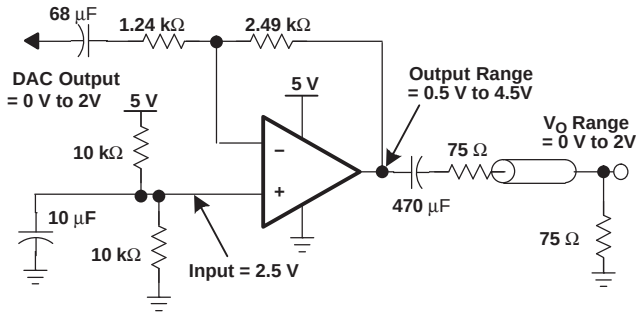


Figure 44. Inverting AC-Coupled Wide Output Swing Single-Supply Video Amplifier

APPLICATION CIRCUITS

Active Filtering With the SN1050x

High-frequency active filtering with the SN1050x is achievable due to the amplifier's high slew rate, wide bandwidth, and voltage feedback architecture. Several options are available for high-pass, low-pass, bandpass, and bandstop filters of varying orders. A simple two-pole, low-pass filter is presented in Figure 45 as an example, with two poles at 25 MHz.

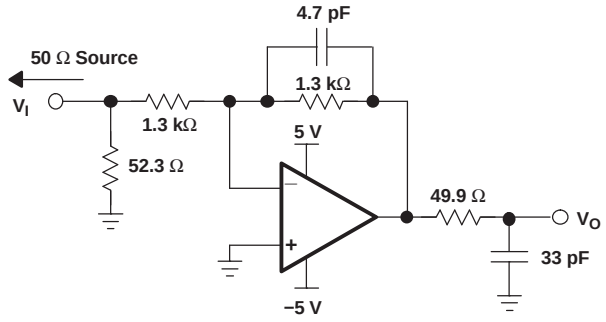


Figure 45. A Two-Pole Active Filter With Two Poles Between 90 MHz and 100 MHz

Driving Capacitive Loads

A demanding, yet very common application for an op amp is capacitive loading. Often, this load is the input of an A/D converter, including additional external capacitance, sometimes recommended to improve A/D linearity. A high-speed, high open-loop gain amplifier like the SN1050x can be very susceptible to decreased stability and closed-loop response peaking when a capacitive load is placed directly on the output pin. When the amplifier's open-loop output resistance is considered, the capacitance introduces an additional pole in the signal path that can decrease the phase margin. When the primary considerations are frequency-response flatness, pulse response fidelity, or distortion, the simplest and most effective solution is to isolate the capacitive load

from the feedback loop by inserting a series isolation resistor between the amplifier output and the capacitive load. This does not eliminate the pole from the loop response, but rather shifts it and adds a zero at a higher frequency. The additional zero cancels the phase lag from the capacitive-load pole, thus increasing the phase margin and improving stability.

Power Supply Decoupling Techniques and Recommendations

Power-supply decoupling is a critical aspect of any high-performance amplifier design process. Careful decoupling provides higher-quality ac performance, most notably improved distortion performance. The following guidelines ensure the highest level of performance.

1. Place decoupling capacitors as close to the power-supply inputs as possible, with the goal of minimizing the inductance of the path from ground to the power supply
2. Placement priority; locate the smallest-value capacitors nearest to the device.
3. Solid power and ground planes are recommended to reduce the inductance along power-supply return-current paths, with the exception of the areas underneath the input and output pins.
4. Recommended values for power supply decoupling include a bulk decoupling capacitor (6.8 to 22 μF), a mid-range decoupling capacitor (0.1 μF) and a high frequency decoupling capacitor (1000 pF) for each supply. A 100 pF capacitor can be used across the supplies as well for extremely high-frequency return currents, but often is not required.

BOARD LAYOUT

Achieving optimum performance with a high-frequency amplifier like the SN1050x requires careful attention to board layout parasitics and external component types.

Recommendations to optimize performance include:

1. **Minimize parasitic capacitance to any ac ground for all signal I/O pins.** Parasitic capacitance on the output and inverting-input pins can cause instability: on the noninverting input, it can react with the source impedance to cause unintentional band limiting. To reduce unwanted capacitance, open a window in all ground and power planes around the signal I/O pins. Keep ground and power planes unbroken elsewhere on the board.
2. **Minimize the distance (< 0.25”) from the power-supply pins to high frequency 0.1-μF decoupling capacitors.** At the device pins, the ground- and power-plane layout should not be in close proximity to the signal I/O pins. Avoid narrow power and ground traces to minimize inductance between the pins and the decoupling capacitors. The power supply connections should always be decoupled with these capacitors. Larger (2.2-μF to 6.8-μF) decoupling capacitors, effective at lower frequency, should also be used on the main supply pins. These may be placed somewhat farther from the device and may be shared among several devices in the same area of the PC board.
3. **Careful selection and placement of external components preserves the high frequency performance of the SN1050x.** Choose low-reactance resistors. Surface-mount resistors work best, and allow a tighter overall layout. Metal-film and carbon-composition axial-lead resistors can also provide good high-frequency performance. Again, keep component leads and PC-board trace length as short as possible. Never use wirewound resistors in a high frequency application. Since the output pin and inverting-input pin are the most sensitive to parasitic capacitance, always position the feedback and series-output resistor, if any, as close as possible to the output pin. Other network components, such as noninverting-input termination resistors, should also be placed close to the package. Where double-sided component mounting is allowed, place the feedback resistor directly under the package on the other side of the board between the output and inverting input pins. Even with a low parasitic capacitance shunting the external resistors, excessively high resistor values can create significant time constants that can degrade performance. Good axial-lead metal-film or surface-mount resistors have approximately 0.2 pF in shunt with the resistor. For resistor values > 2.0 kΩ, this parasitic capacitance can add a pole and/or a zero below 400 MHz that can affect circuit operation. Keep resistor values as low as possible, consistent with load-driving considerations. A good starting point for design is to set the R_f to 1.3 kΩ for low-gain, noninverting applications. This automatically keeps the resistor noise terms low, and minimizes the effect of their parasitic capacitance.
4. **Connections to other wideband devices on the board may be made with short, direct traces or through onboard transmission lines.** For short connections, consider the trace and the input to the next device as a lumped capacitive load. Use relatively wide traces (50 mils to 100 mils), preferably with ground and power planes opened up around them. Low parasitic capacitive loads (<4 pF) may not need an $R_{(ISO)}$, since the SN1050x is nominally compensated to operate

with a 2-pF parasitic load. Higher parasitic capacitive loads without an $R_{(ISO)}$ are allowed as the signal gain increases (increasing the unloaded phase margin). If a long trace is required, and the 6-dB signal loss intrinsic to a doubly-terminated transmission line is acceptable, implement a matched-impedance transmission line using microstrip or stripline techniques (consult an ECL design handbook for microstrip and stripline layout techniques). A 50-Ω environment is normally not necessary onboard, and in fact a higher-impedance environment improves distortion as shown in the distortion-versus-load plots. With a characteristic board-trace impedance definition based on board material and trace dimensions, a matching series resistor in the trace from the output of the SN1050x is used as well as a terminating shunt resistor at the input of the destination device. Remember also that the terminating impedance is the parallel combination of the shunt resistor and the input impedance of the destination device: this total effective impedance should be set to match the trace impedance. If the 6-dB attenuation of a doubly terminated transmission line is unacceptable, a long trace can be series-terminated at the source end only. Treat the trace as a capacitive load in this case and add an $R_{(ISO)}$ resistor in series with the output to isolate any capacitance to the amplifier. This setting does not preserve the signal integrity of a doubly-terminated line. If the input impedance of the destination device is low, the signal is attenuated due to the voltage divider formed by the series output into the terminating impedance.

5. **Socketing a high speed part like the SN1050x is not recommended.** The additional lead length and pin-to-pin capacitance introduced by the socket can create a troublesome parasitic network which can make it almost impossible to achieve a smooth, stable frequency response. Best results are obtained by soldering the SN1050x onto the board.

THERMAL ANALYSIS

The SN1050x family of devices does not incorporate automatic thermal shutoff protection, so the designer must take care to ensure that the design does not violate the absolute-maximum junction temperature of the device. Failure may result if the absolute-maximum junction temperature of 150°C is exceeded.

The thermal characteristics of the device are dictated by the package and the PC board. Maximum power dissipation for a given package can be calculated using the following formula.

$$P_{Dmax} = \frac{T_{max} - T_A}{\theta_{JA}}$$

where:

P_{Dmax} is the maximum power dissipation in the amplifier (W).
T_{max} is the absolute maximum junction temperature (°C).
T_A is the ambient temperature (°C).
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} is the thermal coefficient from the silicon junctions to the case (°C/W).
θ_{CA} is the thermal coefficient from the case to ambient air (°C/W).

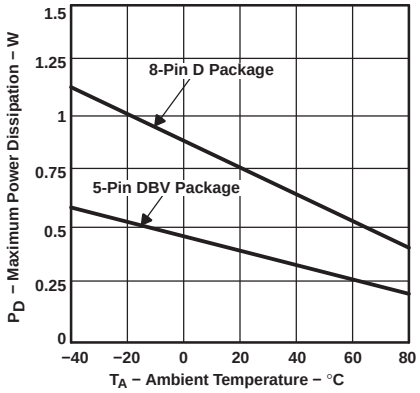


Figure 46. Maximum Power Dissipation vs Ambient Temperature

When determining whether or not the device satisfies the maximum power dissipation requirement, it is important to consider not only quiescent power dissipation, but also dynamic power dissipation. Often maximum power dissipation is difficult to quantify because the signal pattern is inconsistent, but an estimate of the RMS power dissipation can provide visibility into a possible problem.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN10501D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	10501D	Samples
SN10501DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SBBI	Samples
SN10501DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SBBI	Samples
SN10501DBVTG4	LIFEBUY	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SBBI	
SN10501DGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BHA	Samples
SN10501DGKG4	LIFEBUY	VSSOP	DGK	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BHA	
SN10501DGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AJU	Samples
SN10502D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	10502D	Samples
SN10502DGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AJT	Samples
SN10502DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AJT	Samples
SN10502DGN	ACTIVE	HVSSOP	DGN	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AJV	Samples
SN10502DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	10502D	Samples
SN10503D	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	10503D	Samples
SN10503PWP	ACTIVE	HTSSOP	PWP	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	SN10503	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

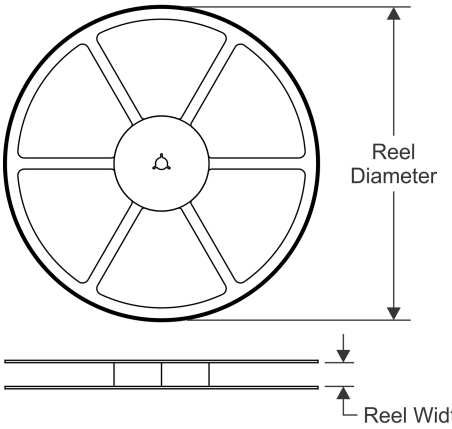
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

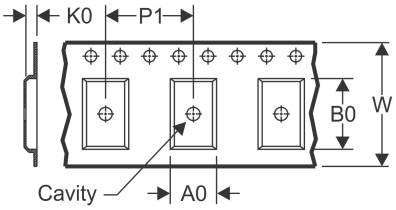
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

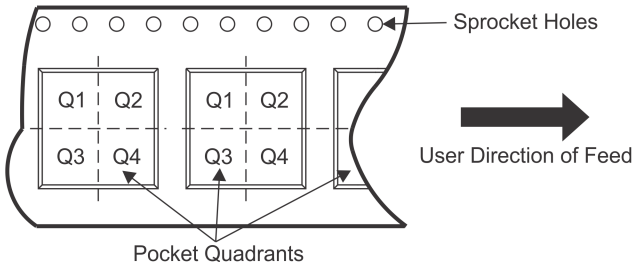


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

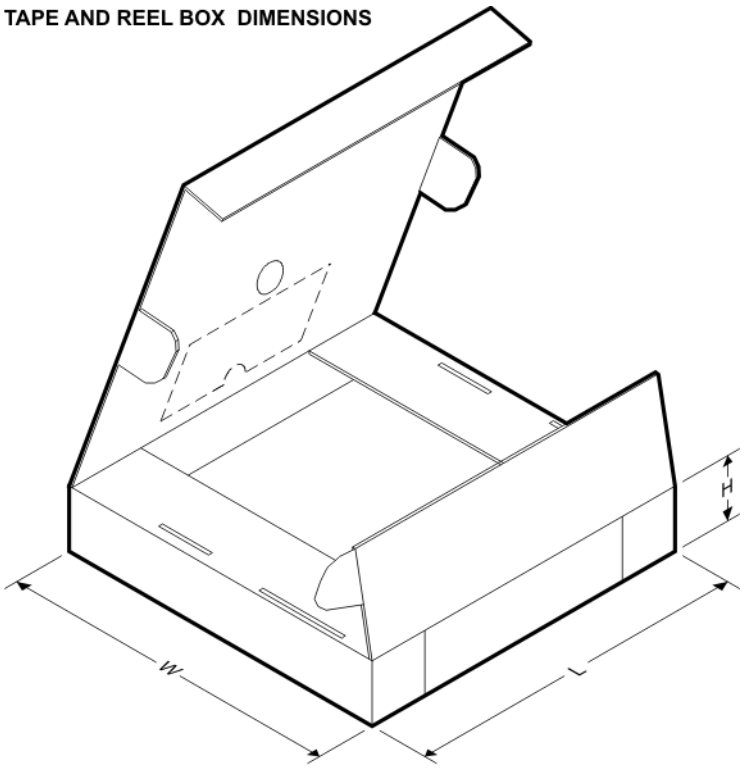
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN10501DBVR	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
SN10501DBVT	SOT-23	DBV	5	250	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
SN10502DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN10502DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

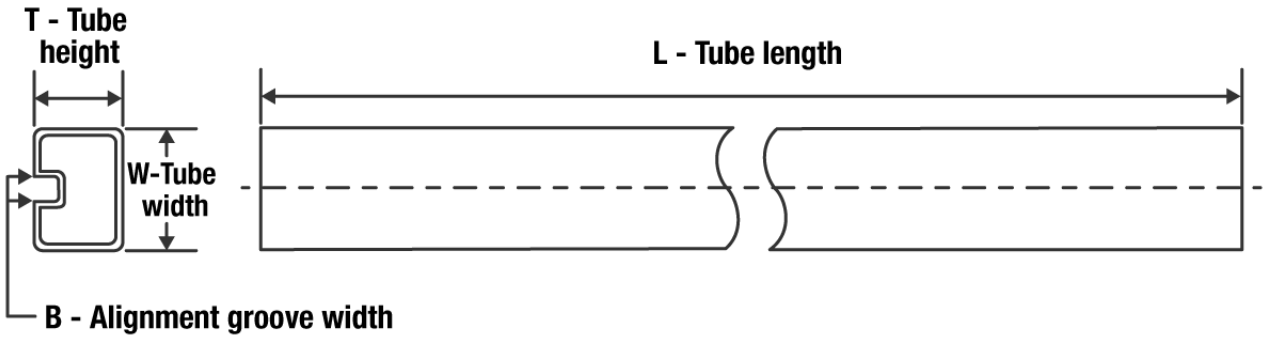
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN10501DBVR	SOT-23	DBV	5	3000	182.0	182.0	20.0
SN10501DBVT	SOT-23	DBV	5	250	182.0	182.0	20.0
SN10502DGKR	VSSOP	DGK	8	2500	358.0	335.0	35.0
SN10502DR	SOIC	D	8	2500	350.0	350.0	43.0

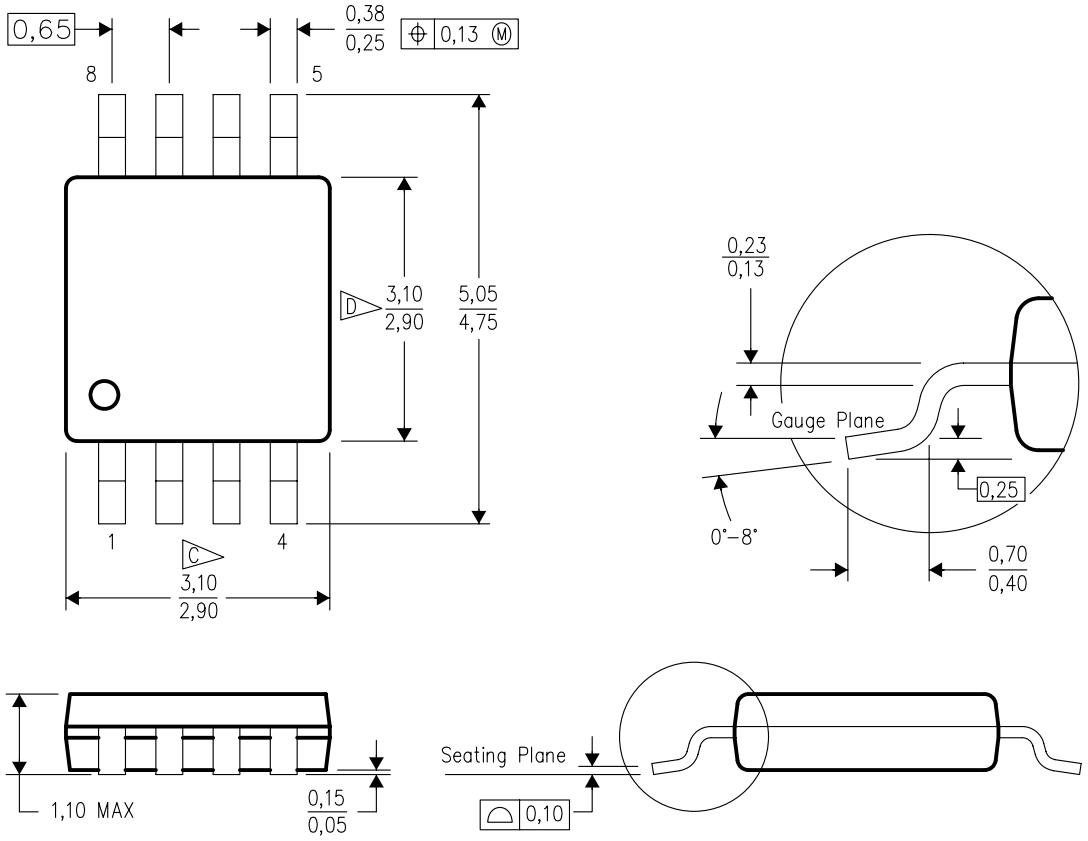
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN10501D	D	SOIC	8	75	505.46	6.76	3810	4
SN10502D	D	SOIC	8	75	505.46	6.76	3810	4
SN10502D	D	SOIC	8	75	505.46	6.76	3810	4
SN10503D	D	SOIC	14	50	505.46	6.76	3810	4
SN10503PWP	PWP	HTSSOP	14	90	530	10.2	3600	3.5

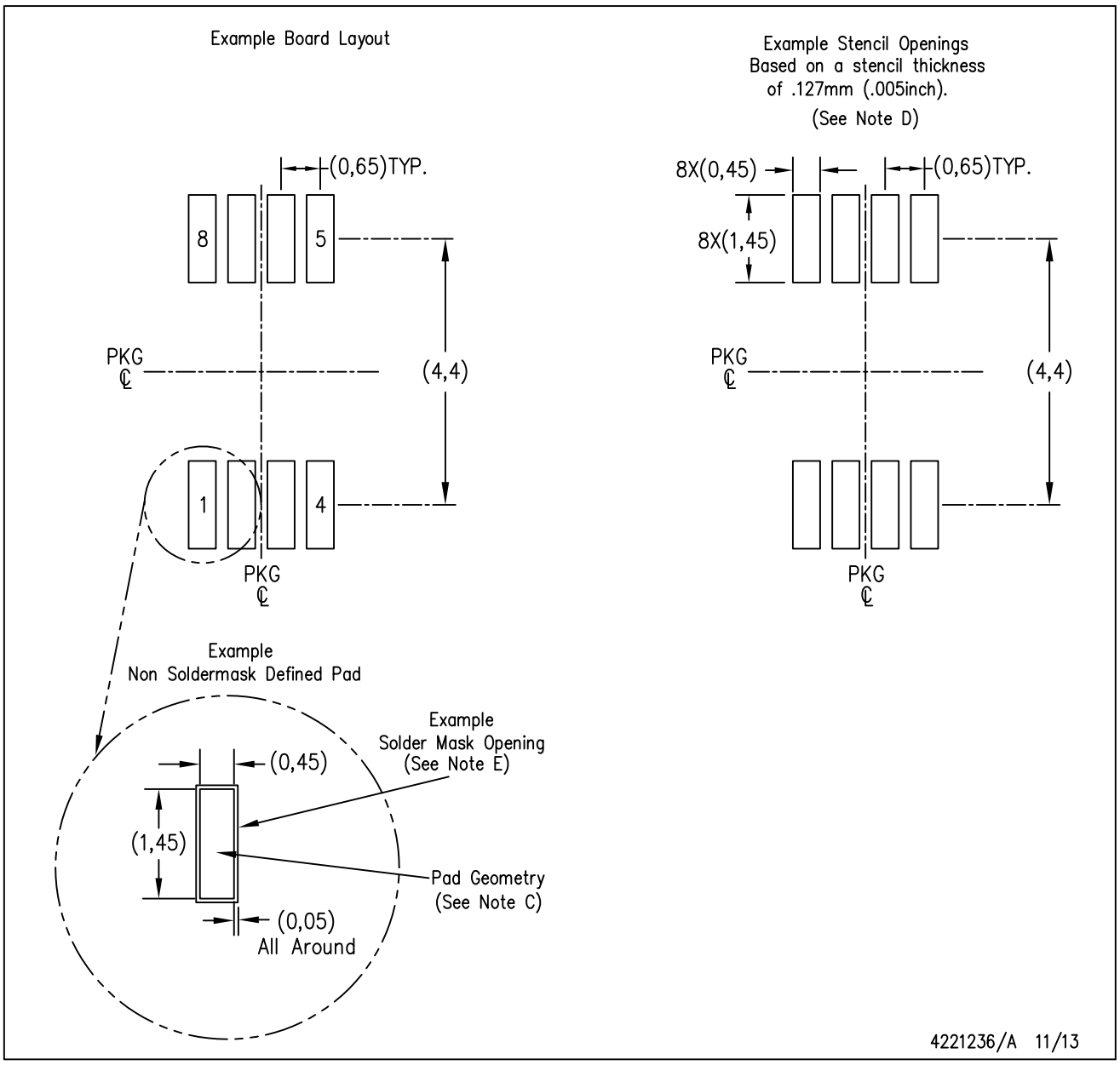
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

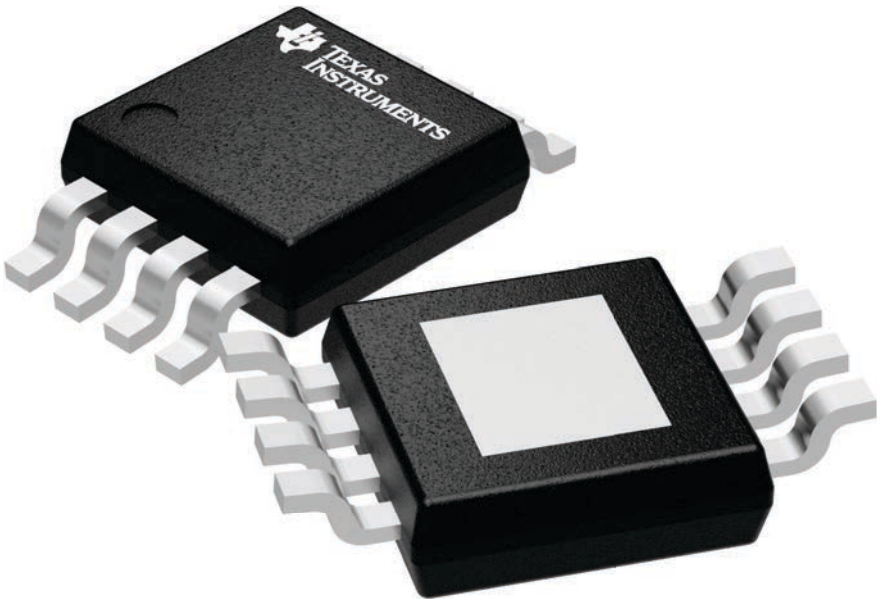
DGN 8

PowerPAD VSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

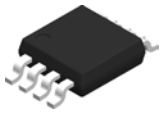
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/A

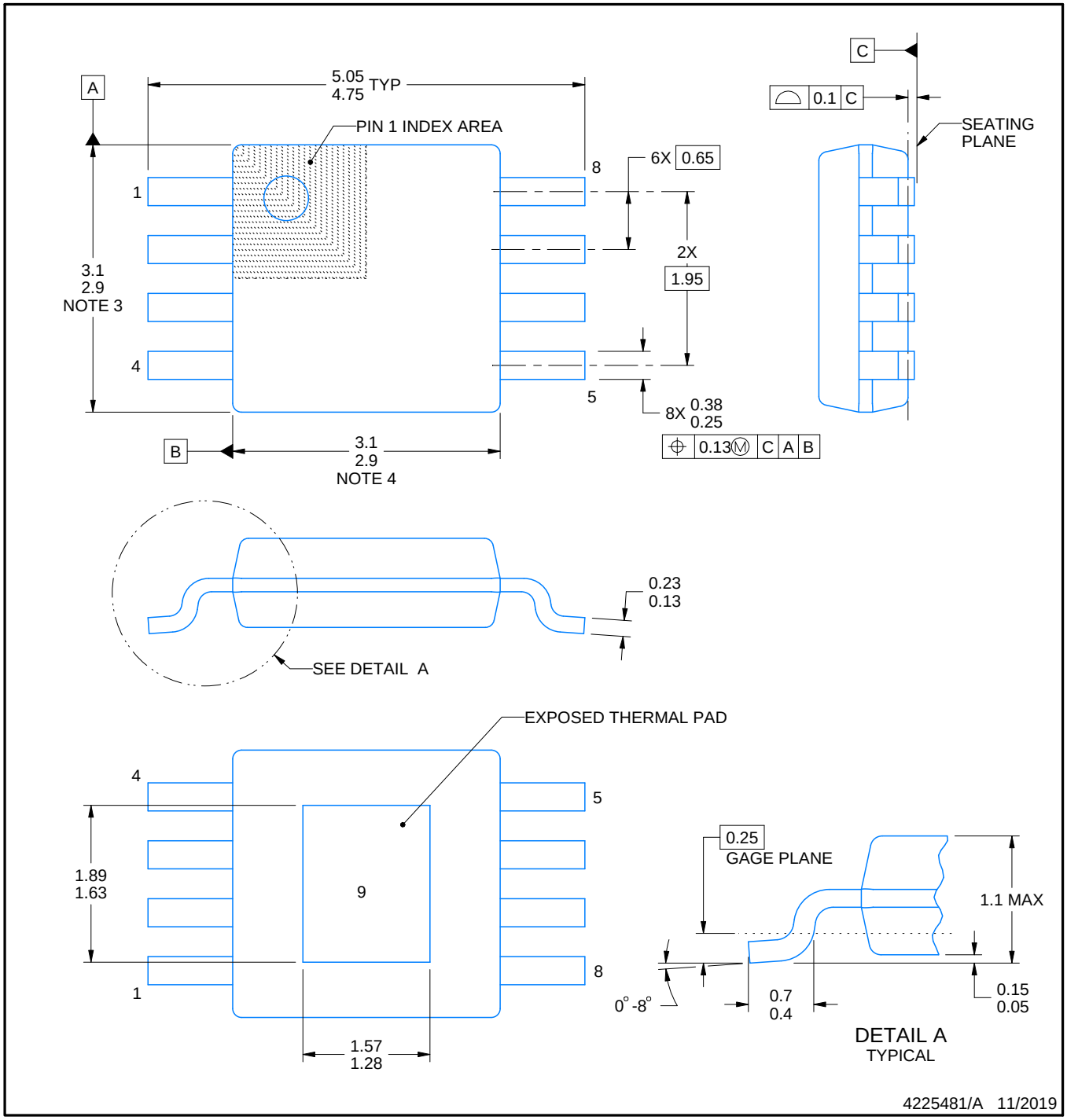
PACKAGE OUTLINE

DGN0008D



PowerPAD™ VSSOP - 1.1 mm max height

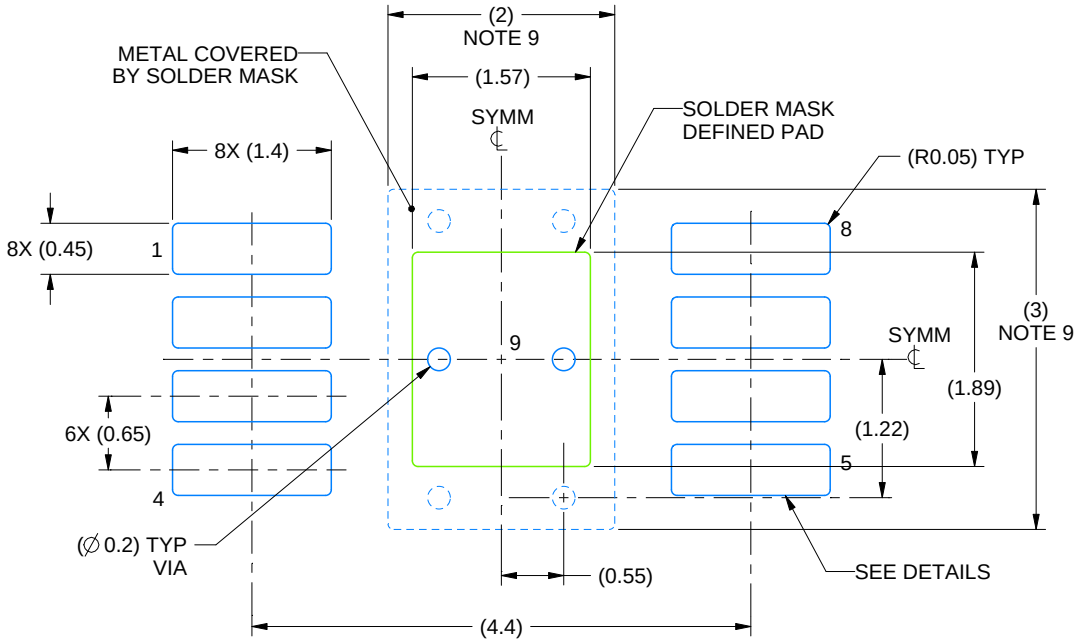
SMALL OUTLINE PACKAGE



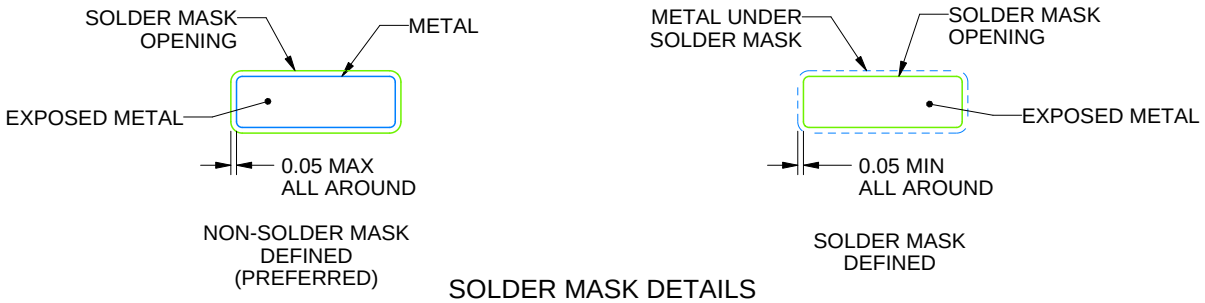
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

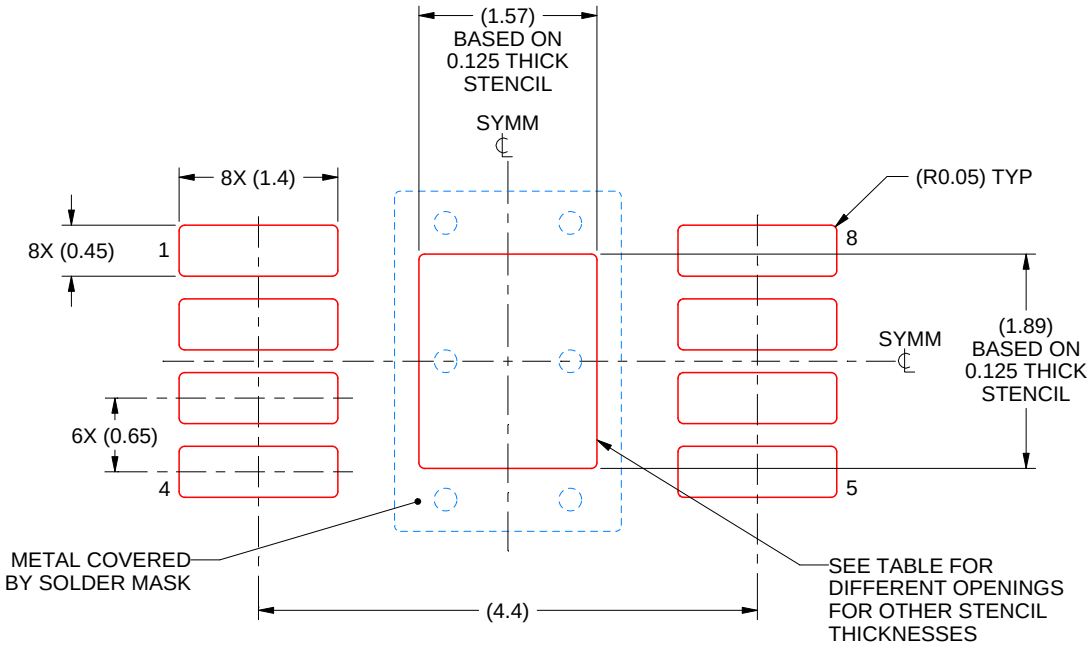


SOLDER MASK DETAILS

4225481/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225481/A 11/2019

NOTES: (continued)

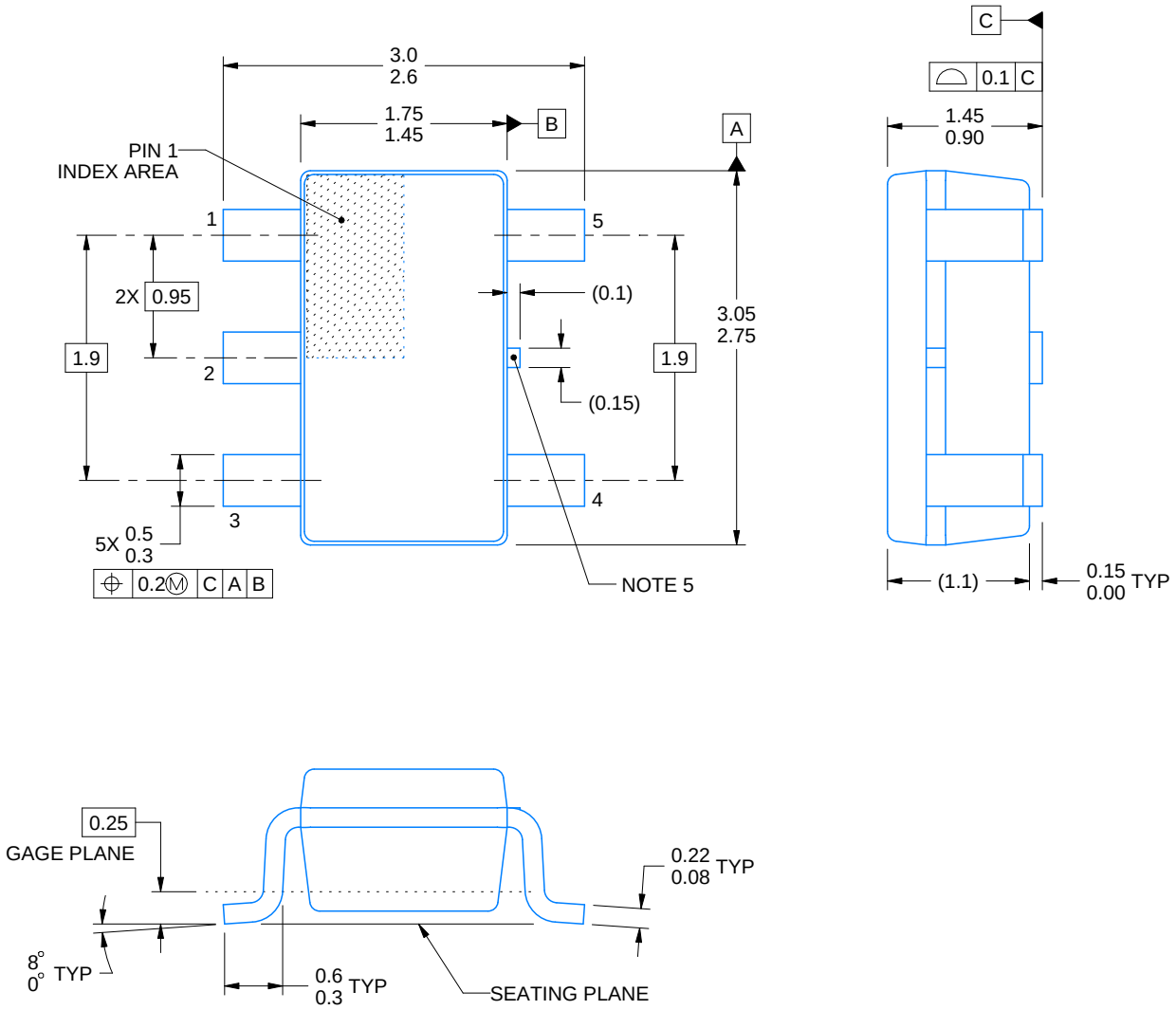
10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

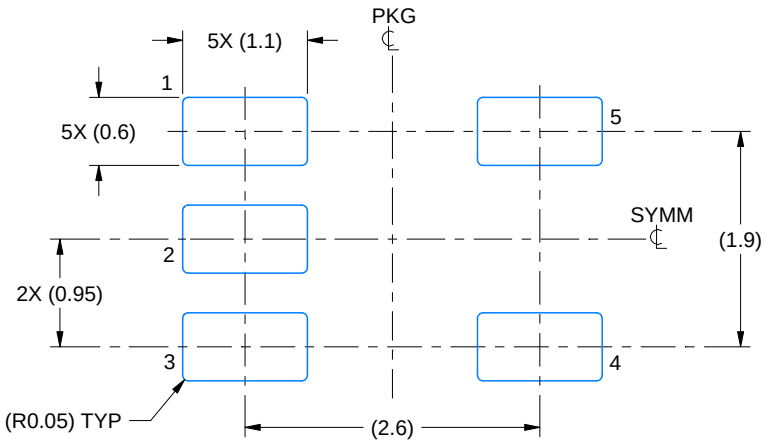
SMALL OUTLINE TRANSISTOR



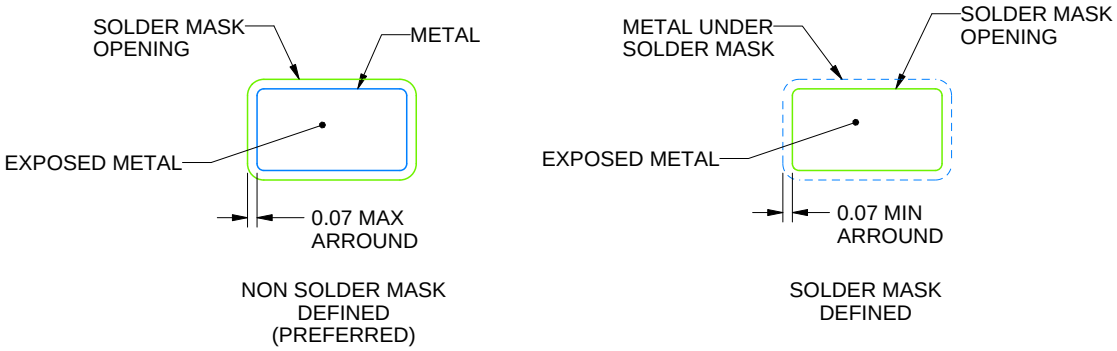
4214839/G 03/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

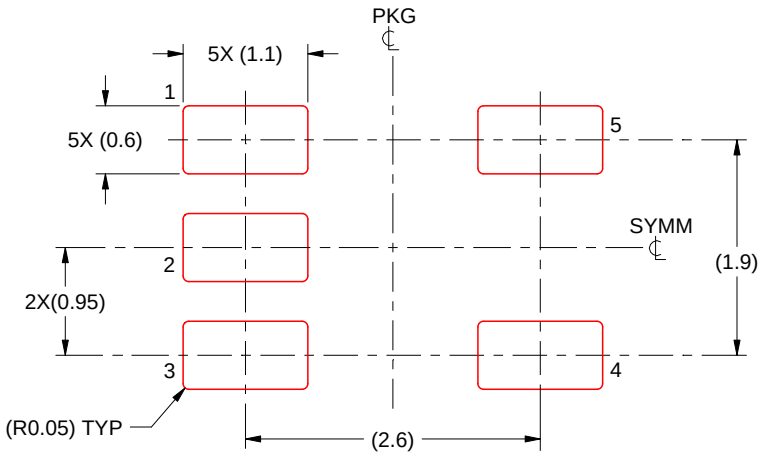


SOLDER MASK DETAILS

4214839/G 03/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



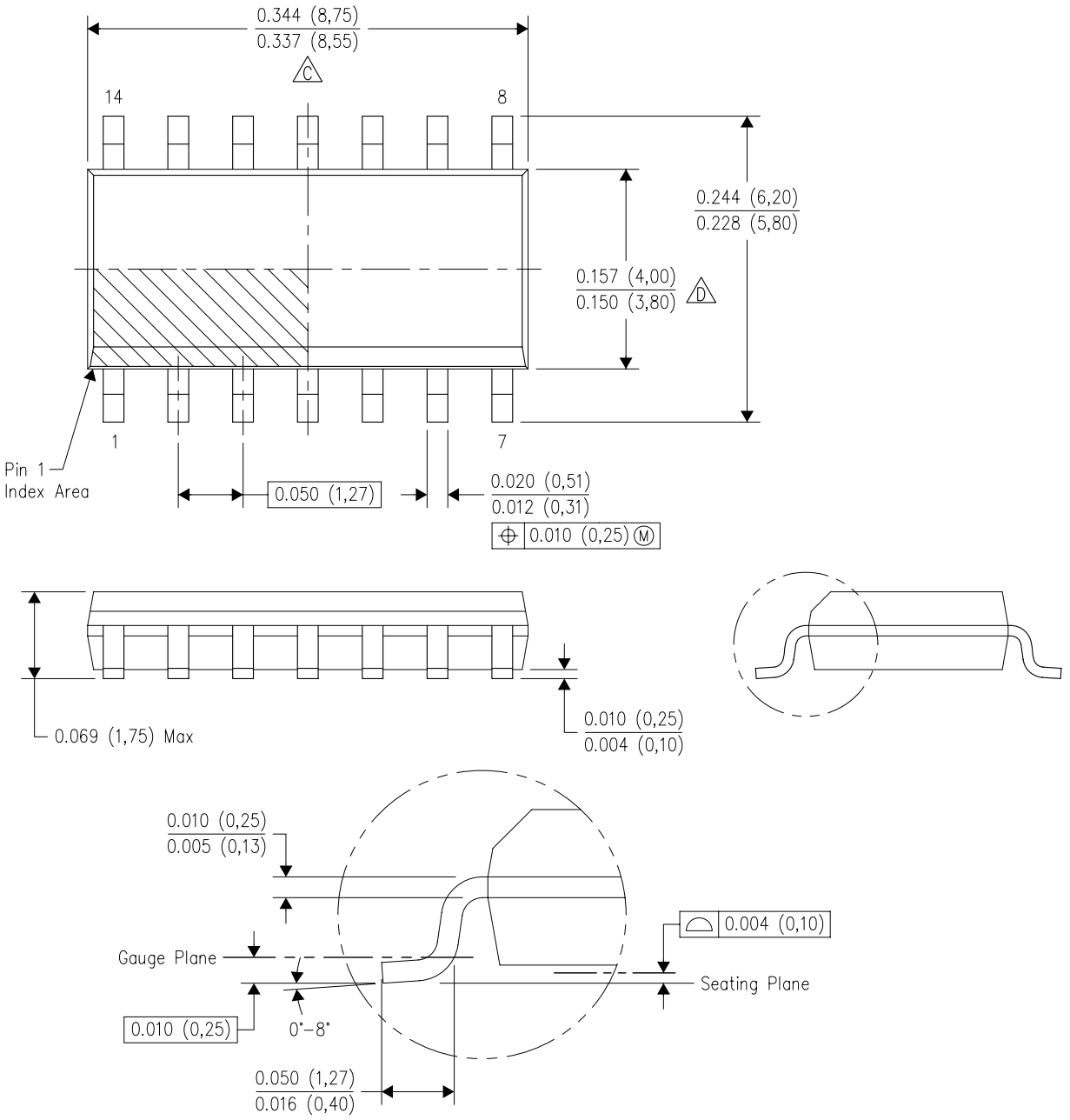
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/G 03/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

GENERIC PACKAGE VIEW

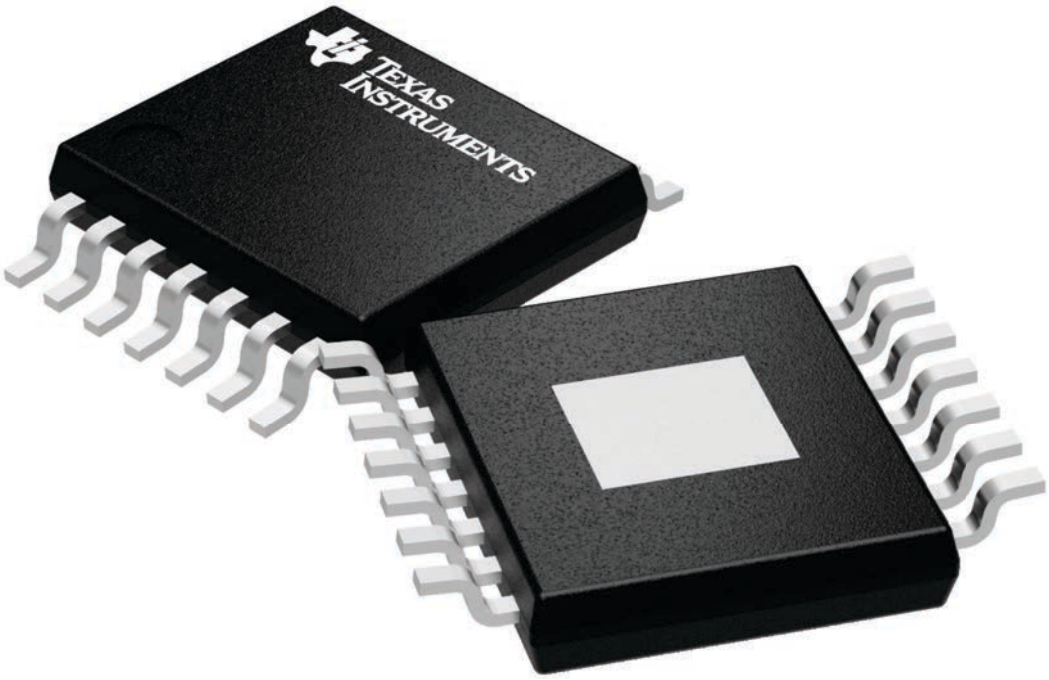
PWP 14

PowerPAD TSSOP - 1.2 mm max height

4.4 x 5.0, 0.65 mm pitch

PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



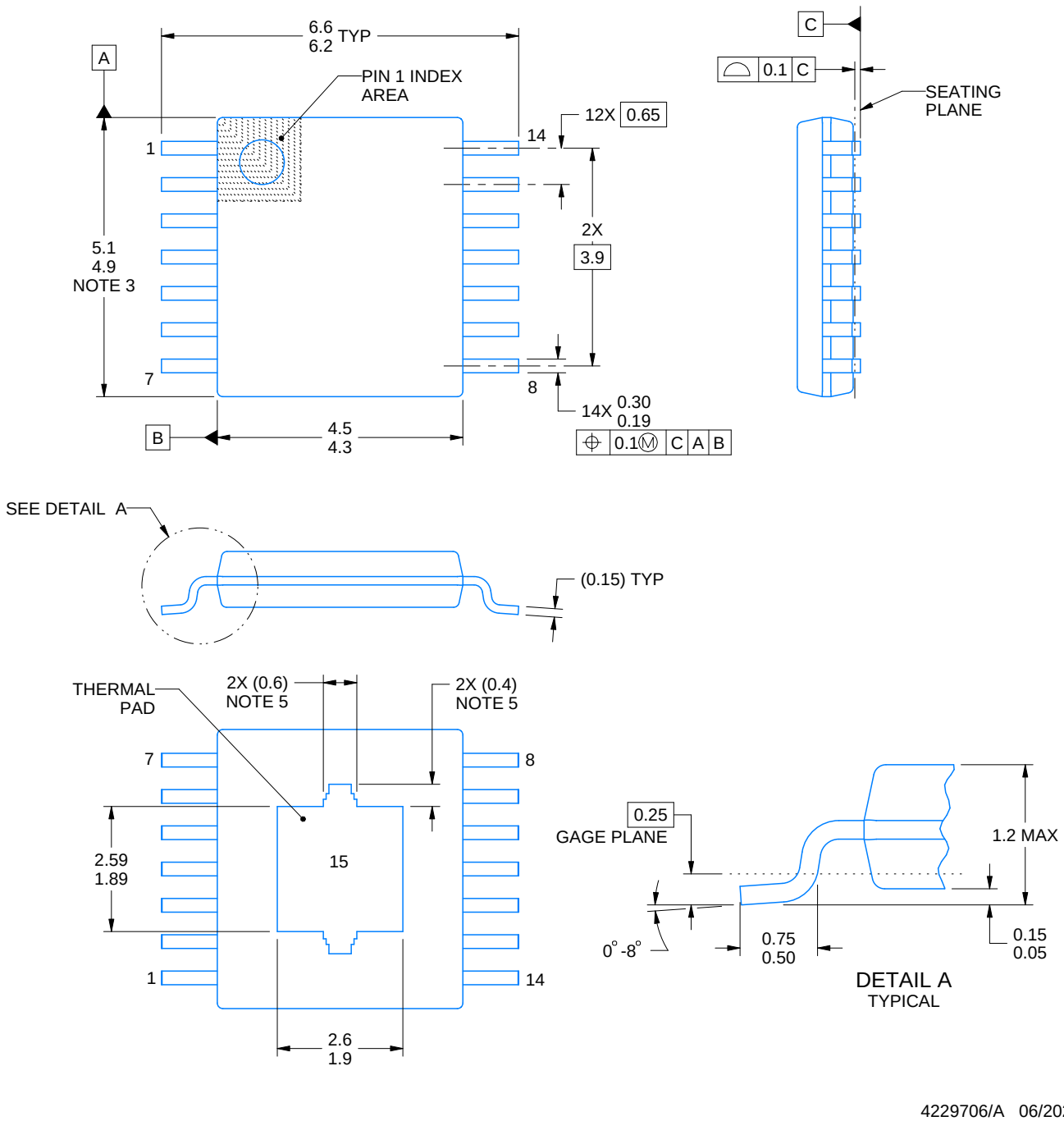
4224995/A

PACKAGE OUTLINE

PWP0014K

PowerPAD™ TSSOP - 1.2 mm max height

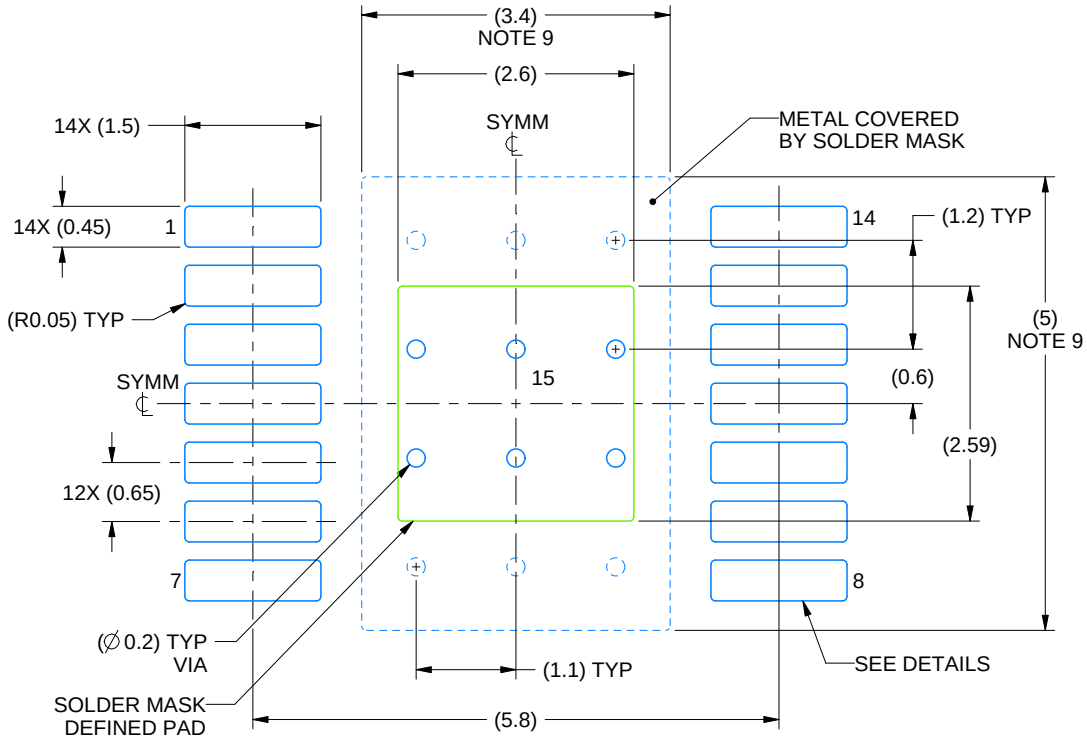
SMALL OUTLINE PACKAGE



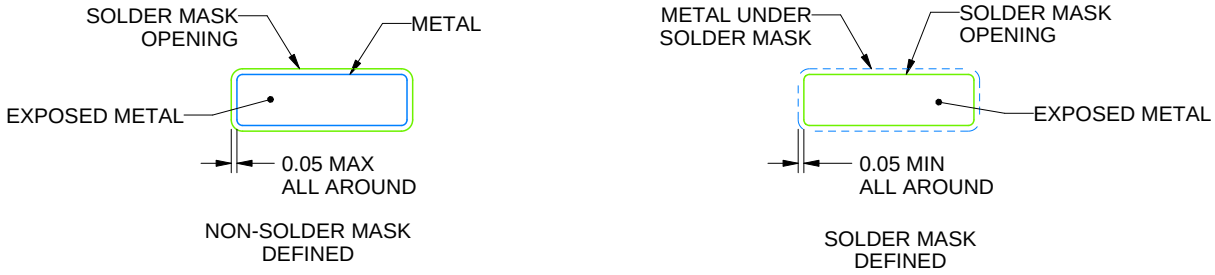
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

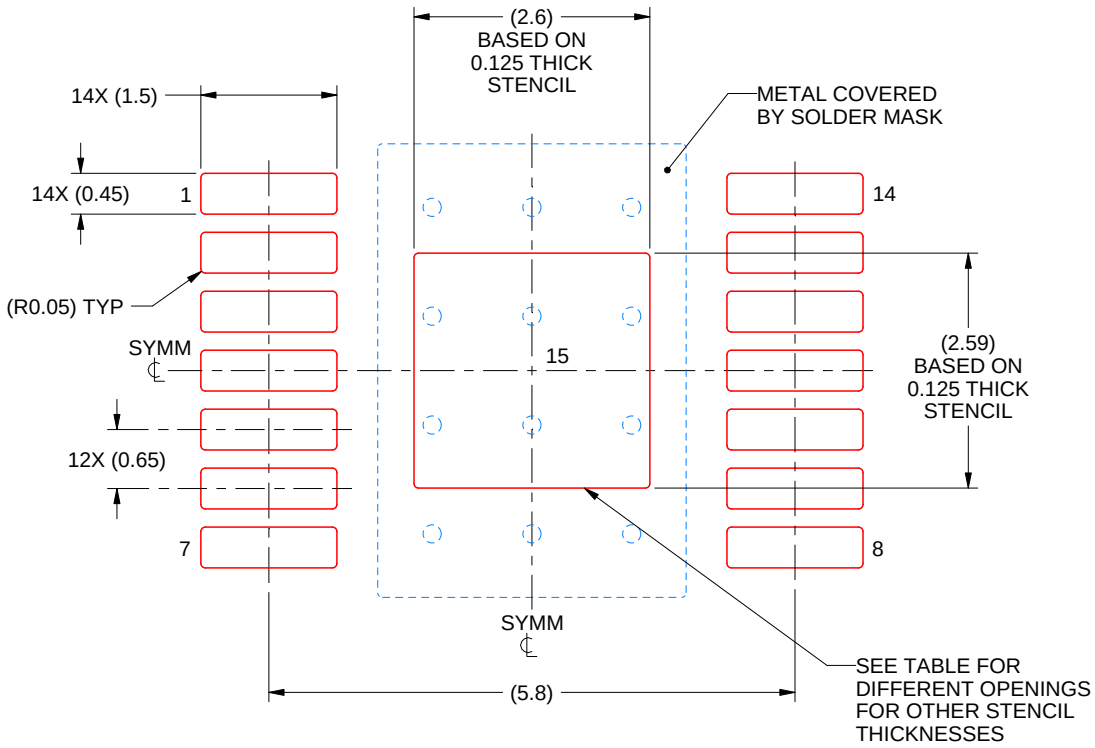


SOLDER MASK DETAILS

4229706/A 06/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



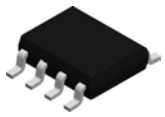
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 2.90
0.125	2.60 X 2.59 (SHOWN)
0.15	2.37 X 2.36
0.175	2.20 X 2.19

4229706/A 06/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

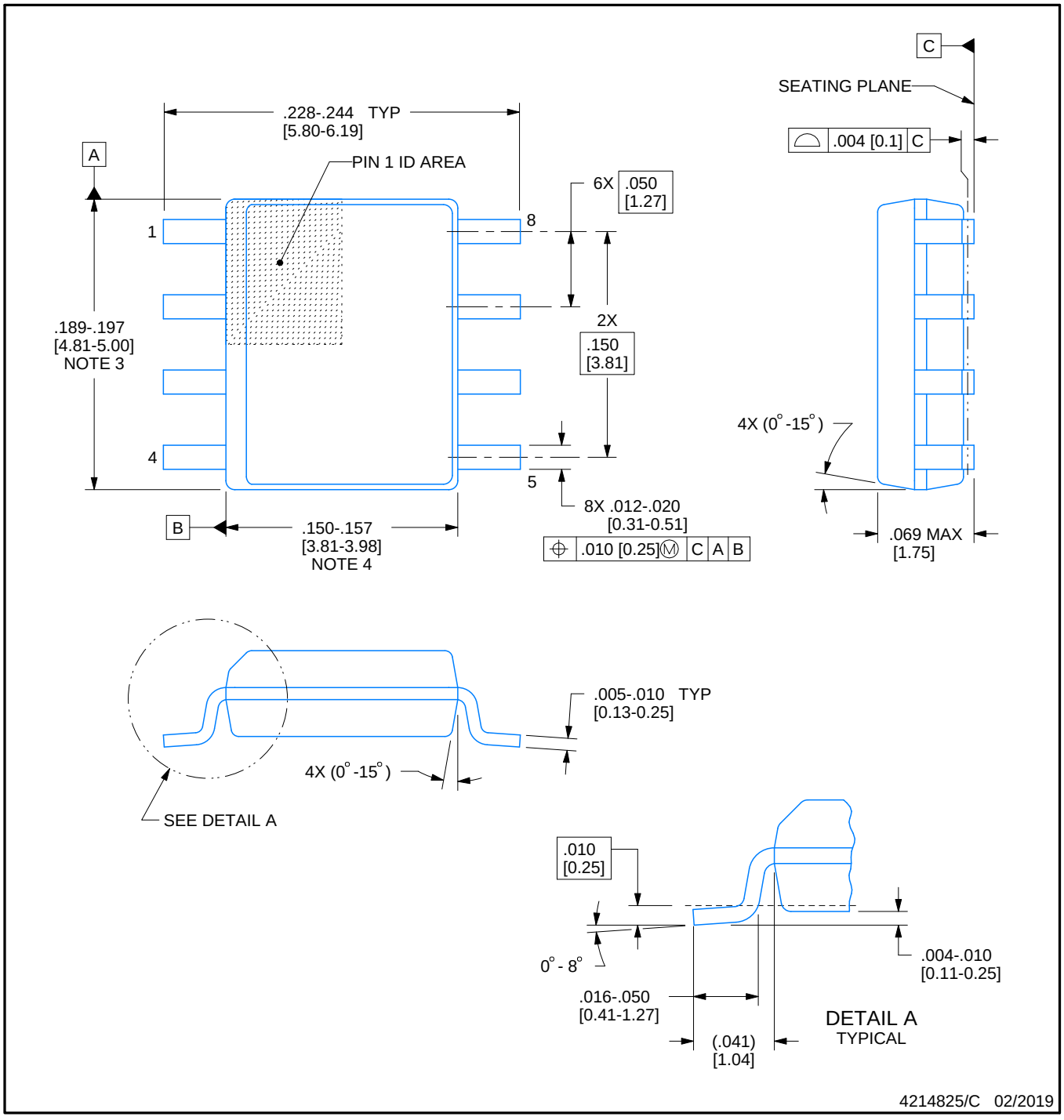


PACKAGE OUTLINE

D0008A

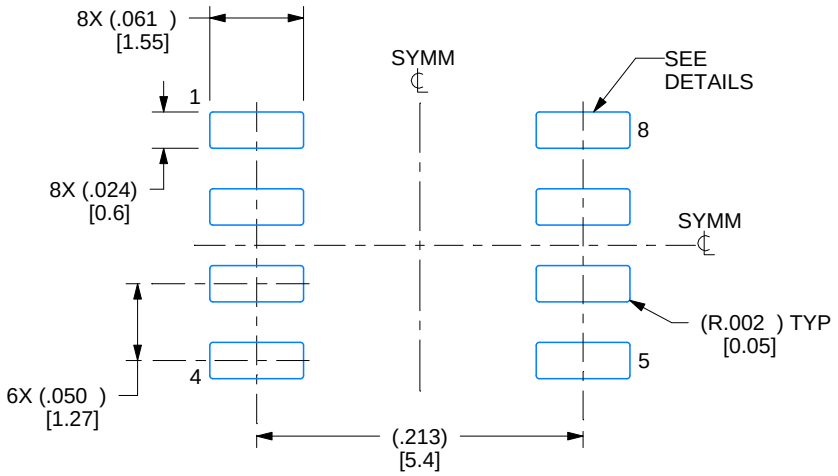
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

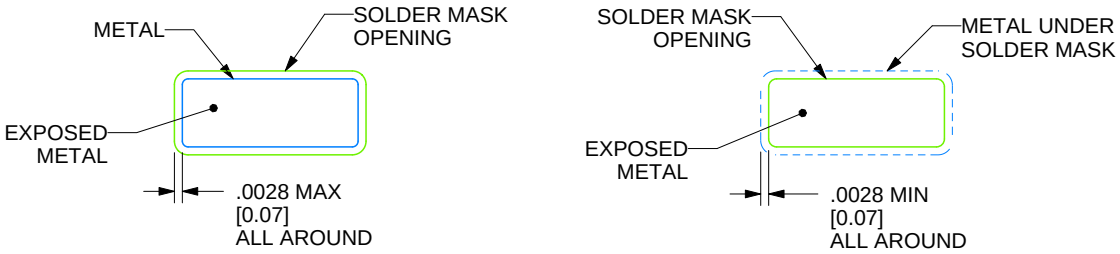


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

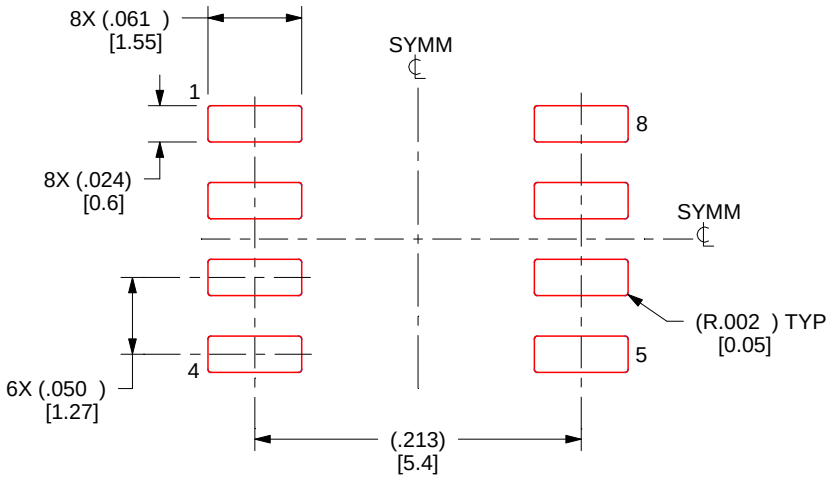
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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