- **Single-Chip and Single-Supply Interface for Two IBM™ PC/AT Serial Ports**
- **Meet or Exceed the Requirements of TIA/EIA-232-F and ITU v.28 Standards**
- **Operate With 3-V to 5.5-V V_{CC} Supply**
- **Always-Active Noninverting Receiver Output ($\overline{\text{ROUT2}}$) Per Port**
- **Operate Up To 250 kbit/s**
- **Low Standby Current . . . 1 μA Typical**
- **External Capacitors . . . 4 × 0.22 μF**
- **Accept 5-V Logic Input With 3.3-V Supply**
- **Allow for Flexible Power Down of Either Serial Port**
- **Serial-Mouse Driveability**
- **RS-232 Bus-Pin ESD Protection Exceeds ±15 kV Using Human-Body Model (HBM)**
- **Applications**
  - **Battery-Powered Systems, Notebooks, Laptops, Palmtop PCs, and Hand-Held Equipment**

DGG OR DL PACKAGE
(TOP VIEW)

RIN5A	1	48	ROUT5A
RIN4A	2	47	ROUT4A
RIN3A	3	46	ROUT3A
RIN2A	4	45	ROUT2A
RIN1A	5	44	ROUT1A
$\overline{\text{INVA}}$	6	43	$\overline{\text{ROUT2A}}$
DOUT3A	7	42	DIN3A
DOUT2A	8	41	DIN2A
DOUT1A	9	40	DIN1A
$\overline{\text{FORCEOFFA}}$	10	39	FORCEON
C2−	11	38	V−
C2+	12	37	V+
GND	13	36	C1+
V_{CC}	14	35	C1−
$\overline{\text{FORCEOFFB}}$	15	34	GND
DOUT1B	16	33	DIN1B
DOUT2B	17	32	DIN2B
DOUT3B	18	31	DIN3B
$\overline{\text{INVB}}$	19	30	$\overline{\text{ROUT2B}}$
RIN1B	20	29	ROUT1B
RIN2B	21	28	ROUT2B
RIN3B	22	27	ROUT3B
RIN4B	23	26	ROUT4B
RIN5B	24	25	ROUT5B

description/ordering information

The SN65C23243 and SN75C23243 consist of two ports, each containing three line drivers and five line receivers, and a dual charge-pump circuit with ±15-kV ESD protection pin to pin (serial-port connection pins, including GND). These devices meet the requirements of TIA/EIA-232-F and provide the electrical interface between an asynchronous communication controller and the serial-port connector. This combination of drivers and receivers matches that needed for two typical serial ports used in an IBM PC/AT, or compatible. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. In addition, these devices include an always-active noninverting output ($\overline{\text{ROUT2}}$) per port, which allows applications using the ring indicator to transmit data while the devices are powered down. The devices operate at data signaling rates up to 250 kbit/s and a maximum of 30-V/μs driver output slew-rate.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−0°C to 70°C	SSOP (DL)	Tube of 25	SN75C23243DL	75C23243
		Reel of 1000	SN75C23243DLR	
	TSSOP (DGG)	Reel of 2000	SN75C23243DGGR	75C23243
−40°C to 85°C	SSOP (DL)	Tube of 25	SN65C23243DL	65C23243
		Reel of 1000	SN65C23243DLR	
	TSSOP (DGG)	Reel of 2000	SN65C23243DGGR	65C23243

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

description/ordering information (continued)

Flexible control options for power management are available when either or both serial ports are inactive. The auto-powerdown feature functions when FORCEON is low and $\overline{\text{FORCEOFF}}$ is high. During this mode of operation, if the device does not sense a valid RS-232 signal, the driver outputs of its respective port are disabled. If $\overline{\text{FORCEOFF}}$ is set low, both drivers and receivers (except $\overline{\text{ROUT2}}$) are shut off, and the supply current is reduced to 1 µA. Disconnecting the serial port or turning off the peripheral drivers causes the auto-powerdown condition to occur.

Auto-powerdown can be disabled when FORCEON and $\overline{\text{FORCEOFF}}$ are high and should be done when driving a serial mouse. With auto-powerdown enabled, the RS-232 port is activated automatically when a valid signal is applied to any respective receiver input. The $\overline{\text{INV}}$ output is used to notify the user if an RS-232 signal is present at any receiver input. $\overline{\text{INV}}$ is high (valid data) if any receiver input voltage is greater than 2.7 V or less than −2.7 V or has been between −0.3 V and 0.3 V for less than 30 µs. $\overline{\text{INV}}$ is low (invalid data) if all receiver input voltages are between −0.3 V and 0.3 V for more than 30 µs. Refer to Figure 5 for receiver input levels.

Function Tables

EACH DRIVER
(each port)

INPUTS				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	$\overline{\text{FORCEOFF}}$	VALID RIN RS-232 LEVEL		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-powerdown enabled
H	L	H	Yes	L	
L	L	H	No	Z	Powered off by auto-powerdown feature
H	L	H	No	Z	

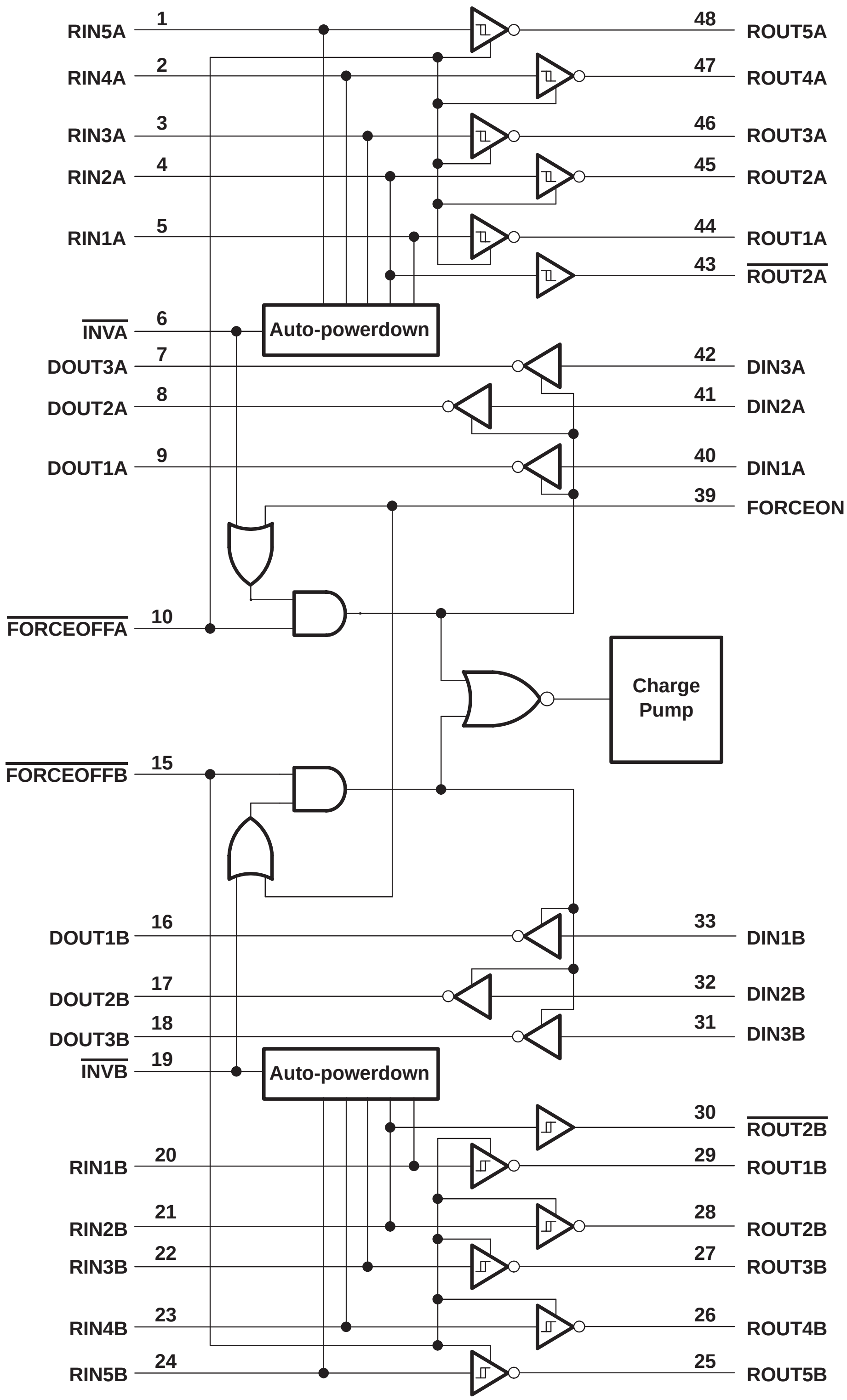
H = high level, L = low level, X = irrelevant, Z = high impedance

EACH RECEIVER
(each port)

INPUTS				OUTPUTS		RECEIVER STATUS
RIN2	RIN1, RIN3−RIN5	$\overline{\text{FORCEOFF}}$	VALID RIN RS-232 LEVEL	$\overline{\text{ROUT2}}$	ROUT	
L	X	L	X	L	Z	Powered off while $\overline{\text{ROUT2}}$ is active
H	X	L	X	H	Z	
L	L	H	Yes	L	H	Normal operation with auto-powerdown disabled/enabled
L	H	H	Yes	L	L	
H	L	H	Yes	H	H	
H	H	H	Yes	H	L	
Open	Open	H	No	L	H	

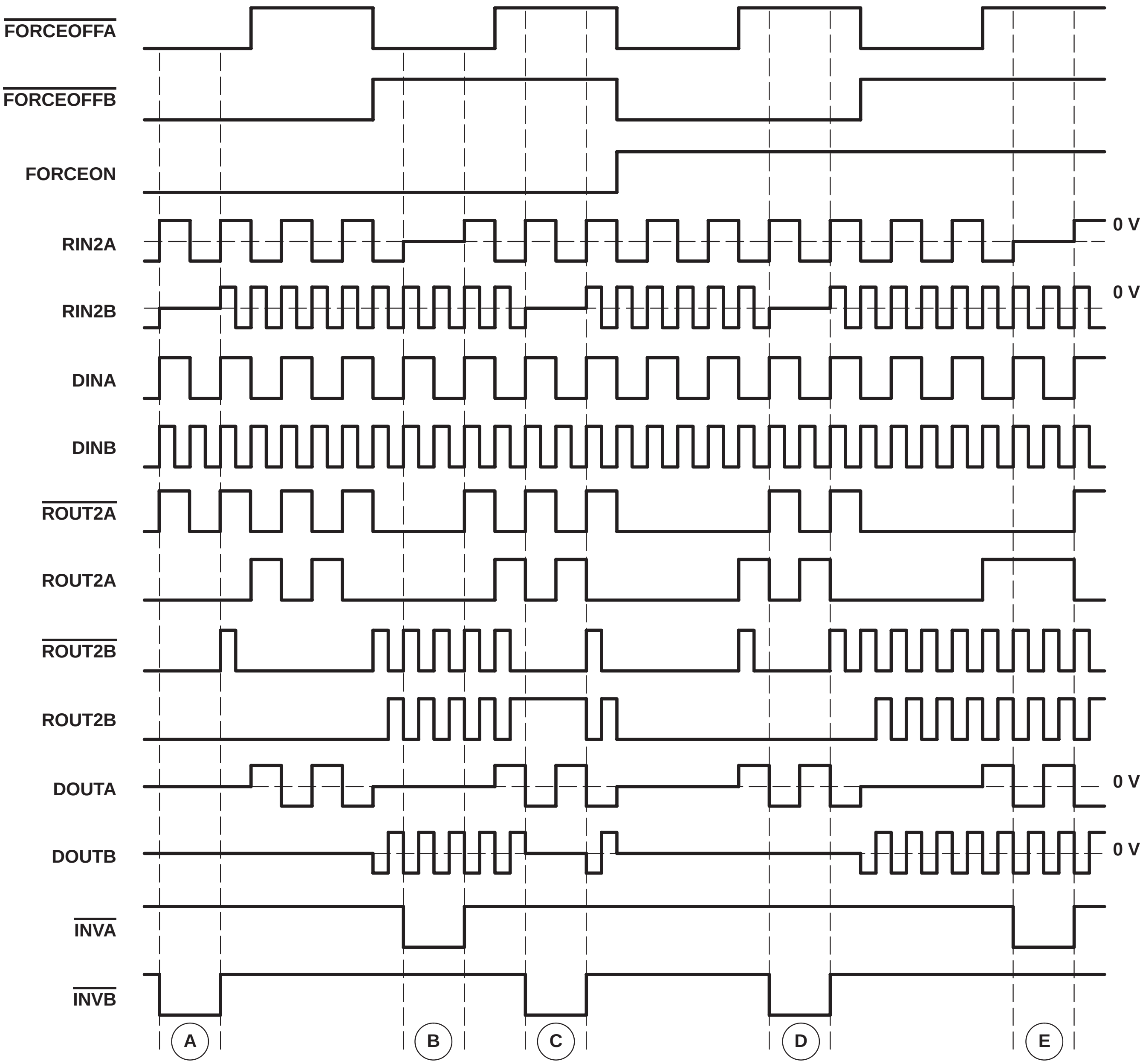
H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

logic diagram (positive logic)



timing

Figure 1 shows how the two independent serial ports can be enabled or disabled. As shown by the logic states, depending on the $\overline{\text{FORCEOFF}}$, FORCEON, and receiver input levels, either port can be powered down. Intermediate receiver input levels indicate a 0-V input. Also, it is assumed a pulldown resistor to ground is used for the receiver outputs. The $\overline{\text{INV}}$ pin goes low when its respective receiver input does not supply a valid RS-232 level. For simplicity, voltage levels, timing differences, and input/output edge rates are not shown.



NOTES: A. Ports A and B manually powered off
B. Port A manually powered off, port B in normal operation with auto-powerdown enabled
C. Port B powered off by auto-powerdown, port A in normal operation with auto-powerdown enabled
D. Port A in normal operation with auto-powerdown disabled, port B manually powered off
E. Ports A and B in normal operation with auto-powerdown disabled

Figure 1. Timing Diagram

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . . . −0.3 V to 6 V
Positive output supply voltage range, V+ (see Note 1) . . . . . . −0.3 V to 7 V
Negative output supply voltage, V− (see Note 1) . . . . . . 0.3 V to −7 V
Supply voltage difference, V+ − V− (see Note 1) . . . . . . 13 V
Input voltage range, V_I: Driver ($\overline{\text{FORCEOFF}}$, FORCEON) . . . . . . −0.3 V to 6 V
Receiver . . . . . . −25 V to 25 V
Output voltage range, V_O: Driver . . . . . . −13.2 V to 13.2 V
Receiver ($\overline{\text{INV}}$) . . . . . . −0.3 V to V_{CC} + 0.3 V
Package thermal impedance, θ_{JA} (see Notes 2 and 3): DGG package . . . . . . 70°C/W
DL package . . . . . . 63°C/W
Operating virtual junction temperature, T_J . . . . . . 150°C
Storage temperature range, T_{stg} . . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to network GND.
2. Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4 and Figure 7)

			MIN	NOM	MAX	UNIT
Supply voltage		V_{CC} = 3.3 V	3	3.3	3.6	V
		V_{CC} = 5 V	4.5	5	5.5	
Driver and control high-level input voltage, V_{IH}	DIN, $\overline{\text{FORCEOFF}}$, FORCEON	V_{CC} = 3.3 V	2			V
		V_{CC} = 5 V	2.4			
Driver and control low-level input voltage, V_{IL}	DIN, $\overline{\text{FORCEOFF}}$, FORCEON				0.8	V
Driver and control input voltage, V_I	DIN, $\overline{\text{FORCEOFF}}$, FORCEON		0		5.5	V
Receiver input voltage, V_I	RIN		−25		25	V
Operating free-air temperature, T_A		SN75C23243	0		70	°C
		SN65C23243	−40		85	

NOTE 4: Test conditions are C1−C4 = 0.22 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2−C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 7)

PARAMETER			TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I_I	Input leakage current	$\overline{\text{FORCEOFF}}$, FORCEON			±0.01	±1	μA
I_{CC}	Supply current (T_A = 25°C)	Auto-powerdown disabled	No load, $\overline{\text{FORCEOFF}}$ and FORCEON at V_{CC}		0.6	2	mA
		Powered off	No load, $\overline{\text{FORCEOFF}}$ at GND		1	20	μA
		Auto-powerdown enabled	No load, $\overline{\text{FORCEOFF}}$ at V_{CC}, FORCEON at GND, All RIN are open or grounded		1	20	

‡ All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V and T_A = 25°C.
NOTE 4: Test conditions are C1−C4 = 0.22 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2−C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 7)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	All DOUT at R_L = 3 kΩ to GND		5	5.4		V
V_{OL}	Low-level output voltage	All DOUT at R_L = 3 kΩ to GND		−5	−5.4		V
V_O	Output voltage (mouse driveability)	DIN1 = DIN2 = GND, DIN3 = V_{CC}, 3-kΩ to GND at DOUT3, DOUT1 = DOUT2 = −2.5 mA		±5			V
I_{IH}	High-level input current	$V_I = V_{CC}$			±0.01	±1	μA
I_{IL}	Low-level input current	V_I at GND			±0.01	±1	μA
I_{OS}	Short-circuit output current‡	V_{CC} = 3.6 V,	V_O = 0 V		±35	±60	mA
		V_{CC} = 5.5 V,	V_O = 0 V				
r_o	Output resistance	V_{CC}, V+, and V− = 0 V,	V_O = ±2 V	300	10M		Ω
I_{off}	Output leakage current	$\overline{\text{FORCEOFF}}$ = GND	V_O = ±12 V, V_{CC} = 3 V to 3.6 V			±25	μA
			V_O = ±10 V, V_{CC} = 4.5 V to 5.5 V			±25	

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V and T_A = 25°C.
‡ Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.
NOTE 4: Test conditions are C1−C4 = 0.22 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2−C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 7)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
	Maximum data rate	C_L = 1000 pF, One DOUT switching,	R_L = 3 kΩ, See Figure 1	250			kbit/s
$t_{sk(p)}$	Pulse skew§	C_L = 150 pF to 2500 pF	R_L = 3 kΩ to 7 kΩ, See Figure 2		100		ns
SR(tr)	Slew rate, transition region (see Figure 1)	V_{CC} = 3.3 V, R_L = 3 kΩ to 7 kΩ	C_L = 150 pF to 1000 pF	6		30	V/μs
			C_L = 150 pF to 2500 pF	4		30	

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V and T_A = 25°C.
§ Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
NOTE 4: Test conditions are C1−C4 = 0.22 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2−C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

RECEIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 7)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −1 mA	V_{CC} − 0.6 V	V_{CC} − 0.1 V		V
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.4	V
V_{IT+}	Positive-going input threshold voltage	V_{CC} = 3.3 V		1.6	2.4	V
		V_{CC} = 5 V		1.9	2.4	
V_{IT-}	Negative-going input threshold voltage	V_{CC} = 3.3 V	0.6	1.1		V
		V_{CC} = 5 V	0.8	1.4		
V_{hys}	Input hysteresis (V_{IT+} − V_{IT-})			0.5		V
I_{off}	Output leakage current (except ROUT2B)	$\overline{\text{FORCEOFF}}$ = 0 V		±0.05	±10	µA
r_i	Input resistance	V_I = ±3 V to ±25 V	3	5	7	kΩ

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V and T_A = 25°C.
NOTE 4: Test conditions are C1−C4 = 0.22 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2−C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 4 and Figure 7)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	C_L = 150 pF, See Figure 4		150		ns
t_{PHL}	Propagation delay time, high- to low-level output			150		ns
t_{en}	Output enable time	C_L = 150 pF, R_L = 3 kΩ, See Figure 5		200		ns
t_{dis}	Output disable time			200		ns
$t_{sk(p)}$	Pulse skew‡	See Figure 4		50		ns

† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V and T_A = 25°C.
‡ Pulse skew is defined as $|t_{PLH} - t_{PHL}|$ of each channel of the same device.
NOTE 4: Test conditions are C1−C4 = 0.22 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2−C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

AUTO-POWERDOWN SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 6)

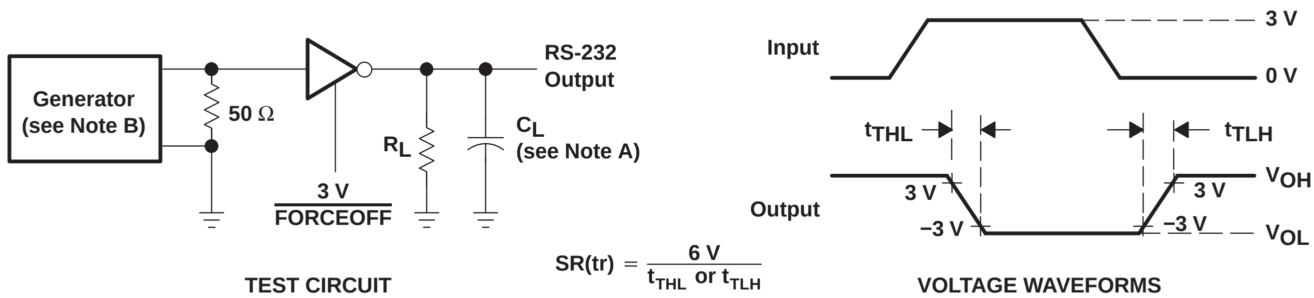
PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{T+(valid)}$	Receiver input threshold for $\overline{INV}$ high-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}		2.7	V
$V_{T-(valid)}$	Receiver input threshold for $\overline{INV}$ high-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}	−2.7		V
$V_{T(invalid)}$	Receiver input threshold for $\overline{INV}$ low-level output voltage	FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}	−0.3	0.3	V
V_{OH}	$\overline{INV}$ high-level output voltage	I_{OH} = −1 mA, FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}	V_{CC} − 0.6		V
V_{OL}	$\overline{INV}$ low-level output voltage	I_{OL} = 1.6 mA, FORCEON = GND, $\overline{FORCEOFF}$ = V_{CC}		0.4	V

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 6)

PARAMETER		MIN	TYP†	MAX	UNIT
t_{valid}	Propagation delay time, low- to high-level output		1		µs
$t_{invalid}$	Propagation delay time, high- to low-level output		30		µs
t_{en}	Supply enable time		100		µs

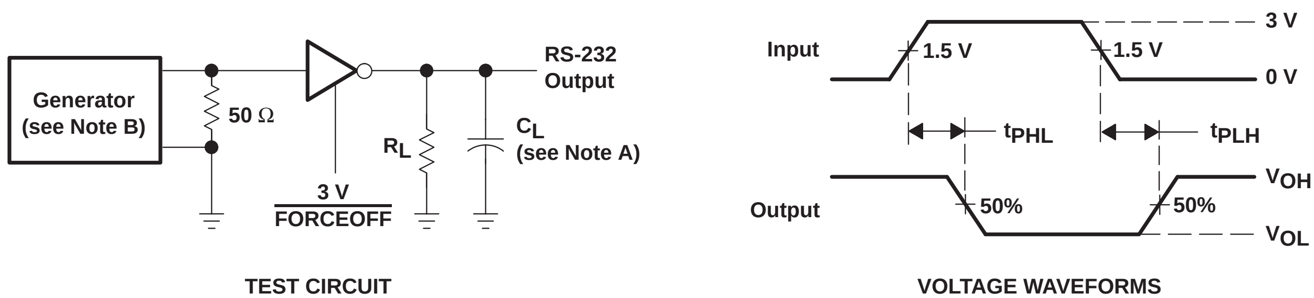
† All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V and T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



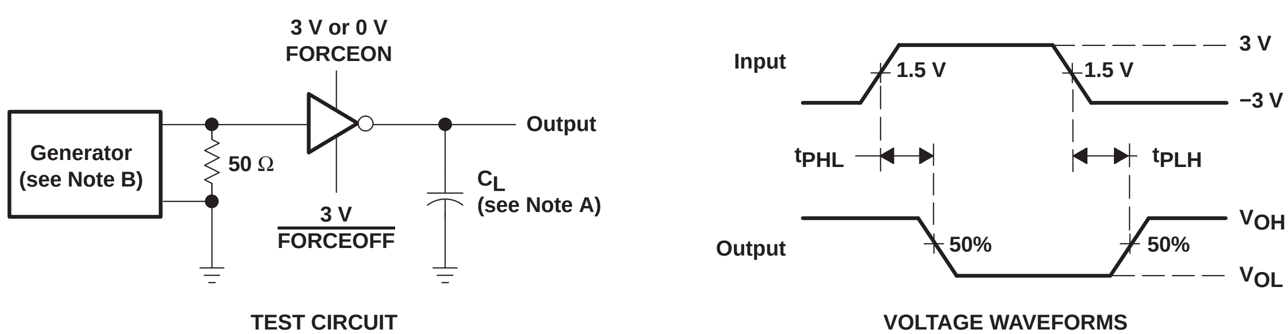
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 2. Driver Slew Rate



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

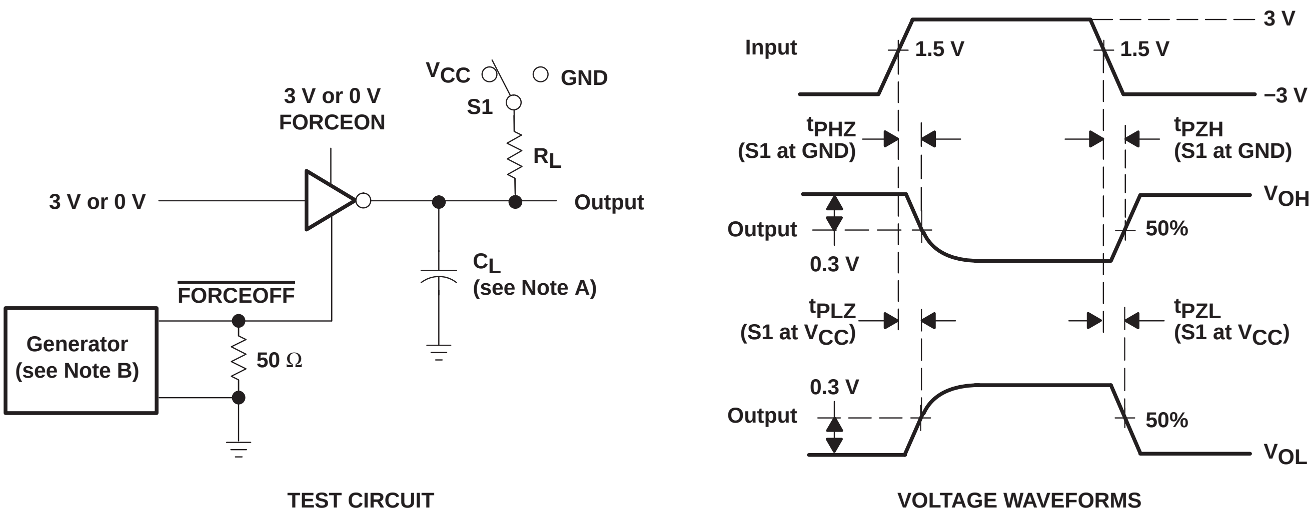
Figure 3. Driver Pulse Skew



NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \le 10$ ns, $t_f \le 10$ ns.

Figure 4. Receiver Propagation Delay Times

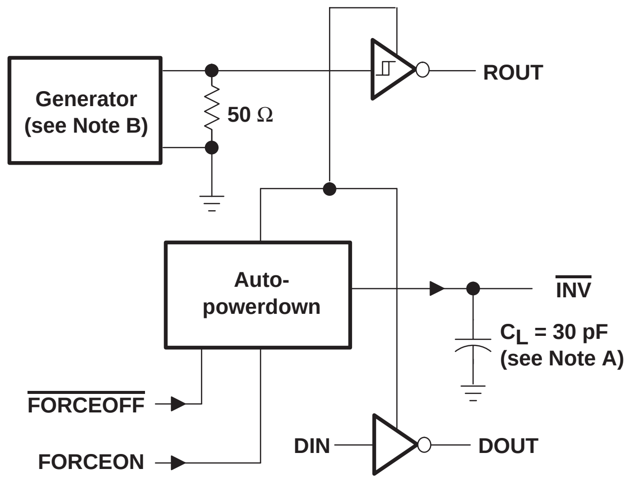
PARAMETER MEASUREMENT INFORMATION



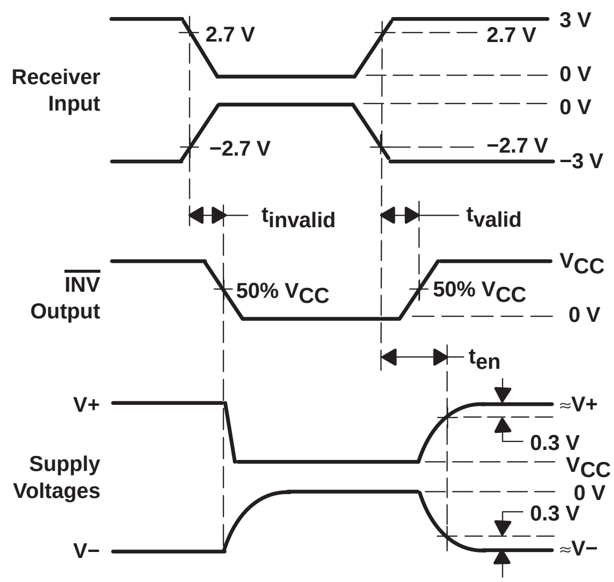
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, $t_r \leq$ 10 ns, $t_f \leq$ 10 ns.
C. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
D. t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 5. Receiver Enable and Disable Times

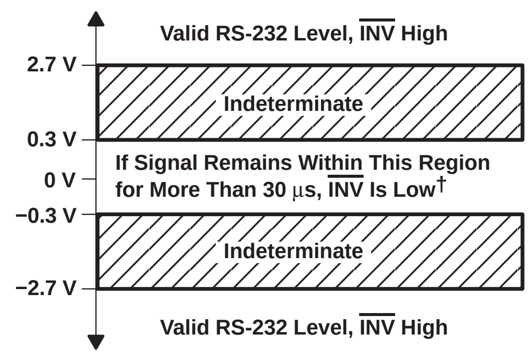
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

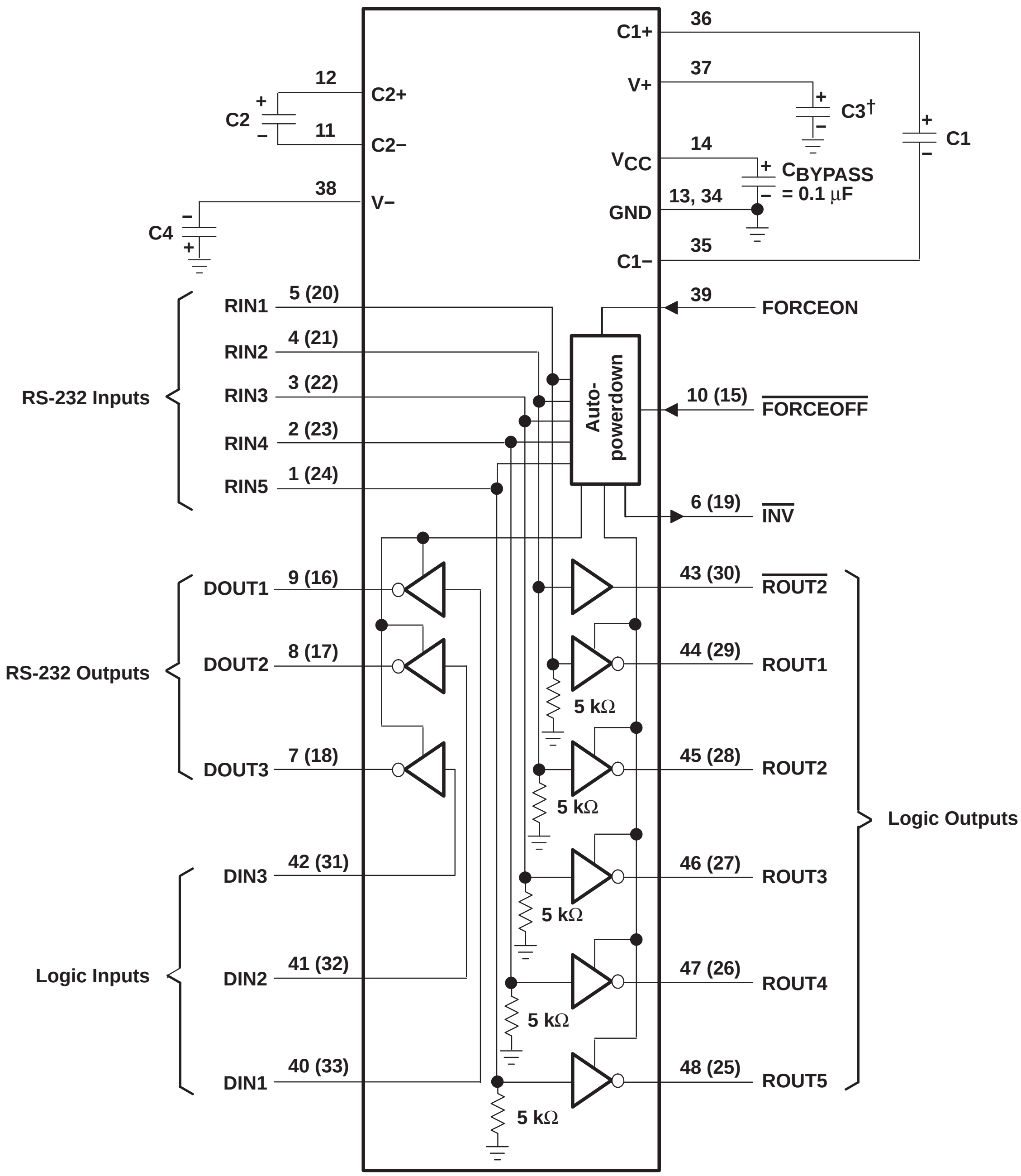


† Auto-powerdown disables drivers and reduces supply current to 1 µA.

NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 5 kbit/s, Z_O = 50 Ω, 50% duty cycle, $t_r \leq 10$ ns, $t_f \leq 10$ ns.

Figure 6. $\overline{\text{INV}}$ Propagation Delay Times and Supply Enabling Time

APPLICATION INFORMATION



† C3 can be connected to V_{CC} or GND.

NOTES: A. Resistor values shown are nominal.
B. Numbers in parentheses are for B section.

V_{CC} vs CAPACITOR VALUES

V_{CC}	C1	C2, C3, and C4
3.3 V ± 0.3 V	0.22 µF	0.22 µF
5 V ± 0.5 V	0.047 µF	0.33 µF
3 V to 5.5 V	0.22 µF	1 µF

Figure 7. Typical Operating Circuit and Capacitor Values

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65C23243DGGR	LIFEBUY	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C23243	
SN65C23243DLR	LIFEBUY	SSOP	DL	48	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C23243	
SN75C23243CDGGR	PREVIEW	TSSOP	DGG	48	2000	TBD	Call TI	Call TI			
SN75C23243CDLR	PREVIEW	SSOP	DL	48	1000	TBD	Call TI	Call TI			
SN75C23243DGGR	LIFEBUY	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C23243	
SN75C23243DLR	LIFEBUY	SSOP	DL	48	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C23243	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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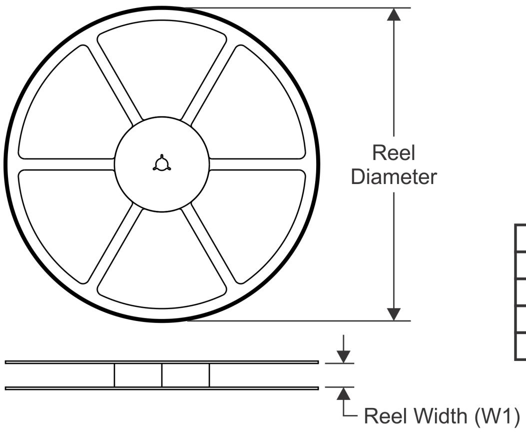
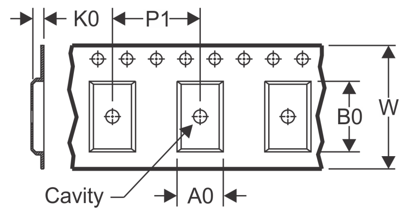
TAPE AND REEL INFORMATION

REEL DIMENSIONS

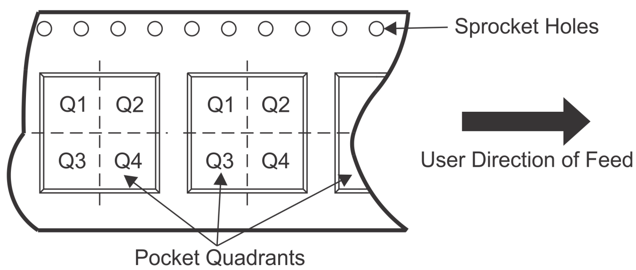


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

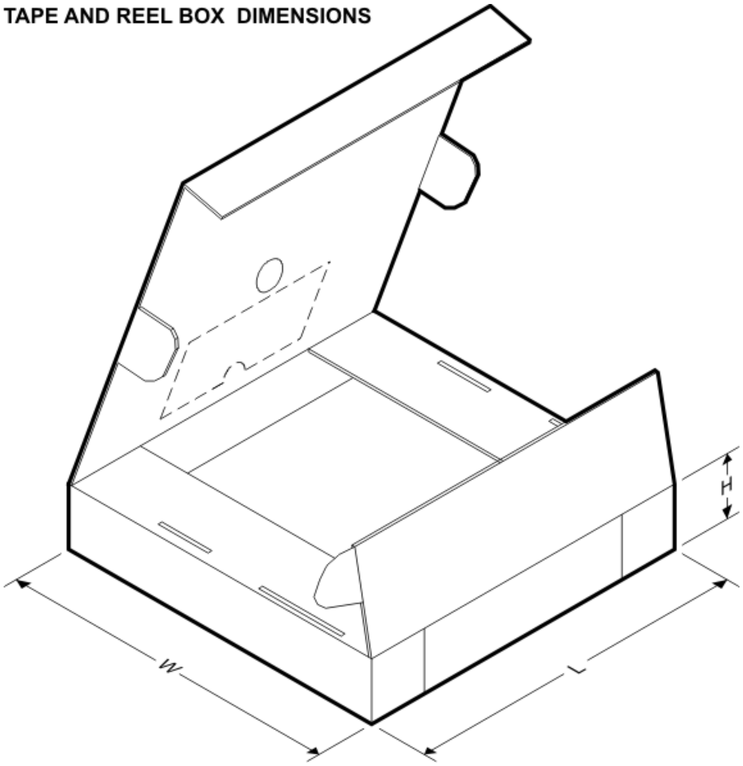
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65C23243DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN65C23243DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1
SN75C23243DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN75C23243DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

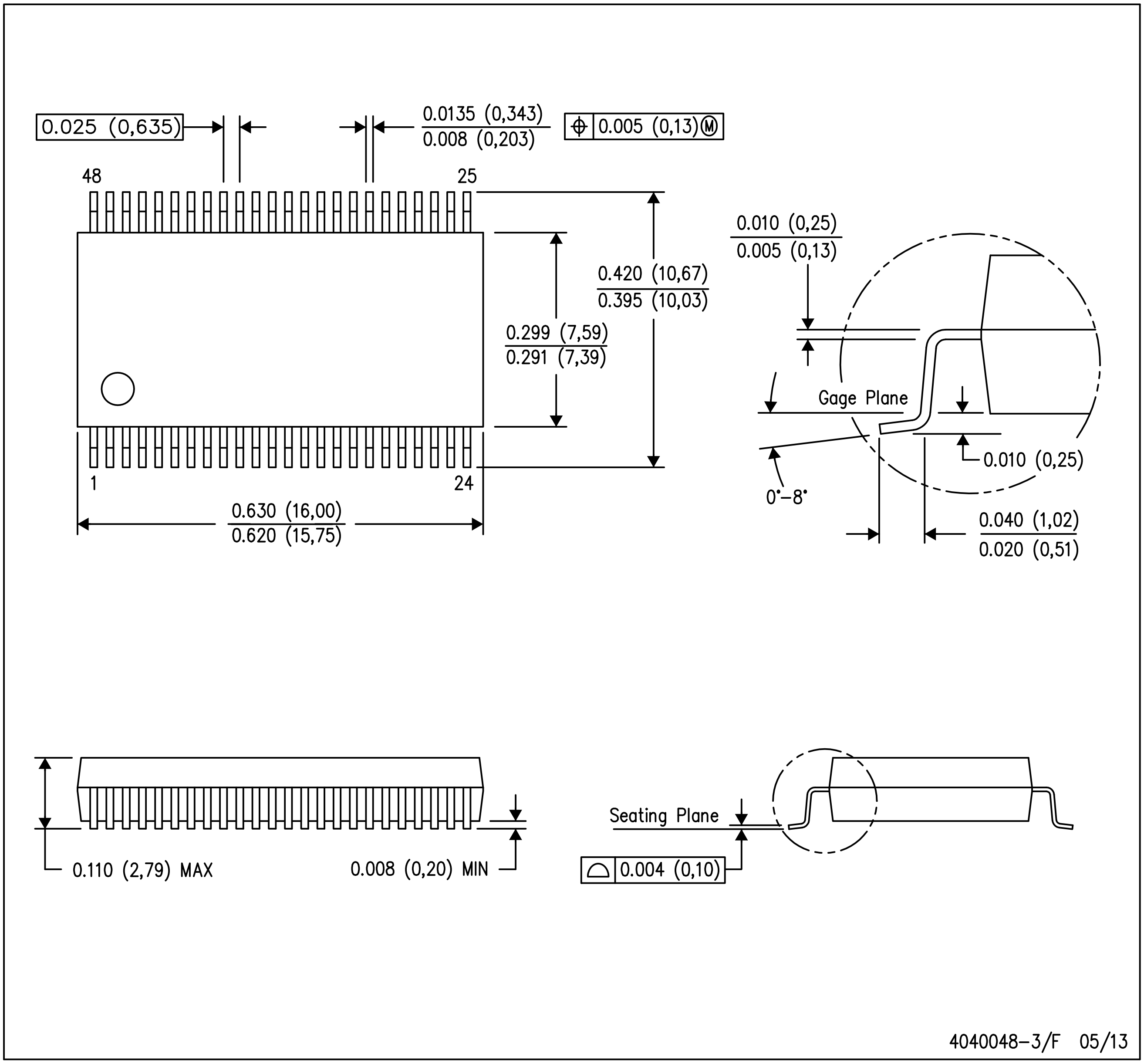
TAPE AND REEL BOX DIMENSIONS



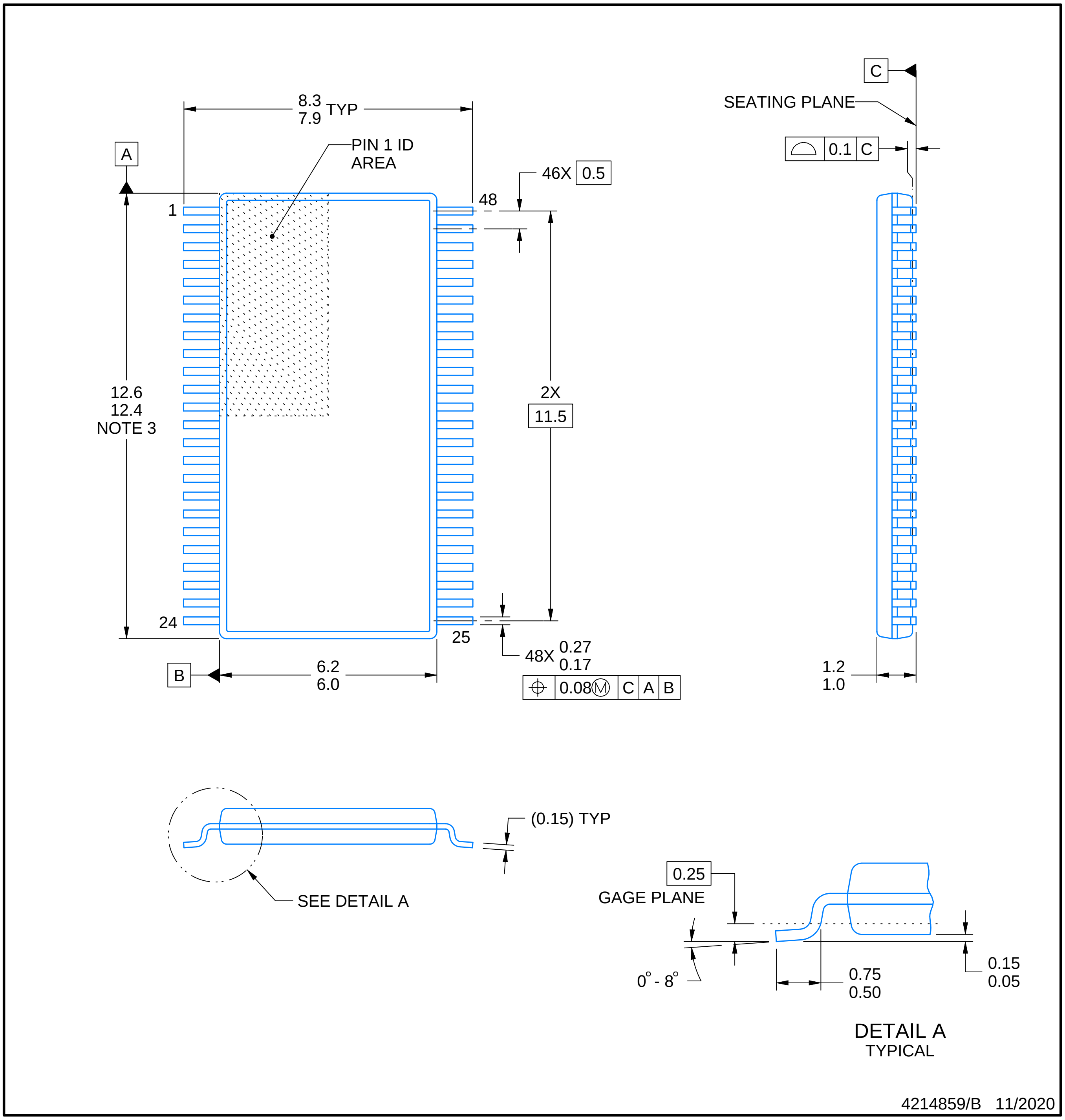
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65C23243DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN65C23243DLR	SSOP	DL	48	1000	367.0	367.0	55.0
SN75C23243DGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN75C23243DLR	SSOP	DL	48	1000	367.0	367.0	55.0

DL (R-PDSO-G48) PLASTIC SMALL-OUTLINE PACKAGE

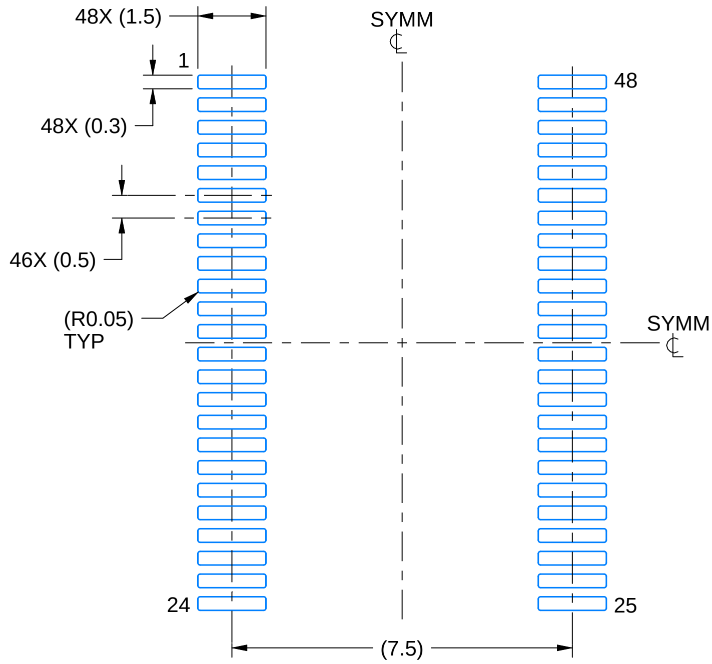


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO-118

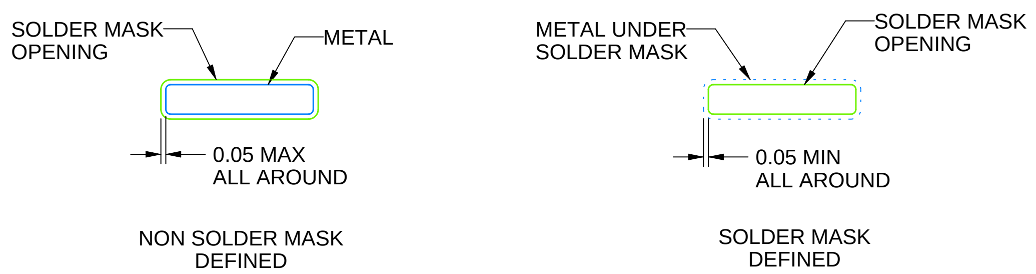


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
SCALE:6X

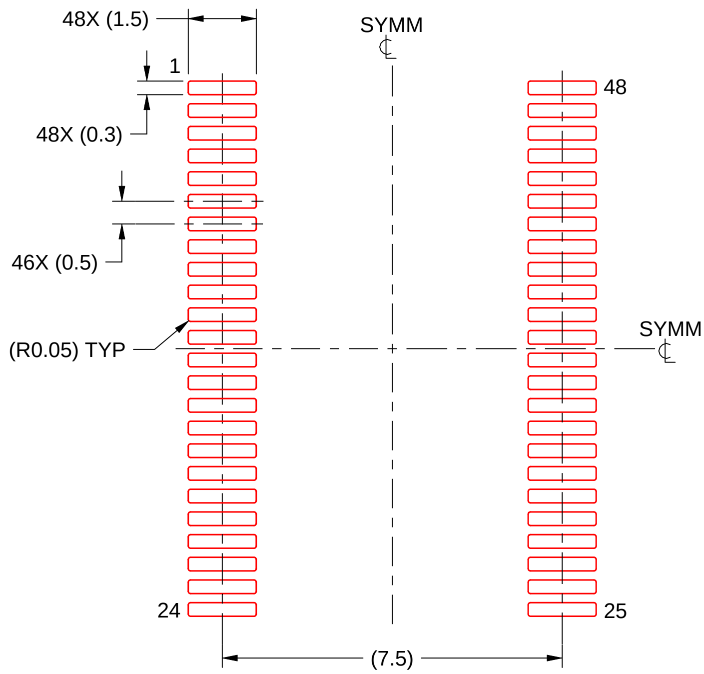


SOLDER MASK DETAILS

4214859/B 11/2020

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

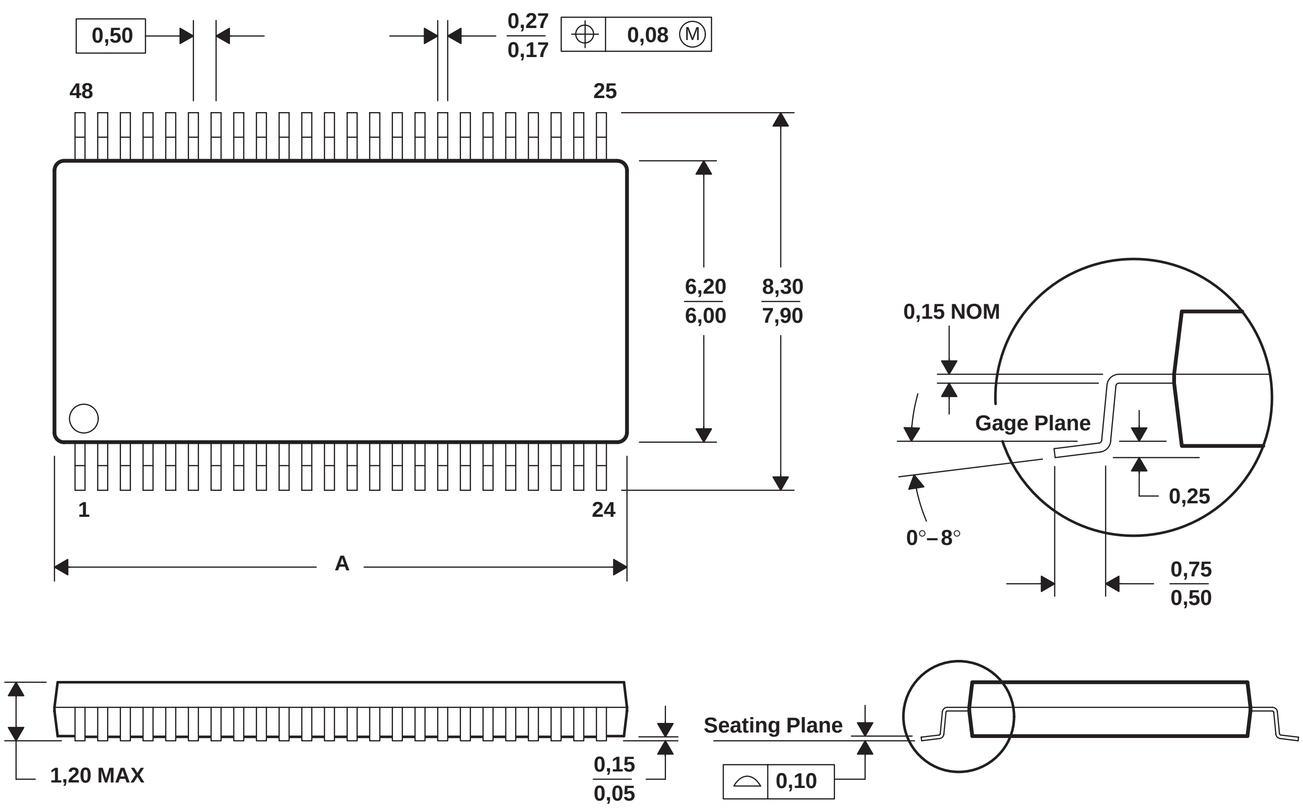
4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



PINS ** / DIM	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

4040078 / F 12/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153