# SN65HVD01 3.3V RS-485，具有灵活 I/O 电源和可选速度

## 1 特性

- 超过 TIA-485 标准的要求
- 针对数据和使能信号的 1.65V 至 3.6V 电源
- 针对总线信号的 3V 至 3.6V 电源
- SLR 引脚可选数据速率：250ksps 或 20Mbps
- 1/8 单位负载在一条总线上支持多达 256 个节点
- 小型 3mm x 3mm 小外形尺寸无引线 (SON) 封装
- 故障安全接收器（总线开路、总线短接、总线闲置）
- 运行温度范围：-40°C 至 125°C
- 总线引脚保护大于：
  - ±15kV 人体模型 (HBM) 保护
  - ±16kV IEC61000-4-2 接触放电
  - ±16kV IEC61000-4-2 空气放电
  - 4kV IEC61000-4-4 快速瞬态突发

## 2 应用范围

- 电信基础设施
- 高速数据链路
- 低压 µC 通信

## 3 说明

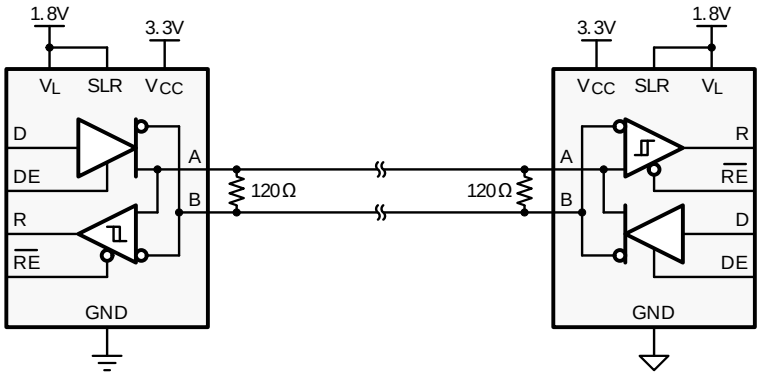
SN65HVD01 是一款低功耗，250ksps 或 20Mbps 数据速率可选 RS-485 收发器，此收发器采用 1.65V 至 3.6V 电源用于数据和使能信号，而针对总线信号采用一个 3.3V ± 10% 电源。 此器件被设计用于要求同步（并行收发器）信号时序的应用。 片上瞬态抑制保护此器件不受 IEC 61000 静电放电 (ESD) 和电快速瞬变 (EFT) 瞬态的影响而损坏。

此器件组合有一个差分驱动器和一个差分接收器，这些器件被内部连接以形成一个适用于半双工（两线制总线）通信的总线端口。 此器件特有一个宽共模电压范围，这使得此器件适合于长线缆运行上的多点应用。SN65HVD01 采用极小型，3mm x 3mm，SON 封装，运行温度范围 -40°C 至 125°C。

器件信息

| 订货编号 | 封装 | 封装尺寸 |
|---|---|---|
| SN65HVD01DRC | SON (10) | 3mm x 3mm |

典型应用



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- 已将说明文本从：3mm x 3mm，VQFN 封装更改为：3mm x 3mm，SON 封装 ..... 1
- Changed the ABSOLUTE MAXIMUM RATINGS for IEC 61000-4-2 ESD (Air-Gap Discharge) From MAX = ±15 To: MAX = ±16 ..... 5
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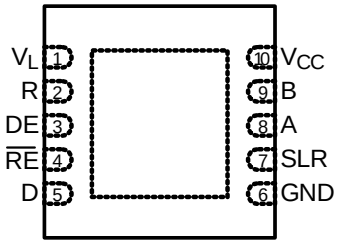
# 5 Pin Configuration and Functions

**DRC 10 PIN**
**(TOP VIEW)**




**Pin Functions**

| NAME | NO. | I/O | DESCRIPTION |
|---|---|---|---|
| $V_L$ | 1 | Logic Supply | 1.65 V to 3.6 V supply for logic I/O signals R, $\overline{RE}$, D, DE, and SLR) |
| R | 2 | Digital Output | Receive data output |
| DE | 3 | Digital Input | Driver enable input |
| $\overline{RE}$ | 4 | Digital Input | Receiver enable input |
| D | 5 | Digital Input | Transmission data input |
| GND | 6 | Reference Potential | Local device ground |
| SLR | 7 | Digital Input | Slew rate select: Low = 20 Mbps, High = 250 kbps. Defaults to 20 Mbps if SLR is left floating |
| A | 8 | Bus I/O | Digital bus I/O, A |
| B | 9 | Bus I/O | Digital bus I/O, B |
| $V_{CC}$ | 10 | Bus Supply | 3 V to 3.6 V supply for A and B bus lines |

# 6 Specifications

## 6.1 Absolute Maximum Ratings(1)

| | VALUE | | UNIT |
|---|---|---|---|
| | MIN | MAX | |
| Control supply voltage, $V_L$ | –0.5 | 4 | V |
| Bus supply voltage, $V_{CC}$ | –0.5 | 5.5 | V |
| Voltage range at A or B Inputs | –13 | 16.5 | V |
| Input voltage range at any logic terminal | –0.3 | 5.7 | V |
| Voltage input range, transient pulse, A and B, through 100Ω | –100 | 100 | V |
| Receiver output current | –12 | 12 | mA |
| Junction temperature, $T_J$ | | 170 | °C |
| Continuous total power dissipation | See the Thermal Information table | | |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 Handling Ratings

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $T_{STG}$ | Storage temperature range | –65 | 150 | °C |
| $V_{ESD}$ | IEC 60749-26 ESD (Human Body Model), bus terminals and GND | | ±15 | kV |
| | IEC 61000-4-2 ESD (Air-Gap Discharge), bus terminals and GND (1) | | ±16 | kV |
| | IEC 61000-4-2 ESD (Contact Discharge), bus terminals and GND | | ±16 | kV |
| | IEC 61000-4-4 EFT (Fast transient or burst) bus terminals and GND | | ±4 | kV |
| | JEDEC Standard 22, Test Method A114 (Human Body Model), all terminals | | ±8 | kV |
| | JEDEC Standard 22, Test Method C101 (Charged Device Model), all terminals | | ±1.5 | kV |

(1) As stated in the IEC 61000-4-2 standard, contact discharge is the preferred transient protection test method. Although IEC air-gap testing is less repeatable than contact testing, air discharge protection levels are inferred from the contact discharge test results.

## 6.3 Recommended Operating Conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_L$ | Control supply voltage | | 1.65 | | 3.6 | V |
| $V_{CC}$ | Bus supply voltage | | 3 | 3.3 | 3.6 | V |
| $V_I$ | Input voltage at any bus terminal (separately or common mode) (1) | | –7 | | 12 | V |
| $V_{IH}$ | High-level input voltage (Driver, driver enable, receiver enable inputs, and slew rate select) | | 0.7×$V_L$ | | $V_L$ | V |
| $V_{IL}$ | Low-level input voltage (Driver, driver enable, receiver enable inputs, and slew rate select) | | 0 | | 0.3×$V_L$ | V |
| $V_{ID}$ | Differential input voltage | | –12 | | 12 | V |
| $I_O$ | Output current | Driver | –80 | | 80 | mA |
| | | Receiver | –2 | | 2 | mA |
| $R_L$ | Differential load resistance | | 54 | 60 | | Ω |
| $C_L$ | Differential load capacitance | | | 50 | | pF |
| $1/t_{UI}$ | Signaling rate | SLR = '0' | | | 20 | Mbps |
| | | SLR = '1' | | | 250 | kbps |
| $T_A$ (2) | Operating free-air temperature Thermal Information | | –40 | | 125 | °C |

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.
(2) Operation is specified for internal (junction) temperatures up to 150°C. Self-heating due to internal power dissipation should be considered for each application. Maximum junction temperature is internally limited by the thermal shut-down (TSD) circuit which disables the driver outputs when the junction temperature reaches 170°C.

## 6.4 Thermal Information

| PARAMETER(1) | | SON (DRC) | UNIT |
|---|---|---|---|
| $\Theta_{JA}$ | Junction-to-Ambient Thermal Resistance | 41.4 | °C/ W |
| $\Theta_{JC(top)}$ | Junction-to-Case(top) Thermal Resistance | 48.7 | |
| $\Theta_{JB}$ | Junction-to-Board Thermal Resistance | 18.8 | |
| $\Psi_{JT}$ | Junction-to-Top characterization parameter | 0.6 | |
| $\Psi_{JB}$ | Junction-to-Board characterization parameter | 19 | |
| $\Theta_{JC(bottom)}$ | Junction-to-Case(bottom) Thermal Resistance | 3.7 | |
| $T_{TSD}$ | Thermal Shut-down junction temperature | 170 | °C |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953

## 6.5 Dissipation Ratings

| PARAMETER | | | TEST CONDITIONS | | VALUE | UNIT |
|---|---|---|---|---|---|---|
| PD | Power Dissipation driver and receiver enabled, $V_{CC}$ = $V_L$ = 3.6 V, $T_J$ = 150°C, 50% duty cycle square-wave signal at signaling rate | Unterminated | $R_L$ = 300 Ω, $C_L$ = 50 pF (driver) | 250 kbps | 125 | mW |
| | | | | 20 Mbps | 175 | |
| | | RS-422 load | $R_L$ = 100 Ω, $C_L$ = 50 pF (driver) | 250 kbps | 165 | mW |
| | | | | 20 Mbps | 215 | |
| | | RS-485 load | $R_L$ = 54 Ω, $C_L$ = 50 pF (driver) | 250 kbps | 200 | mW |
| | | | | 20 Mbps | 250 | |

## 6.6 Electrical Characteristics

over recommended operating range (unless otherwise specified)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $\|V_{OD}\|$ | Driver differential output voltage magnitude | $R_L$ = 60 Ω, 375 Ω on each output to –7 V to 12 V | | See Figure 9 | 1.5 | 2 | | V |
| | | $R_L$ = 54 Ω (RS-485) | | | 1.5 | 2 | | V |
| | | $R_L$ = 100 Ω (RS-422) $T_J \geq 0°C$, $V_{CC} \geq 3.2V$ | | | 2 | | | V |
| $\Delta\|V_{OD}\|$ | Change in magnitude of driver differential output voltage | $R_L$ = 54 Ω, $C_L$ = 50 pF | | | –50 | 0 | 50 | mV |
| $V_{OC(SS)}$ | Steady-state common-mode output voltage | Center of two 27-Ω load resistors | | See Figure 10 | 1 | $V_{CC}/2$ | 3 | V |
| $\Delta V_{OC}$ | Change in differential driver output common-mode voltage | | | | –50 | 0 | 50 | mV |
| $V_{OC(PP)}$ | Peak-to-peak driver common-mode output voltage | | | | | 500 | | mV |
| $C_{OD}$ | Differential output capacitance | | | | | 15 | | pF |
| $V_{IT+}$ | Positive-going receiver differential input voltage threshold | | | | See (1) | –60 | –20 | mV |
| $V_{IT-}$ | Negative-going receiver differential input voltage threshold | | | | –200 | –130 | See (1) | mV |
| $V_{HYS}$ | Receiver differential input voltage threshold hysteresis ($V_{IT+} – V_{IT-}$) | | | | 40 | 70 | | mV |
| $V_{OH}$ | Receiver high-level output voltage | $V_L$ = 1.65 V, $I_{OH}$ = -2 mA | | | 1.3 | 1.45 | | V |
| | | $V_L$ = 3 V, $I_{OH}$ = -2 mA | | | 2.8 | 2.9 | | |
| $V_{OL}$ | Receiver low-level output voltage | $V_L$ = 1.65 V, $I_{OL}$ = 2 mA | | | | 0.2 | 0.35 | V |
| | | $V_L$ = 3 V, $I_{OL}$ = 2 mA | | | | 0.1 | 0.2 | |
| $I_I$ | Driver input, driver enable, and receiver enable input current | | | | –2 | | 2 | µA |
| $I_{OZ}$ | Receiver output high-impedance current | $V_O$ = 0 V or $V_L$, $\overline{RE}$ at $V_L$ | | | –1 | | 1 | µA |
| $I_{OS}$ | Driver short-circuit output current | | | | –150 | | 150 | mA |
| $I_I$ | Bus input current (disabled driver) | $V_L$ = 1.8 V, $V_{CC}$ = 3.3 V, DE at 0 V | $V_I$ = 12 V | | | 85 | 125 | µA |
| | | | $V_I$ = –7 V | | –100 | –60 | | µA |
| $I_{CC}$ | Supply current (quiescent) | Driver and Receiver enabled | DE=$V_L$, RE = GND, No load | | | 750 | 1100 | µA |
| | | | | $T_J \leq 85°C$ | | | 1000 | µA |
| | | Driver enabled, receiver disabled | DE=$V_{CC}$, $\overline{RE}$ = $V_L$, No load | | | 350 | 650 | µA |
| | | Driver disabled, receiver enabled | DE=GND, $\overline{RE}$ = GND, No load | | | 650 | 800 | µA |
| | | Driver and receiver disabled | DE=GND, $\overline{RE}$ = $V_L$, No load | | | 0.1 | 5 | µA |
| | Supply current (dynamic) | See the Typical Characteristics section | | | | | | |

(1) Under any specific conditions, $V_{IT+}$ is specified to be at least $V_{HYS}$ higher than $V_{IT-}$.

## 6.7 Switching Characteristics

over recommended operating conditions

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **DRIVER, SLR = '1', 250 kbps, bit time ≥ 4 µs** | | | | | | | |
| $t_r$, $t_f$ | Driver differential output rise/fall time | $R_L$ = 54 Ω, $C_L$ = 50 pF | See Figure 11 | 0.4 | 0.8 | 1.2 | µs |
| $t_{PHL}$, $t_{PLH}$ | Driver propagation delay | | | 0.4 | 0.8 | 1.2 | µs |
| $t_{SK(P)}$ | Driver pulse skew, $\|t_{PHL} - t_{PLH}\|$ | | | | | 0.2 | µs |
| $t_{PHZ}$, $t_{PLZ}$ | Driver disable time | | See Figure 12 and Figure 13 | | 0.025 | 0.1 | µs |
| $t_{PZH}$, $t_{PZL}$ | Driver enable time | Receiver enabled | | | 0.6 | 1 | µs |
| | | Receiver disabled | | | 3.5 | 8 | µs |
| **DRIVER, SLR = '0', 20 Mbps, bit time ≥ 50 ns** | | | | | | | |
| $t_r$, $t_f$ | Driver differential output rise/fall time | $R_L$ = 54 Ω, $C_L$ = 50 pF | See Figure 11 | 5 | 10 | 15 | ns |
| $t_{PHL}$, $t_{PLH}$ | Driver propagation delay | | | 6 | 15 | 25 | ns |
| $t_{SK(P)}$ | Driver pulse skew, $\|t_{PHL} - t_{PLH}\|$ | | | | | 4 | ns |
| $t_{PHZ}$, $t_{PLZ}$ | Driver disable time | | See Figure 12 and Figure 13 | | 20 | 35 | ns |
| $t_{PZH}$, $t_{PZL}$ | Driver enable time | Receiver enabled | | | 14 | 30 | ns |
| | | Receiver disabled | | | 3 | 7 | µs |
| **RECEIVER, SLR = 'X'** | | | | | | | |
| $t_r$, $t_f$ | Receiver output rise/fall time | $C_L$ = 15 pF | See Figure 14 | | 5 | 15 | ns |
| $t_{PHL}$, $t_{PLH}$ | Receiver propagation delay time | | | 30 | 60 | 90 | ns |
| $t_{SK(P)}$ | Receiver pulse skew, $\|t_{PHL} - t_{PLH}\|$ | | | | | 15 | ns |
| $t_{PLZ}$, $t_{PHZ}$ | Receiver disable time | | | | 10 | 20 | ns |
| $t_{pZL(1)}$, $t_{PZH(1)}$ $t_{PZL(2)}$, $t_{PZH(2)}$ | Receiver enable time | Driver enabled | See Figure 15 | | 15 | 80 | ns |
| | | Driver disabled | See Figure 16 | | 3 | 8 | µs |

## 6.8 Typical Characteristics

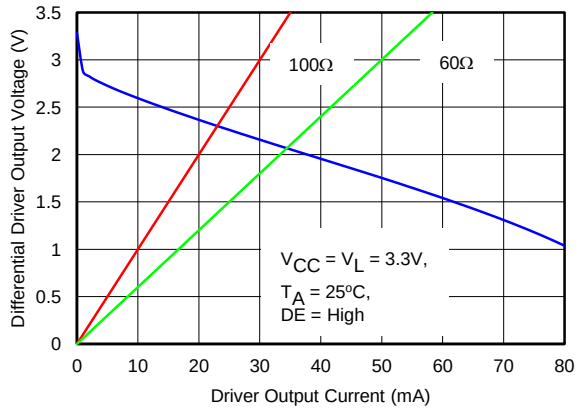



**Figure 1. Differential Driver Output Voltage vs Driver Output Current**

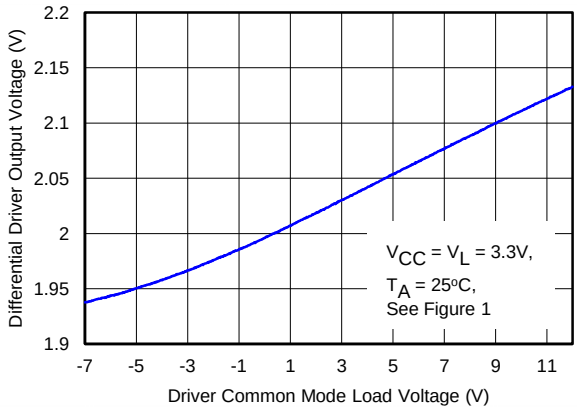



**Figure 2. Differential Driver Output Voltage vs Driver Common Mode Load Voltage**

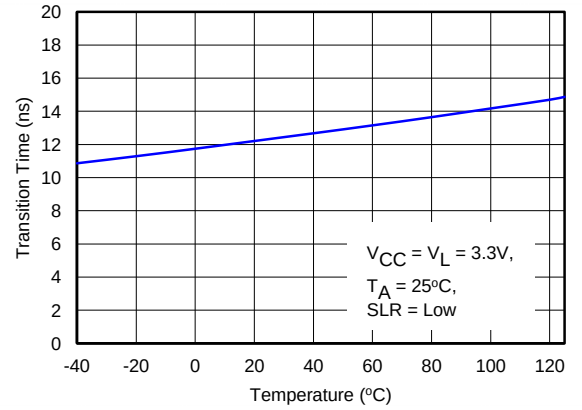



**Figure 3. Transition Time vs Temperature**

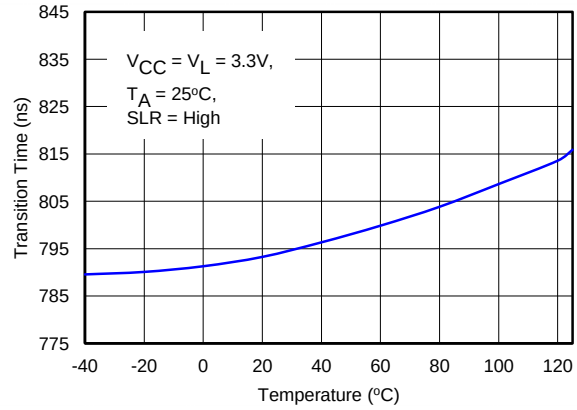



**Figure 4. Transition Time vs Temperature**

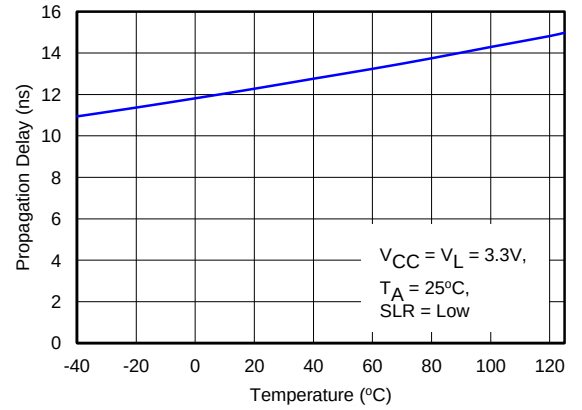



**Figure 5. Propagation Delay vs Temperature**

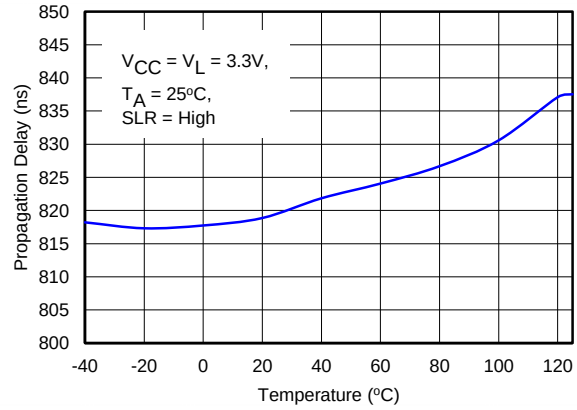



**Figure 6. Propagation Delay vs Temperature**

## Typical Characteristics (continued)

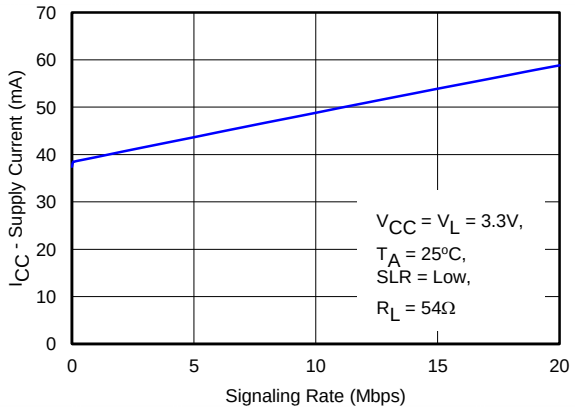



**Figure 7. Supply Current vs Signaling Rate**

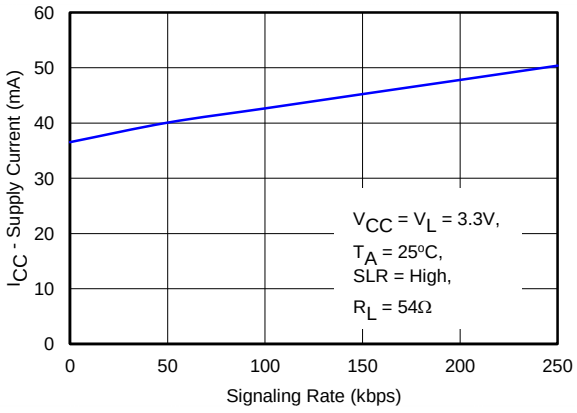



**Figure 8. Supply Current vs Signaling Rate**

## 7 Parameter Measurement Information

Input generator rate is 100 kbps, 50% duty cycle, rise and fall times less than 6 nsec.

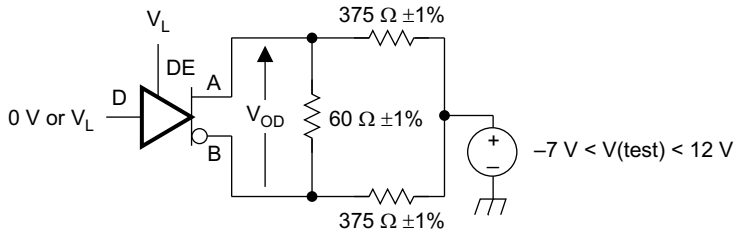



**Figure 9. Measurement of Driver Differential Output Voltage with Common-Mode Load**

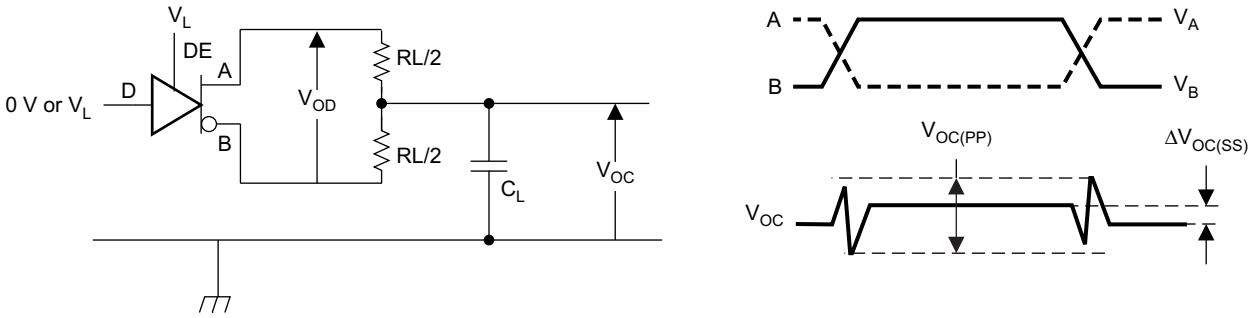



**Figure 10. Measurement of Driver Differential and Common-Mode Output with RS-485 Load**

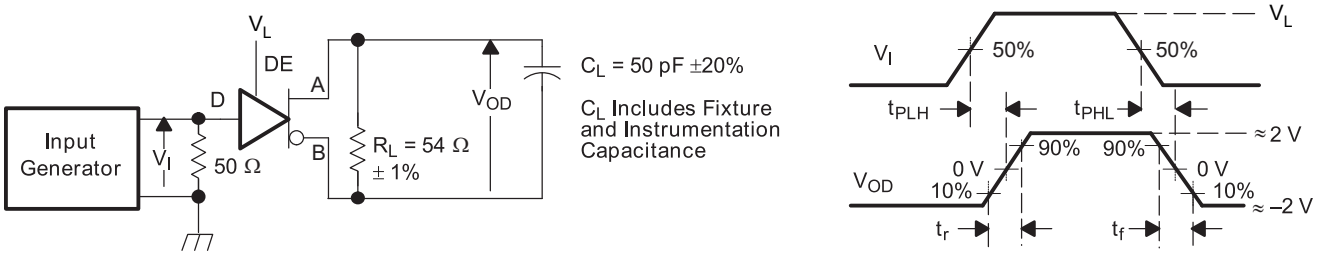
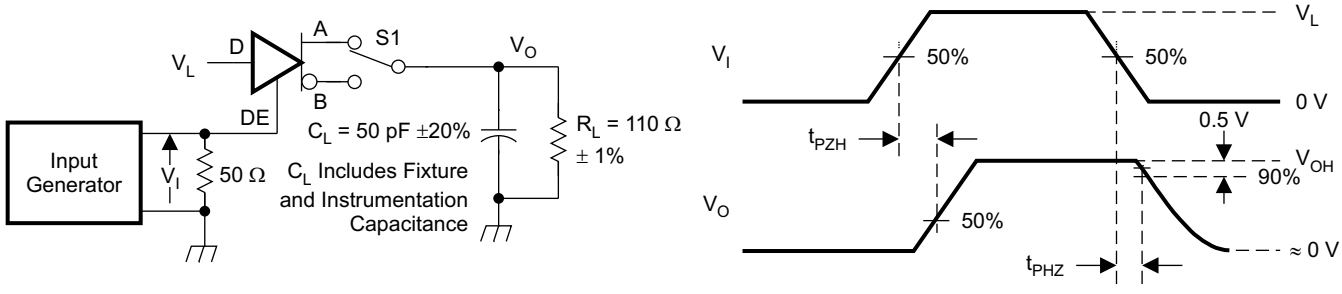


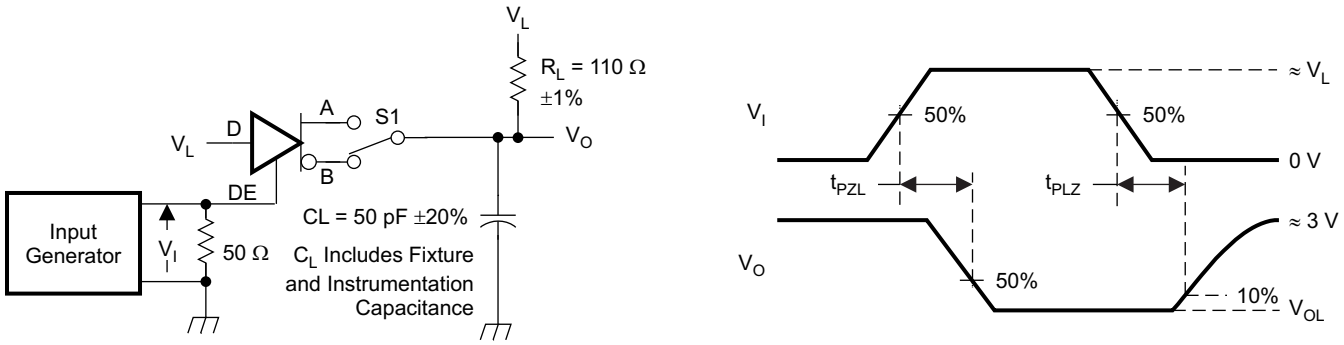

**Figure 11. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays**




D at $V_L$ to test non-inverting output, D at 0 V to test inverting output.

**Figure 12. Measurement of Driver Enable and Disable Times with Active High Output and Pull-Down Load**

## Parameter Measurement Information (continued)




D at 0V to test non-inverting output, D at $V_L$ to test inverting output.

**Figure 13. Measurement of Driver Enable and Disable Times with Active Low Output and Pull-Up Load**

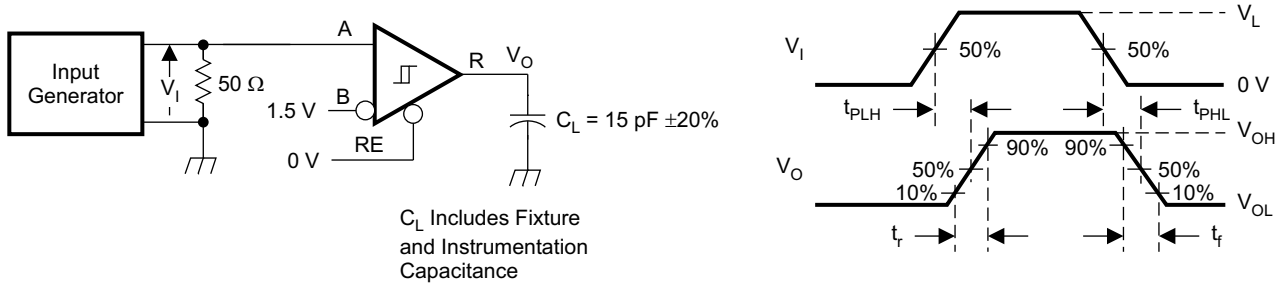



**Figure 14. Measurement of Receiver Output Rise and Fall Times and Propagation Delays**

## Parameter Measurement Information (continued)

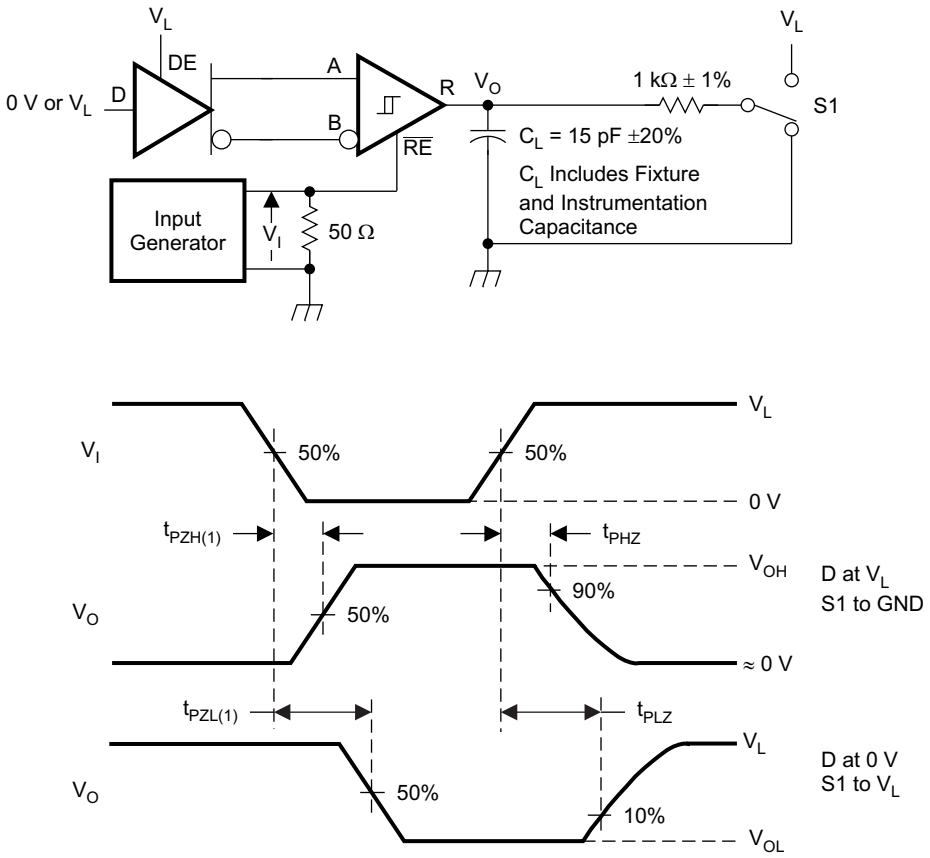



**Figure 15. Measurement of Receiver Enable/Disable Times with Driver Enabled**

## Parameter Measurement Information (continued)

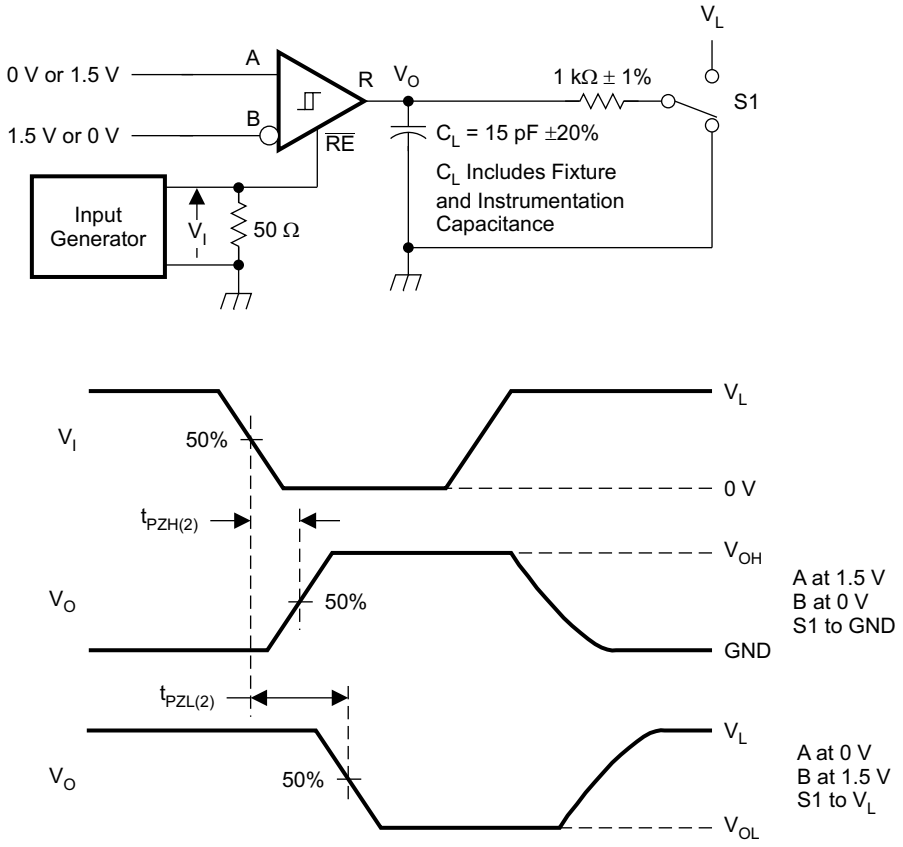



**Figure 16. Measurement of Receiver Enable Times with Driver Disabled**

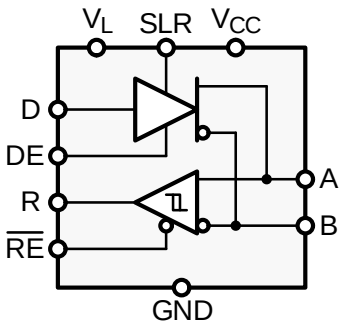
# 8 Detailed Description

## 8.1 Overview

The SN65HVD01 is a low-power, half-duplex RS-485 transceiver whose maximum data rate can be set to either 250 kbps or 20 Mbps via a selection terminal, SLR.

The device possesses two power supply inputs, one for logic control functions, $V_L$, and the other for the bus supply, $V_{CC}$. $V_L$ can range from 1.65 V minimum up to 3.6 V maximum and allows for the direct interface to low-voltage FPGAs and micro controllers. $V_{CC}$ requires a supply between 3 V to 3.6 V to assure sufficient output drive capability across a wide common-mode range.

## 8.2 Functional Block Diagram




## 8.3 Feature Description

Internal ESD protection circuits protect the transceiver against Electrostatic discharges (ESD) according to IEC61000-4-2 of up to ±16 kV, and against electrical fast transients (EFT) according to IEC61000-4-4 of up to ±4 kV.

The SN65HVD01 provides internal biasing of the receiver input thresholds in combination with large input-threshold hysteresis. At a positive input threshold of $V_{IT+}$ = –60 mV and an input hysteresis of VHYS = 70 mV, the receiver output remains logic high even in the presence of 130 $mV_{PK}$ differential noise without the need for external failsafe biasing resistors.

Device operation is specified over a wide temperature range from –40°C to 125°C.

## 8.4 Device Functional Modes

When driver enable terminal, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case the differential output voltage defined as $V_{OD} = V_A – V_B$ is positive. When D is low, the output states reverse, B turns high, A becomes low, and $V_{OD}$ is negative.

When DE is low, both outputs turn high-impedance. In this condition, the logic state at D is irrelevant. The DE terminal has an internal pull-down resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D terminal has an internal pull-up resistor to $V_L$, thus, when left open while the driver is enabled, output A turns high and B turns low.

**Table 1. Driver Function Table**

| INPUT | ENABLE | OUTPUTS | | FUNCTION |
|---|---|---|---|---|
| D | DE | A | B | |
| H | H | H | L | Actively drive bus High |
| L | H | L | H | Actively drive bus Low |
| X | L | Z | Z | Driver disabled |
| X | OPEN | Z | Z | Driver disabled by default |
| OPEN | H | H | L | Actively drive bus High by default |

When the receiver enable terminal, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A - V_B$ is positive and higher than the positive input threshold, $V_{IT+}$, the receiver output, R, turns high. When $V_{ID}$ is negative and less than the negative and lower than the negative input threshold, $V_{IT-}$, the receiver output, R, turns low. If $V_{ID}$ is between $V_{IT+}$ and $V_{IT-}$ the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of $V_{ID}$ are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

**Table 2. Receiver Function Table**

| DIFFERENTIAL INPUT | ENABLE | OUTPUT | FUNCTION |
|---|---|---|---|
| $V_{ID} = V_A - V_B$ | $\overline{RE}$ | R | |
| $V_{IT+} < V_{ID}$ | L | H | Receive valid bus High |
| $V_{IT-} < V_{ID} < V_{IT+}$ | L | ? | Indeterminate bus state |
| $V_{ID} < V_{IT-}$ | L | L | Receive valid bus Low |
| X | H | Z | Receiver disabled |
| X | OPEN | Z | Receiver disabled by default |
| Open-circuit bus | L | H | Fail-safe high output |
| Short-circuit bus | L | H | Fail-safe high output |
| Idle (terminated) bus | L | H | Fail-safe high output |

Connecting SLR to $V_L$ limits the maximum data rate to 250 kbps and increases the driver rise and fall times to 800 ns. Connecting SLR to GND increases the upper data rate limit to 20 Mbps and reduces the driver rise and fall times to 10 ns.

**Table 3. SLR-Terminal Configuration**

| SLR-INPUT | DATA RATE | TYP tr / tf |
|---|---|---|
| $V_L$ | 250 kbps | 800 ns |
| GND or OPEN | 20 Mbps | 10 ns |

### 8.4.1 Equivalent Input and Output Schematic Diagrams

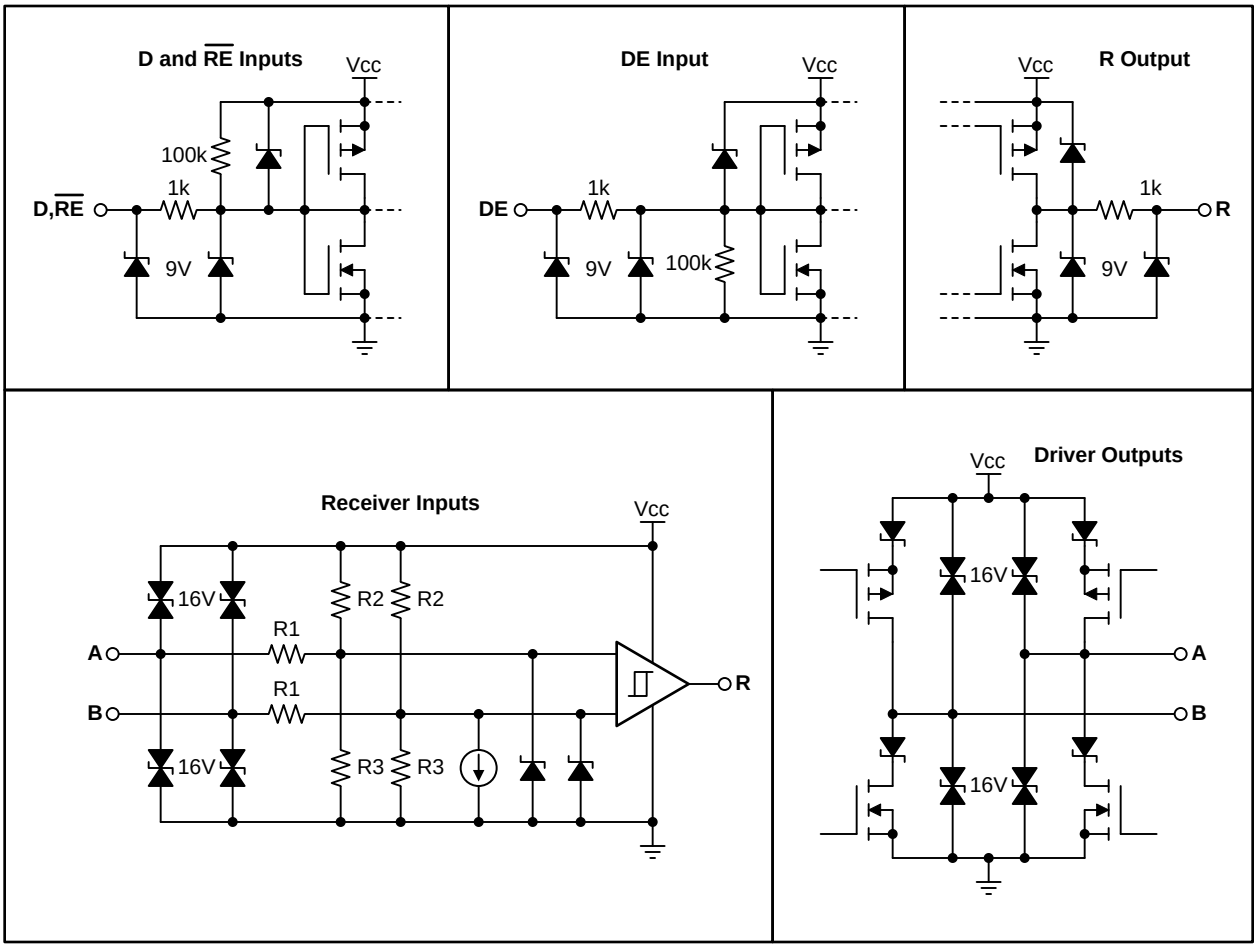
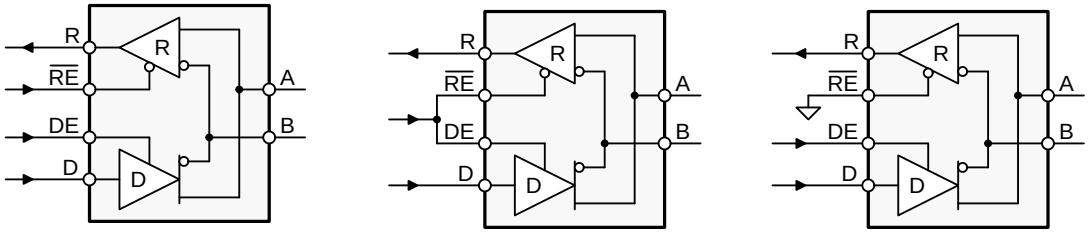



**Figure 17. Equivalent Input and Output Schematic Diagrams**

# 9 Applications and Implementation

## 9.1 Application Information

The SN65HVD01 is a half-duplex RS-485 transceiver commonly used for asynchronous data transmissions. The driver and receiver enable terminals allow for the configuration of different operating modes.




***a)*** *Independent driver and receiver enable signals*

***b)*** *Combined enable signals for use as directional control pin*

***c)*** *Receiver always on*

**Figure 18. SN65HVD01 Transceiver Configurations**

Using independent enable lines provides the most flexible control as it allows for the driver and the receiver to be turned on and off individually. While this configuration requires two control lines, it allows for selective listening into the bus traffic, whether the driver is transmitting data or not.

Combining the enable signals simplifies the interface to the controller by forming a single, direction-control signal. Thus, when the direction- control line is high, the transceiver is configured as a driver, while for a low the device operates as a receiver.

Tying the receiver-enable to ground and controlling only the driver-enable input, also uses one control line only. In this configuration, a node not only receives the data from the bus but also the data it sends and thus can verify that the correct data have been transmitted.

## 9.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, $R_T$, whose value matches the characteristic impedance, $Z_0$, of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

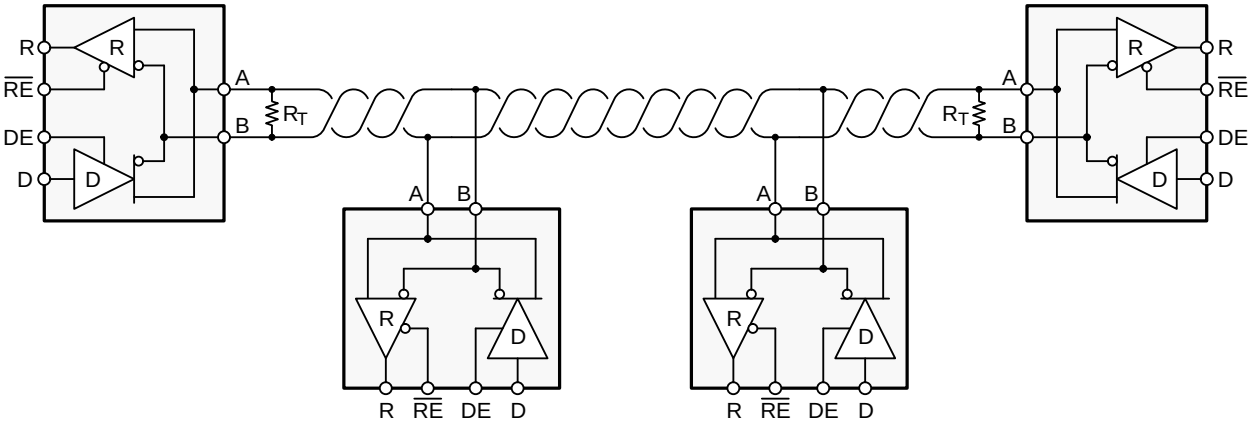



**Figure 19. Typical RS-485 Network with SN65HVD01 Transceivers**

### 9.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

## Typical Application (continued)

### 9.2.1.1 Data Rate and Bus Length

The maximum bus length is limited by the transmission line losses and the signal jitter at a given data rate. Because data reliability sharply decreases for a jitter of 10% or more of the baud period, Figure 20 shows the cable length versus data rate characteristic of a conventional RS-485 cable for signal jitter of 10%.

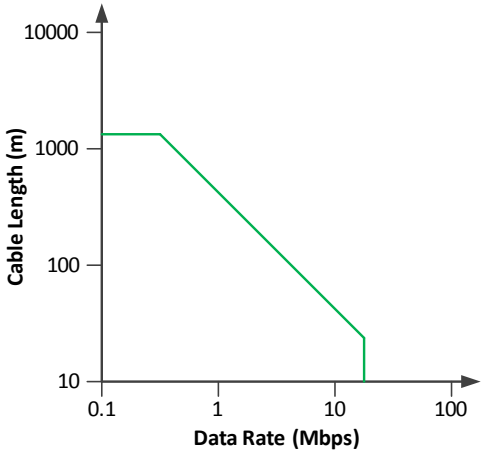



**Figure 20. Cable Length vs Data Rate**

### 9.2.1.2 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to drive 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12kΩ. Because the SN65HVD01 is a 1/8 UL transceiver, it is possible to connect up to 256 devices to the bus.

### 9.2.2 Detailed Design Procedure

In order to protect bus nodes against high-energy transients, the implementation of external transient protection devices is therefore necessary. Figure 21 suggests a protection circuit against 10 kV ESD, 4 kV EFT, and 1 kV surge transients.

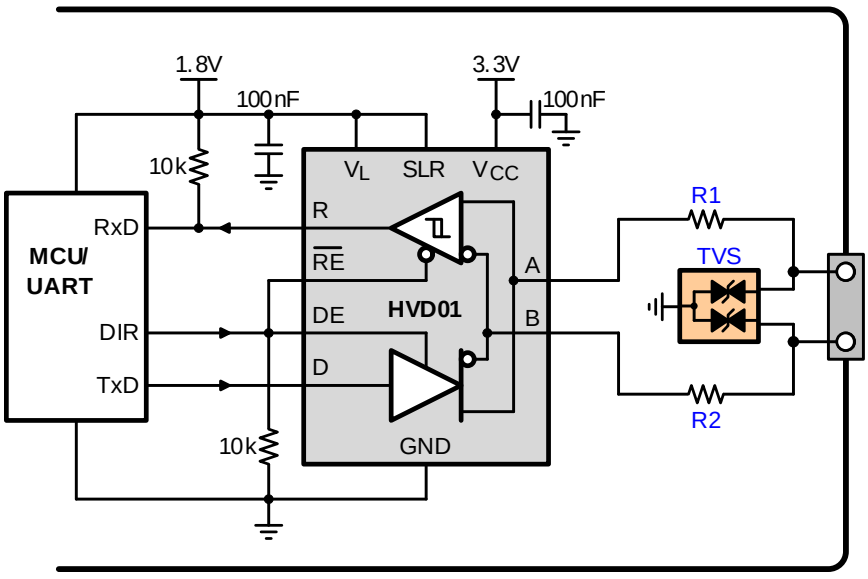


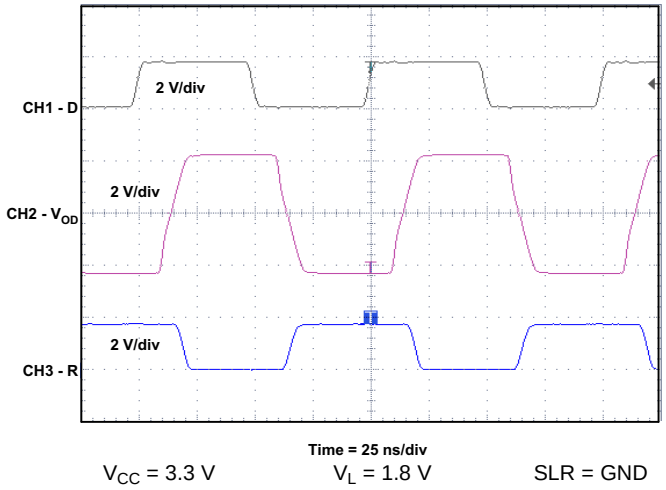

**Figure 21. Transient Protection Against ESD, EFT, and Surge Transients**

## Typical Application (continued)

**Table 4. Recommended Materials**

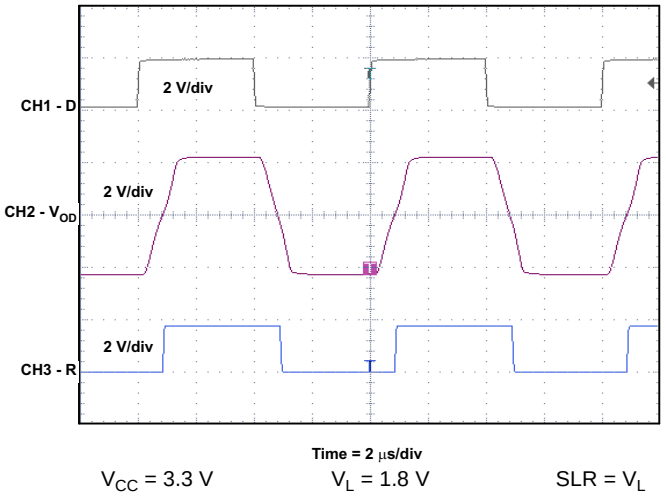
| Device | Function | Order Number |
|---|---|---|
| XCVR | 3.3V, 250kbps RS-485 Transceiver | SN65HVD01D |
| R1,R2 | 10Ω, Pulse-Proof Thick-Film Resistor | CRCW0603010RJNEAHP |
| TVS | Bidirectional 400W Transient Suppressor | CDSOT23-SM712 |

### 9.2.3 Application Performance Curves




$V_{CC}$ = 3.3 V $V_L$ = 1.8 V SLR = GND

**Figure 22. $V_{OD}$ and R Transient Response - 20 Mbps**




$V_{CC}$ = 3.3 V $V_L$ = 1.8 V SLR = $V_L$

**Figure 23. $V_{OD}$ and R Transient Response - 250 kbps**

# 10 Power Supply Recommendations

To assure reliable operation at all data rates and supply voltages, each supply should be buffered with a 100 nF ceramic capacitor located as close to the supply terminals as possible. Linear voltage regulators for the 1.8 V logic and 3.3 V bus supplies are TPS76318 and TPS76333 respectively.

# 11 Layout

On-chip IEC-ESD protection is good for laboratory and portable equipment but never sufficient for EFT and surge transients occurring in industrial environments. Therefore robust and reliable bus node design requires the use of external transient protection devices.

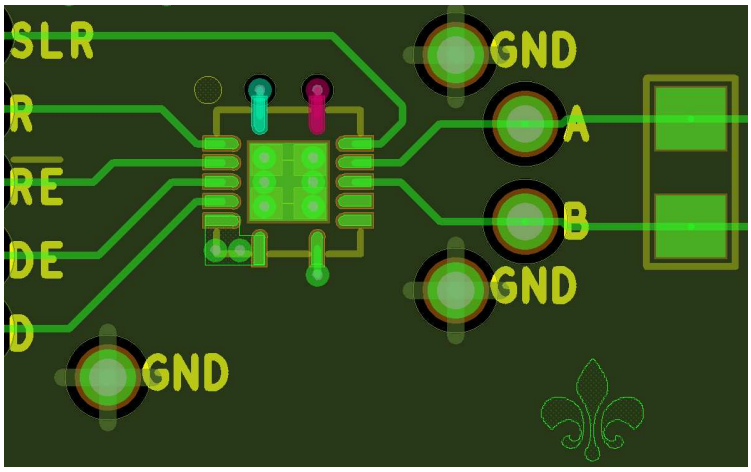
Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high-frequency layout techniques must be applied during PCB design.

In order for your PCB design to be successful start with the design of the protection circuit in mind.

## 11.1 Layout Guidelines

- Place the protection circuitry close to the bus connector to prevent noise transients from penetrating your board.
- Use $V_{CC}$ and ground planes to provide low-inductance. Note that high-frequency currents follow the path of least inductance and not the path of least impedance.
- Design the protection components into the direction of the signal path. Do not force the transients currents to divert from the signal path to reach the protection device.
- Apply 100 nF to 220 nF bypass capacitors as close as possible to the $V_{CC}$ terminals of transceiver, UART, controller ICs on the board.
- Use at least two vias for $V_{CC}$ and ground connections of bypass capacitors and protection devices to minimize effective via-inductance.
- Use 1k to 10k pull-up/down resistors for enable lines to limit noise currents in theses lines during transient events.
- Insert pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus terminals. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
- While pure TVS protection is sufficient for surge transients up to 1kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.

## 11.2 Layout Example



# 12 器件和文档支持

## 12.1 商标

All trademarks are the property of their respective owners.

## 12.2 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

## 12.3 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

# 13 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65HVD01DRCR | ACTIVE | VSON | DRC | 10 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HVD01 | Samples |
| SN65HVD01DRCT | ACTIVE | VSON | DRC | 10 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | HVD01 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

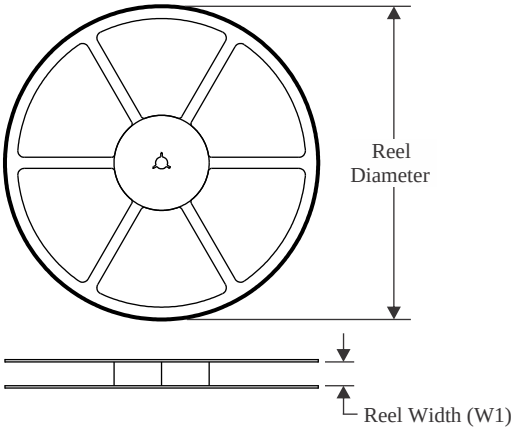
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

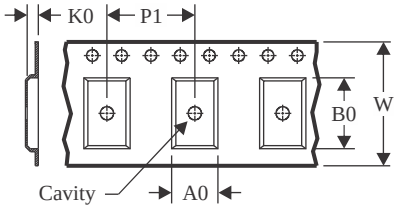
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

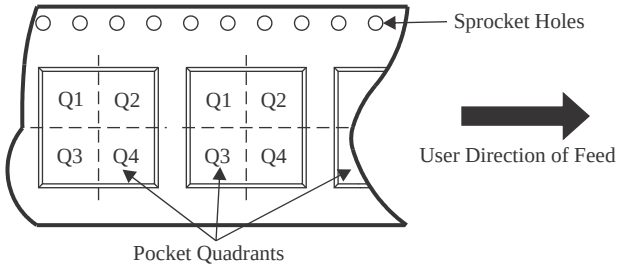



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

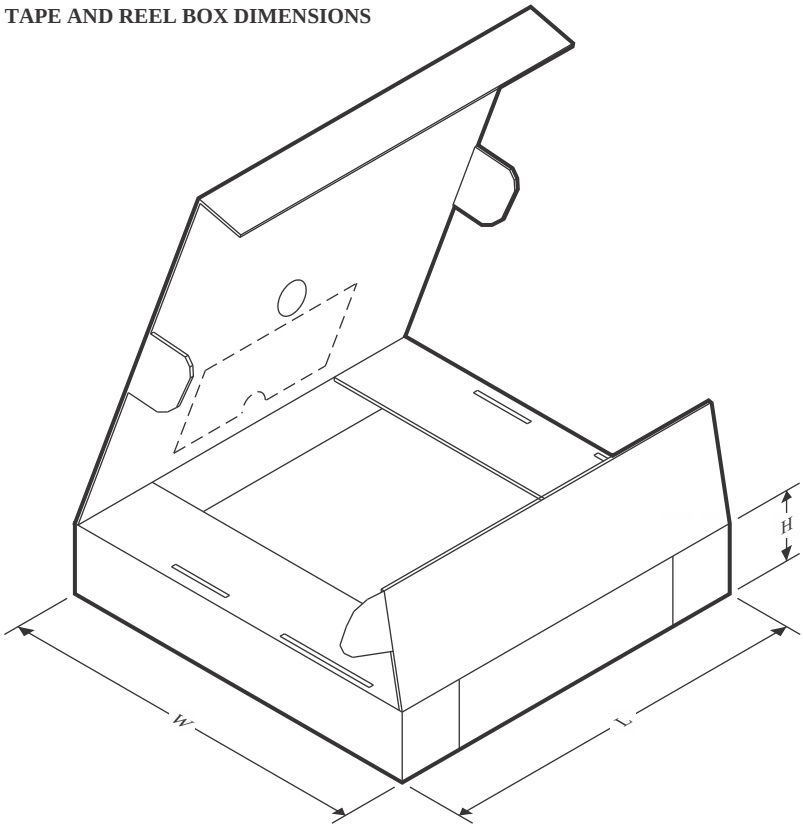
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65HVD01DRCR | VSON | DRC | 10 | 2500 | 330.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |
| SN65HVD01DRCT | VSON | DRC | 10 | 250 | 180.0 | 12.4 | 3.3 | 3.3 | 1.1 | 8.0 | 12.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN65HVD01DRCR | VSON | DRC | 10 | 2500 | 335.0 | 335.0 | 25.0 |
| SN65HVD01DRCT | VSON | DRC | 10 | 250 | 182.0 | 182.0 | 20.0 |

# GENERIC PACKAGE VIEW

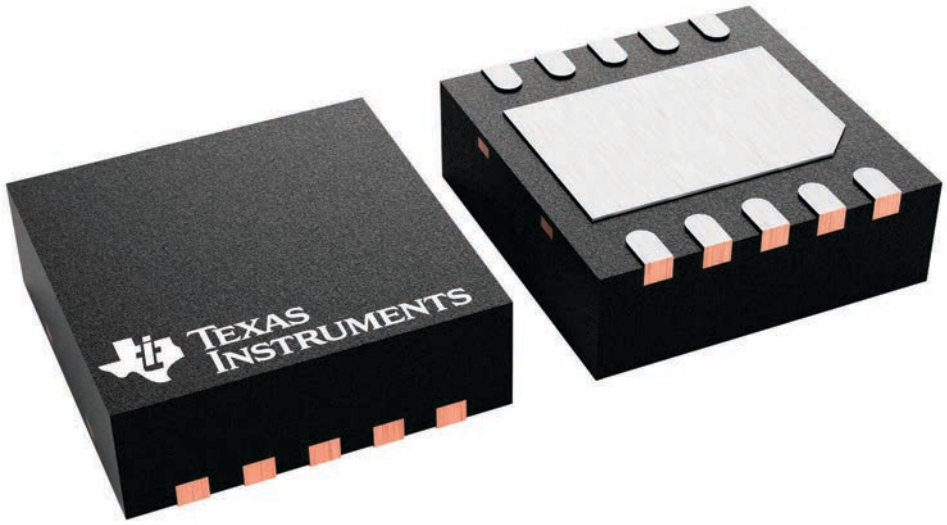
## DRC 10

## VSON - 1 mm max height

**3 x 3, 0.5 mm pitch**

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



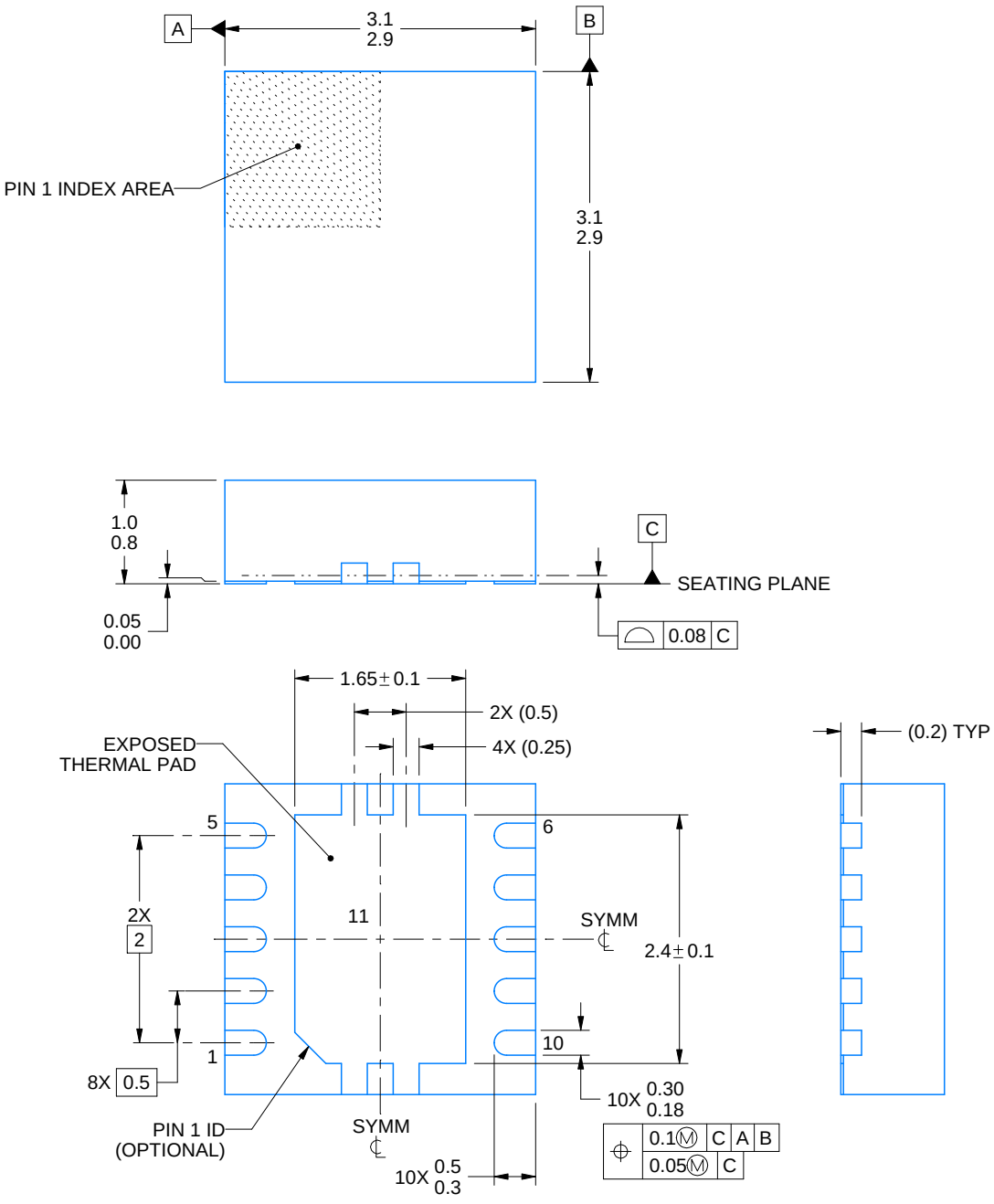

4226193/A

# DRC0010J

# PACKAGE OUTLINE

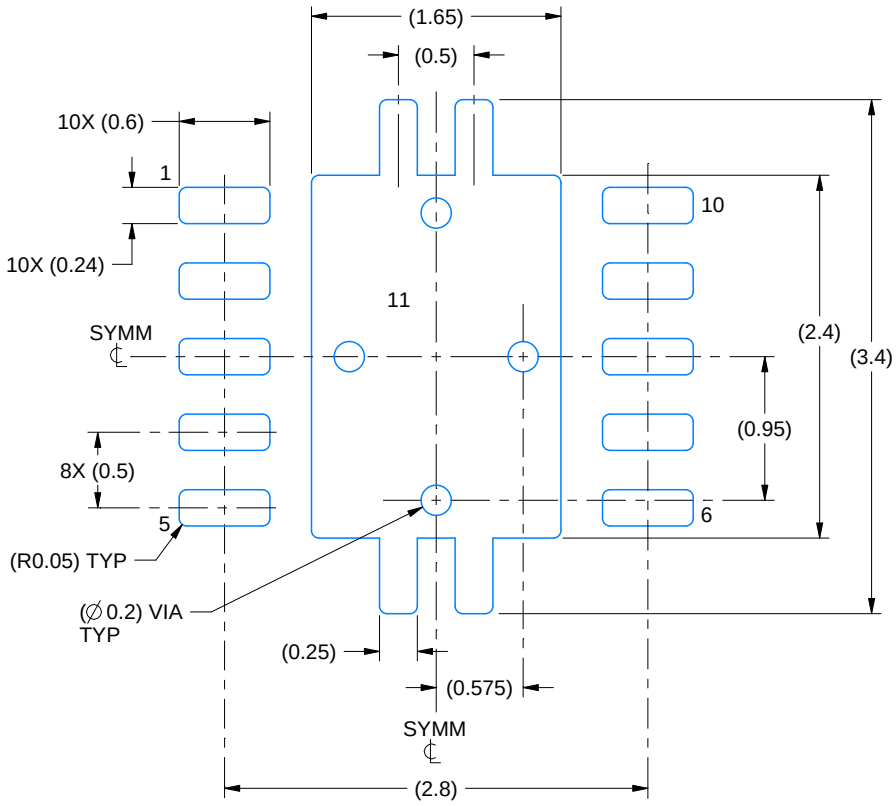
## VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

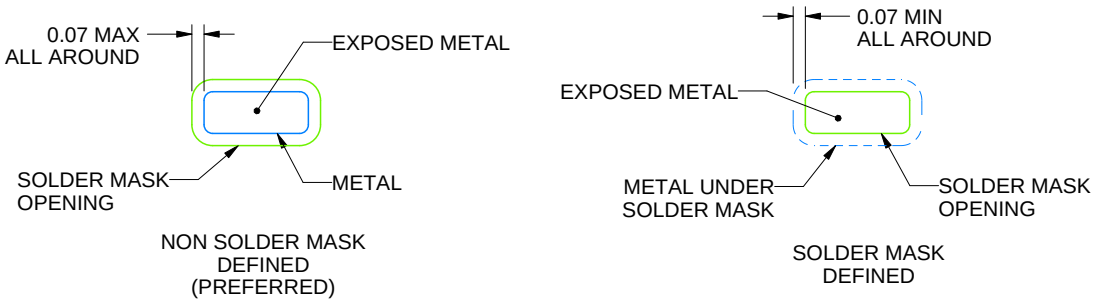



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X




SOLDER MASK DETAILS

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NOTES: (continued)

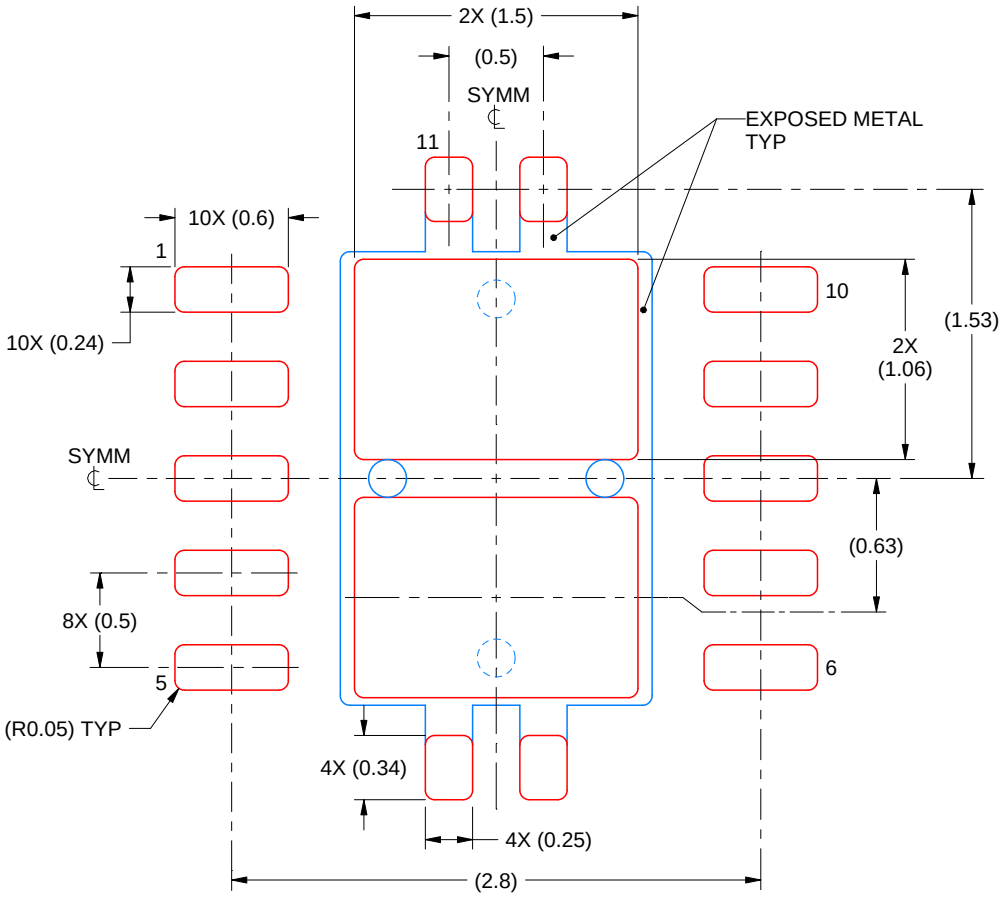
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

## DRC0010J

## VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218878/B 07/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# 重要声明和免责声明

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