SNx5LBC176 差分总线收发器

1 特性

- 双向收发器
- 符合或超出 ANSI 标准 TIA/EIA-485-A 和 ISO 8482:1987(E) 的要求
- 高速低功耗 LinBiCMOS™ 电路
- 专为在串行和并行应用中实现高速运行而设计
- 低偏斜
- 针对嘈杂环境中的长距离总线线路上的多点传输而设计
- 极低的禁用电源电流。..200µA（最大值）
- 宽正负输入/输出总线电压范围
- 热关断保护
- 驱动器正负电流限制
- 开路故障安全接收器设计
- 接收器输入灵敏度..±200mV（最大值）
- 接收器输入迟滞。..50 mV（典型值）
- 采用 5V 单电源供电
- 无干扰上电和断电保护
- 可用于 Q-Temp 汽车高可靠性汽车应用
  配置控制/打印支持
  通过汽车标准认证

2 说明

SN55LBC176、SN65LBC176、SN65LBC176Q 和 SN75LBC176 差分总线收发器是单片集成电路，旨在用于多点总线传输线路上的双向数据通信。这些器件专为平衡传输线路而设计，符合 ANSI 标准 TIA/EIA-485-A (RS-485) 和 ISO 8482:1987(E)。

SN55LBC176、SN65LBC176、SN65LBC176Q 和 SN75LBC176 器件整合了一个三态差分线路驱动器和一个差分输入线路接收器，两者均采用 5V 单电源供电。驱动器和接收器分别具有高电平有效和低电平有效使能端，它们可以在外部连接在一起以用作方向控制。驱动器差分输出端和接收器差分输入端在内部连接以形成差分输入/输出 (I/O) 总线端口，该端口用于在禁用驱动器或 V_{CC} = 0 时为总线提供最小负载。该端口具有较宽的正负共模电压范围，使得该器件适用于合用线应用。可以通过禁用驱动器和接收器来实现较低的器件电源电流。

封装信息

器件型号	封装(1)	封装尺寸（标称值）
SN55LBC176	LCCC (20)	8.89 mm x 8.89 mm
	CDIP (8)	9.60 mm x 6.67 mm
SN65LBC176	SOIC (8)	4.90mm x 3.91mm
	PDIP (8)	9.81mm x 6.35mm
SN75LBC176	SOIC (8)	4.90mm x 3.91mm
	PDIP (8)	9.81mm x 6.35mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

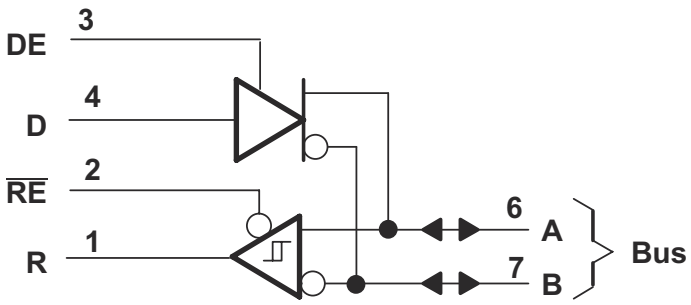

图 2-1. 逻辑图（正逻辑）

本文档旨在为方便起见，提供有关 TI 产品中文版本的信息，以确认产品的概要。有关适用的官方英文版本的最新信息，请访问 www.ti.com，其内容始终优先。TI 不保证翻译的准确性和有效性。在实际设计之前，请务必参考最新版本的英文版本。

Table of Contents

3 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision H (December 2010) to Revision I (October 2022)	Page
• 添加了 *引脚配置和功能* 部分、*热性能信息表*、*详细说明*部分、*器件功能模式*、*器件和文档支持* 部分和 *机械、包装和可订购信息* 部分	1

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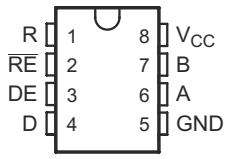
4 说明（续）

这些收发器适用于 ANSI 标准 TIA/EIA−485 (RS-485) 和 ISO 8482 应用，前提是它们在此数据表的运行条件和特性部分中已指定。TIA/EIA−485−A 和 ISO 8482:1987 (E) 中包含的某些限制不符合或无法在整个军用温度范围内进行测试。

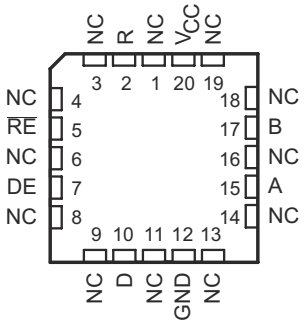
SN55LBC176 的额定工作温度范围是 –55°C 至 125°C。SN65LBC176 的额定工作温度范围是 –40°C 至 85°C，SN65LBC176Q 的额定工作温度范围是 –40°C 至 125°C。SN75LBC176 的额定工作温度范围是 0°C 至 70°C。

5 Pin Configuration and Functions

D, JG, OR P PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection

表 5-1. Pin Functions

PIN			TYPE	DESCRIPTION
NAME	SOIC,PDIP, CDIP	LCCC		
R	1	2	O	Logic output RS485 data
$\overline{RE}$	2	5	I	Receiver enable/disable
DE	3	7	I	Driver enable/disable
D	4	10	I	Logic input RS485 data
GND	5	12	-	Ground
A	6	15	I/O	RS485 bus pin; Non-Inverting
B	7	17	I/O	RS485 bus pin; Inverted
V_{CC}	8	20	-	5V Supply Voltage
NC	-	1,2,3,6,8,9,11,13,14,16,18,19	-	No Internal Connection

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Supply voltage, V_{CC} (2)		7	V
Voltage range at any bus terminal	–10	15	V
Input voltage, V_I (D, DE, R, or $\overline{RE}$)	–0.3	V_{CC} + 0.5	V
Receiver output current, I_O	–10	10	mA
Continuous total power dissipation	See 节 6.5		
Storage temperature range, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under 节 6.2 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.

6.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common mode), V_I or V_{IC}		–7		12	V
High-level input voltage, V_{IH}	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, VIL	D, DE, and $\overline{RE}$			0.8	V
Differential input voltage, V_{ID} (1)		–12		12	V
High-level output current, I_{OH}	Driver	–60			mA
	Receiver	–400			μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			8	
Junction temperature, T_J				140	°C
Operating free-air temperature, T_A	SN55LBC176	−55		125	°C
	SN65LBC176	–40		85	
	SN65LBC176Q	–40		125	
	SN75LBC176	0		70	

(1) Differential input /output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

6.3 Thermal Information: SN55LBC176

THERMAL METRIC(1)		FK	JG	UNIT
		20 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	61.6	99.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	36.8	51.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	36.1	86.5	
ψ_{JT}	Junction-to-top characterization parameter	31.0	23.7	
ψ_{JB}	Junction-to-board characterization parameter	36.0	80.2	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.2	11.6	

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6.4 Thermal Information: SN65LBC176, SN75LBC176

THERMAL METRIC(1)		D	P	UNIT
		8 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.7	65.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.3	54.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	63.4	42.1	
ψ_{JT}	Junction-to-top characterization parameter	8.8	22.9	
ψ_{JB}	Junction-to-board characterization parameter	62.6	41.6	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Dissipation Ratings

PACKAGE	THERMAL MODEL	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 110°C POWER RATING
D	Low K(1)	526 mW	5.0 mW/°C	301 mW	226 mW	—
	High K(2)	882 mW	8.4 mW/°C	504 mW	378 mW	—
P		840 mW	8.0 mW/°C	480 mW	360 mW	—
JG		1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
FK		1375 mW	11.0 mW/°C	880 mW	715 mW	440 mW

(1) In accordance with the low effective thermal conductivity metric definitions of EIA/JESD 51−3.
(2) In accordance with the high effective thermal conductivity metric definitions of EIA/JESD 51−7.

6.6 Driver Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = – 18 mA			– 1.5		V
V_O	Output voltage	I_O = 0			0	6	V
$\lvert V_{OD1} \rvert$	Differential output voltage	I_O = 0			1.5	6	V
$\lvert V_{OD2} \rvert$	Differential output voltage	R_L = 54 Ω, See 图 7-1, See (2)		55LBC176, 65LBC176, 65LBC176Q	1.1		V
				75LBC176	1.5	5	
$\lvert V_{OD3} \rvert$	Differential output voltage	V_{test} = – 7 V to 12 V, See Figure 2, See (2)		55LBC176, 65LBC176, 65LBC176Q	1.1		V
				75LBC176	1.5	5	
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of differential output voltage (1)	R_L = 54 Ω or 100 Ω, See 图 7-1			– 0.2	0.2	V
V_{OC}	Common-mode output voltage				– 1	3	V
$\Delta\lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage(1)				– 0.2	0.2	V
I_O	Output current	Output disabled, See (3)	V_O = 12 V			1	mA
			V_O = – 7 V		– 0.8		
I_{IH}	High-level input current	V_I = 2.4 V			– 100		µA
I_{IL}	Low-level input current	V_I = 0.4 V			– 100		µA

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6.6 Driver Electrical Characteristics (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
I_{OS}	Short circuit output current	V_O = −7 V			−250		mA
		V_O = 0			−150		
		V_O = V_{CC}				250	
		V_O = 12 V					
I_{CC}	Supply current	V_I = 0 or V_{CC}, No load	Receiver disabled and driver enabled	55LBC176, 65LBC176Q		1.75	mA
				65LBC176, 75LBC176		1.5	
			Receiver and driver disabled	55LBC176, 65LBC176Q		0.25	
				65LBC176, 75LBC176		0.2	

(1) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input changes from a high level to a low level.
(2) This device meets the V_{OD} requirements of TIA/EIA−485−A above 0°C only.
(3) This applies for both power on and off; refer to TIA/EIA−485−A for exact conditions.

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6.7 Driver Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	SN55LBC176 SN65LBC176Q			SN65LBC176 SN75LBC176			UNIT
			MIN	TYP	MAX	MIN	TYP(1)	MAX	
$t_{d(OD)}$	Differential output delay time	R_L = 54 Ω, C_L = 50 pF, See 图 7-3	8		31	8		25	ns
$t_{t(OD)}$	Differential output transition time			12			12		ns
$t_{sk(p)}$	Pulse skew ($\lvert t_{d(ODH)} - t_{d(ODL)} \rvert$)				6		0	6	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω, See 图 7-4			65			35	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω, See 图 7-5			65			35	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω, See 图 7-4			105			60	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω, See 图 7-5			105			35	ns

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

表 6-1. Driver Symbol Equivalents

DATA SHEET PARAMETER	RS-485
V_O	V_{oa}, V_{ob}
$\lvert V_{OD1} \rvert$	V_o
$\lvert V_{OD2} \rvert$	V_t (R_L = 54 Ω)
$\lvert V_{OD} \rvert$	V_t (test termination measurement 2)
$\Delta \lvert V_{OD} \rvert$	$\lVert V_t \rvert - \lvert \overline{V}_t \rVert$
V_{OC}	$\lvert V_{os} \rvert$
$\Delta \lvert V_{OC} \rvert$	$\lvert V_{os} - \overline{V}_{os} \rvert$
I_{OS}	None
I_O	I_{ia}, I_{ib}

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6.8 Receiver Electrical Characteristics

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V,	I_O = –0.4 mA				0.2	V
V_{IT-}	Negative-going input threshold voltage	V_O = 0.5 V,	I_O = 8 mA		–0.2(2)			V
V_{hys}	Hysteresis voltage (V_{IT+} – V_{IT-}) (see 图 7-4)					50		mV
V_{IK}	Enable-input clamp voltage	I_I = –18 mA			–1.5			V
V_{OH}	High level output voltage	V_{ID} = 200 mV, See 图 7-6	I_{OH} = –400 µA,		2.7			V
V_{OL}	Low level output voltage	V_{ID} = –200 mV, See 图 7-6	I_{OL} = 8 mA,				0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V			–20		20	µA
I_I	Line input current	Other input = 0 V, See (3)	V_I = 12 V				1	mA
			V_I = –7 V		–0.8			
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V			–100			µA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V			–100			µA
r_I	Input resistance				12			kΩ
I_{CC}	Supply current	V_I = 0 or V_{CC}, No load	Receiver enabled and driver disabled				3.9	mA
			Receiver and driver disabled	SN55LBC176, SN65LBC176, SN65LBC176Q			0.25	mA
				SN75LBC176			0.2	

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) The algebraic convention, in which the less-positive (more-negative) limit is designated minimum, is used in this data sheet.
(3) This applies for both power on and power off. Refer to ANSI Standard RS-485 for exact conditions.

6.9 Receiver Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature, C_L = 15 pF

PARAMETER		TEST CONDITIONS	SN55LBC176 SN65LBC176Q		SN65LBC176 SN75LBC176			UNIT
			MIN	MAX	MIN	TYP(1)	MAX	
t_{PLH}	Propagation delay time, low- to high-level single-ended output	V_{ID} = –1.5 V to 1.5 V, See 图 7-7	11	37	11		33	ns
t_{PHL}	Propagation delay time, high- to low-level single-ended output		11	37	11		33	ns
$t_{sk(p)}$	Pulse skew (| t_{PLH} – t_{PHL} |)			10		3	6	ns
t_{PZH}	Output enable time to high level	See 图 7-8		35			35	ns
t_{PZL}	Output enable time to low level			35			30	ns
t_{PHZ}	Output disable time from high level	See 图 7-8		35			35	ns
t_{PLZ}	Output disable time from low level			35			30	ns

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.

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7 Parameter Measurement Information

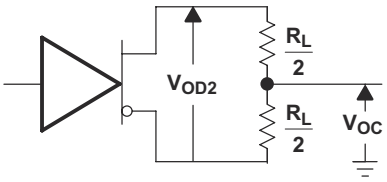

图 7-1. Driver V_{OD} and V_{OC}

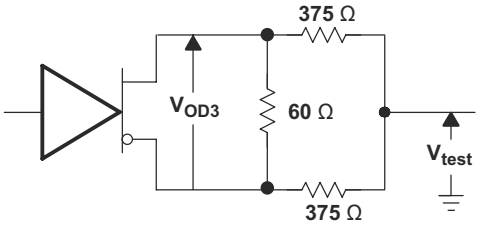

图 7-2. Driver V_{OD3}

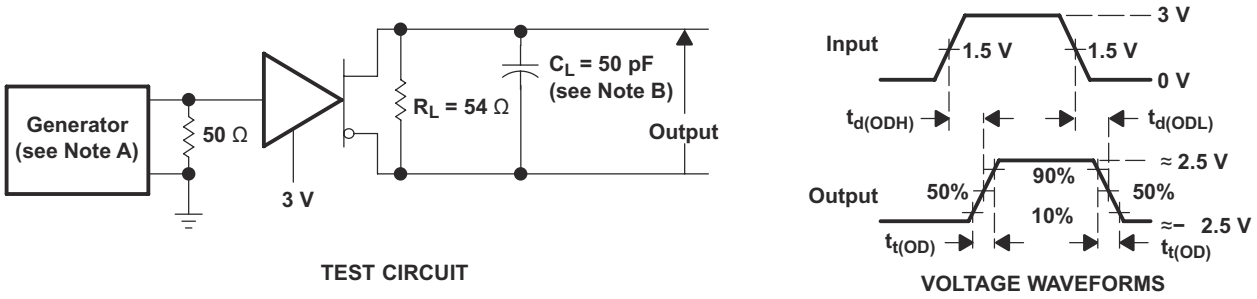

图 7-3. Driver Test Circuit and Voltage Waveforms

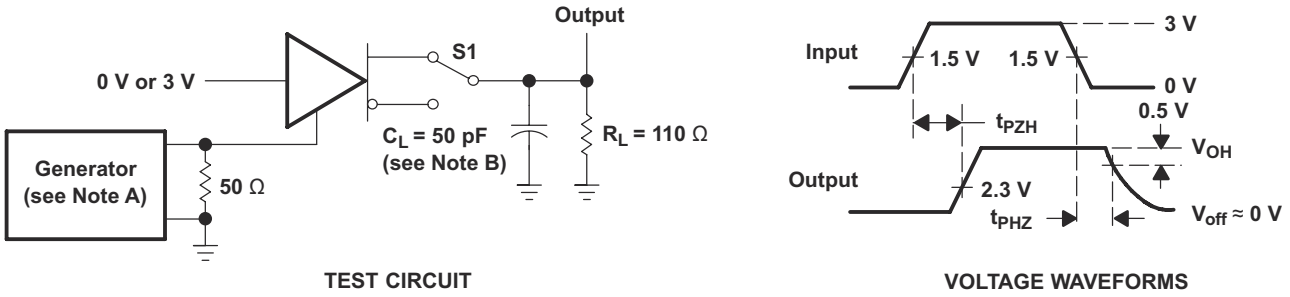

图 7-4. Driver Test Circuit and Voltage Waveforms

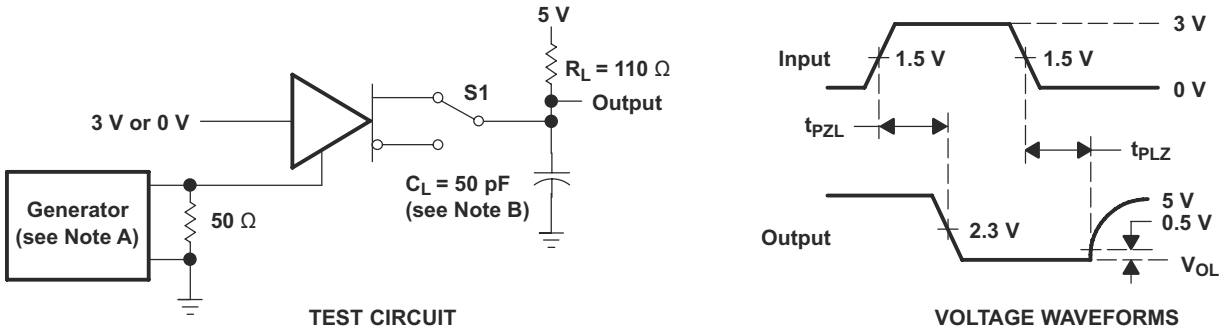

图 7-5. Driver Test Circuit and Voltage Waveforms

A. The input pulse is supplied by a generator having the following characteristics: PRR ⩽ 1 MHz, 50% duty cycle, t_r ⩽ 6 ns, t_f ⩽ 6 ns, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. The input pulse is supplied by a generator having the following characteristics: PRR ⩽ 1 MHz, 50% duty cycle, t_r ⩽ 6 ns, t_f ⩽ 6 ns, Z_O = 50 Ω.
D. C_L includes probe and jig capacitance.

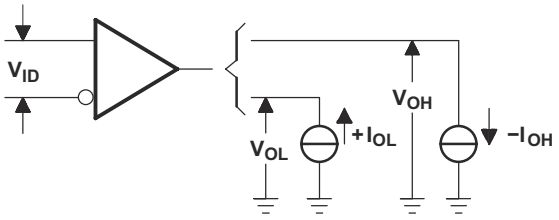

图 7-6. Receiver V_{OH} and V_{OL}

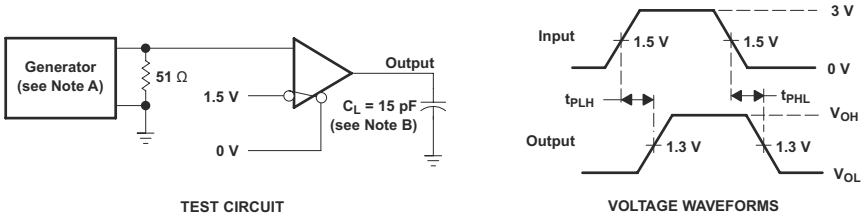

图 7-7. Receiver Test Circuit and Voltage Waveforms

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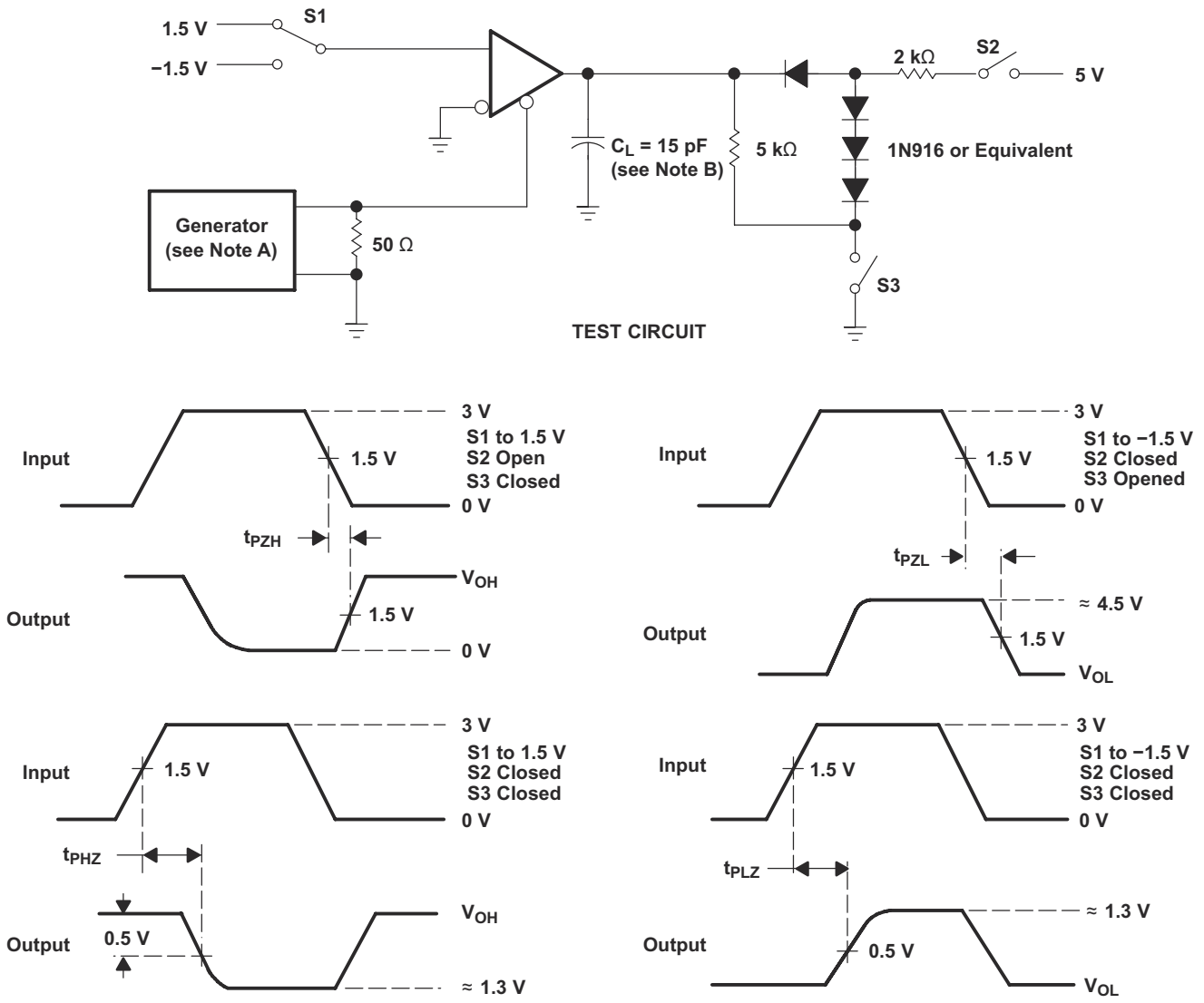


VOLTAGE WAVEFORMS

A. The input pulse is supplied by a generator having the following characteristics: PRR ⩽ 1 MHz, 50% duty cycle, t_r ⩽ 6 ns, t_f ⩽ 6 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

图 7-8. Receiver Test Circuit and Voltage Waveforms

8 Detailed Description

8.1 Functional Block Diagram

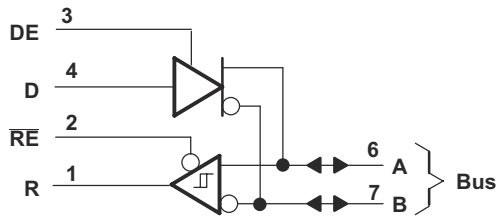
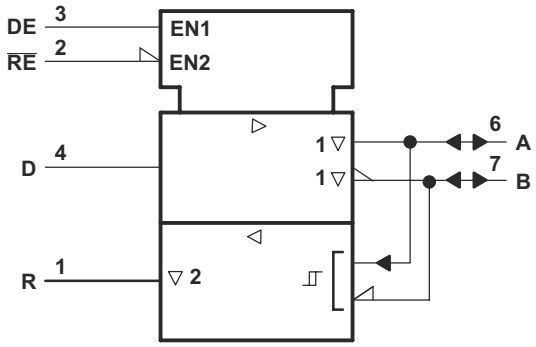


图 8-1. Logic Diagram (Positive Logic)



A. This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

图 8-2. Logic Symbol(A)

8.2 Device Functional Modes

表 8-1. Driver Function Tables(1)

DRIVER			
INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = high level, L = low level, ? = indeterminate, X = irrelevant, Z = high impedance (off)

表 8-2. Receiver Function Tables(1)

RECEIVER		
DIFFERENTIAL INPUTS $V_{ID} = V_{IA} - V_{IB}$	ENABLE $\overline{RE}$	OUTPUTS R
$V_{ID} \geq 0.2$ V	L	H
-0.2 V < V_{ID} < 0.2 V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z
Open	L	H

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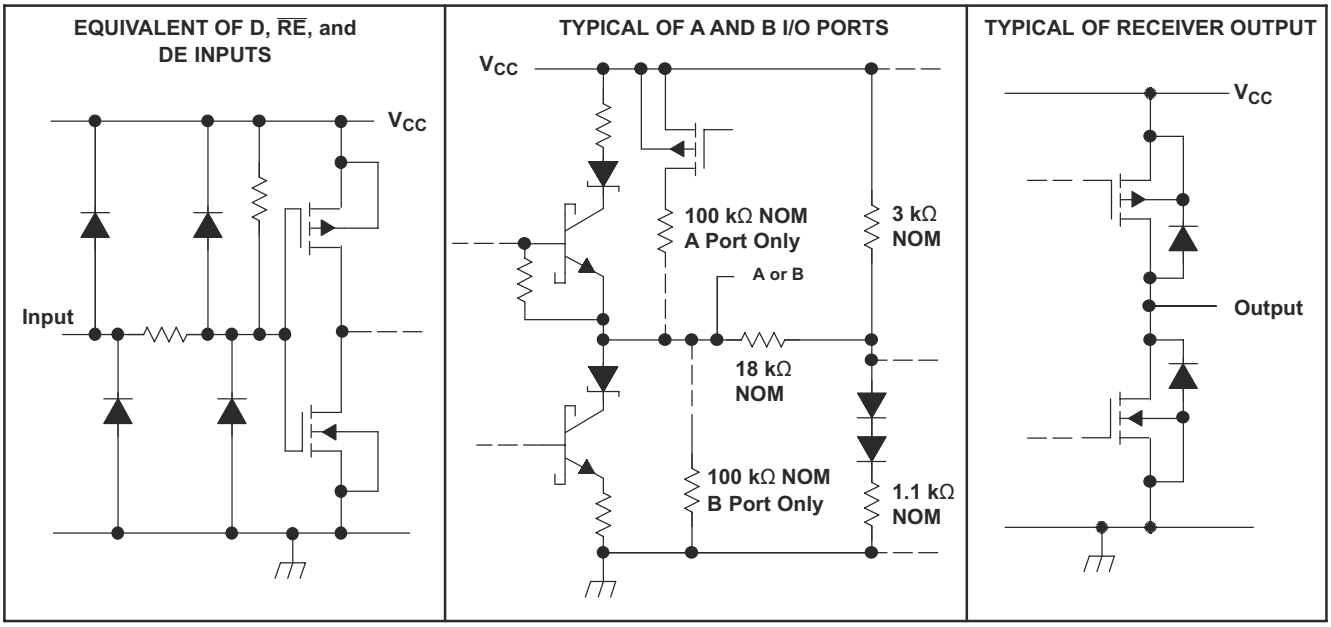

图 8-3. Schematics of Inputs and Outputs

9 Device and Documentation Support

9.1 Device Support

9.1.1 Thermal Characteristics of IC Packages

θ_{JA} (Junction-to-Ambient Thermal Resistance) is defined as the difference in junction temperature to ambient temperature divided by the operating power.

θ_{JA} is NOT a constant and is a strong function of

- the PCB design (50% variation)
- altitude (20% variation)
- device power (5% variation)

θ_{JA} can be used to compare the thermal performance of packages if the specific test conditions are defined and used. Standardized testing includes specification of PCB construction, test chamber volume, sensor locations, and the thermal characteristics of holding fixtures. θ_{JA} is often misused when it is used to calculate junction temperatures for other installations.

TI uses two test PCBs as defined by JEDEC specifications. The low-k board gives average in-use condition thermal performance and consists of a single trace layer 25 mm long and 2-oz thick copper. The high-k board gives best case in-use condition and consists of two 1-oz buried power planes with a single trace layer 25 mm long with 2-oz thick copper. A 4% to 50% difference in θ_{JA} can be measured between these two test cards.

θ_{JC} (Junction-to-Case Thermal Resistance) is defined as difference in junction temperature to case divided by the operating power. It is measured by putting the mounted package up against a copper block cold plate to force heat to flow from die, through the mold compound into the copper block.

θ_{JC} is a useful thermal characteristic when a heatsink is applied to package. It is NOT a useful characteristic to predict junction temperature as it provides pessimistic numbers if the case temperature is measured in a non-standard system and junction temperatures are backed out. It can be used with θ_{JB} in 1-dimensional thermal simulation of a package system.

θ_{JB} (Junction-to-Board Thermal Resistance) is defined to be the difference in the junction temperature and the PCB temperature at the center of the package (closest to the die) when the PCB is clamped in a cold−plate structure. θ_{JB} is only defined for the high-k test card.

θ_{JB} provides an overall thermal resistance between the die and the PCB. It includes a bit of the PCB thermal resistance (especially for BGA’s with thermal balls) and can be used for simple 1-dimensional network analysis of package system (see 图 9-1).

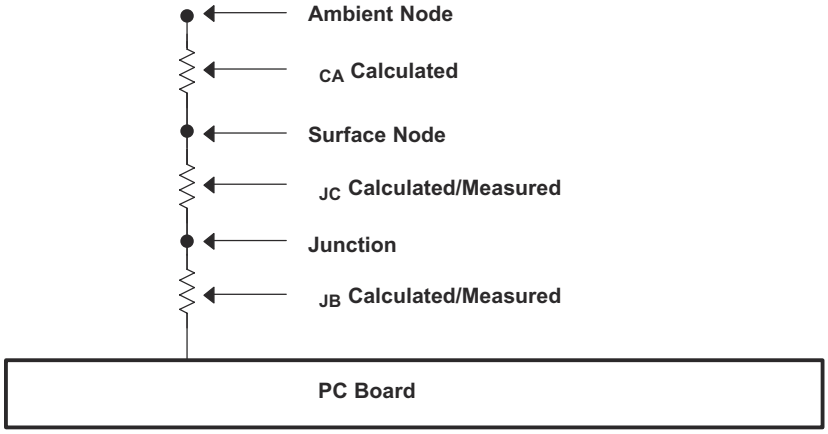

图 9-1. Thermal Resistance

9.2 Trademarks

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9.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.4 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9318301Q2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9318301Q2A SNJ55 LBC176FK	Samples
5962-9318301QPA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9318301QPA SNJ55LBC176	Samples
SN65LBC176D	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB176	
SN65LBC176DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB176	Samples
SN65LBC176DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB176	Samples
SN65LBC176P	LIFEBUY	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	65LBC176	
SN65LBC176QD	NRND	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LB176Q	
SN65LBC176QDG4	NRND	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LB176Q	
SN65LBC176QDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LB176Q	Samples
SN65LBC176QDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(J176Q1, LB176Q)	Samples
SN75LBC176D	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7LB176	
SN75LBC176DR	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7LB176	
SN75LBC176DRG4	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7LB176	
SN75LBC176P	LIFEBUY	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	75LBC176	
SNJ55LBC176FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9318301Q2A SNJ55 LBC176FK	Samples
SNJ55LBC176JG	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	9318301QPA SNJ55LBC176	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN55LBC176, SN65LBC176, SN75LBC176 :

- Catalog : SN75LBC176
- Automotive : SN65LBC176-Q1
- Military : SN55LBC176

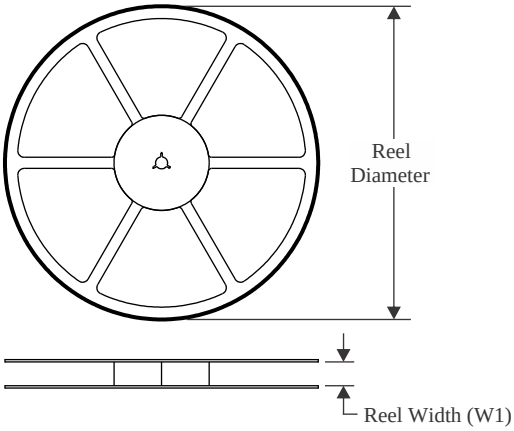
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

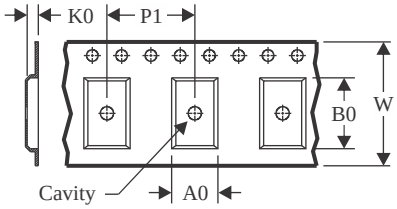
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

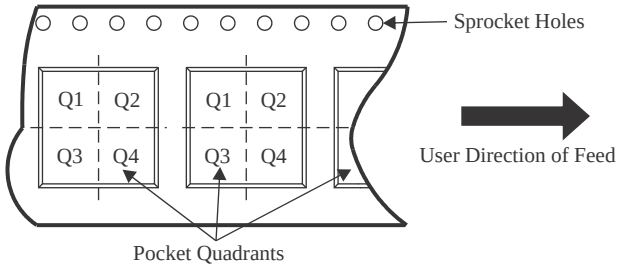


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

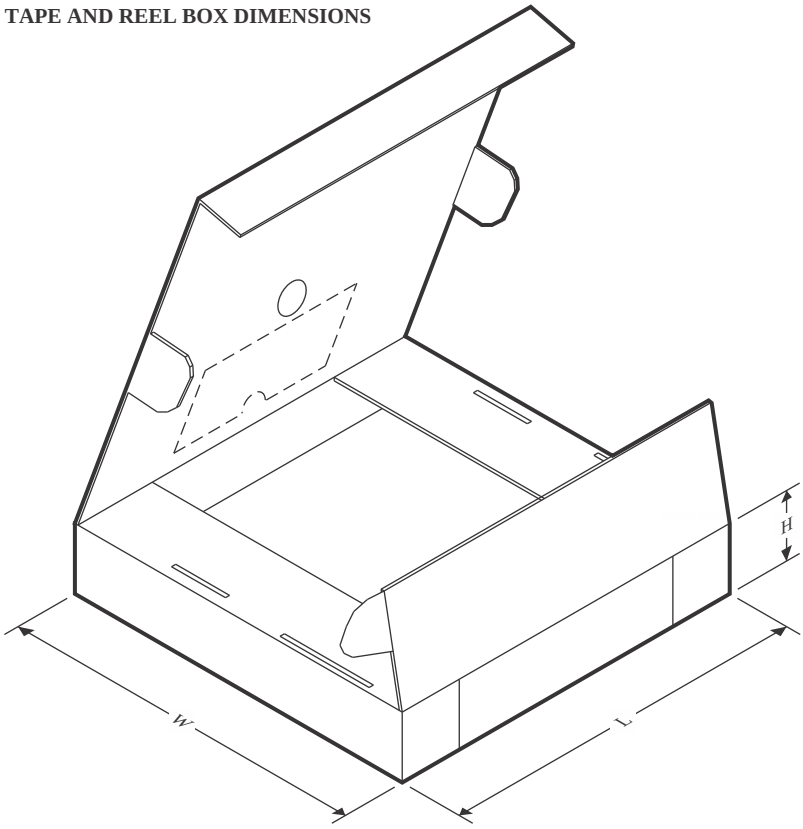
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC176DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65LBC176QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65LBC176QDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75LBC176DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

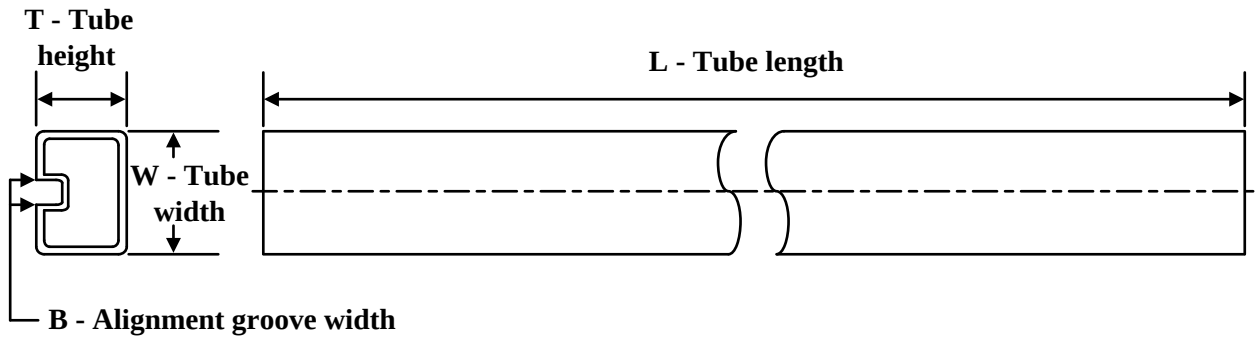
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC176DR	SOIC	D	8	2500	356.0	356.0	35.0
SN65LBC176QDR	SOIC	D	8	2500	350.0	350.0	43.0
SN65LBC176QDRG4	SOIC	D	8	2500	350.0	350.0	43.0
SN75LBC176DR	SOIC	D	8	2500	340.5	336.1	25.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-9318301Q2A	FK	LCCC	20	1	506.98	12.06	2030	NA
SN65LBC176D	D	SOIC	8	75	507	8	3940	4.32
SN65LBC176P	P	PDIP	8	50	506	13.97	11230	4.32
SN65LBC176QD	D	SOIC	8	75	505.46	6.76	3810	4
SN65LBC176QDG4	D	SOIC	8	75	505.46	6.76	3810	4
SN75LBC176D	D	SOIC	8	75	507	8	3940	4.32
SN75LBC176P	P	PDIP	8	50	506	13.97	11230	4.32
SNJ55LBC176FK	FK	LCCC	20	1	506.98	12.06	2030	NA

GENERIC PACKAGE VIEW

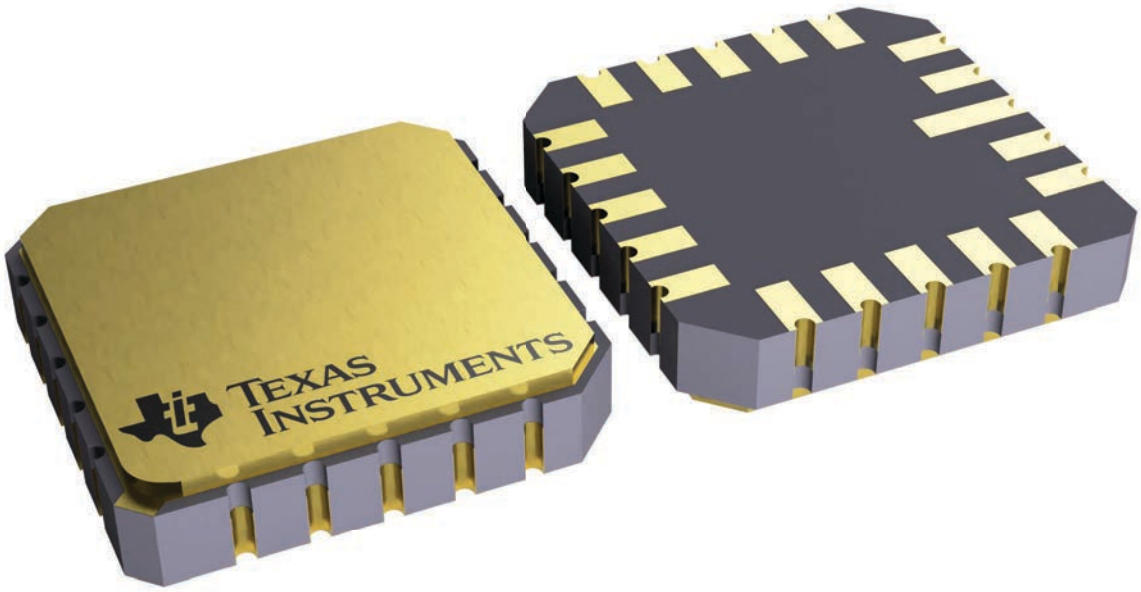
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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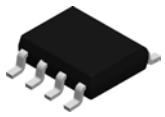
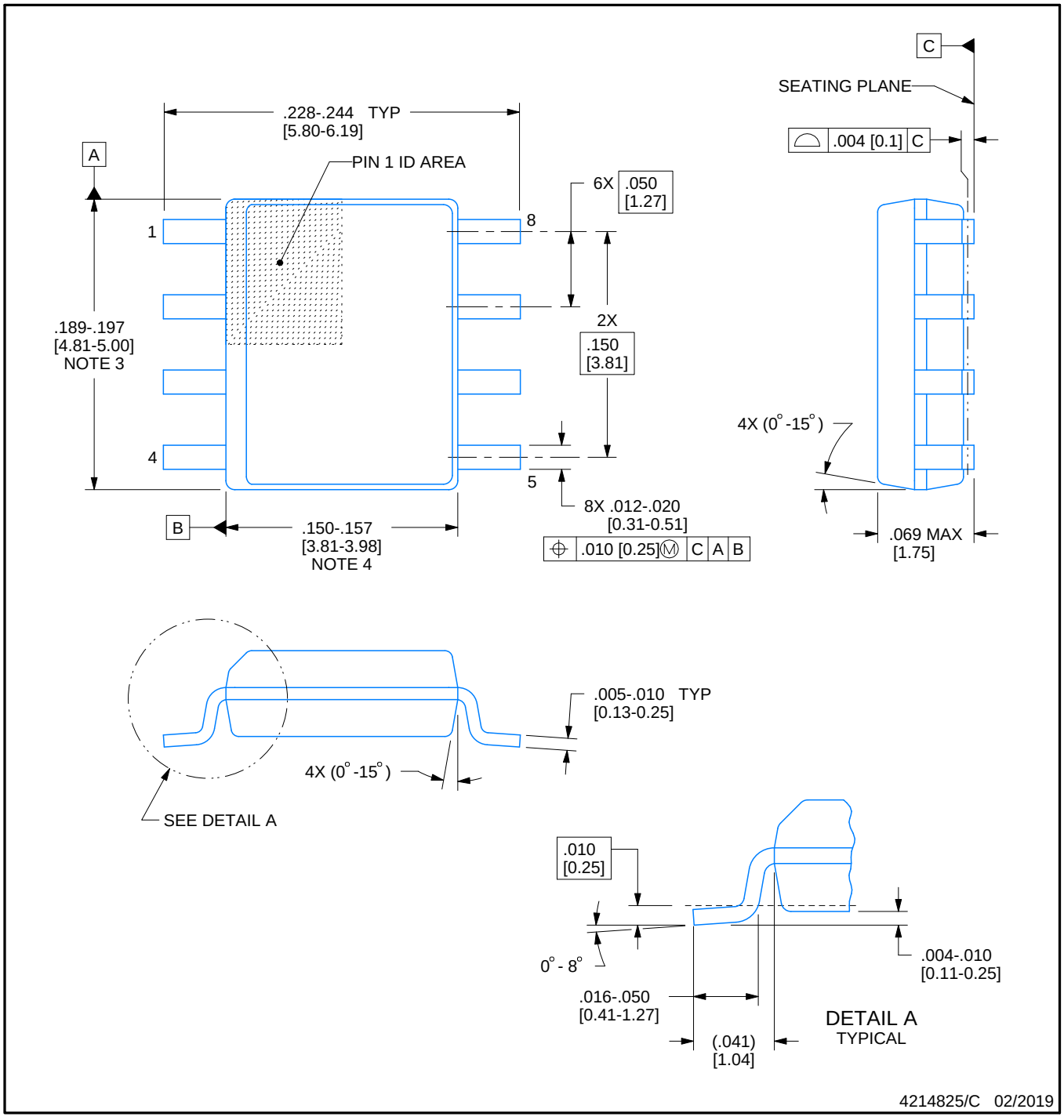


PACKAGE OUTLINE

D0008A

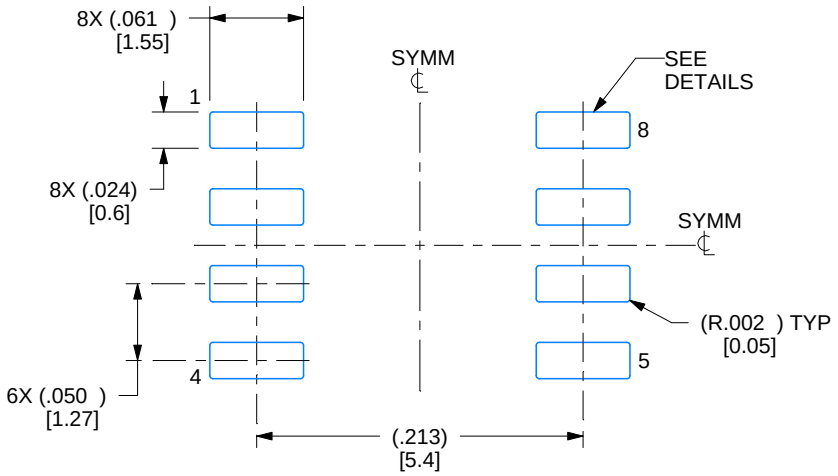
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

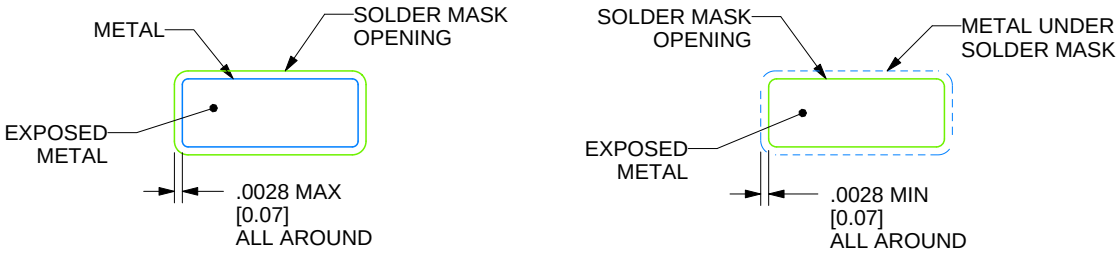


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

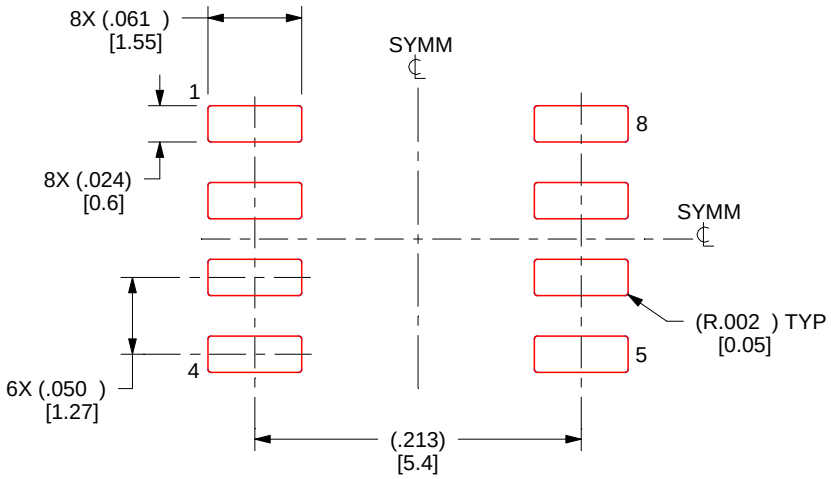
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

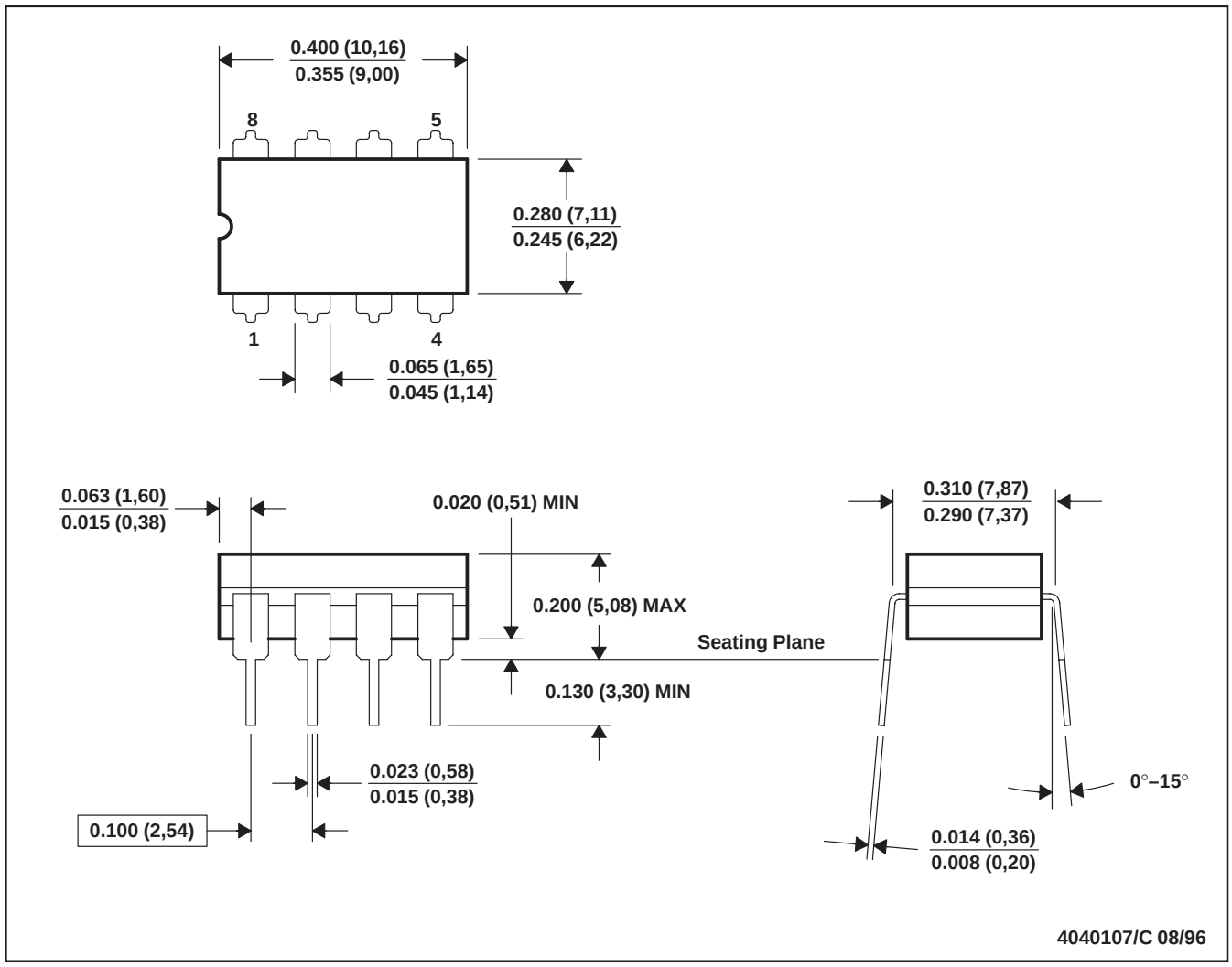
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

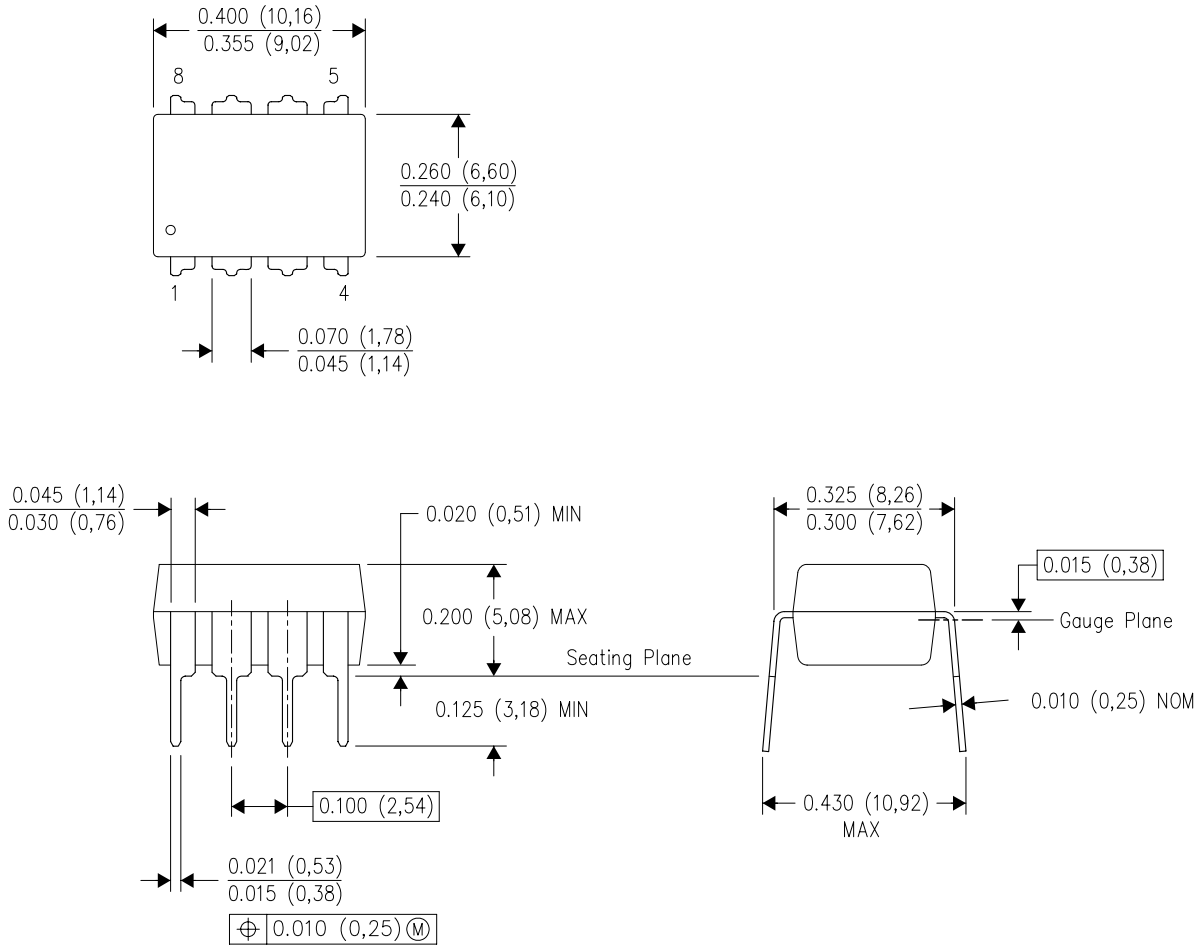
MCER001A – JANUARY 1995 – REVISED JANUARY 1997

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification.
E. Falls within MIL STD 1835 GDIP1-T8

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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