

SNx4AHC240 具有三态输出的八路缓冲器/驱动器

1 特性

- V_{CC} 工作范围为 2V 至 5.5V
- 闩锁性能超过 250mA，符合 JESD 17 规范

2 应用

- 手持终端：智能手机
- 网络交换机
- 健康与健身/可穿戴设备

3 说明

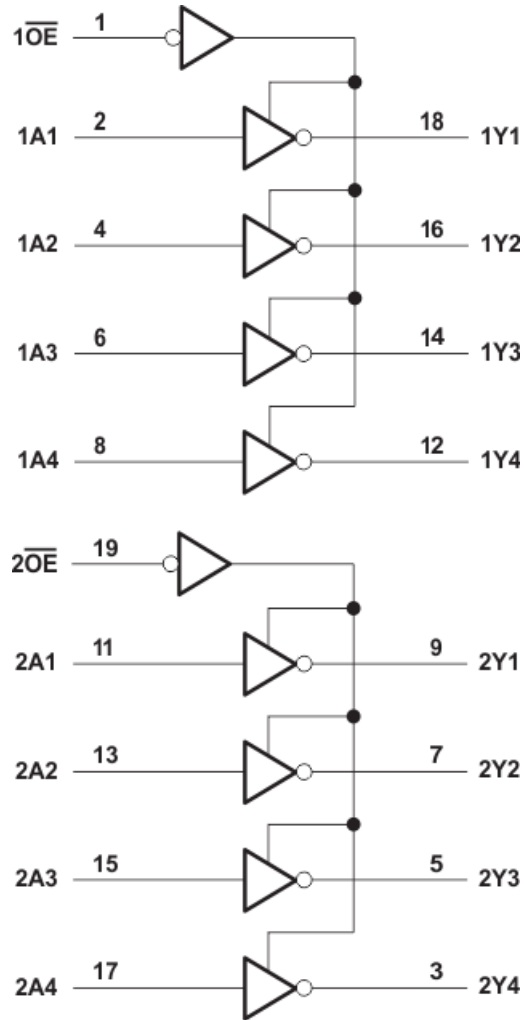
这些八路缓冲器/驱动器专门设计用于提高三态存储器地址驱动器、时钟驱动器以及总线导向接收器和发送器的性能和密度。

封装信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
SN54AHC240	J (CDIP, 20)	24.2 mm × 6.92 mm
	W (CFP, 20)	13.09mm × 6.92mm
	FK (LCCC, 20)	8.89mm × 8.89mm
SN74AHC240	N (PDIP, 20)	24.33mm × 6.35mm
	DW (SOIC, 20)	12.8mm × 7.5mm
	NS (SOP, 20)	12.6 mm × 5.30 mm
	PW (TSSOP, 20)	6.5 mm × 4.40 mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。





逻辑图 (正逻辑)

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4 Revision History

Changes from Revision H (July 2003) to Revision I (April 2023)	Page
• 添加了应用、封装信息表、引脚功能表、ESD 等级表、热性能信息表、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分.....	1

5 Pin Configuration and Functions

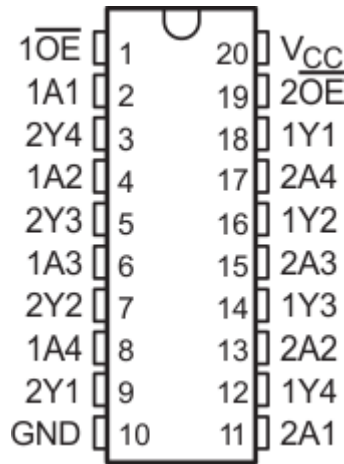


图 5-1. SN54AHC240 J or W Package; SN74AHC240 DB, DGV, DW, N, NS, or PW Package (Top View)

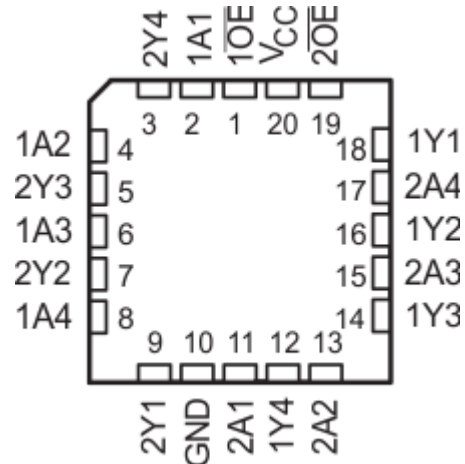


图 5-2. SN54AHC240 FK Package (Top View)

PIN	I/O	DESCRIPTION
1	1OE	Output enable 1
2	1A1	1A1 input
3	2Y4	2Y4 output
4	1A2	1A2 input
5	2Y3	2Y3 output
6	1A3	1A3 input
7	2Y2	2Y2 output
8	1A4	1A4 input
9	2Y1	2Y1 output
10	GND	Ground pin
11	2A1	2A1 input
12	1Y4	1Y4 output
13	2A2	2A2 input
14	1Y3	1Y3 output
15	2A3	2A3 input
16	1Y2	1Y2 output
17	2A4	2A4 input
18	1Y1	1Y1 output
19	2OE	Output enable 2
20	VCC	Power pin

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	- 0.5	7	V
V _I	Input voltage ⁽²⁾	- 0.5	7	V
V _O	Output voltage ⁽²⁾	- 0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0	- 20	mA
I _{OK}	Output clamp current	V _O < 0 or V _O > V _{CC}	±20	mA
I _O	Continuous output current	V _O = 0 to V _{CC}	±25	mA
Continuous current through V _{CC} or GND			±75	mA
T _{stg}	Storage temperature	- 65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

see (Note 1)

		SN54AHC240		SN74AHC240		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage	2	5.5	2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5	1.5		V
		$V_{CC} = 3\text{ V}$	2.1	2.1		
		$V_{CC} = 5.5\text{ V}$	3.85	3.85		
V_{IL}	Low-level input voltage	$V_{CC} = 2\text{ V}$		0.5	0.5	V
		$V_{CC} = 3\text{ V}$		0.9	0.9	
		$V_{CC} = 5.5\text{ V}$		1.65	1.65	
V_I	Input voltage	0	5.5	0	5.5	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2\text{ V}$		-50	-50	μA
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		-4	-4	mA
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		-8	-8	
I_{OL}	Low-level output current	$V_{CC} = 2\text{ V}$		50	50	μA
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		4	4	mA
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		8	8	
$\Delta t / \Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		100	100	ns/V
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$		20	20	
T_A	Operating free-air temperature	-55	125	-40	85	$^{\circ}\text{C}$

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		DW	DB	DGV	N	NS	PW	UNIT
		20 PINS						
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽²⁾	58	70	92	69	60	83	$^{\circ}\text{C/W}$

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

(2) The package thermal impedance is calculated in accordance with JESD 51-7.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	TA = 25°C			SN54AHC240		SN74AHC240		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = - 50 μA	2 V	1.9	2		1.9		1.9	V	
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I _{OH} = - 4 mA	3 V	2.58			2.48		2.48		
	I _{OH} = - 8 mA	4.5 V	3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 μA	2 V			0.1		0.1		V	
		3 V			0.1		0.1			
		4.5 V			0.1		0.1			
	I _{OL} = 4 mA	3 V			0.36		0.5	0.44		
	I _{OL} = 8 mA	4.5 V			0.36		0.5	0.44		
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			± 0.1		± 1 ₁		± 1	μA
I _{OZ 2}	V _O = V _{CC} or GND, V _I (OE) = V _{IL} or V _{IH}	5.5 V			± 0.25		± 2.5		± 2.5	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4		40		40	μA
C _i	V _I = V _{CC} or GND	5 V		2.5	10				10	pF
C _o	V _O = V _{CC} or GND	5 V		3.5						pF

- On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.
- The parameter I_{OZ} includes the input leakage current.

6.6 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	TA = 25°C			SN54AHC240		SN74AHC240		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t _{PLH}	A	Y	C _L = 15 pF		5.3 ⁽¹⁾	7.5 ⁽¹⁾	1 ⁽¹⁾	9 ⁽¹⁾	1	9	ns
t _{PHL}							5.3 ⁽¹⁾	7.5 ⁽¹⁾	1 ⁽¹⁾	9 ⁽¹⁾	
t _{PZH}	OE	Y	C _L = 15 pF		6.6 ⁽¹⁾	10.6 ⁽¹⁾	1 ⁽¹⁾	12.5 ⁽¹⁾	1	12.5	ns
t _{PZL}							6.6 ⁽¹⁾	10.6 ⁽¹⁾	1 ⁽¹⁾	12.5 ⁽¹⁾	
t _{PHZ}	OE	Y	C _L = 15 pF		7.8 ⁽¹⁾	11.5 ⁽¹⁾	1 ⁽¹⁾	12.5 ⁽¹⁾	1	12.5	ns
t _{PLZ}							7.8 ⁽¹⁾	11.5 ⁽¹⁾	1 ⁽¹⁾	12.5 ⁽¹⁾	
t _{PLH}	A	Y	C _L = 50 pF		7.8	11	1	12.5	1	12.5	ns
t _{PHL}							7.8	11	1	12.5	
t _{PZH}	OE	Y	C _L = 50 pF		9.1	14.1	1	16	1	16	ns
t _{PZL}							9.1	14.1	1	16	
t _{PHZ}	OE	Y	C _L = 50 pF		10.3	14	1	16	1	16	ns
t _{PLZ}							10.3	14	1	16	
t _{sk(o)}			C _L = 50 pF			1.5 ⁽²⁾				1.5	ns

- On products compliant to MIL-PRF-38535, this parameter is not production tested.
- On products compliant to MIL-PRF-38535, this parameter does not apply.

6.7 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC240		SN74AHC240		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	$C_L = 15\text{ pF}$	3.6 ⁽¹⁾	5.5 ⁽¹⁾	1 ⁽¹⁾	6.5 ⁽¹⁾	1	6.5 ⁽¹⁾	ns	
t_{PHL}				3.6 ⁽¹⁾	5.5 ⁽¹⁾	1 ⁽¹⁾	6.5 ⁽¹⁾	1	6.5 ⁽¹⁾		
t_{PZH}	\overline{OE}	Y	$C_L = 15\text{ pF}$	4.7 ⁽¹⁾	7.3 ⁽¹⁾	1 ⁽¹⁾	8.5 ⁽¹⁾	1	8.5	ns	
t_{PZL}				4.7 ⁽¹⁾	7.3 ⁽¹⁾	1 ⁽¹⁾	8.5 ⁽¹⁾	1	8.5		
t_{PHZ}	\overline{OE}	Y	$C_L = 15\text{ pF}$	5.2 ⁽¹⁾	7.2 ⁽¹⁾	1 ⁽¹⁾	8.5 ⁽¹⁾	1	8.5	ns	
t_{PLZ}				5.2 ⁽¹⁾	7.2 ⁽¹⁾	1 ⁽¹⁾	8.5 ⁽¹⁾	1	8.5		
t_{PLH}	A	Y	$C_L = 50\text{ pF}$	5.1	7.5	1	8.5	1	8.5	ns	
t_{PHL}				5.1	7.5	1	8.5	1	8.5		
t_{PZH}	\overline{OE}	Y	$C_L = 50\text{ pF}$	6.2	9.3	1	10.5	1	10.5	ns	
t_{PZL}				6.2	9.3	1	10.5	1	10.5		
t_{PHZ}	\overline{OE}	Y	$C_L = 50\text{ pF}$	6.7	9.2	1	10.5	1	10.5	ns	
t_{PLZ}				6.7	9.2	1	10.5	1	10.5		
$t_{sk(o)}$			$C_L = 50\text{ pF}$		1 ⁽²⁾				1	ns	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

6.8 Noise Characteristics

$V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see [Note 1](#))

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.6		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.6		
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.6		
$V_{IH(D)}$	High-level dynamic input voltage	3.5			
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	

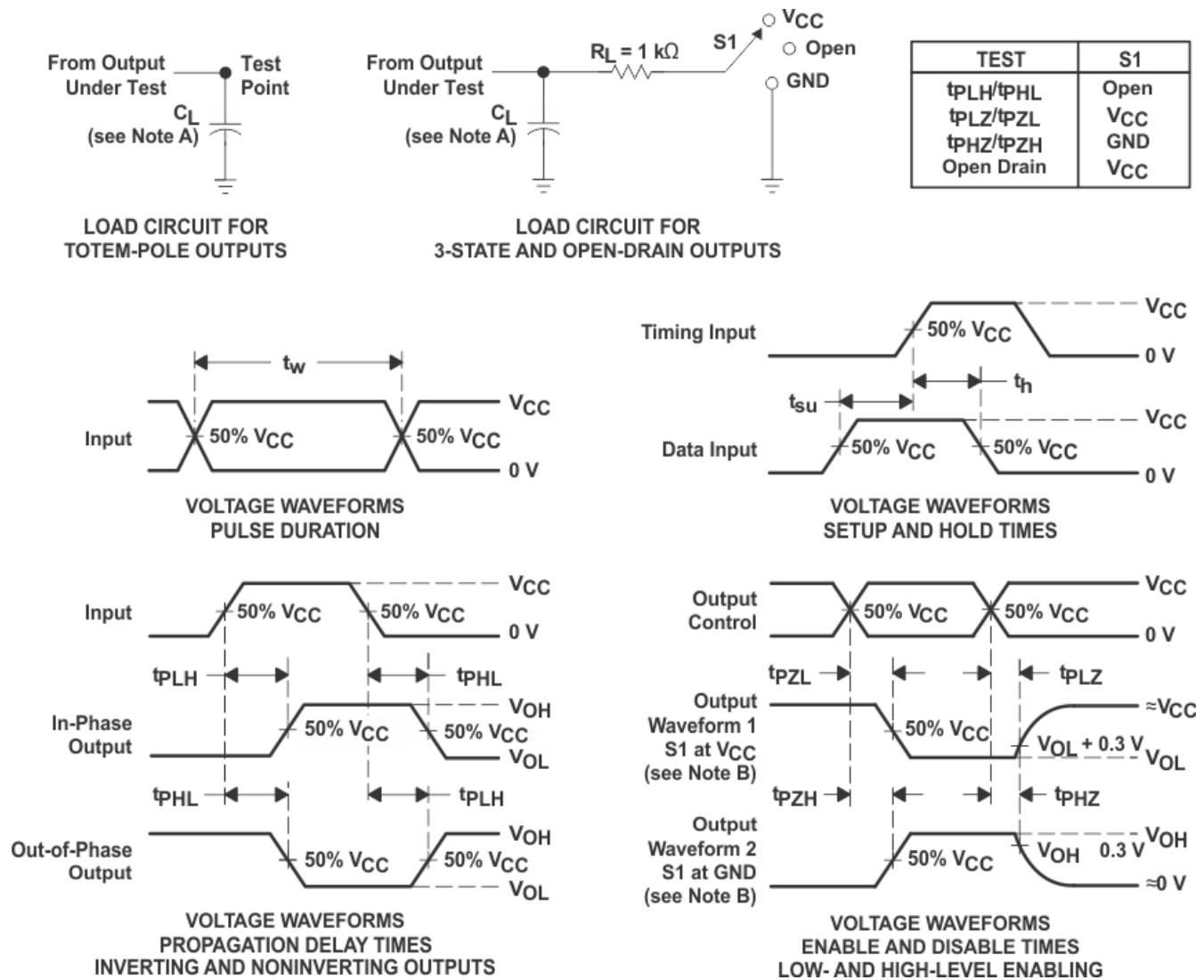
(1) Characteristics are for surface-mount packages only.

6.9 Operating Characteristics

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	No load, $f = 1\text{ MHz}$	10	pF

7 Parameter Measurement Information



NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_0 = 50 \Omega$, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$.

D. The outputs are measured one at a time with one input transition per measurement. E. All parameters and waveforms are not applicable to all devices.

图 7-1. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The 'AHC240 devices are organized as two 4-bit buffers/line drivers with separate output-enable (\overline{OE}) inputs. When \overline{OE} is low, the device passes data from the A inputs to the Y outputs. When \overline{OE} is high, the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

8.2 Functional Block Diagram

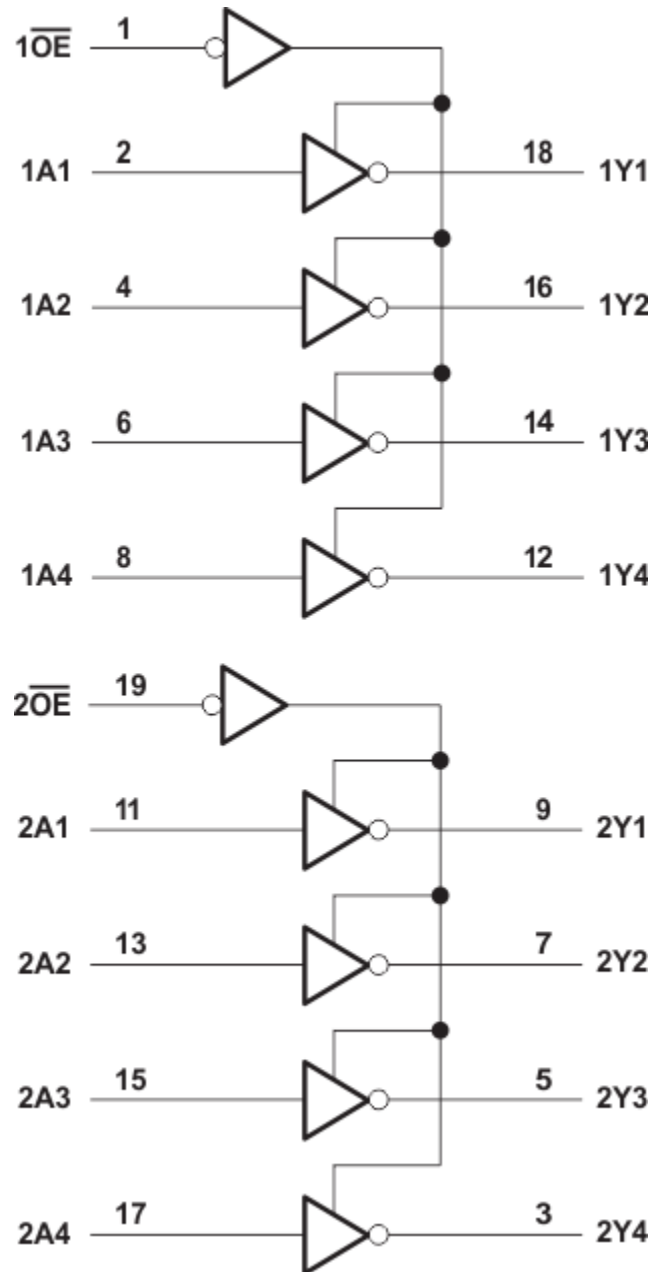


图 8-1. Logic Diagram (Positive Logic)

8.3 Device Functional Modes

表 8-1. Function Table
(Each Buffer)

INPUTS ⁽¹⁾		OUTPUT ⁽²⁾
OE	A	Y
L	H	L
L	L	H
H	X	Z

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

(2) H = Driving High, L = Driving Low, Z = High Impedance State

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in [节 6.3](#).

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends $0.1\ \mu\text{F}$ and if there are multiple V_{CC} terminals, then TI recommends $.01\ \mu\text{F}$ or $.022\ \mu\text{F}$ for each power terminal. It is okay to parallel multiple bypass capacitors to reject different frequencies of noise. A $0.1\ \mu\text{F}$ and $1\ \mu\text{F}$ are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9.2 Layout

9.2.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. It is generally okay to float outputs unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This does not disable the input section of the IOs so they cannot float when disabled.

9.2.1.1 Layout Example

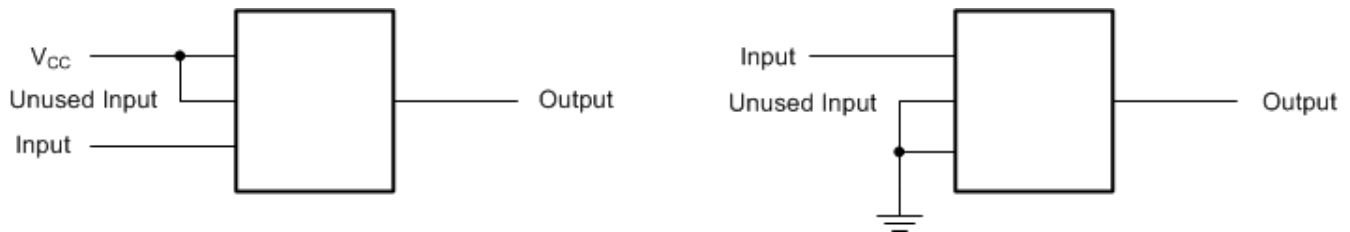


图 9-1. Layout Recommendation

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 10-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54AHC240	Click here	Click here	Click here	Click here	Click here
SN74AHC240	Click here	Click here	Click here	Click here	Click here

10.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

10.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

10.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.6 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9680701Q2A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9680701Q2A SNJ54AHC 240FK	Samples
5962-9680701QRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9680701QR A SNJ54AHC240J	Samples
5962-9680701QSA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9680701QS A SNJ54AHC240W	Samples
SN74AHC240DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC240	Samples
SN74AHC240N	ACTIVE	PDIP	N	20	20	RoHS & Non-Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74AHC240N	Samples
SN74AHC240NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AHC240	Samples
SN74AHC240PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HA240	Samples
SNJ54AHC240FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9680701Q2A SNJ54AHC 240FK	Samples
SNJ54AHC240J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9680701QR A SNJ54AHC240J	Samples
SNJ54AHC240W	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9680701QS A SNJ54AHC240W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN54AHC240, SN74AHC240 :

● Catalog : [SN74AHC240](#)

● Military : [SN54AHC240](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC240DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AHC240NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AHC240PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC240DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74AHC240NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74AHC240PWR	TSSOP	PW	20	2000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9680701Q2A	FK	LCCC	20	1	506.98	12.06	2030	NA
5962-9680701QSA	W	CFP	20	1	506.98	26.16	6220	NA
SN74AHC240N	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54AHC240FK	FK	LCCC	20	1	506.98	12.06	2030	NA
SNJ54AHC240W	W	CFP	20	1	506.98	26.16	6220	NA

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

GENERIC PACKAGE VIEW

FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4229370VA\

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within Mil-Std 1835 GDFP2-F20

PW0020A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

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