SN74LV4040A 12 位异步二进制计数器

1 特性

- 2V 至 5.5V V_{CC} 运行
- V_{OLP}（输出接地反弹）典型值小于 0.8V（V_{CC} = 3.3V，T_A = 25°C）
- V_{CC} = 3.3V、T_A = 25°C 时，V_{OHV}（输出 VOH 下冲）典型值为 2.3V
- 所有端口上均支持以混合模式电压运行
- 高开关输出电压比
- 低开关间串扰
- 单独的开关控制
- 极低输入电流
- I_{off} 支持局部断电模式运行
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范的要求

2 说明

'LV4040A 器件是 12 位异步二进制计数器，可从外部获得所有级的输出。

封装信息

器件型号	封装 [1]	封装尺寸 [2]
SN74LV4040A	N（PDIP，16）	19.3mm x 9.4mm
	D（SOIC，16）	9.9mm x 6mm
	NS（SOP，16）	10.2mm x 7.8mm
	DB（SSOP，16）	6.2mm x 7.8mm
	PW（TSSOP，16）	5mm x 6.4mm
	DGV（TVSOP，16）	3.6mm x 6.4mm
	RGY（VQFN，16）	4mm x 3.5mm

1. 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
2. 封装尺寸（长 x 宽）为标称值，并包括引脚（如适用）。

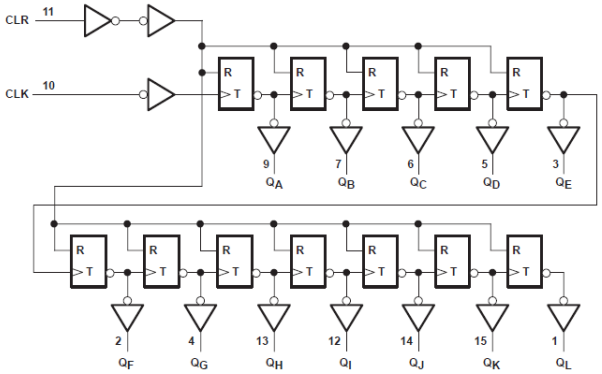

图 2-1. 逻辑图（正逻辑）

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3 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision I (May 2005) to Revision J (July 2023)	Page
• 添加了*封装信息* 表、*引脚功能* 表、*ESD 等级* 表、*热信息* 表、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分	1
• Updated thermal values for RθJA: D = 73 to 99.5, PW = 108 to 122.3, all values in °C/W	5

4 Pin Configuration and Functions

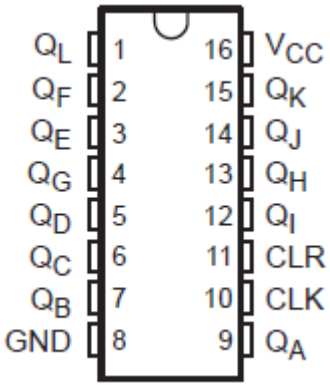
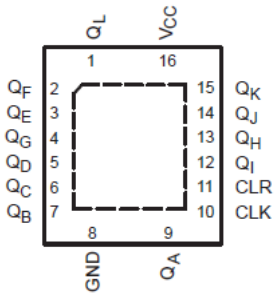


图 4-1. SN74LV4040A D, DB, DGV, N, NS, or PW Package (Top View)



A. NC - no internal connection

图 4-2. SN74LV4040A RGY Package (Top View)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
Q_L	1	O	Q_L output
Q_F	2	O	Q_F output
Q_E	3	O	Q_E output
Q_G	4	O	Q_G output
Q_D	5	O	Q_D output
Q_C	6	O	Q_C output
Q_B	7	O	Q_B output
GND	8	-	Ground
V_{CC}	9	-	Positive supply
Q_K	10	O	Q_K output
Q_J	11	O	Q_J output
Q_H	12	O	Q_H output
Q_I	13	O	Q_I output
CLR	14	I	Clear, active high
CLK	15	I	Clock, falling edge triggered
Q_A	16	O	Q_A output

1. I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	7	V
V_I	Input voltage range		-0.5	7	V
V_O	Voltage range applied to any output in the high-impedance or power-off state		-0.5	7	V
V_O	Output voltage range		−0.5 V to V_{CC}	0.5	V
I_{IK}	Input clamp current(2)	(V_I < 0)		−20	mA
I_{OK}	Output clamp current(2)	(V_O < 0)		±50	mA
I_O	Continuous output current	V_O = 0 to V_{CC}		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_{stg}	Storage temperature range		-65	150	℃

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over recommended operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		2	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 2.3 V to 2.7 V	V_{CC} × 0.7		
		V_{CC} = 3 V to 3.6 V	V_{CC} × 0.7		
		V_{CC} = 4.5 V to 5.5 V	V_{CC} × 0.7		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 2.3 V to 2.7 V		V_{CC} × 0.3	
		V_{CC} = 3 V to 3.6 V		V_{CC} × 0.3	
		V_{CC} = 4.5 V to 5.5 V		V_{CC} × 0.3	
V_I	Input voltage		0	5.5	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 2 V		− 50	μA
		V_{CC} = 2.3 V to 2.7 V		− 2	mA
		V_{CC} = 3 V to 3.6 V		− 6	
		V_{CC} = 4.5 V to 5.5 V		− 12	
I_{OL}	Low-level output current	V_{CC} = 2 V		50	
		V_{CC} = 2.3 V to 2.7 V		2	
		V_{CC} = 3 V to 3.6 V		6	
		V_{CC} = 4.5 V to 5.5 V		12	
Δt/Δv	Input transition rise/fall time	V_{CC} = 2.3 V to 2.7 V		200	ns
		V_{CC} = 3 V to 3.6 V		100	
		V_{CC} = 4.5 V to 5.5 V		20	
T_A	Operating free-air temperature		-40	85	℃

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5.4 Thermal Information

THERMAL METRIC[1]		D (SOIC)	DB (SSOP)	DGV (TVSOP)	N (PDIP)	NS (SOP)	PW (TSSOP)	RGY (VQFN)	UNIT
		16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	16 PINS	
$R_{θJA}$	Junction-to-ambient thermal resistance	99.5	82	120	67	64	122.3	39	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics.*

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	SN74LV4040A			UNIT
			MIN	TYP	MAX	
V_{OH}	I_{OH} = −50 μA	2 V to 5.5 V	V_{CC} − 0.1			V
	I_{OH} = −2 mA	2.3 V	2			
	I_{OH} = −6 mA	3 V	2.48			
	I_{OH} = −12 mA	4.5 V	3.8			
V_{OL}	I_{OL} = 50 μA	2 V to 5.5 V			0.1	V
	I_{OL} = 2 mA	2.3 V			0.4	
	I_{OL} = 6 mA	3 V			0.44	
	I_{OL} = 12 mA	4.5 V			0.55	
I_I	V_I = 5.5 V or GND	0 to 5.5 V			±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			20	μA
I_{off}	V_I or V_O = 0 to 5.5 V	0			5	μA
C_i	V_I = V_{CC} or GND	3.3 V		1.9		pF

5.6 Timing Requirements, V_{CC} = 2.5 V ± 0.2 V

timing requirements over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted)

			T_A = 25°C		SN74LV4040A		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low	7		7		ns
		CLR high	6.5		6.5		
t_{su}	Setup time	CLR inactive before CLK↓	6.5		6.5		

5.7 Timing Requirements, V_{CC} = 3.3 V ± 0.3 V

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted)

			T_A = 25°C		SN74LV4040A		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low	5		5		ns
		CLR high	5		5		
t_{su}	Setup time	CLR inactive before CLK↓	5		5		

5.8 Timing Requirements, V_{CC} = 5 V ± 0.5 V

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted)

			T_A = 25°C		SN74LV4040A		UNIT
			MIN	MAX	MIN	MAX	
t_w	Pulse duration	CLK high or low	5		5		ns
		CLR high	5		5		
t_{su}	Setup time	CLR inactive before CLK↓	5		5		

5.9 Switching Characteristics, V_{CC} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, V_{CC} = 2.5 V ± 0.2 V (unless otherwise noted) (Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN74LV4040A		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	50[1]	115[1]		40[1]		MHz
			C_L = 50 pF	40	95		35		
t_{PLH}	CLK	Q_A	C_L = 15 pF		8.7[1]	19.4[1]	1[1]	23[1]	ns
t_{PHL}					8.7[1]	19.4[1]	1[1]	23[1]	
t_{PHL}	CLR	Any Q	C_L = 15 pF		9.3[1]	19.9[1]	1[1]	24[1]	
t_{PLH}	$\overline{CLK}$	Q_A	C_L = 50 pF		10.5	24.1	1	28	
t_{PHL}					10.5	24.1	1	28	
t_{PHL}	CLR	Any Q	C_L = 50 pF		11.7	24.5	1	28	ns
Δt_{pd}	Q_n	Q_{n+1}	C_L = 50 pF		1.7	5.9		7	

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

5.10 Switching Characteristics, V_{CC} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 (unless otherwise noted) (Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN74LV4040A		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	75[1]	160[1]		75		MHz
			C_L = 50 pF	55	130		50		
t_{PLH}	CLK	Q_A	C_L = 15 pF		6.1[1]	11.9[1]	1	14	ns
t_{PHL}					6.1[1]	11.9[1]	1	14	ns
t_{PHL}	CLR	Any Q	C_L = 15 pF		7.1[1]	12.8[1]	1	15	ns
t_{PLH}	$\overline{CLK}$	Q_A	C_L = 50 pF		7.5	15.4	1	17.5	ns
t_{PHL}					7.5	15.4	1	17.5	ns
t_{PHL}	CLR	Any Q	C_L = 50 pF		9	16.3	1	18.5	ns
Δt_{pd}	Q_n	Q_{n+1}	C_L = 50 pF		1.2	4.4		5	ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

5.11 Switching Characteristics, V_{CC} = 5 V ± 0.5 V

over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (Load Circuit and Voltage Waveforms)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C			SN74LV4040A		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			C_L = 15 pF	150[1]	235[1]		125		MHz
			C_L = 50 pF	95	185		80		
t_{PLH}	CLK	Q_A	C_L = 15 pF		4.2[1]	7.3[1]	1	8.5	ns
t_{PHL}					4.2[1]	7.3[1]	1	8.5	ns
t_{PHL}	CLR	Any Q	C_L = 15 pF		5.3[1]	8.6[1]	1	10	ns
t_{PLH}	$\overline{CLK}$	Q_A	C_L = 50 pF		5.3	9.3	1	10.5	ns
t_{PHL}					5.3	9.3	1	10.5	ns
t_{PHL}	CLR	Any Q	C_L = 50 pF		6.8	10.6	1	12	ns
Δt_{pd}	Q_n	Q_{n+1}	C_L = 50 pF		0.8	3.1		3.5	ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

5.12 Noise Characteristics

V_{CC} = 3.3 V, C_L = 50 pF, T_A = 25°C

PARAMETER[(1)]		SN74LV4040A			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.5	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		− 0.5	− 0.8	V
$V_{IH(D)}$	High-level dynamic input voltage	2.31			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	V

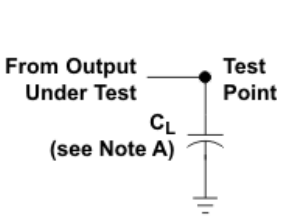
(1) Characteristics for surface-mount packages only.

5.13 Operating Characteristics

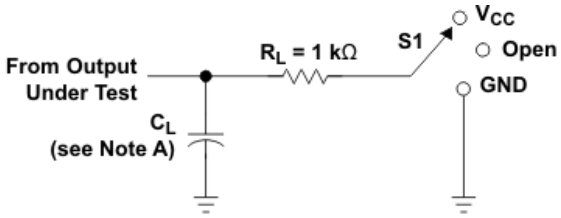
T_A = 25°C

PARAMETER		TEST CONDITIONS		V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = 50 pF,	f = 10 MHz	3.3 V	11.9	pF
				5 V	13.1	

6 Parameter Measurement Information

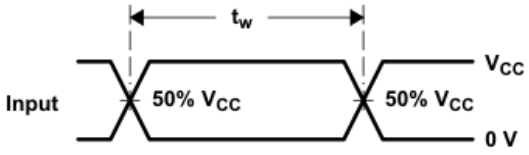


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

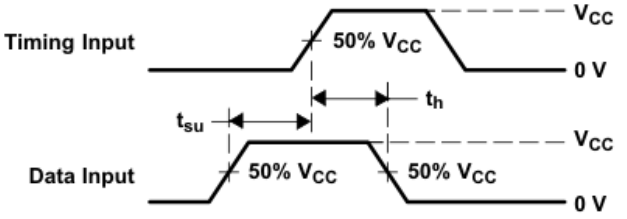


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

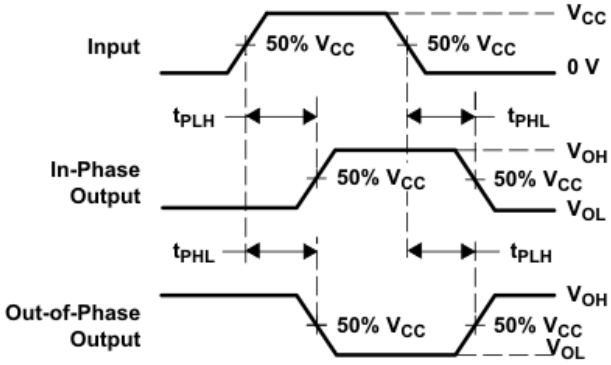
LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS



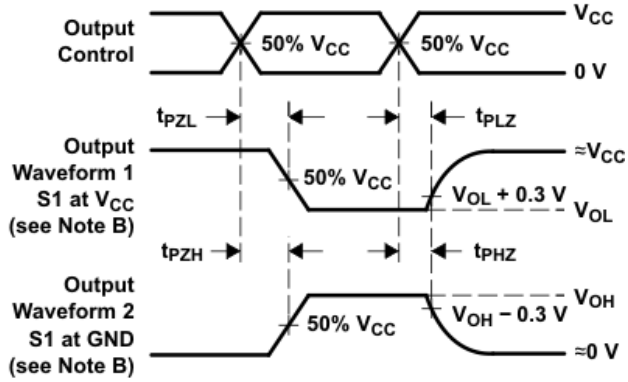
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, and t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

图 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

The ’LV4040A devices are 12-bit asynchronous binary counters with the outputs of all stages available externally. A high level at the clear (CLR) input asynchronously clears the counter and resets all outputs low. The count is advanced on a high-to-low transition at the clock (CLK) input. Applications include time-delay circuits, counter controls, and frequency-dividing circuits.

These devices are fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

7.2 Functional Block Diagram

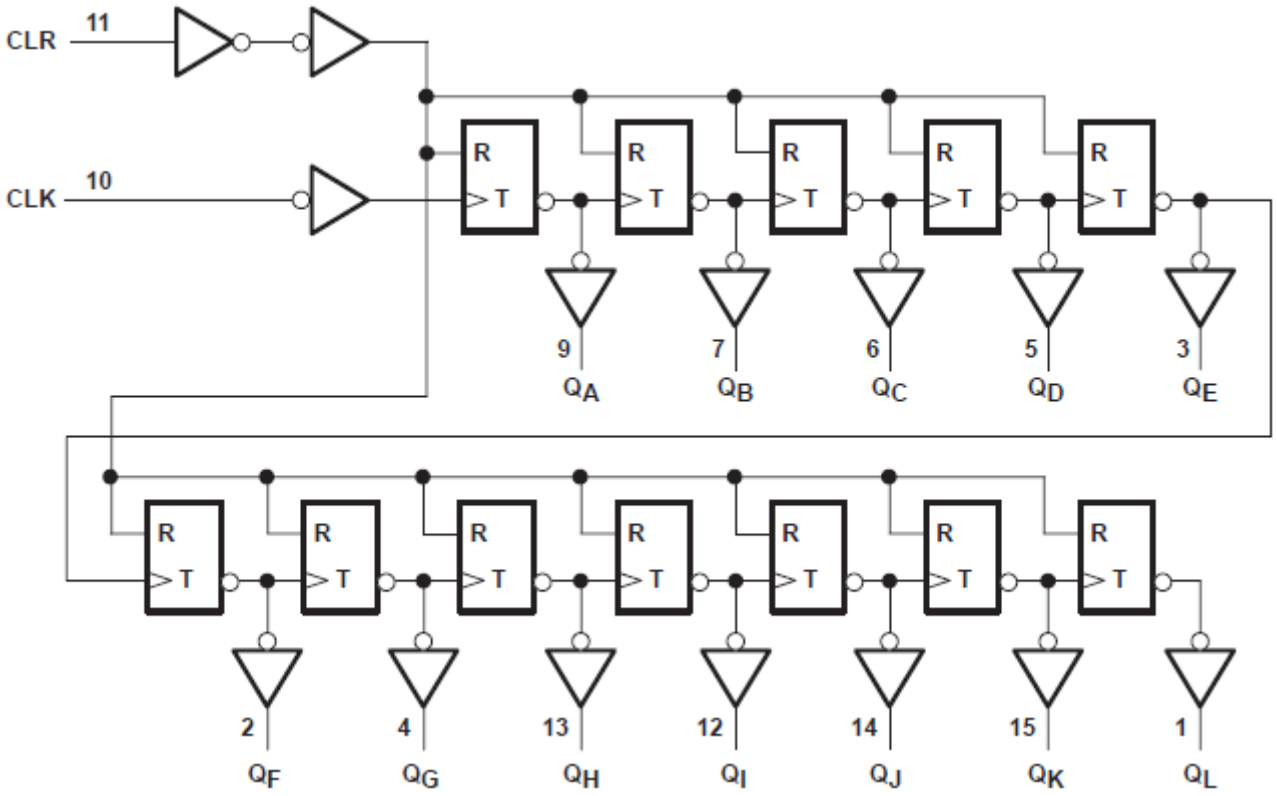


图 7-1. Logic Diagram (Positive Logic)

7.3 Device Functional Modes

表 7-1. Function Table (Each Buffer)

INPUTS		FUNCTION
CLK	CLR	
↑	L	No change
↓	L	Advance to next stage
X	H	All outputs L

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Documentation Support (Analog)

8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74LV4040A	Click here	Click here	Click here	Click here	Click here

8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

8.4 Trademarks

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8.5 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要声明和免责声明

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