TEXAS INSTRUMENTS

SN74TVC3306

SCDS112D – MARCH 2001 – REVISED DECEMBER 2014

SN74TVC3306 Dual Voltage Clamp

1 Features

- Designed to Be Used in Voltage-Limiting Applications
- 3.5-Ω On-State Connection Between Ports A and B
- Flow-Through Pinout for Ease of Printed Circuit Board Trace Routing
- Direct Interface With GTL+ Levels
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model
  - 200-V Machine Model
  - 1000-V Charged-Device Model

2 Applications

- Voltage Level Translation
- Signal Switching
- Bus Isolation
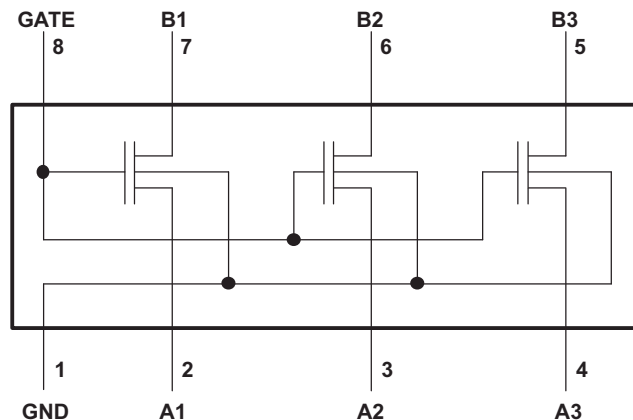
3 Description

The SN74TVC3306 device provides three parallel NMOS pass transistors with a common unbuffered gate. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device can be used as a dual switch, with the gates cascaded together to a reference transistor. The low-voltage side of each pass transistor is limited to a voltage set by the reference transistor. This is done to protect components with inputs that are sensitive to high-state voltage-level overshoots.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74TVC3306	SM8 (8)	3.00 mm x 2.80 mm
	US8 (8)	2.30 mm x 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic

The SN74TVC3306 device has bidirectional capability across many voltage levels. The voltage levels documented in this data sheet are examples.

Table of Contents

5 Revision History

Changes from Revision C (March 2002) to Revision D   **Page**

- Added *Applications*, *Device Information* table, *Pin Functions* table, *Handling Ratings* table, *Thermal Information* table, *Typical Characteristics*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. 1

- Deleted *Ordering Information* table. 1

- Changed the R_{ON} parameter in the *Electrical Characersitics* table. 5

6 Pin Configuration and Functions

Top View

DCT OR DCU PACKAGE
(TOP VIEW)

```
GND  [ 1      8 ]  GATE
 A1  [ 2      7 ]  B1
 A2  [ 3      6 ]  B2
 A3  [ 4      5 ]  B3
```
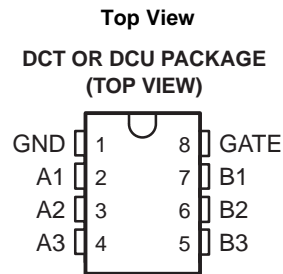
Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
A1	2	I/O	I/O of gate 1
A2	3	I/O	I/O of gate 1
A3	4	I/O	I/O of gate 1
B1	5	I/O	I/O of gate 2
B2	6	I/O	I/O of gate 2
B3	7	I/O	I/O of gate 2
GATE	8	I	Gate pin. Set high to enable the switches. Connect to B1 (V_{BIAS}) for translation application.
GND	1	—	Ground

7 Specifications

7.1 Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_I	Input voltage range[2]		−0.5	7	V
$V_{I/O}$	Input/output voltage range[2]		−0.5	7	V
	Continuous channel current			128	mA
I_{IK}	Input clamp current	$V_I < 0$		−50	mA
T_{stg}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and input/output negative-voltage ratings may be exceeded if the input and input/output clamp-current ratings are observed.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]	2000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	MAX	UNIT
$V_{I/O}$	Input/output voltage	0	5	V
V_{GATE}	GATE voltage	0	5	V
I_{PASS}	Pass transistor current		64	mA
T_A	Operating free-air temperature	−40	85	°C

7.4 Thermal Information

		SN74TVC3306		UNIT
THERMAL METRIC[1]		DCT	DCU	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	220	227	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP[1]	MAX	UNIT
V_{IK}	I_I = -18 mA,	V_{GATE} = 0				−1.2	V
I_{IH}	V_I = 5 V,	V_{GATE} = 0				5	µA
$C_{i(GATE)}$	V_I = 3 V or 0				11		pF
$C_{io(off)}$	V_O = 3 V or 0,	V_{GATE} = 0			4	6	pF
$C_{io(on)}$	V_O = 3 V or 0,	V_{GATE} = 3 V			10.5	12.5	pF
R_{on} [2]	V_I = 0,	I_O = 64 mA	V_{GATE} = 4.5 V		3.5	5.5	Ω
			V_{GATE} = 3 V		4.7	7	
			V_{GATE} = 2.3 V		6.3	9.5	
	V_I = 2.4 V,	I_O = 15 mA	V_{GATE} = 4.5 V		4.8	7.5	
	V_I = 1.8 V,	I_O = 15 mA	V_{GATE} = 4.5 V		4.5	5	

(1) All typical values are at T_A = 25°C.
(2) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

7.6 Switching Characteristics (AC, V_{GATE} = 3.3 V, Translating Down)

over recommended operating free-air temperature range, V_{GATE} = 3.3 V, V_{IH} = 3.3 V, V_{IL} = 0, and V_M = 1.15 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	0	0.8	0	0.6	0	0.3	ns
t_{PHL}			0	1.2	0	1	0	0.5	

7.7 Switching Characteristics (AC, V_{GATE} = 2.5 V, Translating Down)

over recommended operating free-air temperature range, V_{GATE} = 2.5 V, V_{IH} = 2.5 V, V_{IL} = 0, and V_M = 0.75 V (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	0	1	0	0.7	0	0.4	ns
t_{PHL}			0	1.3	0	1	0	0.6	

7.8 Switching Characteristics (AC, V_{GATE} = 3.3 V, Translating Up)

over recommended operating free-air temperature range, V_{GATE} = 3.3 V, V_{IH} = 2.3 V, V_{IL} = 0, V_T = 3.3 V, V_M = 1.15 V, and R_L = 300 Ω (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	0	0.9	0	0.6	0	0.4	ns
t_{PHL}			0	1.4	0	1.1	0	0.7	

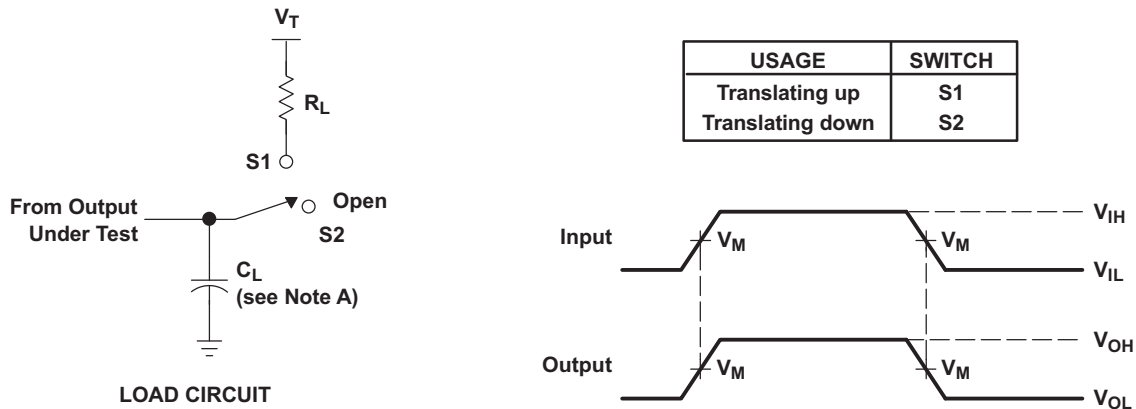## 7.9 Switching Characteristics (AC, V_{GATE} = 2.5 V, Translating Up)

over recommended operating free-air temperature range, V_{GATE} = 2.5 V, V_{IH} = 1.5 V, V_{IL} = 0, V_T = 2.5 V, V_M = 0.75 V, and R_L = 300 Ω (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	0	1	0	0.6	0	0.4	ns
t_{PHL}			0	1.3	0	1.3	0	0.8	

7.10 Typical Characteristics

Figure 1. R_{ON} vs V_{IN} at I_{IN} = 15 mA.
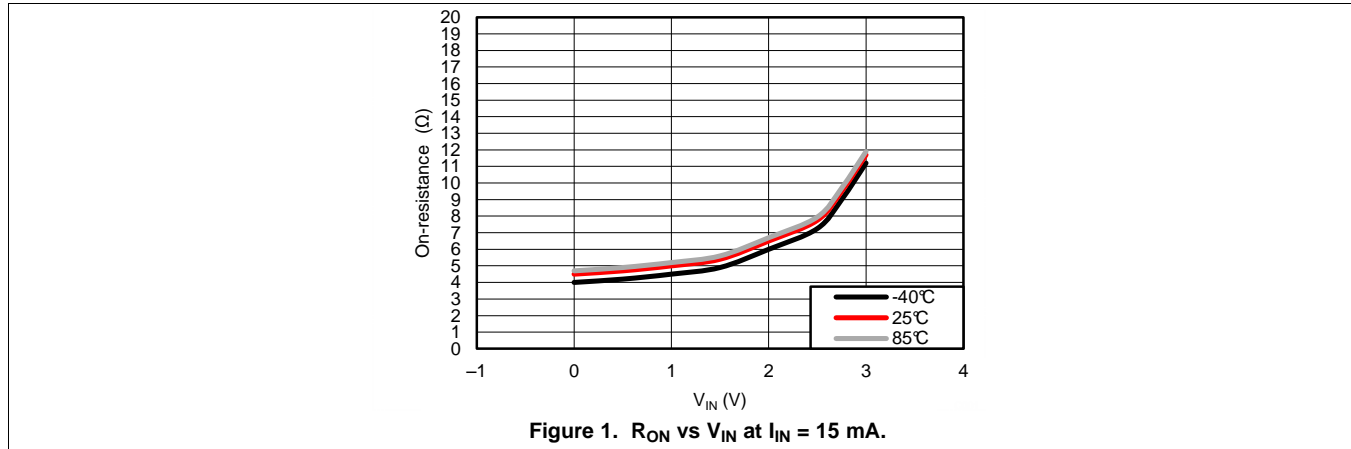
8 Parameter Measurement Information

USAGE	SWITCH
Translating up	S1
Translating down	S2

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
C. The outputs are measured one at a time, with one transition per measurement.

**Figure 2. Load Circuit for Outputs**

Product Folder Links: *SN74TVC3306*

9 Detailed Description

9.1 Overview

The SN74TVC3306 device provides three parallel NMOS pass transistors with a common unbuffered gate. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device can be used as a dual switch, with the gates cascaded together to a reference transistor. The low-voltage side of each pass transistor is limited to a voltage set by the reference transistor. This is done to protect components with inputs that are sensitive to high-state voltage-level overshoots.

9.2 Functional Block Diagram
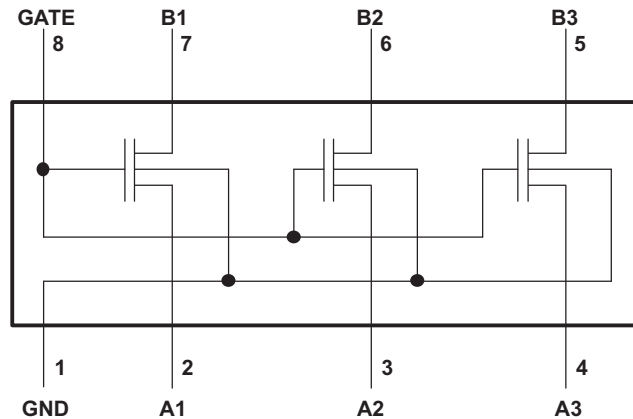
The SN74TVC3306 device has bidirectional capability across many voltage levels. The voltage levels documented in this data sheet are examples.

9.3 Feature Description

9.3.1 Voltage Clamping

The internal NMOS transistors allow the SN74TVC3306 device to act as a voltage clamp and be configured as a voltage level translator. See *Application and Implementation*.

9.4 Device Functional Modes

9.4.1 Voltage Clamping

Whenever the signal on the inputs on the side with V_{REF} goes higher than V_{REF}, the voltage clamps on the opposite side to the value of V_{DPU} due to the pullup resistors. In this case, the voltage is translating up. See *Application and Implementation*.

9.4.2 Voltage Passing

Whenever the signal on the inputs on the VREF side is lower than VREF, the signal will pass to the other side as intended. In this case, the low pulse is staying low (no translation). See *Application and Implementation*.

10 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

Because of the voltage-clamping mechanism, the SN74TVC3306 device performs best as a level translator for signals that have sharp edges (as opposed to analog audio signals).

10.2 Typical Application
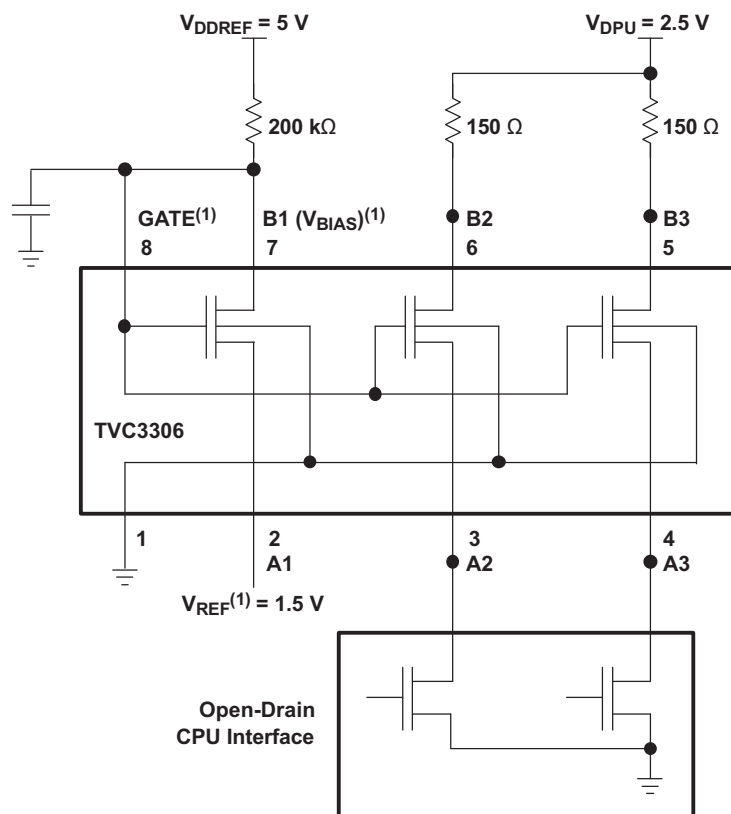
V_{REF} and V_{BIAS} can be applied to any one of the pass transistors. GATE must be connected externally to V_{BIAS}

Figure 3. Typical Application Circuit

Typical Application (continued)

10.2.1 Design Requirements

10.2.1.1 Application Operating Conditions

Application Operating Conditions (See Figure 3)

		MIN	TYP[1]	MAX	UNIT
V_{BIAS}	BIAS voltage	V_{REF} + 0.6	2.1	5	V
V_{GATE}	GATE voltage	V_{REF} + 0.6	2.1	5	V
V_{REF}	Reference voltage	0	1.5	4.4	V
V_{DPU}	Drain pullup voltage	2.36	2.5	2.64	V
I_{PASS}	Pass-transistor current		14		mA
I_{REF}	Reference-transistor current		5		µA
T_A	Operating free-air temperature	−40		85	°C

(1)   All typical values are at T_A = 25°C.

10.2.2 Detailed Design Procedure

For the clamping configuration, the common GATE input must be connected to one side (An or Bn) of any one of the pass transistors, making that the V_{BIAS} connection of the reference transistor and the opposite side (Bn or An) the V_{REF} connection. When V_{BIAS} is connected through a 200-kΩ resistor to a 3-V to 5.5-V V_{CC} supply and V_{REF} is set to 0 V to V_{CC} − 0.6 V, the output of each switch has a maximum clamp voltage equal to V_{REF}. A filter capacitor on V_{BIAS} is recommended.

10.2.3 Application Curves

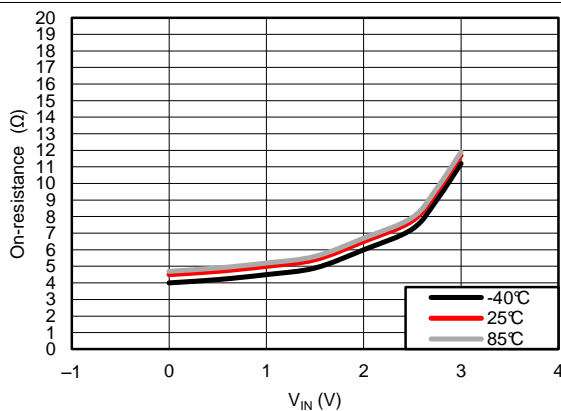**Figure 4. On-resistance vs VIN (A to B, 15 mA current)**

11 Power Supply Recommendations

A 200-kΩ resistor is recommended from the input to V_{CC} when the device is being used as a voltage clamp. A filter capacitor is recommended on B1 as well.

12 Layout

12.1 Layout Guidelines

If used, the filter capacitor should be placed as close to the input of the device as possible.
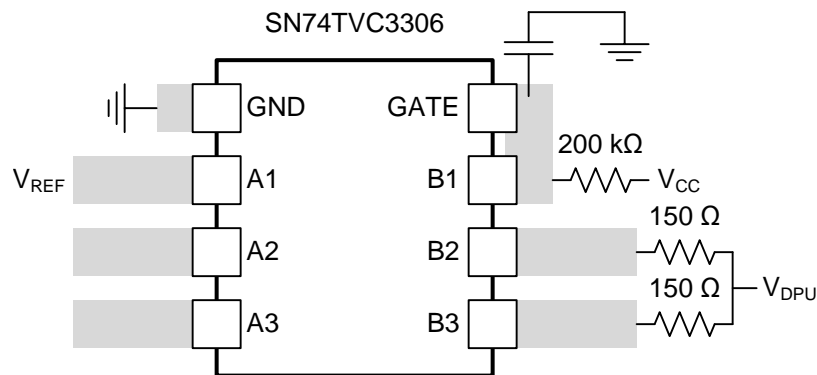
12.2 Layout Example

Figure 5. Layout example for voltage-clamp configuration

13 Device and Documentation Support

13.1 Trademarks

All trademarks are the property of their respective owners.

13.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74TVC3306DCTR	ACTIVE	SM8	DCT	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FA6 (S, Y)	Samples
SN74TVC3306DCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	(29O4, FA6P, FA6S)	Samples
SN74TVC3306DCURG4	LIFEBUY	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FA6S	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74TVC3306DCTR	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74TVC3306DCTR	SM8	DCT	8	3000	177.8	12.4	3.45	4.4	1.45	4.0	12.0	Q3
SN74TVC3306DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74TVC3306DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74TVC3306DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74TVC3306DCTR	SM8	DCT	8	3000	182.0	182.0	20.0
SN74TVC3306DCTR	SM8	DCT	8	3000	183.0	183.0	20.0
SN74TVC3306DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
SN74TVC3306DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74TVC3306DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0

$\frac{3.2}{3.0}$ TYP

A

PIN 1 INDEX AREA

1

8

6X $\boxed{0.5}$

2X

$\boxed{1.5}$

$\frac{2.1}{1.9}$
NOTE 3

4

5

B

$\frac{2.4}{2.2}$
NOTE 3

8X $\frac{0.25}{0.17}$

$\boxed{\oplus\ \boxed{0.08\,\text{Ⓜ}}\ C\ A\ B}$

C

$\boxed{\frown\ \boxed{0.1}\ C}$

SEATING
PLANE

SEE DETAIL A

(0.13) TYP

$\boxed{0.12}$
GAGE PLANE

0°-6°

$\frac{0.35}{0.20}$

$\frac{0.9}{0.6}$

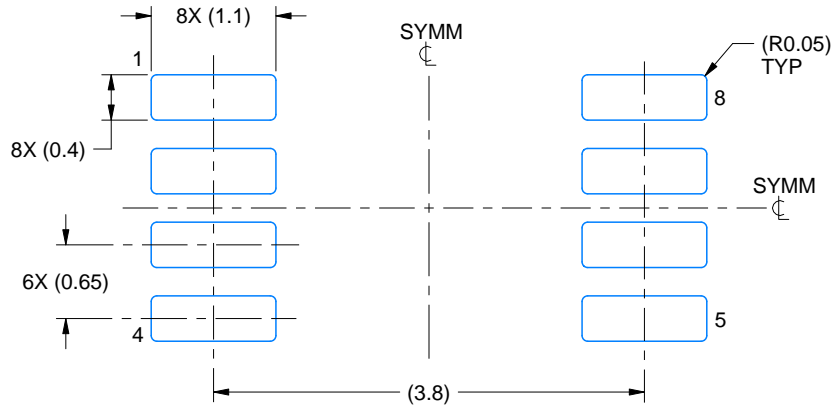$\frac{0.1}{0.0}$

DETAIL A
TYPICAL
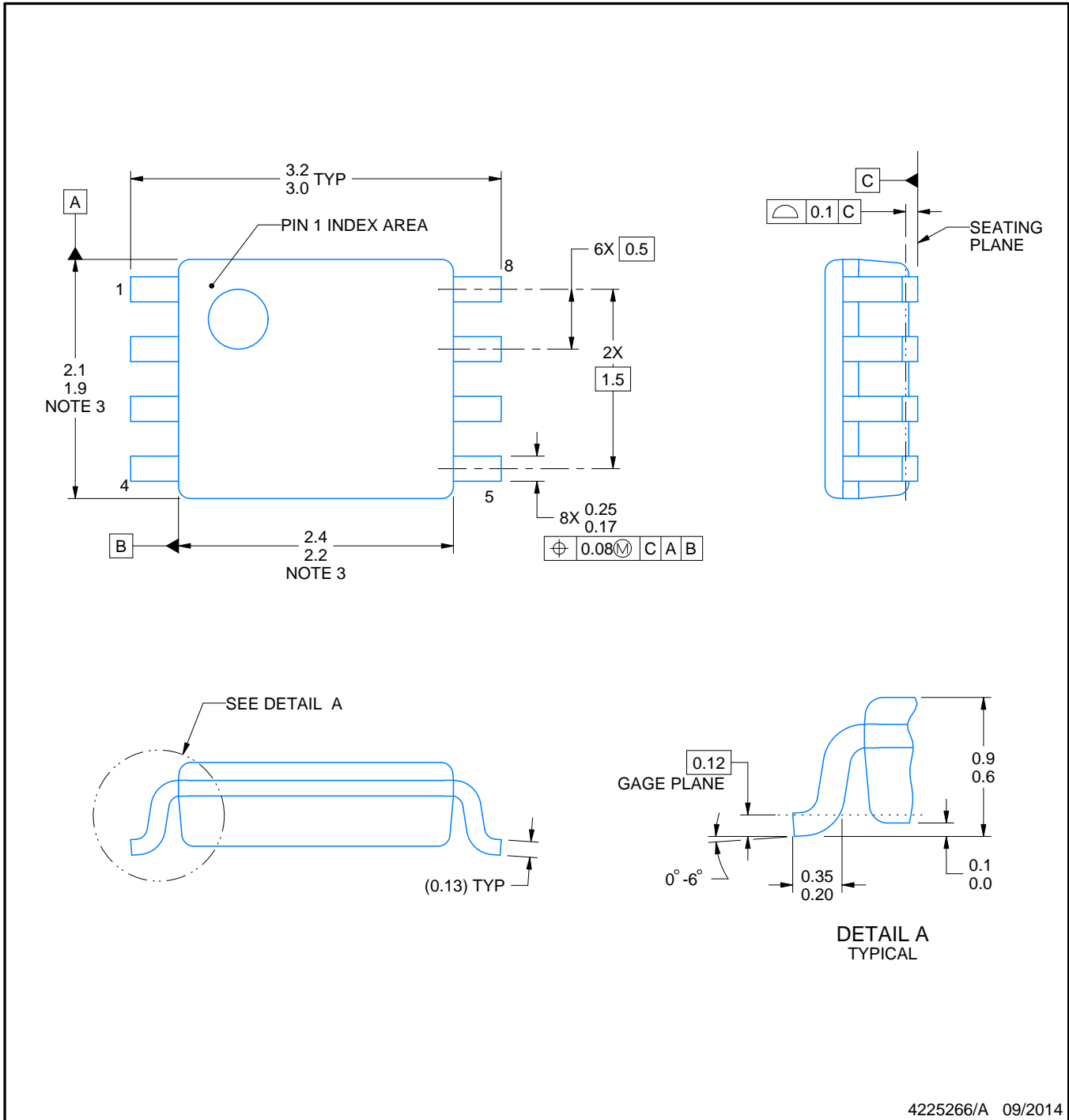
4225266/A 09/2014

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.

TEXAS INSTRUMENTS

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8X (0.85)

SYMM

SEE SOLDER MASK
DETAILS

(R0.05) TYP

8X (0.3)   1

8

SYMM

6X (0.5)

4

5

(3.1)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

NON-SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

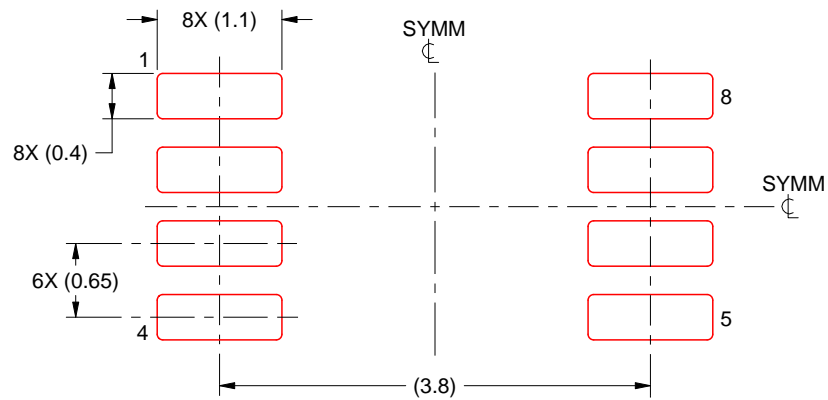4225266/A   09/2014

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

TEXAS
INSTRUMENTS
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8X (0.85)

8X (0.3)

SYMM

(R0.05) TYP

1

8

6X (0.5)

SYMM

4

5

(3.1)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A   09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

4220784/C   06/2021
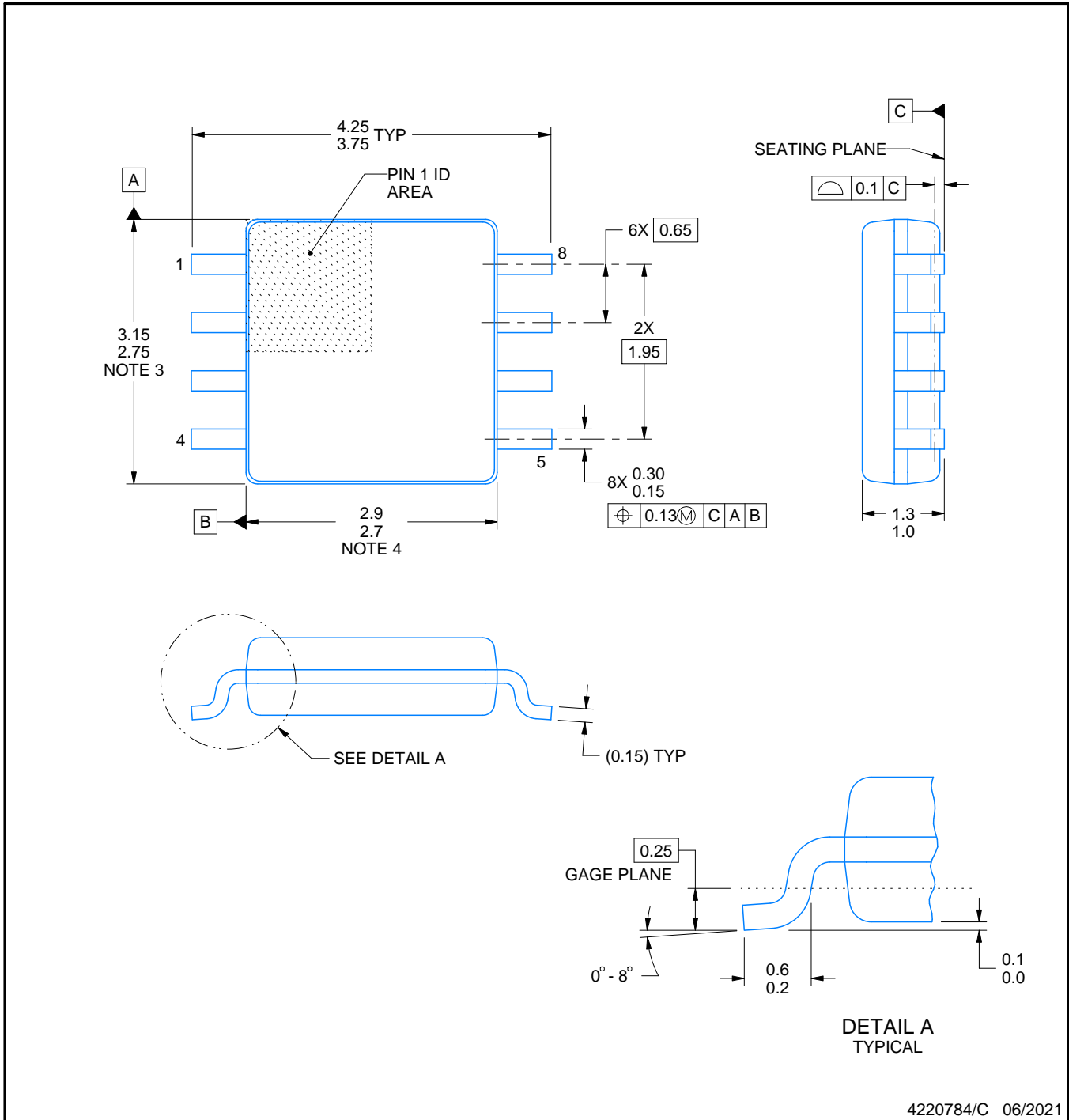
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

8X (1.1)

SYMM

(R0.05)
TYP

1

8

8X (0.4)

SYMM

6X (0.65)

4

5

(3.8)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

EXPOSED METAL

0.07 MAX
ALL AROUND

0.07 MIN
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED
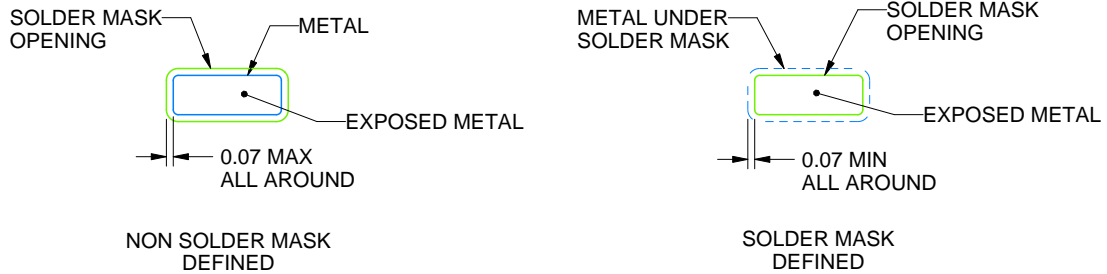
SOLDER MASK DETAILS

4220784/C   06/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

8X (1.1)

8X (0.4)

6X (0.65)

(3.8)

SYMM

SYMM

4220784/C   06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER