

SN75ALS174A 四路差动线路驱动器

1 特性

- 符合或超过 ANSI EIA/TIA-422-B 和 RS-485 标准要求
- 高速高级低功耗肖特基电路
- 在串行和并行应用中均可实现高达 20Mbit/s 的运行速率
- 适用于嘈杂环境中的长距离总线线路上的多点传输
- 最高 55mA 低电源电流要求
- 宽正负输入/输出总线电压范围
- 驱动器输出容量：60mA
- 热关断保护
- 驱动器正负电流限制
- 可借助 SN75174 实现功能互换

2 应用

- 电机驱动器
- 工厂自动化与控制

3 说明

SN75ALS174A 是一款具有三态差动输出的四路线路驱动器。设计可满足 ANSI 标准 EIA/TIA-422-B 和 RS-485 的要求。该器件经优化，能够以高达 20Mbit/s 的速率实现平衡多点总线传输。

每个驱动器都具有宽正负共模输出电压范围，使其适用于嘈杂环境中的同线应用。

SN75ALS174A 可提供正负电流限制和热关断功能，避免总线线路出现线路故障状况。在结温约 150°C 时关闭电源。

SN75ALS174A 的工作温度范围是 0°C 至 70°C。

器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
SN75ALS174A	PDIP (N) (16)	19.3mm x 6.50mm
	SOIC (DW) (20)	12.8mm x 7.50mm
	TSSOP (PW) (20)	6.50mm x 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

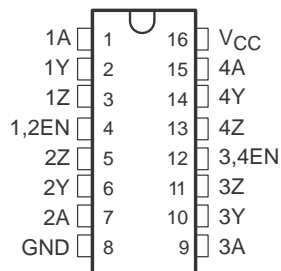
功能表 (每个驱动器) (1) (2)

INPUT A	启用	输出	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

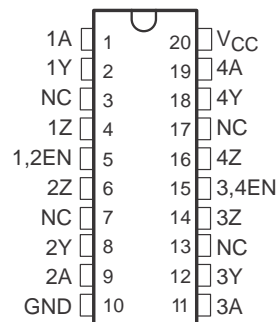
(1) H = 高电平, L = 低电平, X = 不相关。

(2) Z = 高阻抗 (关闭)

N 封装 (顶视图)



DW、PW 封装 (顶视图)



NC – No internal connection



目录

1 特性 1 2 应用 1 3 说明 1 4 修订历史记录 2 5 Specifications 3 5.1 Absolute Maximum Ratings 3 5.2 Dissipation Rating Table 3 5.3 Recommended Operating Conditions 3 5.4 Electrical Characteristics 4 5.5 Switching Characteristics 4	6 Parameter Measurement Information 5 7 器件和文档支持 8 7.1 文档支持 8 7.2 接收文档更新通知 8 7.3 社区资源 8 7.4 商标 8 7.5 静电放电警告 8 7.6 Glossary 8 8 机械、封装和可订购信息 8
--	--

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision E (April 1998) to Revision F	Page
• 添加了 PW 封装，应用列表、器件信息表、器件和文档支持部分和机械、封装和可订购信息部分。	1

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
Supply voltage, V_{CC} ⁽²⁾		7	V
Input voltage, V_I		7	V
Output voltage range, V_O	–9	14	V
Continuous total dissipation	See the <i>Dissipation Rating</i> table		
Storage temperature, T_{stg}	–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network GND.

5.2 Dissipation Rating Table

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 85^\circ\text{C}$ POWER RATING
DW	1125 mW	9.0 mW/°C	720 mW	596 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.75	5	5.25	V
V_{IH} High-level input voltage	2			V
V_{IL} Low-level input voltage			0.8	V
V_{OC} Common-mode output voltage			12	V
			–7	V
I_{OH} High-level output current			–60	mA
I_{OL} Low-level output current			60	mA
T_A Operating free-air temperature	0		70	°C

5.4 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V _{IK}	Input clamp voltage	I _I = -18 mA			-1.5	V
V _O	Output voltage	I _O = 0	0		6	V
V _{OD1}	Differential output voltage	I _O = 0	1.5		6	V
V _{OD2}	Differential output voltage	R _L = 100 Ω	See Note Figure 1		1/2 V _{OD1} or 2 ⁽²⁾	V
		R _L = 54 Ω	1.5	2.5	5	V
V _{OD3}	Differential output voltage	See ⁽³⁾	1.5		5	V
Δ V _{OD}	Change in magnitude of differential output voltage ⁽⁴⁾	R _L = 54 Ω or 100 Ω	See Figure 1		±0.2	V
V _{OC}	Common-mode output voltage ⁽⁵⁾	R _L = 54 Ω or 100 Ω	See Figure 1		3	V
					-1	V
Δ V _{OC}	Change in magnitude of common-mode output voltage ⁽⁴⁾	R _L = 54 Ω or 100 Ω	See Figure 1		±0.2	V
I _O	Output current with power off	V _{CC} = 0, V _O = -7 V to 12 V			±100	μA
I _{OZ}	High-impedance-state output current	V _O = -7 V to 12 V			±100	μA
I _{IH}	High-level input current	V _I = 2.7 V			20	μA
I _{IL}	Low-level input current	V _I = 0.4 V			-100	μA
I _{OS}	Short-circuit output current	V _O = -7 V to 12 V			±250	mA
I _{CC}	Supply current (all drivers)	No load	Outputs enabled	36	55	mA
			Outputs disabled	16	30	mA

 (1) All typical values are at V_{CC} = 5 V and T_A = 25°C.

 (2) The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.

(3) See EIA Standard RS-485, Figures 3-5, Test Termination Measurement 2.

 (4) Δ|V_{OD}| and Δ|V_{OC}| are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

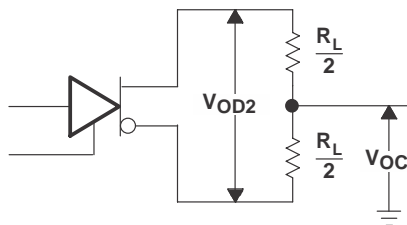
 (5) In ANSI Standard EIA/TIA-422-B, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

5.5 Switching Characteristics

 over operating free-air temperature range (unless otherwise noted), C_L = 50 pF

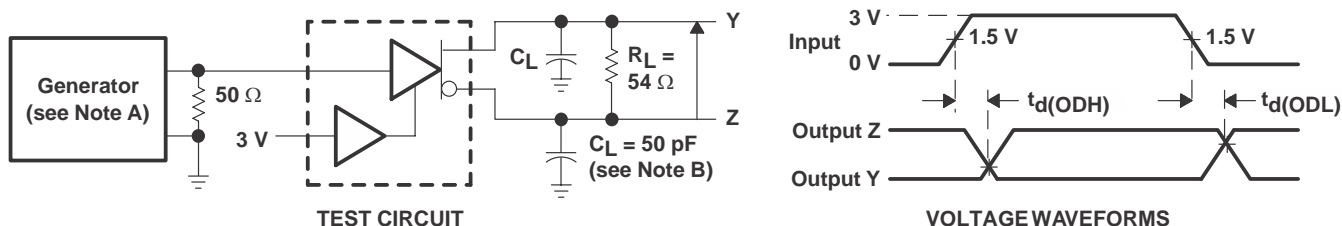
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{d(OD)}	Differential output delay time	R _L = 54 Ω, See Figure 2	9	15	22	ns
t _{PZH}	Output enable time to high level	R _L = 110 Ω, See Figure 3	30	45	70	ns
t _{PZL}	Output enable time to low level	R _L = 110 Ω, See Figure 4	25	40	65	ns
t _{PHZ}	Output disable time from high level	R _L = 110 Ω, See Figure 3	10	20	35	ns
t _{PLZ}	Output disable time from low level	R _L = 110 Ω, See Figure 4	10	30	45	ns

6 Parameter Measurement Information



Copyright © 2018, Texas Instruments Incorporated

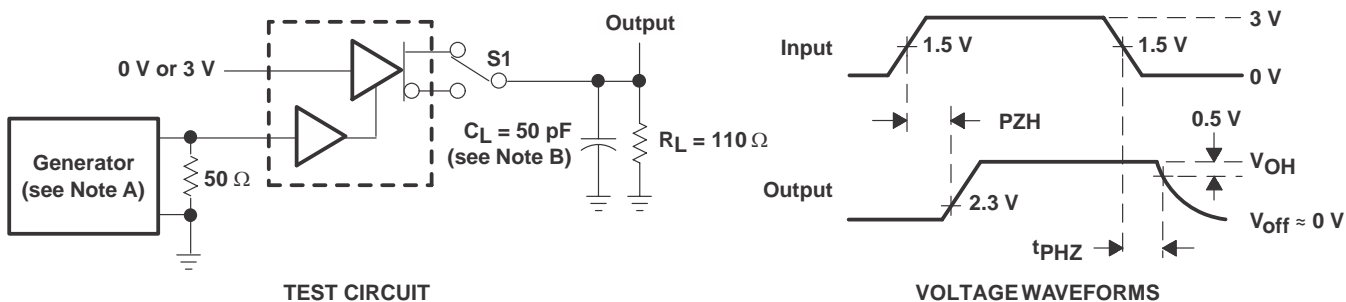
Figure 1. Differential and Common-Mode Output Voltages



Copyright © 2018, Texas Instruments Incorporated

- A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, $Z_0 = 50 \Omega$, duty cycle = 50%, t_r 5 ns, t_f 5 ns.
- B. C_L includes probe and stray capacitance.

Figure 2. Differential-Output Test Circuit and Delay and Transition Times Voltage Waveforms

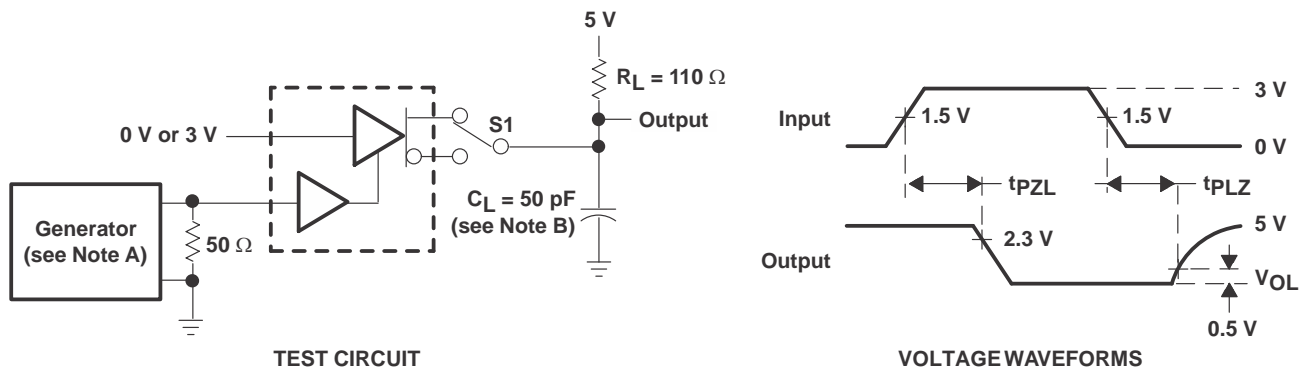


Copyright © 2018, Texas Instruments Incorporated

- A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, $Z_0 = 50 \Omega$, duty cycle = 50%, t_r 5 ns, t_f 5 ns.
- B. C_L includes probe and stray capacitance.

Figure 3. Test Circuit and Voltage Waveforms, t_{PHZ} and t_{PHZ}

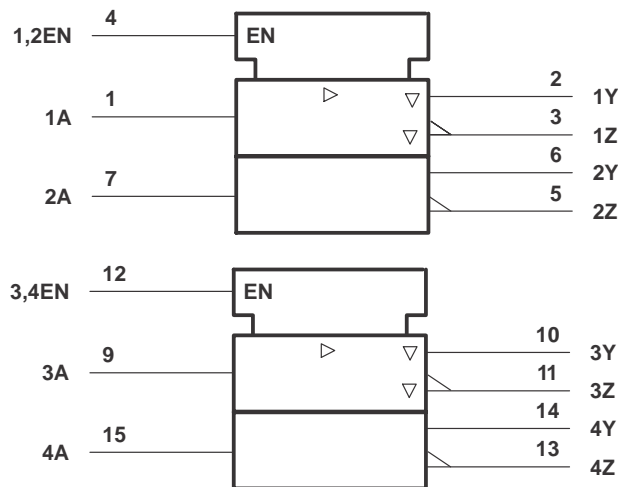
Parameter Measurement Information (continued)



Copyright © 2018, Texas Instruments Incorporated

- A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, $Z_O = 50 \Omega$, duty cycle = 50%, $t_r = 5 \text{ ns}$, $t_f = 5 \text{ ns}$.
- B. C_L includes probe and stray capacitance.

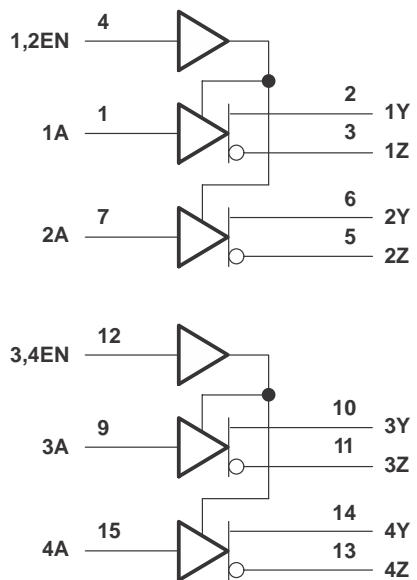
Figure 4. Test Circuit and Voltage Waveforms, t_{PZL} and t_{PLZ}



- (1) This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
- (2) Pin numbers shown are for the N package.

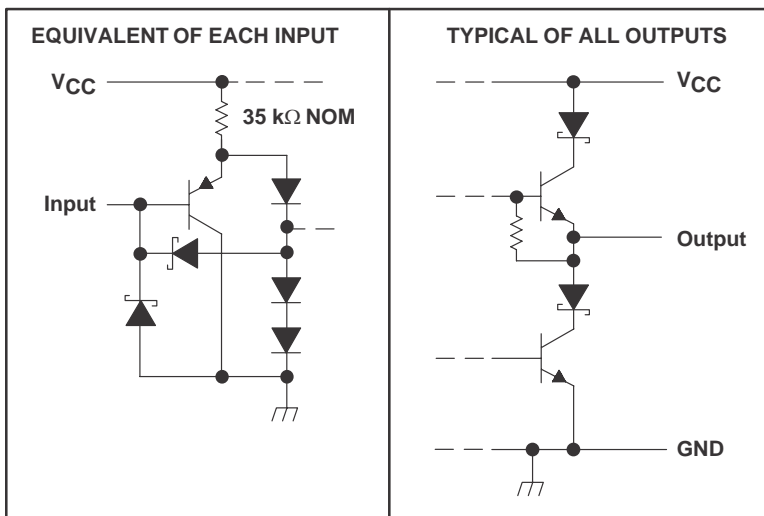
Figure 5. Logic Symbol

Parameter Measurement Information (continued)



(1) Pin numbers shown are for the N package.

Figure 6. Logic Diagram (Positive Logic)



Copyright © 2018, Texas Instruments Incorporated

Figure 7. Schematics of Inputs and Outputs

7 器件和文档支持

7.1 文档支持

7.2 接收文档更新通知

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. 有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

7.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

TI E2E™ 在线社区 *TI 的工程师对工程师 (E2E) 社区*。此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

设计支持 *TI 参考设计支持* 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

7.4 商标

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

7.5 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

7.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

8 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75ALS174ADW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS174A	Samples
SN75ALS174ADWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS174A	Samples
SN75ALS174AN	LIFEBUY	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75ALS174AN	
SN75ALS174APWR	LIFEBUY	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS174A	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75ALS174ADWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN75ALS174APWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75ALS174ADWR	SOIC	DW	20	2000	350.0	350.0	43.0
SN75ALS174APWR	TSSOP	PW	20	2000	356.0	356.0	35.0

TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN75ALS174ADW	DW	SOIC	20	25	506.98	12.7	4826	6.6
SN75ALS174AN	N	PDIP	16	25	506	13.97	11230	4.32

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - (C) Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - (D) The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW0020A



PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

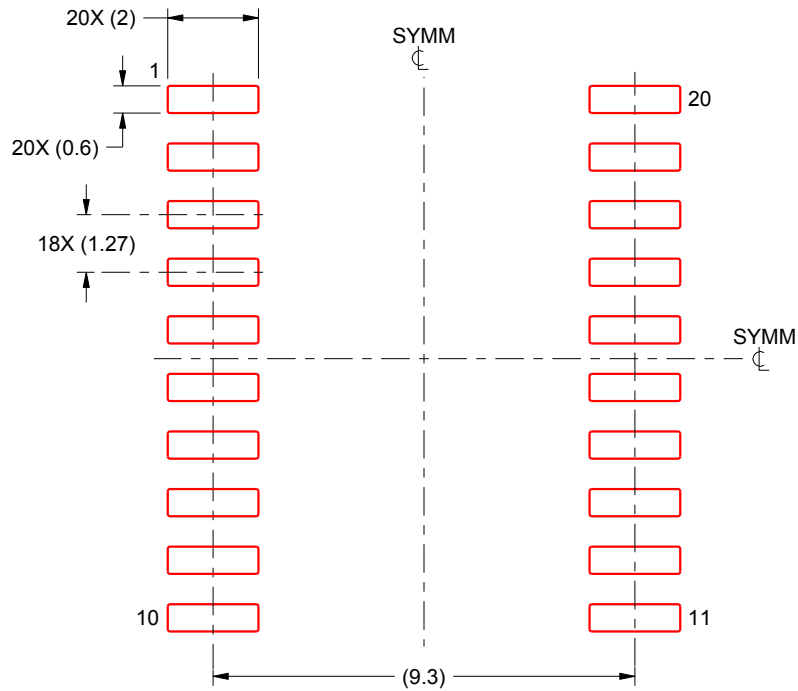
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

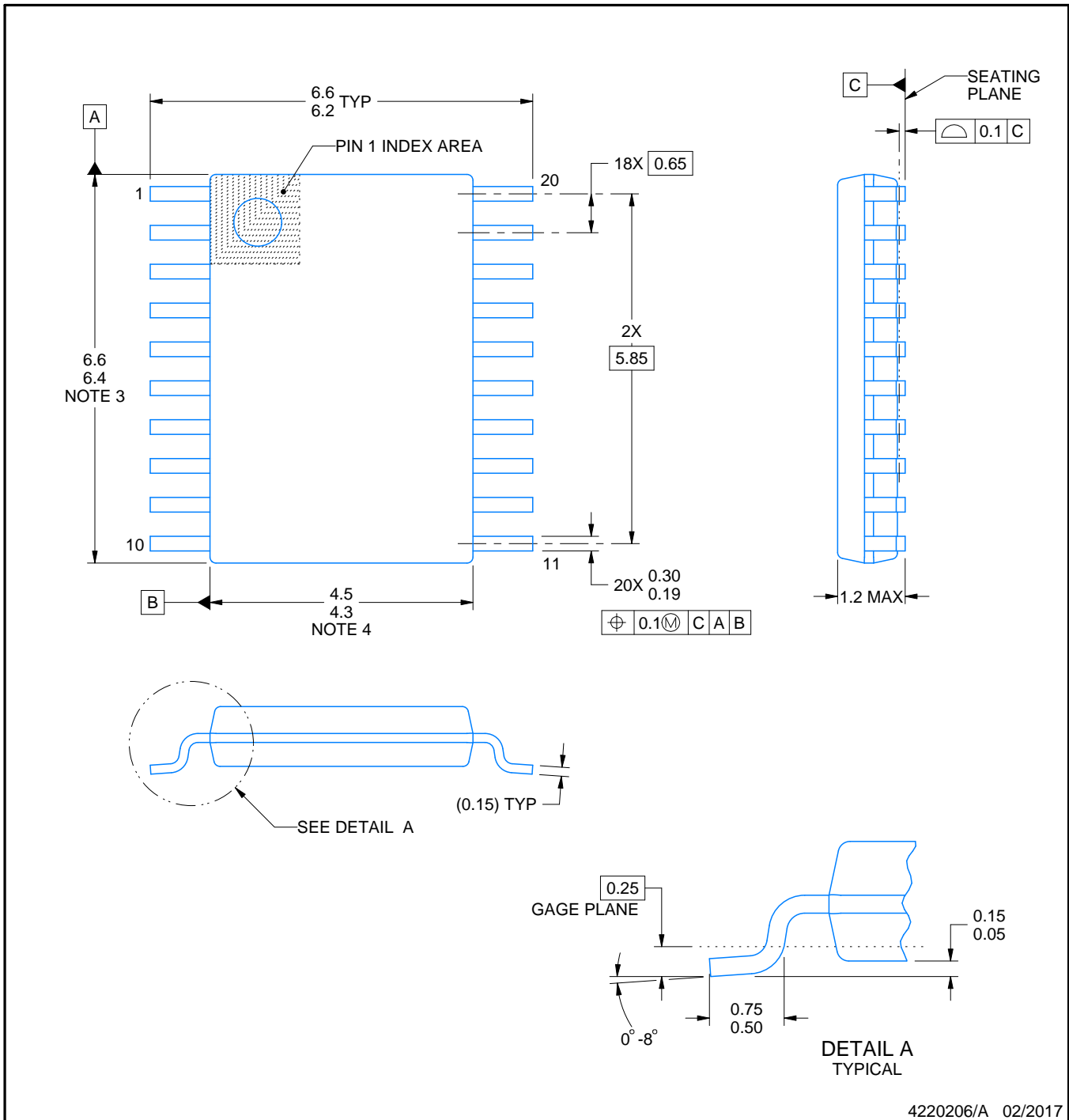
PW0020A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 [TI 的销售条款](#) 或 [ti.com](#) 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2023，德州仪器 (TI) 公司