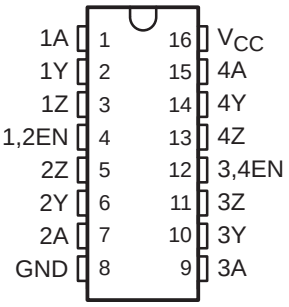
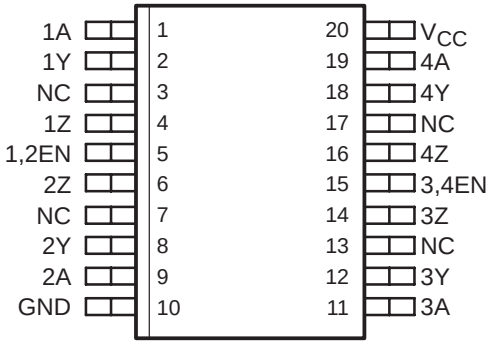
SLLS162D – JULY 1993 – REVISED SEPTEMBER 2003

- **Meets or Exceeds the Standard EIA-485**
- **Designed for High-Speed Multipoint Transmission on Long Bus Lines in Noisy Environments**
- **Supports Data Rates up to and Exceeding Ten Million Transfers Per Second**
- **Common-Mode Output Voltage Range of –7 V to 12 V**
- **Positive- and Negative-Current Limiting**
- **Low Power Consumption . . . 1.5 mA Max (Output Disabled)**
- **Functionally Interchangeable With SN75174**

**N PACKAGE**
**(TOP VIEW)**




**DW PACKAGE**
**(TOP VIEW)**




NC – No internal connection

## description

The SN65LBC174 and SN75LBC174 are monolithic, quadruple, differential line drivers with 3-state outputs. Both devices are designed to meet the requirements of the Electronics Industry Association Standard EIA-485. These devices are optimized for balanced multipoint bus transmission at data rates up to and exceeding 10 million bits per second. Each driver features wide positive and negative common-mode output voltage ranges, current limiting, and thermal-shutdown protection, making it suitable for party-line applications in noisy environments. Both devices are designed using LinBiCMOS™, facilitating ultralow power consumption and inherent robustness.

Both the SN65LBC174 and SN75LBC174 provide positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. These devices offer optimum performance when used with the SN75LBC173 or SN75LBC175 quadruple line receivers. The SN65LBC174 and SN75LBC174 are available in the 16-terminal DIP package (N) and the 20-terminal wide-body small outline intergrated circuit (SOIC) package (DW).

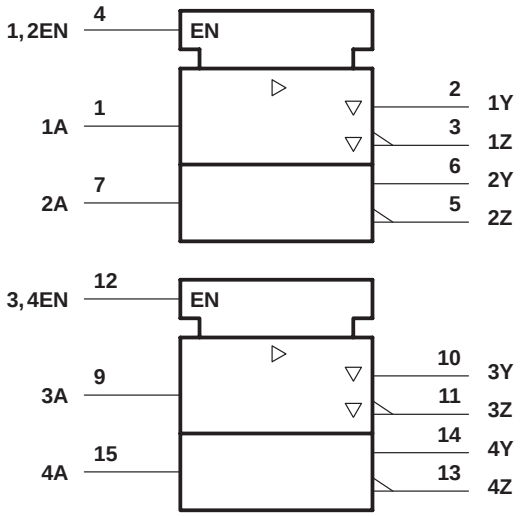
**FUNCTION TABLE**
**(each driver)**

| INPUT | ENABLE | OUTPUTS | |
|---|---|---|---|
| | | Y | Z |
| H | H | H | L |
| L | H | L | H |
| X | L | Z | Z |

H = high level, L = low level,
X = irrelevant, Z = high impedance (off)

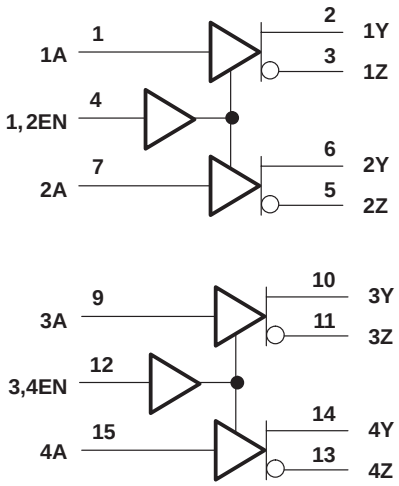
The SN75LBC174 is characterized for operation over the commercial temperature range of 0°C to 70°C. The SN65LBC174 is characterized over the industrial temperature range of –40°C to 85°C.

## logic symbol†

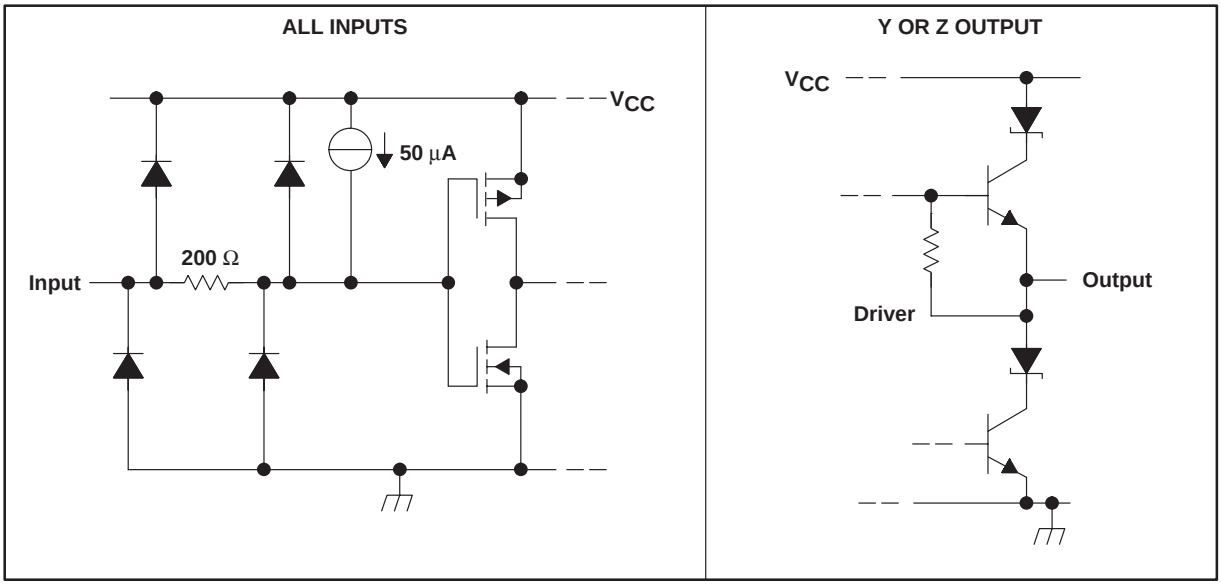



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Terminal numbers shown are for the N package.

## logic diagram (positive logic)




## schematic of inputs and outputs



### absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, $V_{CC}$ (see Note 1) . . . . . –0.3 V to 7 V
Output voltage range, $V_O$ . . . . . –10 V to 15 V
Voltage range at A, 1/2EN, 3/4EN . . . . . –0.3 V to $V_{CC}$ +0.5 V
Continuous total power dissipation . . . . . Internally limited‡
Operating free-air temperature range, $T_A$: SN65LBC174 . . . . . –40°C to 85°C
SN75LBC174 . . . . . 0°C to 70°C
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . . 260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ The maximum operating junction temperature is internally limited. Use the Dissipation Rating Table to operate below this temperature.
NOTE 1: All voltage values are with respect to GND.

### recommended operating conditions

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage, $V_{CC}$ | | 4.75 | 5 | 5.25 | V |
| High-level input voltage, $V_{IH}$ | | 2 | | | V |
| Low-level input voltage, $V_{IL}$ | | | | 0.8 | V |
| Voltage at any bus terminal (separately or common-mode), $V_O$ | Y or Z | | | 12 | V |
| | | | | –7 | |
| High-level output current, $I_{OH}$ | Y or Z | | | –60 | mA |
| Low-level output current, $I_{OL}$ | Y or Z | | | 60 | mA |
| Continuous total power dissipation | | See Dissipation Rating Table | | | |
| Operating free-air temperature, $T_A$ | SN65LBC174 | –40 | | 85 | °C |
| | SN75LBC174 | 0 | | 70 | |

**DISSIPATION RATING TABLE**

| PACKAGE | $T_A \le 25°C$ POWER RATING | DERATING FACTOR ABOVE $T_A = 25°C$ | $T_A = 70°C$ POWER RATING | $T_A = 85°C$ POWER RATING |
|---|---|---|---|---|
| DW | 1125 mW | 9.0 mW/°C | 720 mW | 585 mW |
| N | 1150 mW | 9.2 mW/°C | 736 mW | 598 mW |

## electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | Input clamp voltage | $I_I$ = –18 mA | | | | –1.5 | V |
| $\|V_{OD}\|$ | Differential output voltage‡ | $R_L$ = 54 Ω, See Figure 1 | SN65LBC174 | 1.1 | 1.8 | 5 | V |
| | | | SN75LBC174 | 1.5 | 1.8 | 5 | |
| | | $R_L$ = 60 Ω, See Figure 2 | SN65LBC174 | 1.1 | 1.7 | 5 | |
| | | | SN75LBC174 | 1.5 | 1.7 | 5 | |
| $\Delta\|V_{OD}\|$ | Change in magnitude of common-mode output voltage§ | $R_L$ = 54 Ω, See Figure 1 | | | | ±0.2 | V |
| $V_{OC}$ | Common-mode output voltage | | | | | 3<br>– 1 | V |
| $\Delta\|V_{OC}\|$ | Change in magnitude of common-mode output voltage§ | | | | | ±0.2 | V |
| $I_O$ | Output current with power off | $V_{CC}$ = 0, $V_O$ = – 7 V to 12 V | | | | ±100 | µA |
| $I_{OZ}$ | High-impedance-state output current | $V_O$ = – 7 V to 12 V | | | | ±100 | µA |
| $I_{IH}$ | High-level input current | $V_I$ = 2.4 V | | | | –100 | µA |
| $I_{IL}$ | Low-level input current | $V_I$ = 0.4 V | | | | –100 | µA |
| $I_{OS}$ | Short-circuit output current | $V_O$ = –7 V to 12 V | | | | ±250 | mA |
| $I_{CC}$ | Supply current (all drivers) | No load | Outputs enabled | | | 7 | mA |
| | | | Outputs disabled | | | 1.5 | |

† All typical values are at $V_{CC}$ = 5 V and $T_A$ = 25°C.
‡ The minimum $V_{OD}$ specification does not fully comply with EIA-485 at operating temperatures below 0°C. The lower output signal should be used to determine the maximum signal transmission distance.
§ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of $V_{OD}$ and $V_{OC}$, respectively, that occur when the input is changed from a high level to a low level.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{d(OD)}$ | Differential output delay time | $R_L$ = 54 Ω, | See Figure 3 | 2 | 11 | 20 | ns |
| $t_{t(OD)}$ | Differential output transition time | | | 10 | 15 | 25 | ns |
| $t_{PZH}$ | Output enable time to high level | $R_L$ = 110 Ω, | See Figure 3 | | 20 | 30 | ns |
| $t_{PZL}$ | Output enable time to low level | $R_L$ = 110 Ω, | See Figure 5 | | 21 | 30 | ns |
| $t_{PHZ}$ | Output disable time from high level | $R_L$ = 110 Ω, | See Figure 4 | | 48 | 70 | ns |
| $t_{PLZ}$ | Output disable time from low level | $R_L$ = 110 Ω, | See Figure 5 | | 21 | 30 | ns |

## PARAMETER MEASUREMENT INFORMATION

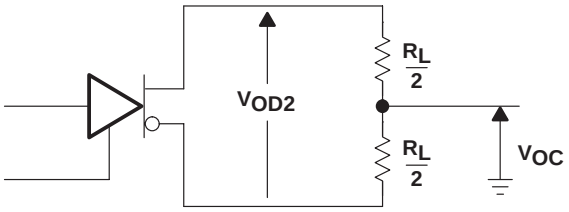



**Figure 1. Differential and Common-Mode Output Voltages**

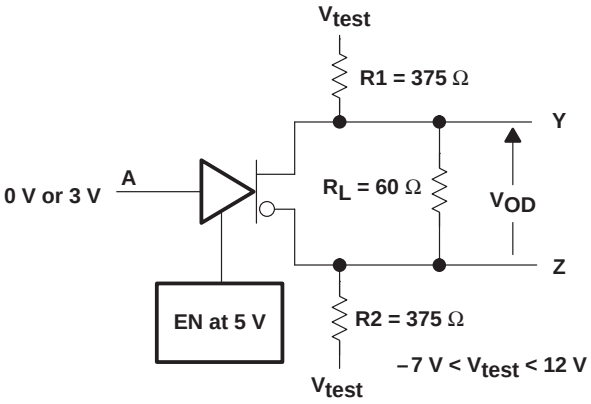
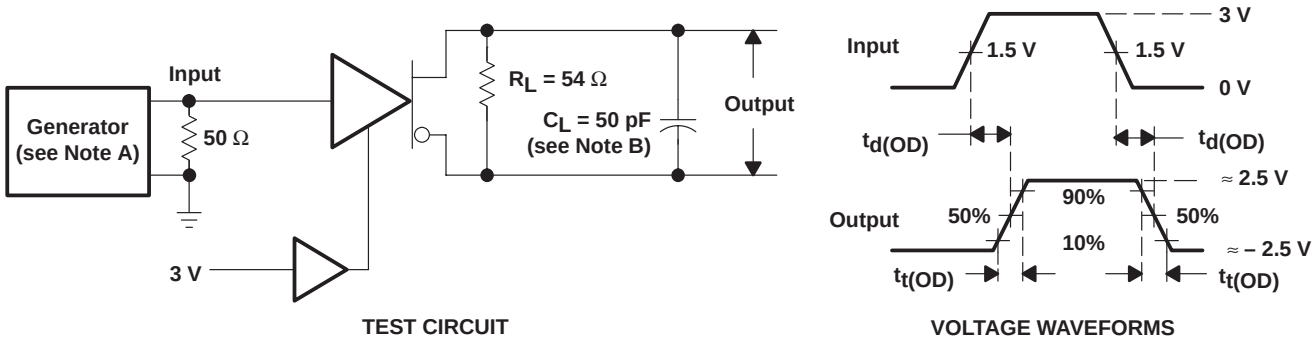



**Figure 2. Driver $V_{OD}$ Test Circuit**




NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, $t_r$ ≤ 5 ns, $t_f$ ≤ 5 ns, $Z_O$ = 50 Ω.
B. $C_L$ includes probe and stray capacitance.

**Figure 3. Time Waveforms for Driver Differential Output Test Circuit Delay and Transition**

## PARAMETER MEASUREMENT INFORMATION

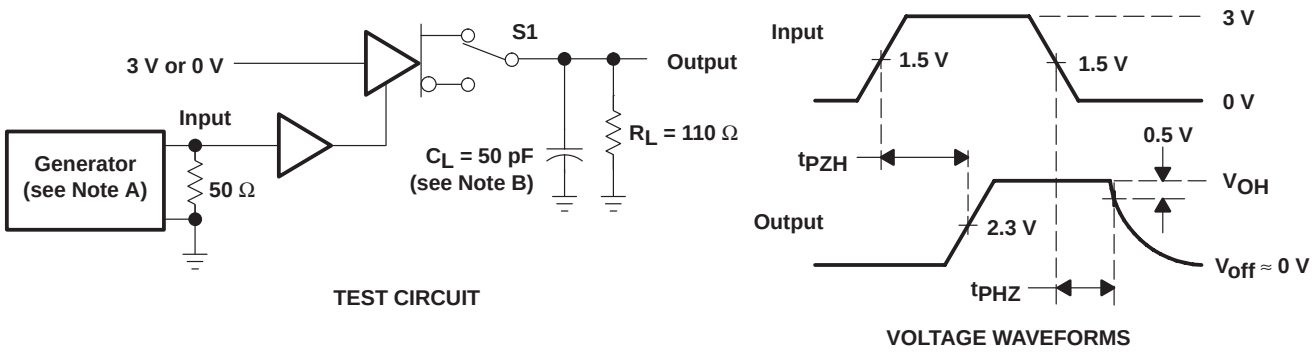
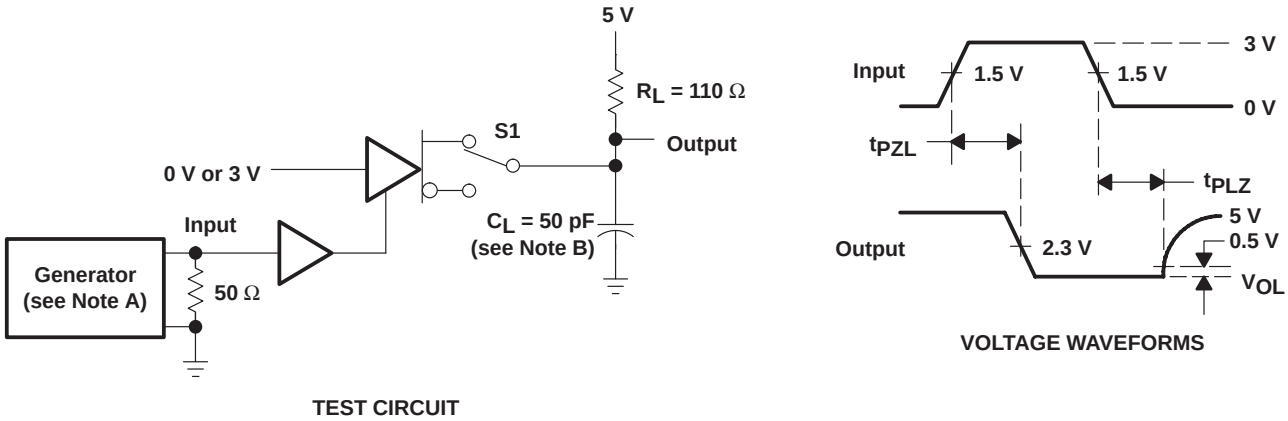



**Figure 4. $t_{PZH}$ and $t_{PHZ}$ Test Circuit and Waveforms**




NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, $t_r$ ≤ 5 ns, $t_f$ ≤ 5 ns, $Z_O$ = 50 Ω.
B. $C_L$ includes probe and stray capacitance.

**Figure 5. $t_{PZL}$ and $t_{PLZ}$ Test Circuit and Waveforms**

## TYPICAL CHARACTERISTICS

**OUTPUT CURRENT vs OUTPUT VOLTAGE**

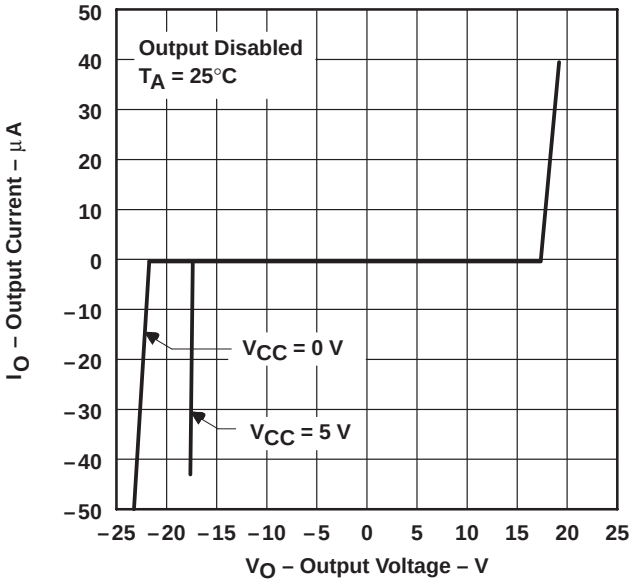



Figure 6

**LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT**

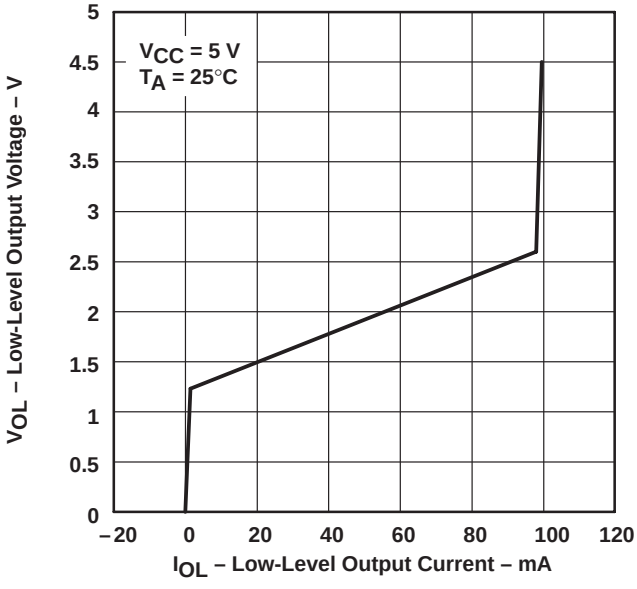



Figure 7

**DIFFERENTIAL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE**

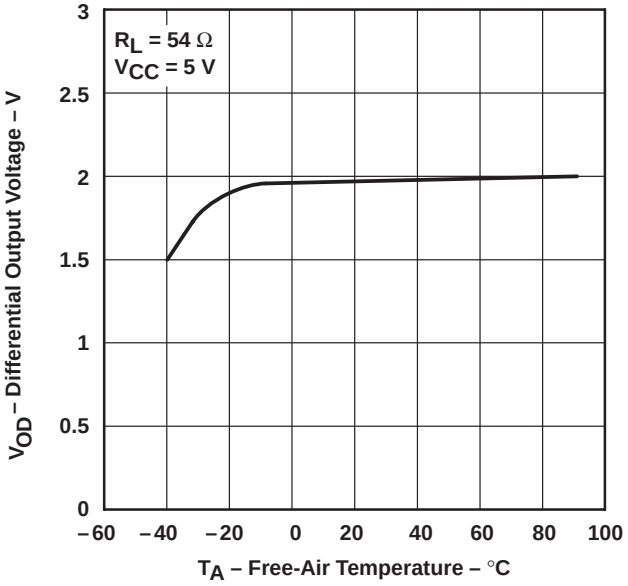



Figure 8

**HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT**

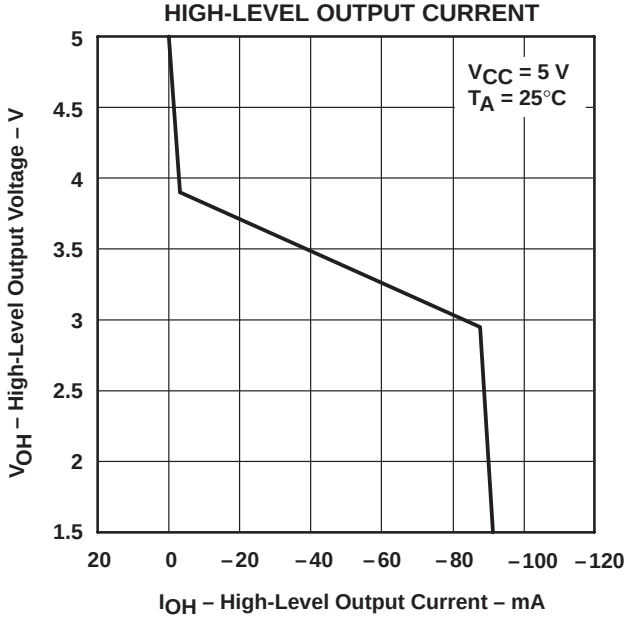



Figure 9

## TYPICAL CHARACTERISTICS

**DIFFERENTIAL OUTPUT VOLTAGE vs OUTPUT CURRENT**

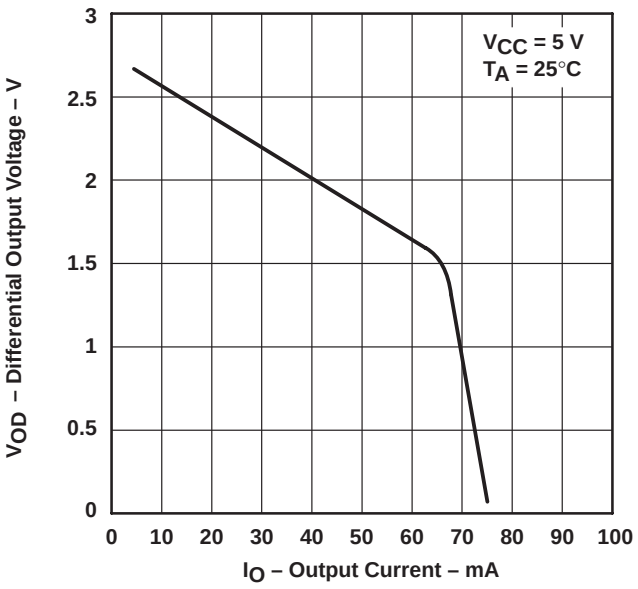



Figure 10

**PROPAGATION DELAY TIME, DIFFERENTIAL OUTPUT vs FREE-AIR TEMPERATURE**

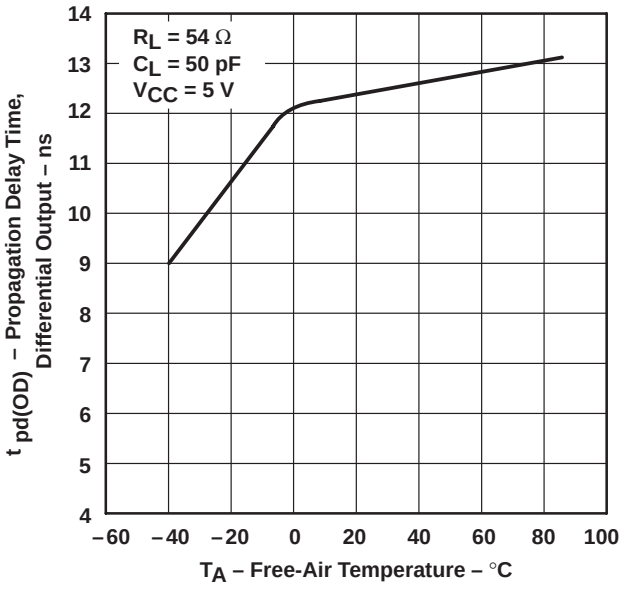



Figure 11

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65LBC174DW | ACTIVE | SOIC | DW | 20 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | SN65LBC174 | Samples |
| SN65LBC174DWR | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | SN65LBC174 | Samples |
| SN65LBC174N | LIFEBUY | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -40 to 85 | SN65LBC174N | |
| SN75LBC174DW | ACTIVE | SOIC | DW | 20 | 25 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75LBC174 | Samples |
| SN75LBC174DWR | ACTIVE | SOIC | DW | 20 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | SN75LBC174 | Samples |
| SN75LBC174N | LIFEBUY | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | 0 to 70 | SN75LBC174N | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**OTHER QUALIFIED VERSIONS OF SN75LBC174 :**

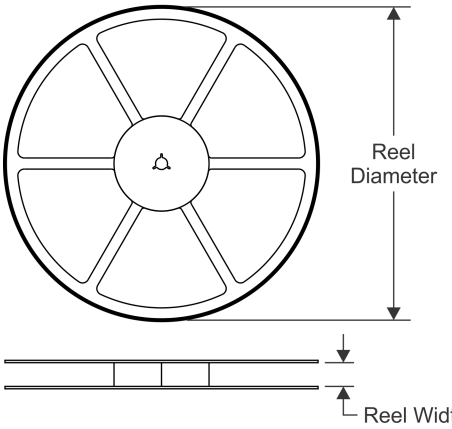
- Military : SN55LBC174

NOTE: Qualified Version Definitions:

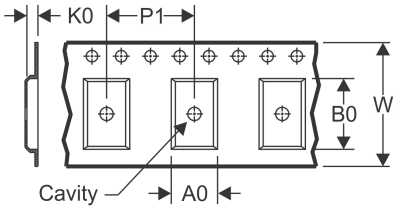
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

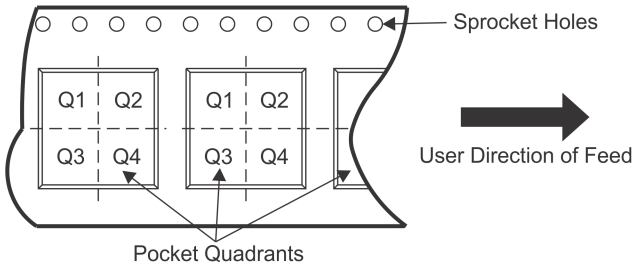



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

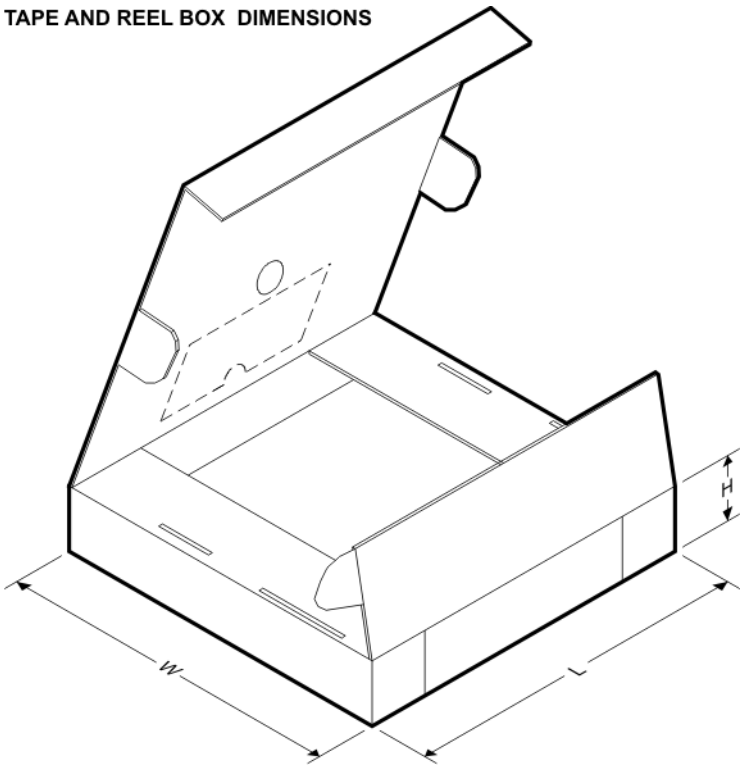
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65LBC174DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN75LBC174DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |

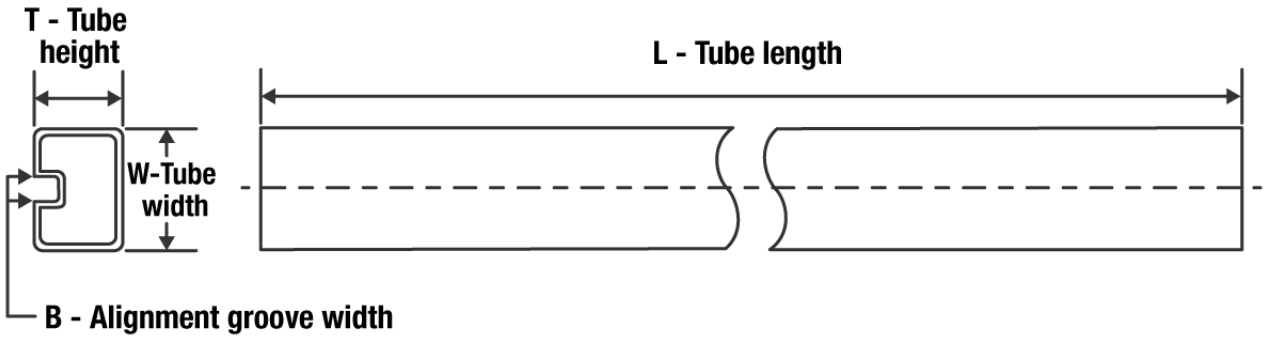
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN65LBC174DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN75LBC174DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |

## TUBE



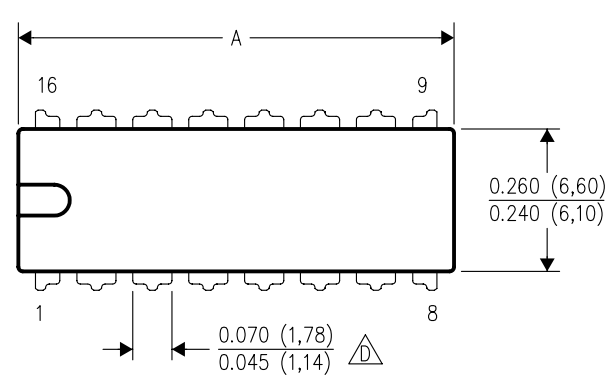

*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| SN65LBC174DW | DW | SOIC | 20 | 25 | 506.98 | 12.7 | 4826 | 6.6 |
| SN65LBC174DW | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| SN65LBC174N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |
| SN75LBC174DW | DW | SOIC | 20 | 25 | 507 | 12.83 | 5080 | 6.6 |
| SN75LBC174DW | DW | SOIC | 20 | 25 | 506.98 | 12.7 | 4826 | 6.6 |
| SN75LBC174N | N | PDIP | 16 | 25 | 506 | 13.97 | 11230 | 4.32 |

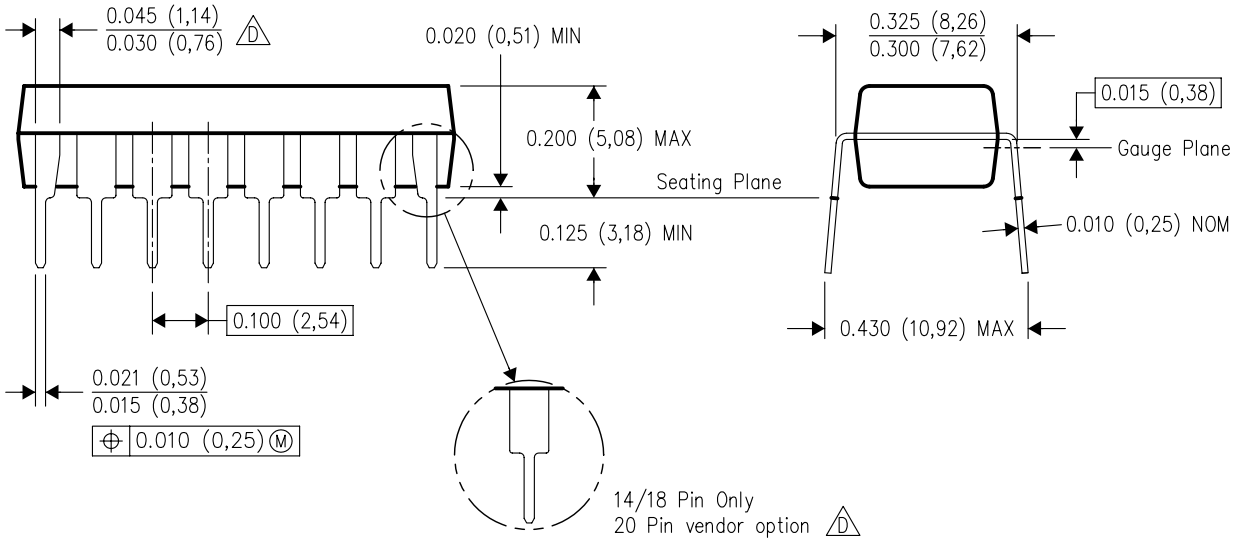
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

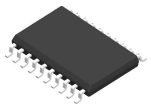



| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

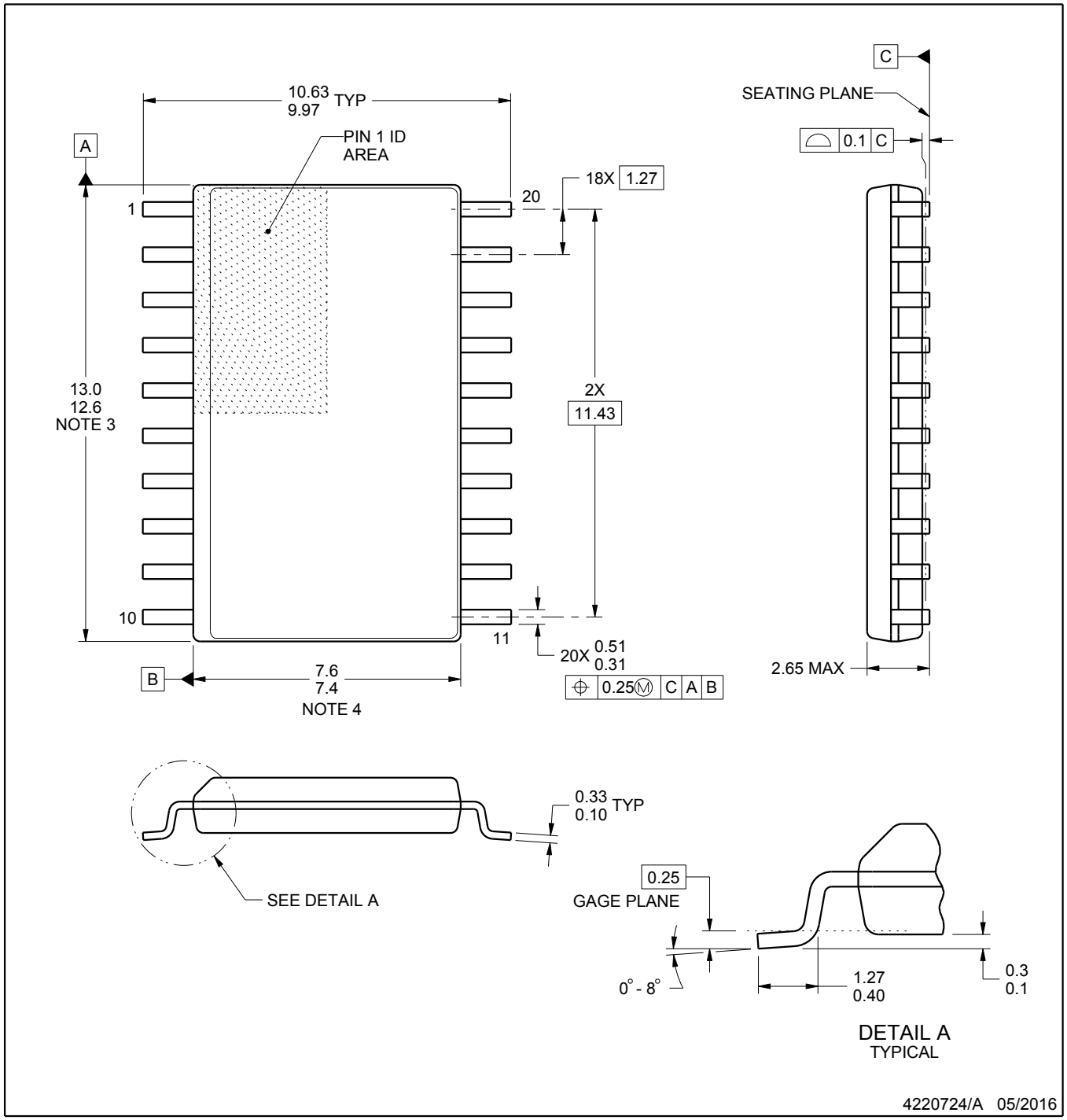


# PACKAGE OUTLINE

## DW0020A

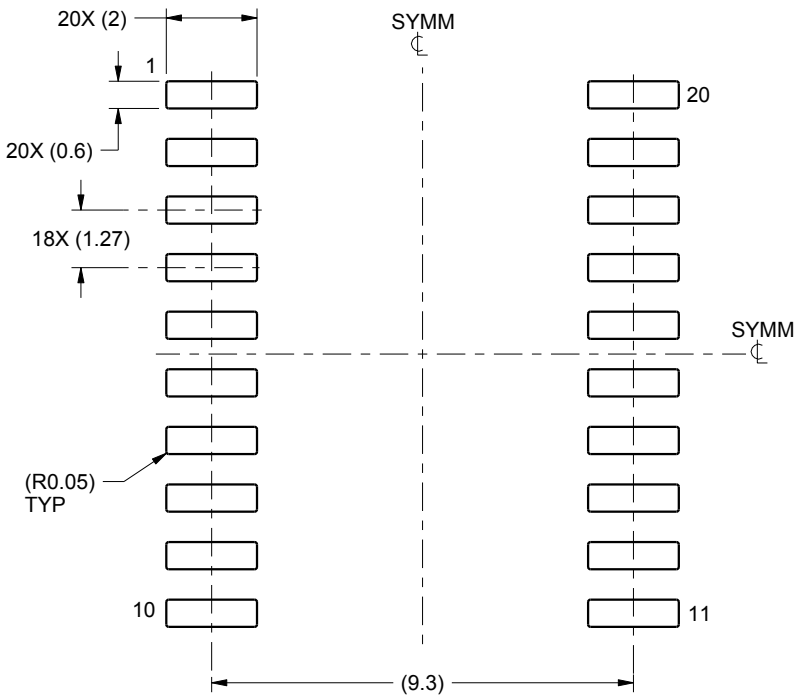
## SOIC - 2.65 mm max height

SOIC

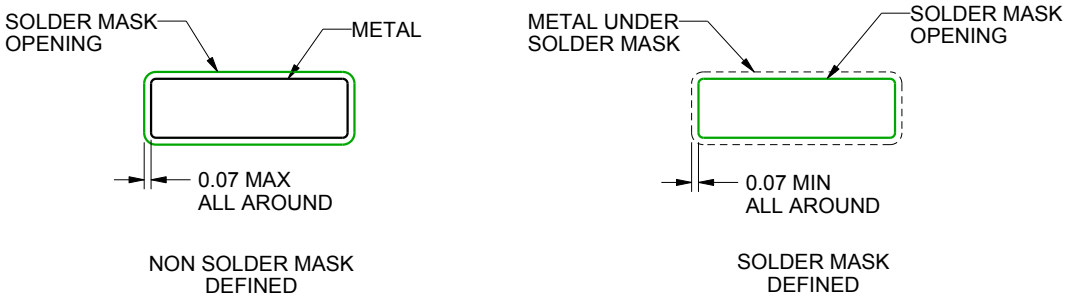



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.




LAND PATTERN EXAMPLE
SCALE:6X




SOLDER MASK DETAILS

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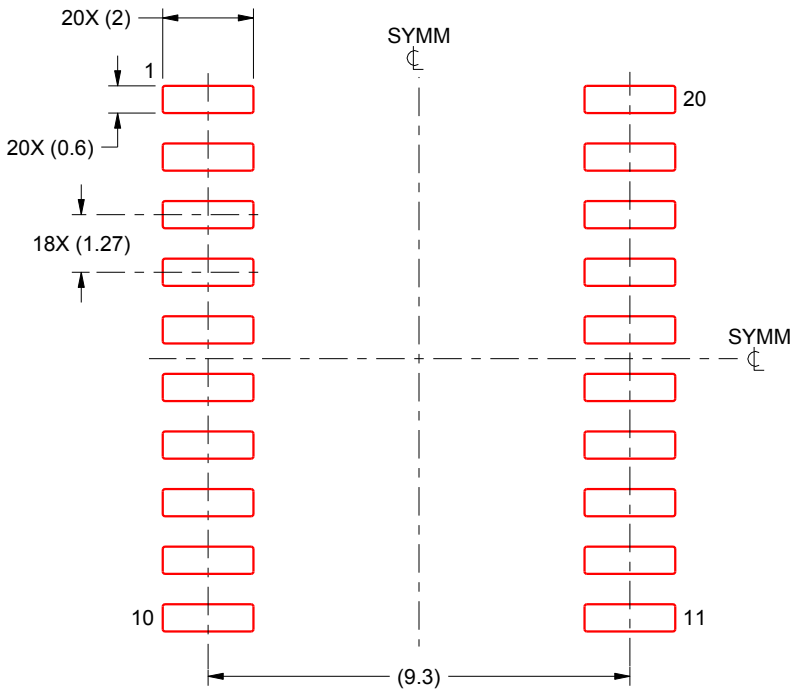
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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