TCA9534A 具有中断输出和配置寄存器的低压 8 位 I²C 和系统管理总线 (SMBUS) 低功耗输入输出 (I/O) 扩展器

1 特性

- 低待机电流消耗
- I²C 至并行端口扩展器
- 开漏电路低电平有效中断输出
- 1.65V 至 5.5V 的工作电源电压范围
- 可耐受 5V 电压的 I/O 端口
- 400kHz 快速 I²C 总线
- 3 个硬件地址引脚可在 I²C/SMBus 上支持最多 8 个器件
- 输入和输出配置寄存器
- 极性反转寄存器
- 内部加电复位
- 所用通道在加电时被配置为输入
- 加电时无毛刺脉冲
- SCL/SDA 输入端上的噪声滤波器
- 具有最大高电流驱动能力的锁存输出，适用于直接驱动 LED
- 锁断性能超过 100mA，符合 JESD 78 II 类规范的要求）
- 静电放电 (ESD) 保护性能超过 JESD 22 规范的要求
  - 2000V 人体放电模型 (A114-A)
  - 1000V 充电器件模型 (C101)

2 应用

- 服务器
- 路由器（电信交换设备）
- 个人计算机
- 个人电子产品（例如：游戏机）
- 工业自动化
- 采用 GPIO 受限处理器的产品

3 说明

TCA9534A 是一款 16 引脚器件，可为两线双向 I²C 总线（或 SMBus）协议提供 8 位通用并行输入和输出 (I/O) 扩展。该器件可在 1.65V 至 5.5V 的电源电压范围内运行，从而允许使用各种器件。该器件支持 100kHz（标准模式）和 400kHz（快速模式）时钟频率。当开关、传感器、按钮、LED、风扇和其它类似器件需要额外的 I/O 时，I/O 扩展器（如 TCA9534A）可提供简单解决方案。

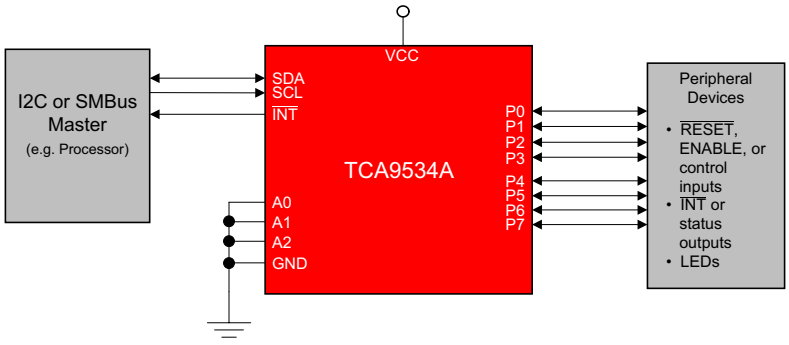
TCA9534A 的 功能 包括在 $\overline{INT}$ 引脚上生成中断。这样，主设备就知道输入端口状态何时发生了变化。硬件可选地址引脚 A0、A1 和 A2 最多允许 8 个 TCA9534A 器件位于同一 I²C 总线上。该器件还可通过电源循环供电以生成加电复位，从而复位到默认状态 。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TCA9534A	TSSOP (16)	5.00mm x 4.40mm
	SOIC (16)	10.30mm x 7.50mm

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

简化的原理图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

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- Updated Figure 20 ... 13
- Updated address in Table 1 ... 18

Changes from Revision A (September 2014) to Revision B — **Page**

- 更新了 *说明* 部分 ... 1
- 已添加 DW 封装 ... 1
- Corrected ESD ratings to reflect ± ratings ... 5
- VIH values, improved performance ... 5
- Made changes to I_{OL} in the *Recommended Operating Conditions* table ... 5
- Changed V_{PORR} limits ... 6
- Changed V_{OH} at V_{CC} = 1.65 V ... 6
- Updated I_{OL} in the *Electrical Characteristics* table ... 6
- Changed I_{CC} in the *Electrical Characteristics* table ... 7
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- Updated graphs in *Typical Characteristics* section ... 9
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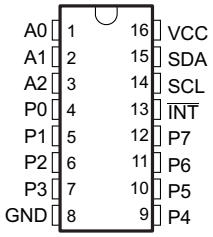
5 Pin Configuration and Functions

PW and DW Package
16-Pin TSSOP and SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	A0	I	Address input. Connect directly to V_{CC} or ground
2	A1	I	Address input. Connect directly to V_{CC} or ground
3	A2	I	Address input. Connect directly to V_{CC} or ground
4	P0	I/O	P-port input-output. Push-pull design structure. At power on, P0 is configured as an input
5	P1	I/O	P-port input-output. Push-pull design structure. At power on, P1 is configured as an input
6	P2	I/O	P-port input-output. Push-pull design structure. At power on, P2 is configured as an input
7	P3	I/O	P-port input-output. Push-pull design structure. At power on, P3 is configured as an input
8	GND	—	Ground
9	P4	I/O	P-port input-output. Push-pull design structure. At power on, P4 is configured as an input
10	P5	I/O	P-port input-output. Push-pull design structure. At power on, P5 is configured as an input
11	P6	I/O	P-port input-output. Push-pull design structure. At power on, P6 is configured as an input
12	P7	I/O	P-port input-output. Push-pull design structure. At power on, P7 is configured as an input
13	$\overline{INT}$	O	Interrupt output. Connect to V_{CC} through a pull-up resistor
14	SCL	I	Serial clock bus. Connect to V_{CC} through a pull-up resistor
15	SDA	I/O	Serial data bus. Connect to V_{CC} through a pull-up resistor
16	VCC	—	Supply voltage

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	6	V
V_I	Input voltage (2)		–0.5	6	V
V_O	Output voltage (2)		–0.5	6	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$		–20	mA
I_{IOK}	Input-output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_{OL}	Continuous output low current through a single P-port	V_O = 0 to V_{CC}		50	mA
I_{OH}	Continuous output high current through a single P-port	V_O = 0 to V_{CC}		–50	mA
I_{CC}	Continuous current through GND by all P-ports, $\overline{INT}$, and SDA			250	mA
	Continuous current through V_{CC} by all P-ports			–160	
$T_{J(MAX)}$	Maximum junction temperature			100	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 Handling Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

				MIN	MAX	UNIT
V_{CC}	Supply voltage			1.65	5.5	V
V_{IH}	High-level input voltage	SCL, SDA	V_{CC} = 1.65 V to 5.5 V	0.7 × V_{CC}	V_{CC}(1)	V
		A0, A1, A2, P7–P0	V_{CC} = 1.65 V to 2.7 V	0.7 × V_{CC}	5.5	
V_{IL}	Low-level input voltage	SCL, SDA	V_{CC} = 1.65 V to 5.5 V	–0.5	0.3 × V_{CC}	V
		A0, A1, A2, P7–P0	V_{CC} = 1.65 V to 2.7 V	–0.5	0.3 × V_{CC}	
			V_{CC} = 3 V to 5.5 V	–0.5	0.2 × V_{CC}	
I_{OH}	High-level output current	Any P-port, P7–P0			–10	mA
I_{OL}	Low-level output current(2)	P00-P07, P10-P17	$T_j \le 65°C$		25	mA
			$T_j \le 85°C$		18	
			$T_j \le 100°C$		9	
		$\overline{INT}$, SDA	$T_j \le 85°C$		6	
			$T_j \le 100°C$		3	
I_{CC}	Continuous current through GND	All P-ports P7-P0, $\overline{INT}$, and SDA			200	mA
	Continuous current through V_{CC}	All P-ports P7-P0			–80	
T_A	Operating free-air temperature			–40	85	°C

(1) The SCL and SDA pins shall not be at a higher potential than the supply voltage V_{CC} in the application, or an increase in leakage current, I_I, will result.
(2) The values shown apply to specific junction temperatures. See the *Calculating Junction Temperature and Power Dissipation* section on how to calculate the junction temperature.

6.4 Thermal Information

THERMAL METRIC[1]		TCA9534A		UNIT
		PW (TSSOP)	DW (SOIC)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	122	92.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.4	53.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	67.1	56.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.8	26.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	66.5	56.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP[1]	MAX	UNIT
V_{IK}	Input diode clamp voltage	I_I = –18 mA	1.65 V to 5.5 V	–1.2			V
V_{PORR}	Power-on reset voltage, V_{CC} rising	V_I = V_{CC} or GND, I_O = 0			1.2	1.5	V
V_{PORF}	Power-on reset voltage, V_{CC} falling	V_I = V_{CC} or GND, I_O = 0		0.75	1		V
V_{OH}	P-port high-level output voltage[2]	I_{OH} = –8 mA	1.65 V	1.2			V
			2.3 V	1.8			
			3 V	2.6			
			4.5 V	4.1			
		I_{OH} = –10 mA	1.65 V	1			
			2.3 V	1.7			
			3 V	2.5			
			4.5 V	4			
I_{OL}	SDA[3]	V_{OL} = 0.4 V	1.65 V to 5.5 V	3			mA
	P port[4]	V_{OL} = 0.5 V	1.65 V to 5.5 V	8			
		V_{OL} = 0.7 V	1.65 V to 5.5 V	10			
	$\overline{INT}$ [5]	V_{OL} = 0.4 V	1.65 V to 5.5 V	3			
I_I	SCL, SDA	V_I = V_{CC} or GND	1.65 V to 5.5 V			±1	µA
	A2–A0					±1	
I_{IH}	P port	V_I = V_{CC}	1.65 V to 5.5 V			1	µA
I_{IL}	P port	V_I = GND	1.65 V to 5.5 V			–1	µA

(1) All typical values are at nominal supply voltage (1.8-, 2.5-, 3.3-, or 5-V V_{CC}) and T_A = 25°C.
(2) Each P-port I/O configured as a high output must be externally limited to a maximum of 10 mA, and the total current sourced by all I/Os (P-ports P7-P0) through V_{CC} must be limited to a maximum current of 80 mA.
(3) The SDA pin must be externally limited to a maximum of 12 mA, and the total current sunk by all I/Os (P-ports P7-P0, $\overline{INT}$, and SDA) through GND must be limited to a maximum current of 200 mA.
(4) Each P-port I/O configured as a low output must be externally limited to a maximum of 25 mA, and the total current sunk by all I/Os (P-ports P7-P0, $\overline{INT}$, and SDA) through GND must be limited to a maximum current of 200 mA.
(5) The $\overline{INT}$ pin must be externally limited to a maximum of 7 mA, and the total current sunk by all I/Os (P-ports P7-P0, $\overline{INT}$, and SDA) through GND must be limited to a maximum current of 200 mA.

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP(1)	MAX	UNIT
I_{CC}	Operating mode	$V_I = V_{CC}$ or GND, $I_O = 0$, I/O = inputs, f_{scl} = 400 kHz, no load		5.5 V		22	40	µA
				3.6 V		11	30	
				2.7 V		8	19	
				1.65		5	11	
	Standby mode	V_I = GND, $I_O = 0$, I/O = inputs, f_{scl} = 0 kHz, no load	$V_I = V_{CC}$	5.5 V		1.5	3.9	
				3.6 V		0.9	2.2	
				2.7 V		0.6	1.8	
				1.95 V		0.4	1.5	
			V_I = GND	5.5 V		1.5	8.7	
				3.6 V		0.9	4	
				2.7 V		0.6	3	
				1.95 V		0.4	2.2	
C_i	SCL	$V_I = V_{CC}$ or GND		1.65 V to 5.5 V		3	8	pF
C_{io}	SDA	$V_{IO} = V_{CC}$ or GND		1.65 V to 5.5 V		3	9.5	pF
	P port					3.7	9.5	

6.6 I²C Interface Timing Requirements

over operating free-air temperature range (unless otherwise noted) (see Figure 19)

			MIN	MAX	UNIT
STANDARD MODE					
f_{scl}	I²C clock frequency		0	100	kHz
t_{sch}	I²C clock high time		4		µs
t_{scl}	I²C clock low time		4.7		µs
t_{sp}	I²C spike time			50	ns
t_{sds}	I²C serial-data setup time		250		ns
t_{sdh}	I²C serial-data hold time		0		ns
t_{icr}	I²C input rise time			1000	ns
t_{icf}	I²C input fall time			300	ns
t_{ocf}	I²C output fall time	10-pF to 400-pF bus		300	ns
t_{buf}	I²C bus free time between stop and start		4.7		µs
t_{sts}	I²C start or repeated start condition setup		4.7		µs
t_{sth}	I²C start or repeated start condition hold		4		µs
t_{sps}	I²C stop condition setup		4		µs
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid		3.45	ns
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low		3.45	µs
C_b	I²C bus capacitive load			400	pF
FAST MODE					
f_{scl}	I²C clock frequency		0	400	kHz
t_{sch}	I²C clock high time		0.6		µs
t_{scl}	I²C clock low time		1.3		µs
t_{sp}	I²C spike time			50	ns
t_{sds}	I²C serial-data setup time		100		ns
t_{sdh}	I²C serial-data hold time		0		ns
t_{icr}	I²C input rise time		20	300	ns

I²C Interface Timing Requirements (continued)

over operating free-air temperature range (unless otherwise noted) (see Figure 19)

			MIN	MAX	UNIT
t_{icf}	I²C input fall time		20 × (V_{DD} / 5.5 V)	300	ns
t_{ocf}	I²C output fall time	10-pF to 400-pF bus	20 × (V_{DD} / 5.5 V)	300	ns
t_{buf}	I²C bus free time between stop and start		1.3		µs
t_{sts}	I²C start or repeated start condition setup		0.6		µs
t_{sth}	I²C start or repeated start condition hold		0.6		µs
t_{sps}	I²C stop condition setup		0.6		µs
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid		0.9	ns
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low		0.9	µs
C_b	I²C bus capacitive load			400	pF

6.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted) (see Figure 20 and Figure 21)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
STANDARD and FAST MODE						
t_{iv}	Interrupt valid time	P port	$\overline{INT}$		4	µs
t_{ir}	Interrupt reset delay time	SCL	$\overline{INT}$		4	µs
t_{pv}	Output data valid	SCL	P7–P0		350	ns
t_{ps}	Input data setup time	P port	SCL	100		ns
t_{ph}	Input data hold time	P port	SCL	1		µs

6.8 Typical Characteristics

T_A = 25°C (unless otherwise noted)

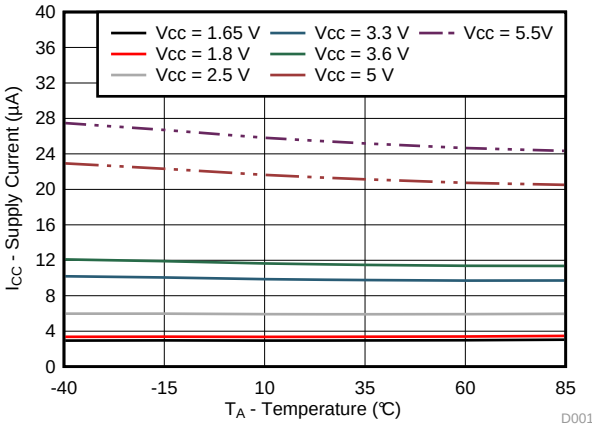


Figure 1. Supply Current vs Temperature for Different Supply Voltage (V_{CC})

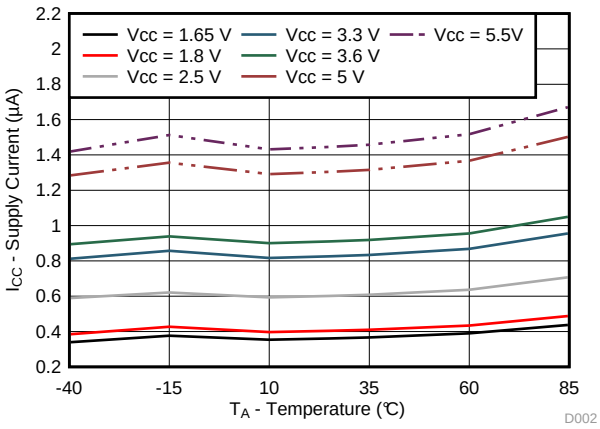


Figure 2. Standby Supply Current vs Temperature for Different Supply Voltage (V_{CC})

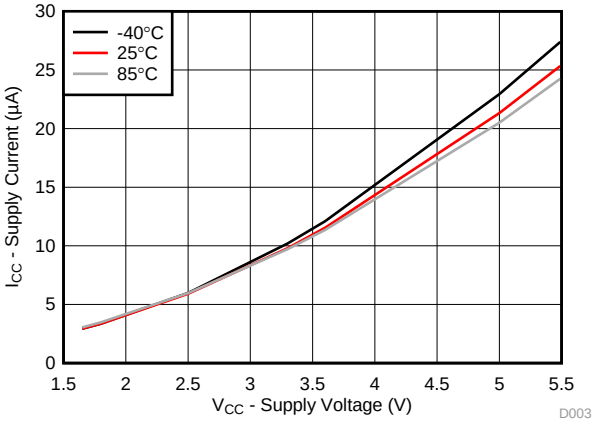


Figure 3. Supply Current vs Supply Voltage for Different Temperature (T_A)

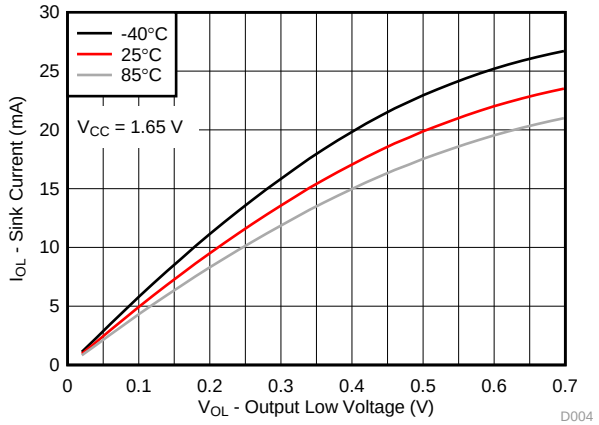


Figure 4. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 1.65 V

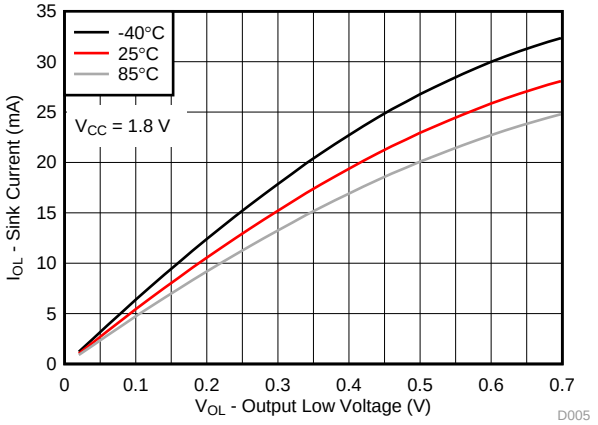


Figure 5. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 1.8 V

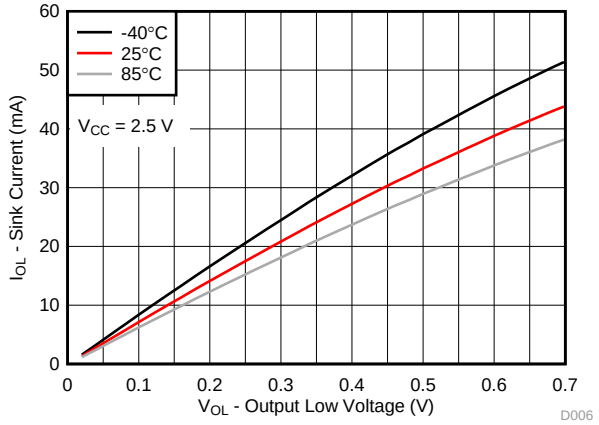


Figure 6. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 2.5 V

Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

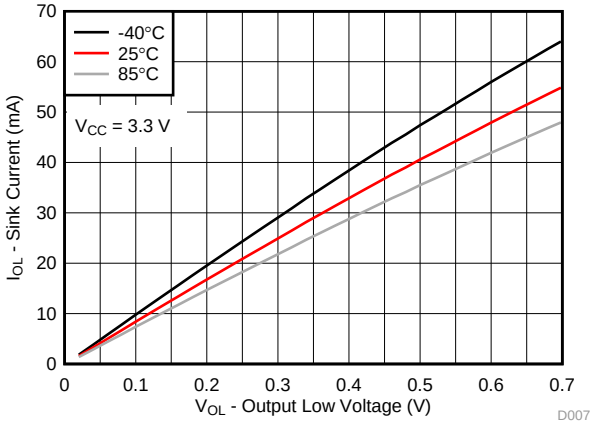


Figure 7. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 3.3 V

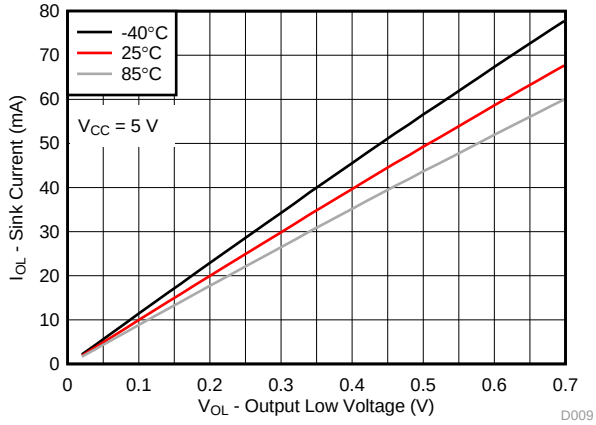


Figure 8. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 5 V

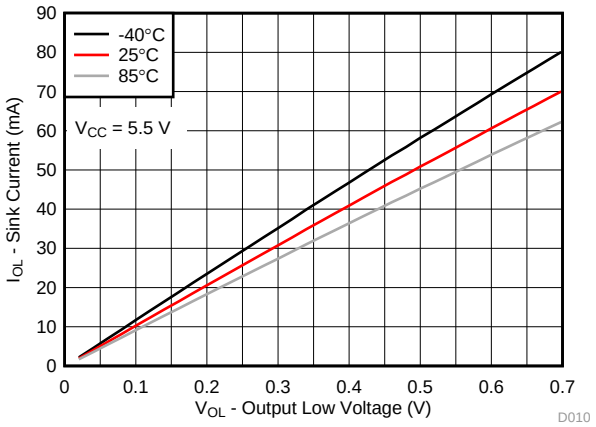


Figure 9. I/O Sink Current vs Output Low Voltage for Different Temperature (T_A) for V_{CC} = 5.5 V

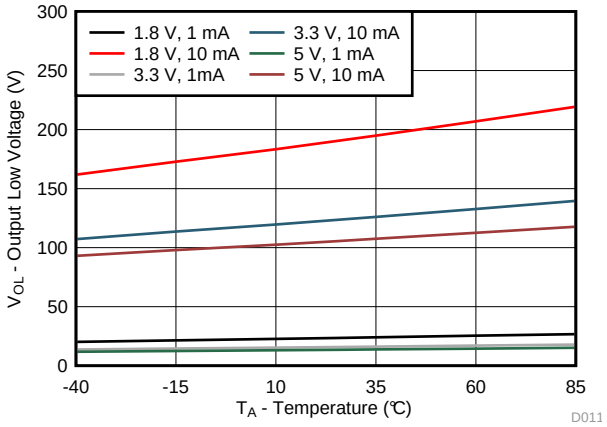


Figure 10. II/O Low Voltage vs Temperature for Different V_{CC} and I_{OL}

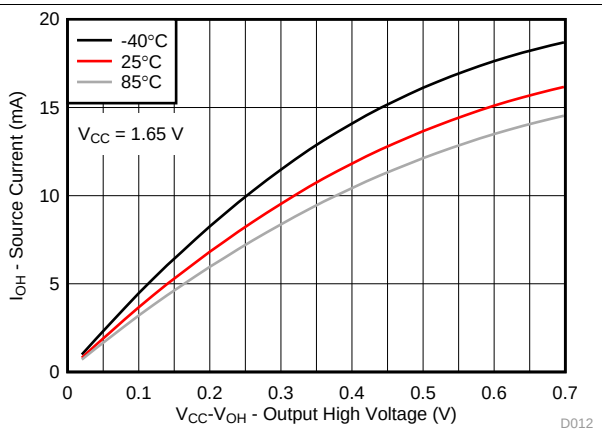


Figure 11. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 1.65 V

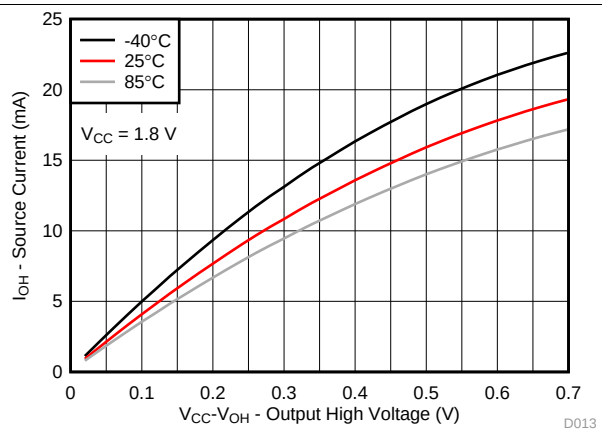


Figure 12. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 1.8 V

Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

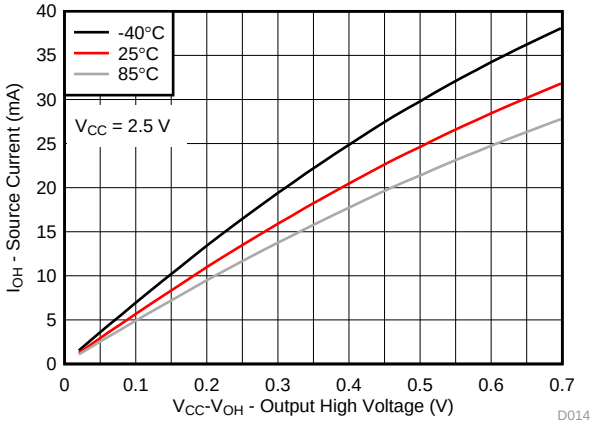


Figure 13. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 2.5 V

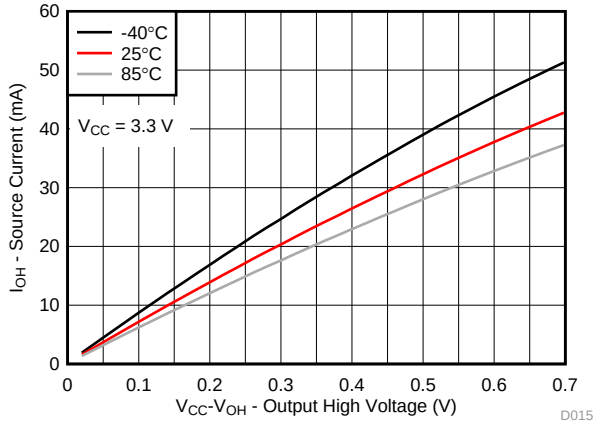


Figure 14. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 3.3 V

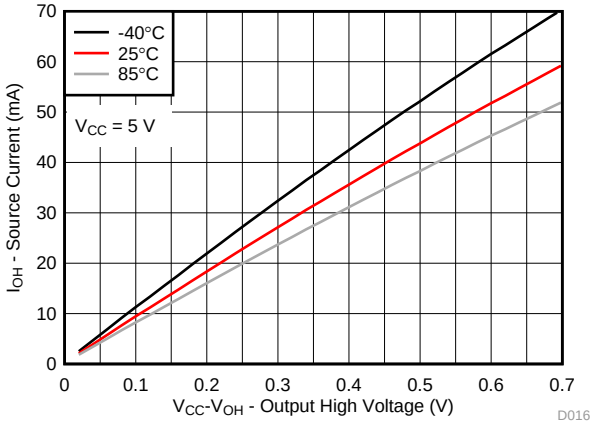


Figure 15. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 5 V

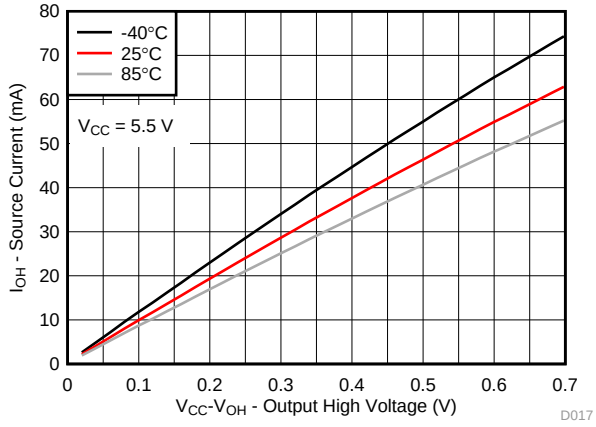


Figure 16. I/O Source Current vs Output High Voltage for Different Temperature (T_A) for V_{CC} = 5.5 V

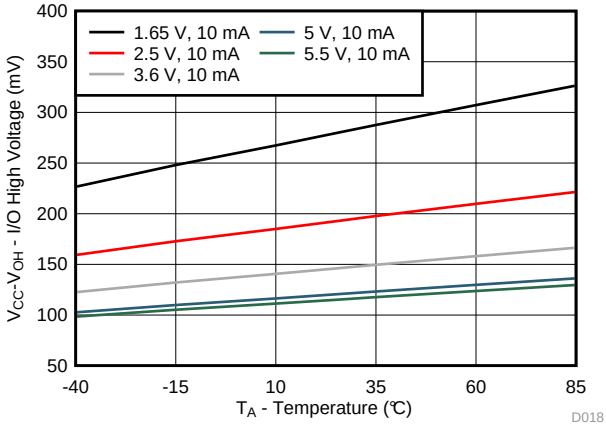


Figure 17. V_{CC} – V_{OH} Voltage vs Temperature for Different V_{CC}

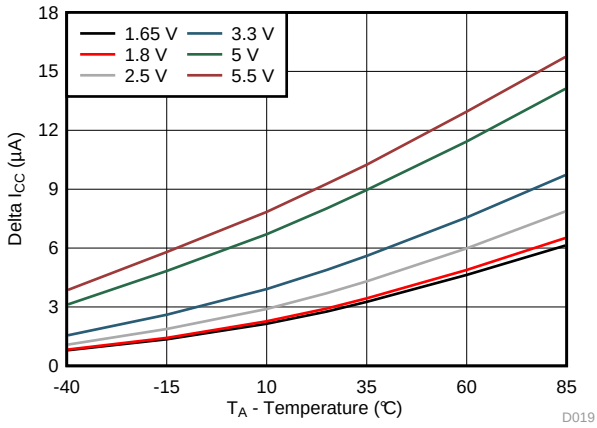
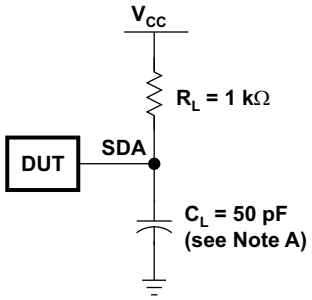
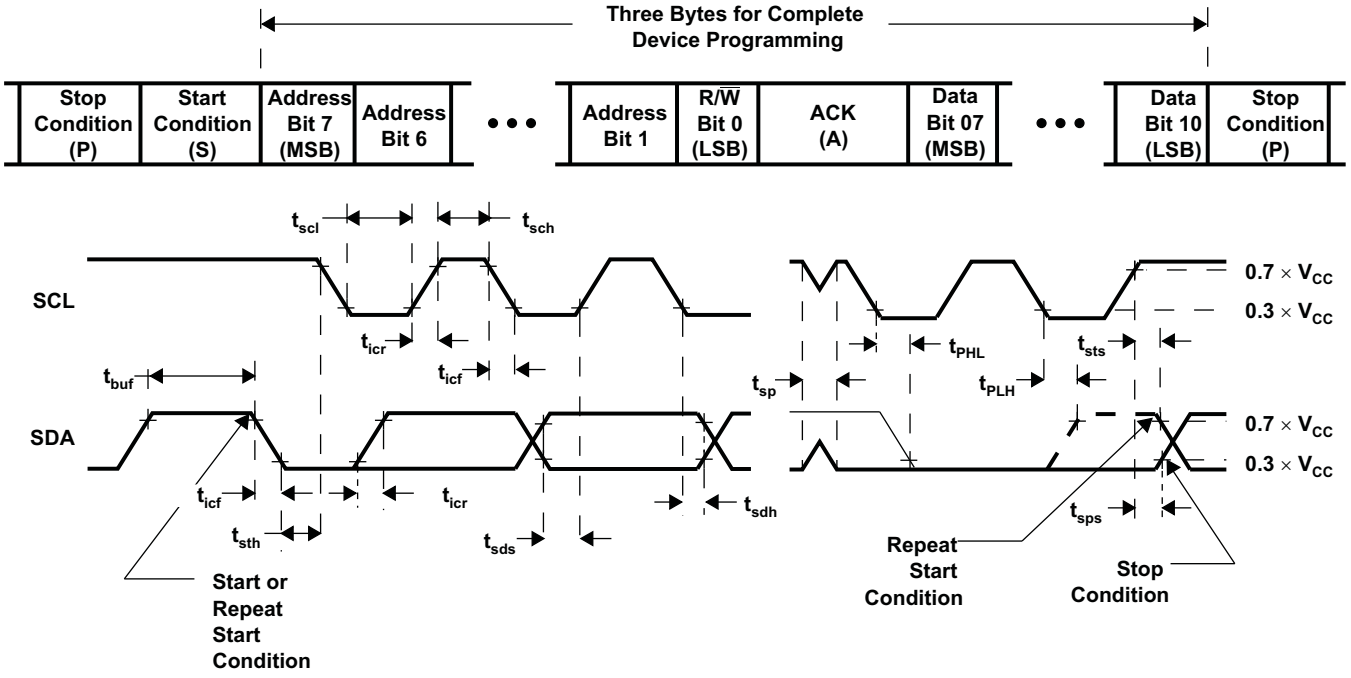


Figure 18. Δ I_{CC} vs Temperature for Different V_{CC} (V_I = V_{CC} – 0.6 V)

7 Parameter Measurement Information



SDA LOAD CONFIGURATION



VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I^2C address
2, 3	P-port data

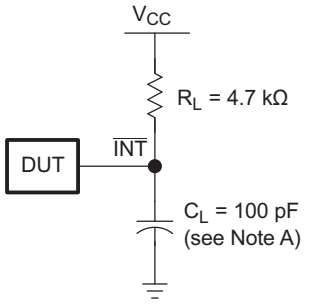
A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

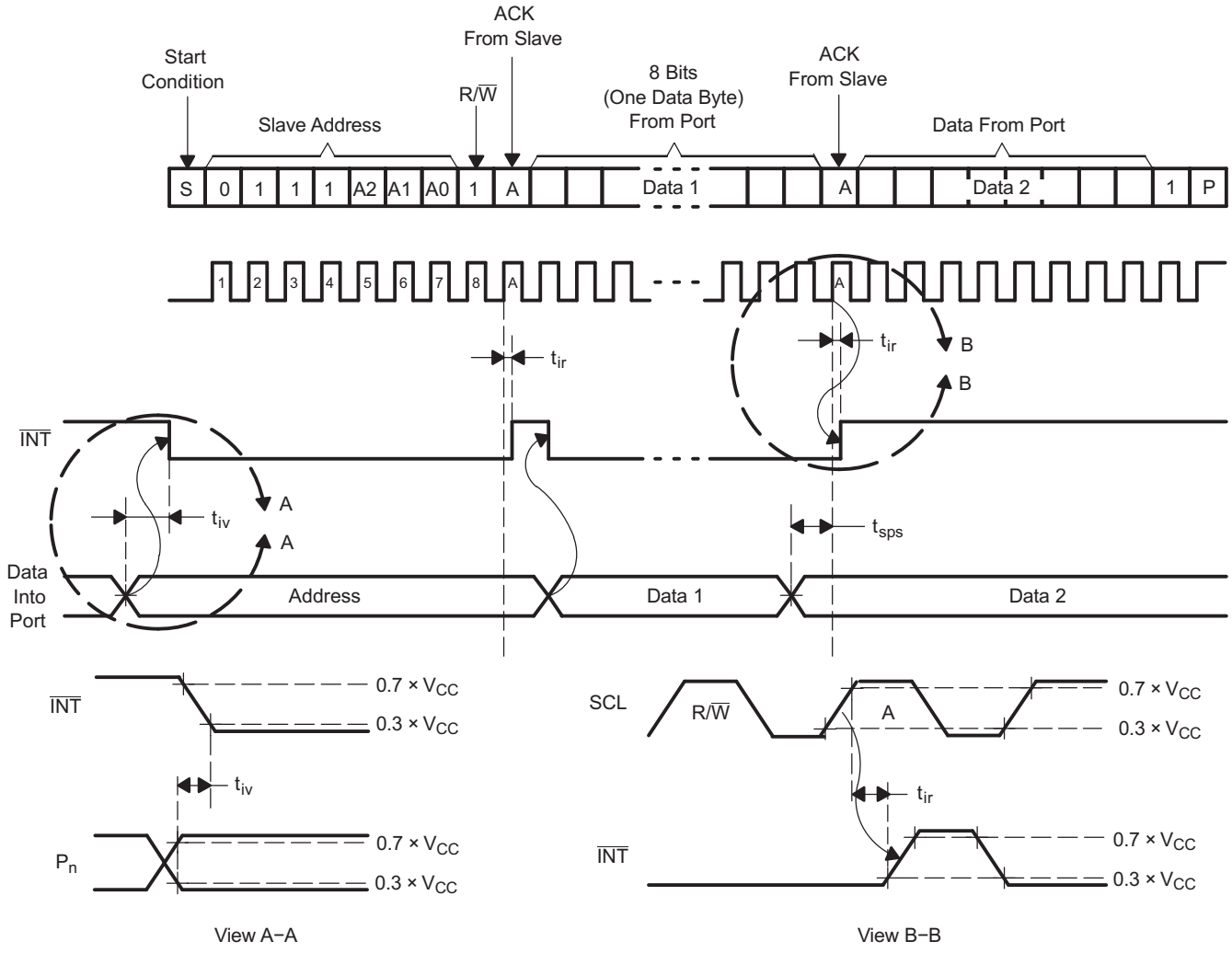
C. All parameters and waveforms are not applicable to all devices.

Figure 19. I^2C Interface Load Circuit and Voltage Waveforms

Parameter Measurement Information (continued)



INTERRUPT LOAD CONFIGURATION



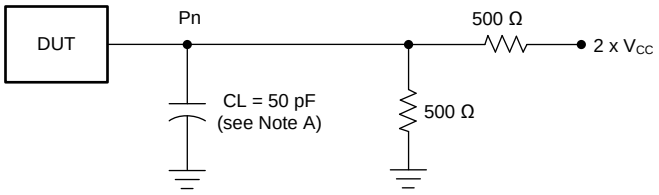
A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

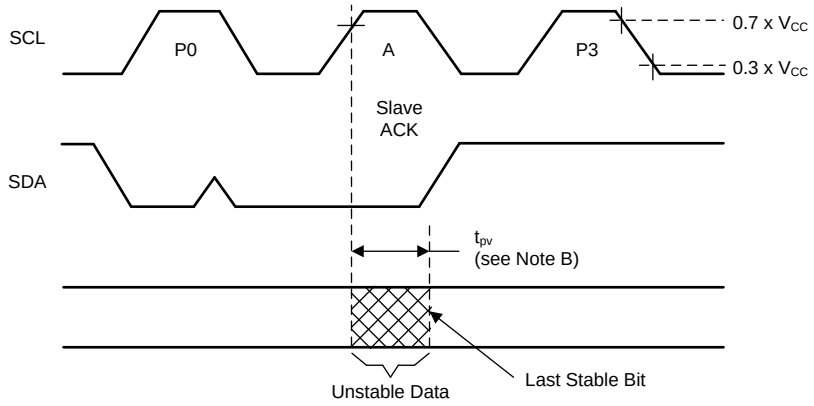
C. All parameters and waveforms are not applicable to all devices.

Figure 20. Interrupt Load Circuit and Voltage Waveforms

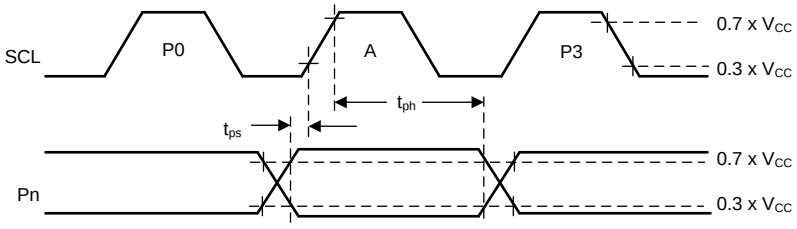
Parameter Measurement Information (continued)



P-PORT LOAD CONFIGURATION



WRITE MODE (R/$\overline{W}$ = 0)



READ MODE (R/$\overline{W}$ = 1)

A. C_L includes probe and jig capacitance.

B. t_{pv} is measured from 0.7 × V_{CC} on SCL to 50% I/O (Pn) output.

C. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

D. The outputs are measured one at a time, with one transition per measurement.

E. All parameters and waveforms are not applicable to all devices.

Figure 21. P-Port Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The TCA9534A is an 8-bit I/O expander for the two-line bidirectional bus (I^2C) is designed for 1.65-V to 5.5-V V_{CC} operation. It provides general-purpose remote I/O expansion for most micro-controller families via the I^2C interface (serial clock, SCL, and serial data, SDA, pins).

The TCA9534A open-drain interrupt ($\overline{INT}$) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed. The $\overline{INT}$ pin can be connected to the interrupt input of a micro-controller. By sending an interrupt signal on this line, the remote I/O can inform the micro-controller if there is incoming data on its ports without having to communicate via the I^2C bus. Thus, the TCA9534A can remain a simple slave device. The device outputs (latched) have high-current drive capability for directly driving LEDs.

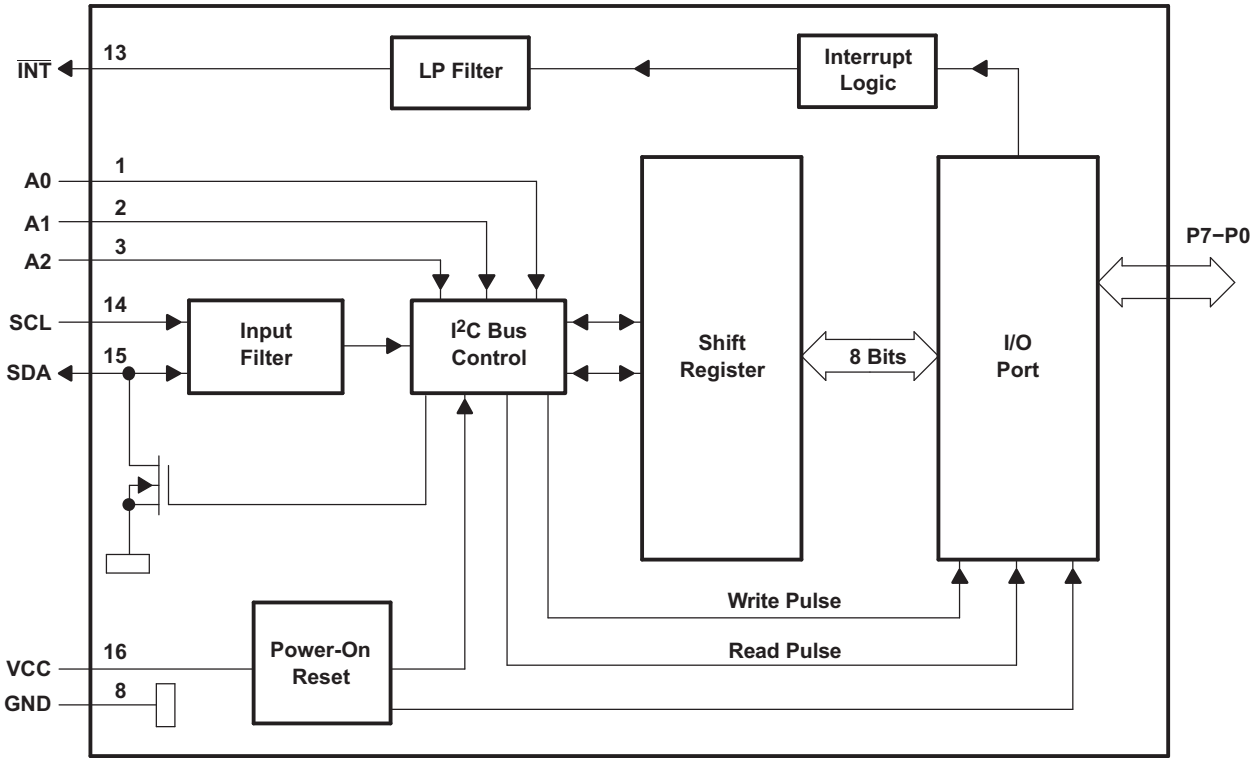
Three hardware pins (A0, A1, and A2) are used to program and vary the fixed I^2C slave address and allow up to eight devices to share the same I^2C bus or SMBus.

The system master can reset the TCA9534A in the event of a timeout or other improper operation by cycling the power supply and causing a power-on reset (POR). A reset puts the registers in their default state and initializes the I^2C /SMBus state machine.

The TCA9534A consists of one 8-bit Configuration (input or output selection), Input Port, Output Port, and Polarity Inversion (active high or active low) registers. At power on, the I/Os are configured as inputs. However, the system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input Port or Output Port register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

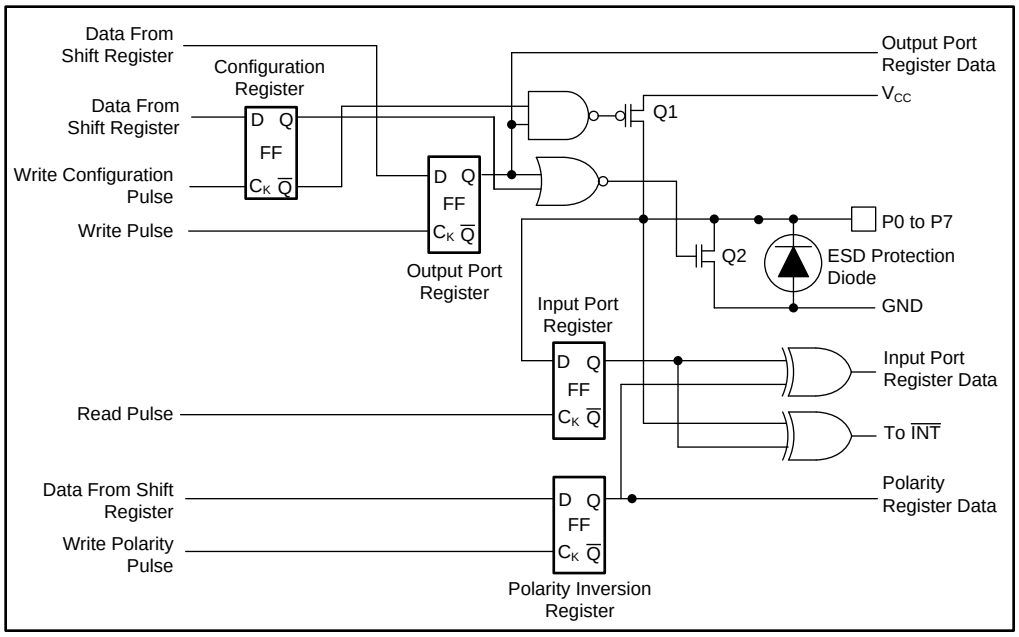
The TCA9534A is identical to the TCA9554 except for the removal of the internal I/O pull-up resistors, which greatly reduces power consumption when the I/Os are held LOW.

8.2 Functional Block Diagram



Pin numbers shown are for the PW package.

Figure 22. Functional Block Diagram



At power-on reset, all registers return to default values.

Figure 23. Simplified Schematic Of P0 To P7

8.3 Feature Description

8.3.1 I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input. The input voltage may be raised above V_{CC} to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled depending on the state of the output port register. In this case, there are low impedance paths between the I/O pin and either V_{CC} or GND. The external voltage applied to this I/O pin must not exceed the recommended levels for proper operation.

8.3.2 Interrupt Output ($\overline{INT}$)

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time, t_{iv}, the signal $\overline{INT}$ is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) bit after the rising edge of the SCL signal. Note that the $\overline{INT}$ is reset at the ACK just before the byte of changed data is sent. Interrupts that occur during the ACK clock pulse can be lost (or be very short) because of the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{INT}$.

Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

The $\overline{INT}$ output has an open-drain structure and requires pull-up resistor to V_{CC}.

8.4 Device Functional Modes

8.4.1 Power-On Reset

When power (from 0 V) is applied to VCC, an internal power-on reset holds the TCA9534A in a reset condition until V_{CC} has reached V_{PORR}. At that point, the reset condition is released and the TCA9534A registers and SMBus/I^2C state machine initialize to their default states. After that, V_{CC} must be lowered to below V_{PORF} and then back up to the operating voltage for a power-on reset cycle.

8.5 Programming

8.5.1 I^2C Interface

The TCA9534A has a standard bidirectional I^2C interface that is controlled by a master device in order to be configured or read the status of this device. Each slave on the I^2C bus has a specific device address to differentiate between other slave devices that are on the same I^2C bus. Many slave devices require configuration upon startup to set the behavior of the device. This is typically done when the master accesses internal register maps of the slave, which have unique register addresses. A device can have one or multiple registers where data is stored, written, or read. For more information see the *Understanding the I^2C Bus* application report.

The physical I^2C interface consists of the serial clock (SCL) and serial data (SDA) lines. Both SDA and SCL lines must be connected to V_{CC} through a pull-up resistor. The size of the pull-up resistor is determined by the amount of capacitance on the I^2C lines. For further details, see the *I^2C Pull-up Resistor Calculation* application report. Data transfer may be initiated only when the bus is idle. A bus is considered idle if both SDA and SCL lines are high after a STOP condition.

Figure 24 and Figure 25 show the general procedure for a master to access a slave device:

1. If a master wants to send data to a slave:
   - Master-transmitter sends a START condition and addresses the slave-receiver.
   - Master-transmitter sends data to slave-receiver.
   - Master-transmitter terminates the transfer with a STOP condition.
2. If a master wants to receive or read data from a slave:
   - Master-receiver sends a START condition and addresses the slave-transmitter.
   - Master-receiver sends the requested register to read to slave-transmitter.
   - Master-receiver receives data from the slave-transmitter.

Programming (continued)

– Master-receiver terminates the transfer with a STOP condition.

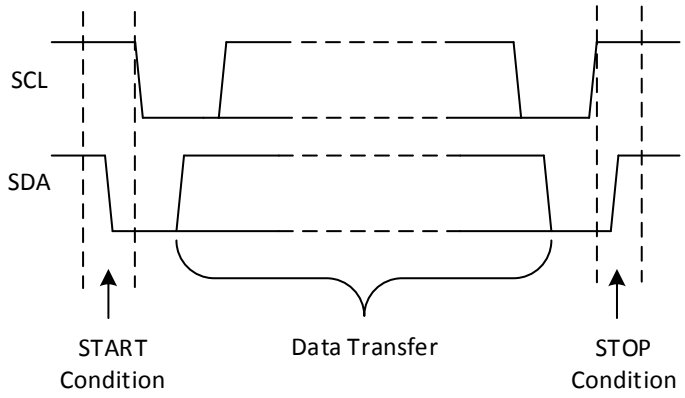


Figure 24. Definition of Start and Stop Conditions

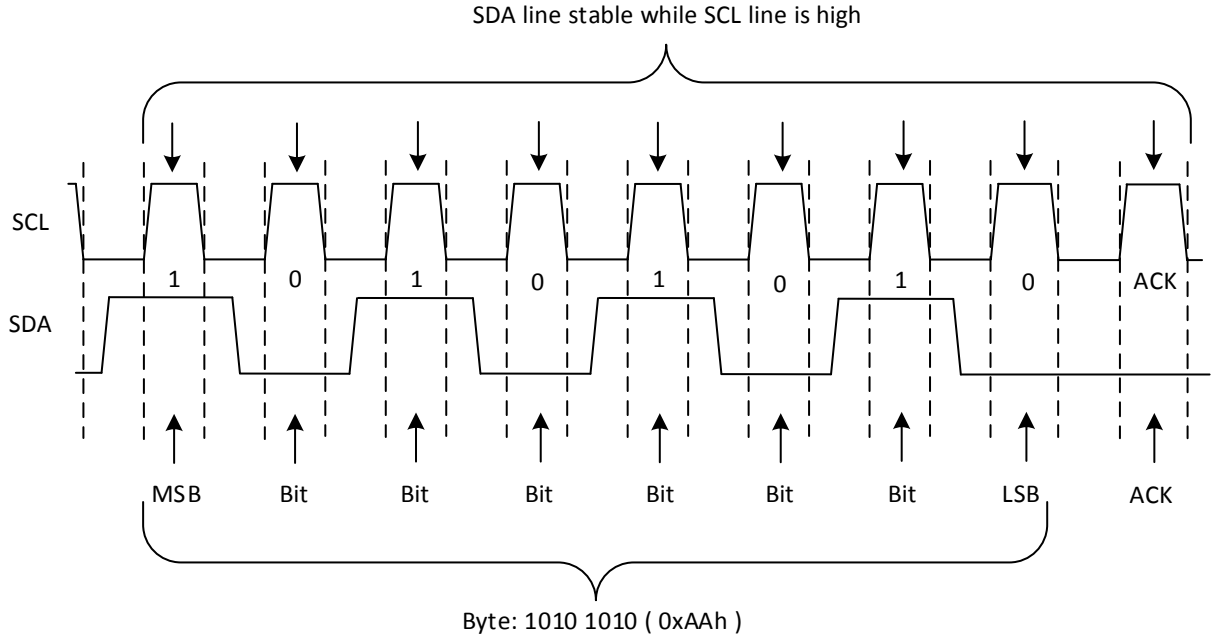


Figure 25. Bit Transfer

Table 1 shows the TCA9534A interface definition.

Table 1. Interface Definition Table

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I^2C slave address	L	H	H	H	A2	A1	A0	R/$\overline{W}$
Px I/O data bus	P7	P6	P5	P4	P3	P2	P1	P0

8.6 Register Maps

8.6.1 Device Address

Figure 26 shows the address byte of the TCA9534A.

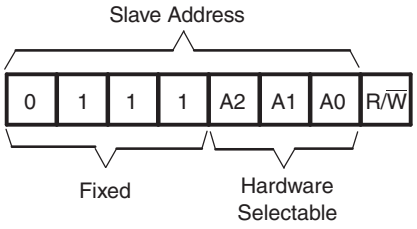


Figure 26. TCA9534A Address

Table 2 shows the TCA9534A address reference.

Table 2. Address Reference

INPUTS			I^2C BUS SLAVE ADDRESS
A2	A1	A0	
L	L	L	56 (decimal), 38 (hexadecimal)
L	L	H	57 (decimal), 39 (hexadecimal)
L	H	L	58 (decimal), 3A (hexadecimal)
L	H	H	59 (decimal), 3B (hexadecimal)
H	L	L	60 (decimal), 3C (hexadecimal)
H	L	H	61 (decimal), 3D (hexadecimal)
H	H	L	62 (decimal), 3E (hexadecimal)
H	H	H	63 (decimal), 3F (hexadecimal)

The last bit of the slave address defines the operation (read or write) to be performed. When it is high (1), a read is selected, while a low (0) selects a write operation.

8.6.2 Control Register and Command Byte

Following the successful Acknowledgment of the address byte, the bus master sends a command byte that is stored in the control register in the TCA9534A (see Figure 27). Two bits of this command byte state the operation (read or write) and the internal register (input, output, polarity inversion or configuration) that is affected. This register can be written or read through the I^2C bus. The command byte is sent only during a write transmission.

Once a command byte has been sent, the register that was addressed continues to be accessed by reads until a new command byte has been sent.

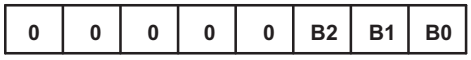


Figure 27. Control Register Bits

Table 3 shows the TCA9534A command byte.

Table 3. Command Byte Table

CONTROL REGISTER BITS		COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B1	B0				
0	0	0×00	Input Port	Read byte	XXXX XXXX
0	1	0×01	Output Port	Read/write byte	1111 1111
1	0	0×02	Polarity Inversion	Read/write byte	0000 0000
1	1	0×03	Configuration	Read/write byte	1111 1111

8.6.3 Register Descriptions

The Input Port register (register 0) reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level. See Table 4.

Before a read operation, a write transmission is sent with the command byte to indicate to the I^2C device that the Input Port register is accessed next.

Table 4. Register 0 (Input Port Register) Table

BIT	I7	I6	I5	I4	I3	I2	I1	I0
DEFAULT	X	X	X	X	X	X	X	X

The Output Port register (register 1) shows the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value. See Table 5.

Table 5. Register 1 (Output Port Register) Table

BIT	O7	O6	O5	O4	O3	O2	O1	O0
DEFAULT	1	1	1	1	1	1	1	1

The Polarity Inversion register (register 2) allows polarity inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with 1), the corresponding port pin polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding port pin original polarity is retained. See Table 6.

Table 6. Register 2 (Polarity Inversion Register) Table

BIT	N7	N6	N5	N4	N3	N2	N1	N0
DEFAULT	0	0	0	0	0	0	0	0

The Configuration register (register 3) configures the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output. See Table 7.

Table 7. Register 3 (Configuration Register) Table

BIT	C7	C6	C5	C4	C3	C2	C1	C0
DEFAULT	1	1	1	1	1	1	1	1

8.6.3.1 Bus Transactions

Data is exchanged between the master and the TCA9534A through write and read commands.

8.6.3.1.1 Writes

To write on the I^2C bus, the master sends a START condition on the bus with the address of the slave, as well as the last bit (the R/$\overline{W}$ bit) set to 0, which signifies a write. After the slave sends the acknowledge bit, the master then sends the register address of the register to which it wishes to write. The slave acknowledges again, letting the master know it is ready. After this, the master starts sending the register data to the slave until the master has sent all the data necessary (which is sometimes only a single byte), and the master terminates the transmission with a STOP condition.

See Table 3 to see list of the internal registers and a description of each one.

Figure 28 shows an example of writing a single byte to a slave register.

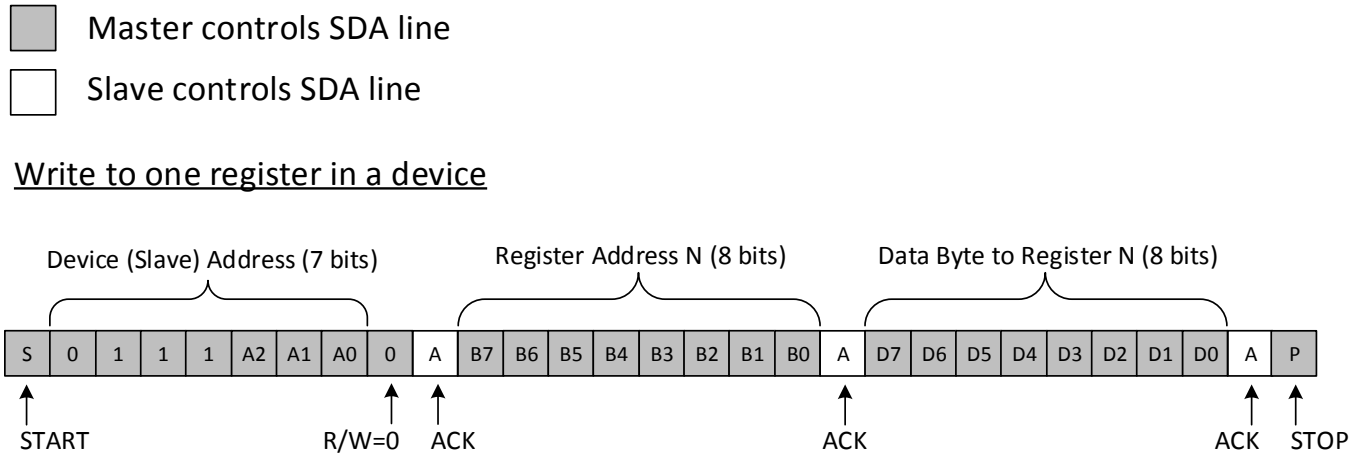


Figure 28. Write to Register

Figure 29 shows an example of writing to the output port register.

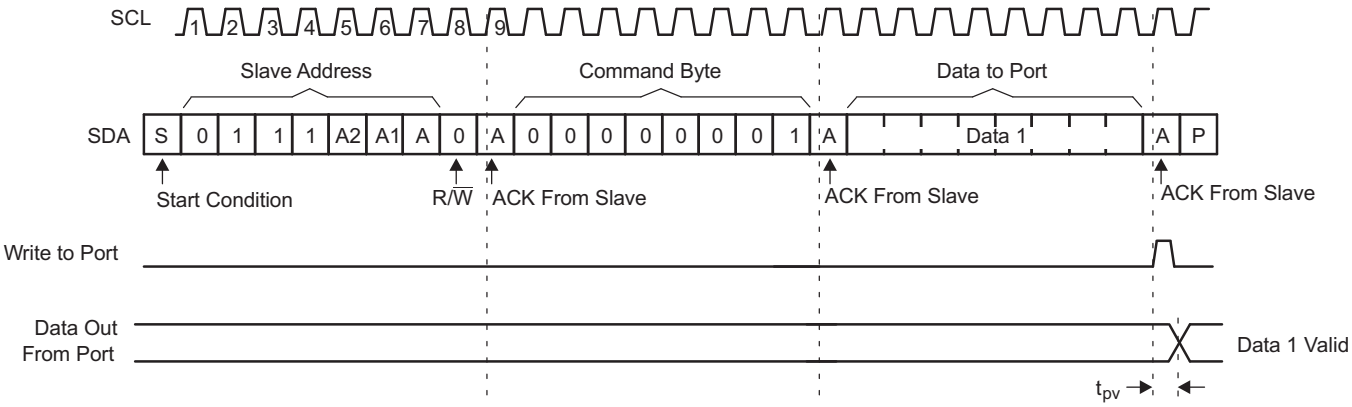


Figure 29. Write to Output Port Register

Figure 30 shows an example of writing to the configuration or polarity inversion registers.

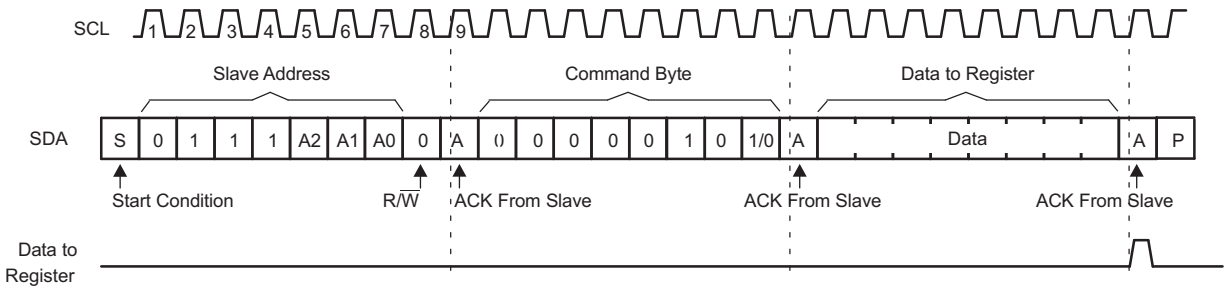


Figure 30. Write to Configuration or Polarity Inversion Registers

8.6.3.1.2 Reads

Reading from a slave is very similar to writing, but requires some additional steps. In order to read from a slave, the master must first instruct the slave which register it wishes to read from. This is done by the master starting off the transmission in a similar fashion as the write, by sending the address with the R/$\overline{W}$ bit equal to 0 (signifying a write), followed by the register address it wishes to read from. When the slave acknowledges this register address, the master sends a START condition again, followed by the slave address with the R/$\overline{W}$ bit set to 1 (signifying a read). This time, the slave acknowledges the read request, and the master releases the SDA bus but continues supplying the clock to the slave. During this part of the transaction, the master becomes the master-receiver, and the slave becomes the slave-transmitter.

The master continues to send out the clock pulses, but releases the SDA line so that the slave can transmit data. At the end of every byte of data, the master sends an ACK to the slave, letting the slave know that it is ready for more data. When the master has received the number of bytes it is expecting, it sends a NACK, signaling to the slave to halt communications and release the bus. The master follows this up with a STOP condition.

See Table 3 for the list of the internal registers and a description of each one.

If a read is requested by the master after a POR without first setting the command byte via a write, the device will NACK until a command byte-register address is set as described above.

Figure 31 shows an example of reading a single byte from a slave register.

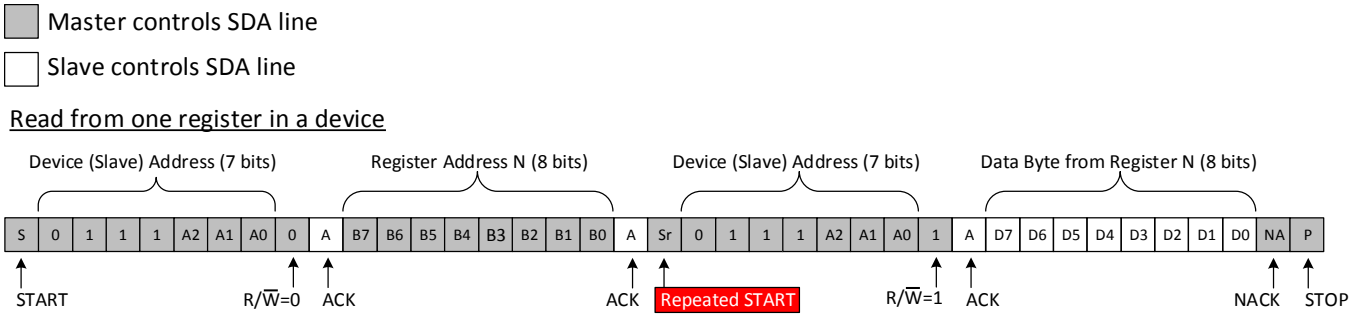
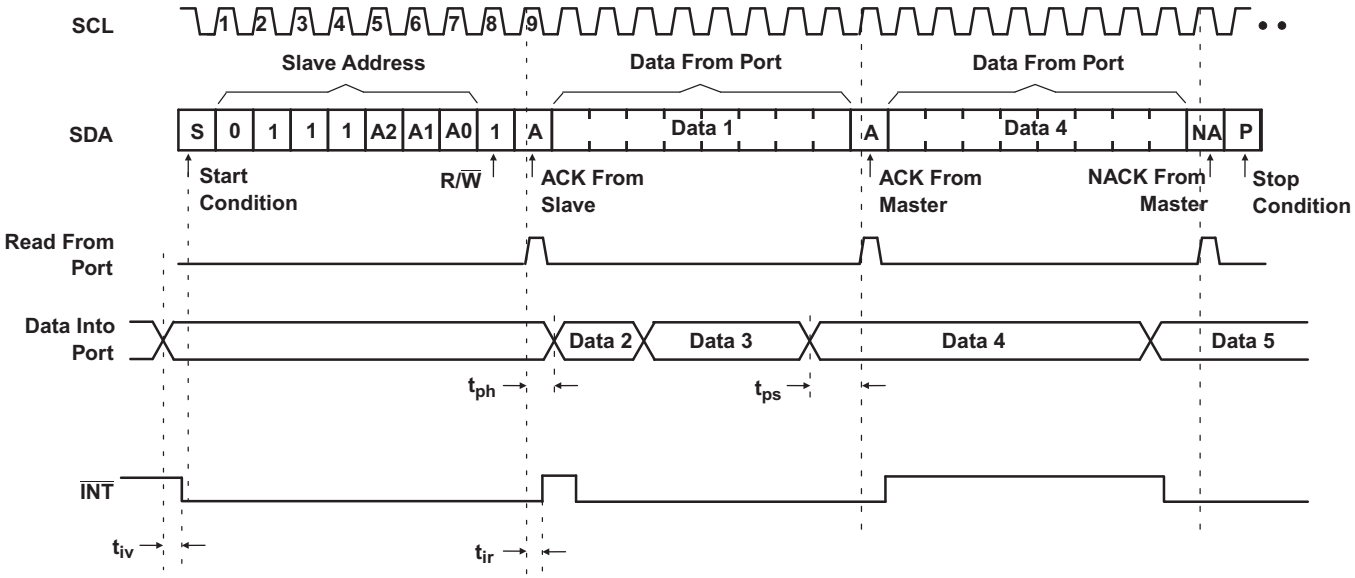


Figure 31. Read From Register

Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data. See Figure 32.



A. This figure assumes the command byte has previously been programmed with 00h.

B. Transfer of data can be stopped at any moment by a Stop condition.

C. This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port. See the *Reads* section for these details.

Figure 32. Read From Input Port Register

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

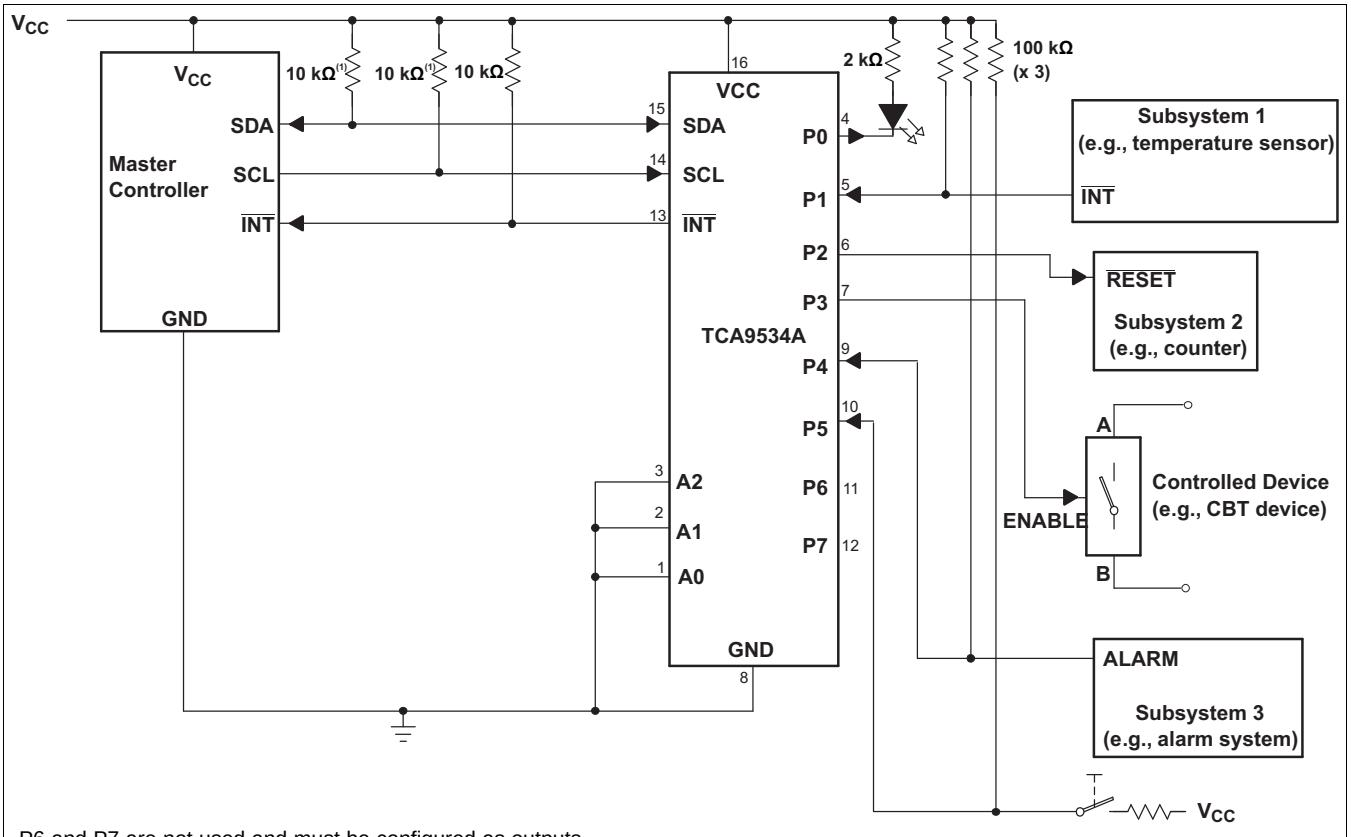
9.1 Application Information

Figure 33 shows an application in which the TCA9534A can be used.

IO Expanders such as the TCA9534A are commonly used to obtain more general purpose I/Os. There are many common uses for these additional I/Os:

- Inputs from other ICs, such as interrupt signals from sensors
- Inputs from physical buttons (for detecting button presses)
- Outputs to control RESET or ENABLE signals on other ICs
- Outputs for controlling LEDs for visual feedback to a user

9.2 Typical Application



P6 and P7 are not used and must be configured as outputs.

Figure 33. Application Schematic

Typical Application (continued)

9.2.1 Design Requirements

9.2.1.1 Calculating Junction Temperature and Power Dissipation

When designing with the TCA9534A, it is important that the *Recommended Operating Conditions* not be violated. Many of the parameters of this device are rated based on junction temperature. So junction temperature must be calculated in order to verify that safe operation of the device is met. The basic equation for junction temperature is shown in Equation 1.

$$T_j = T_A + (\theta_{JA} \times P_d) \quad (1)$$

θ_{JA} is the standard junction to ambient thermal resistance measurement of the package, as seen in *Thermal Information* table. P_d is the total power dissipation of the device, and the approximation is shown in Equation 2.

$$P_d \approx (I_{CC\_STATIC} \times V_{CC}) + \sum P_{d\_PORT\_L} + \sum P_{d\_PORT\_H} \quad (2)$$

Equation 2 is the approximation of power dissipation in the device. The equation is the static power plus the summation of power dissipated by each port (with a different equation based on if the port is outputting high, or outputting low. If the port is set as an input, then power dissipation is the input leakage of the pin multiplied by the voltage on the pin). Note that this ignores power dissipation in the $\overline{INT}$ and SDA pins, assuming these transients to be small. They can easily be included in the power dissipation calculation by using Equation 3 to calculate the power dissipation in $\overline{INT}$ or SDA while they are pulling low, and this gives maximum power dissipation.

$$P_{d\_PORT\_L} = (I_{OL} \times V_{OL}) \quad (3)$$

Equation 3 shows the power dissipation for a single port which is set to output low. The power dissipated by the port is the V_{OL} of the port multiplied by the current it is sinking.

$$P_{d\_PORT\_H} = (I_{OH} \times (V_{CC} - V_{OH})) \quad (4)$$

Equation 4 shows the power dissipation for a single port which is set to output high. The power dissipated by the port is the current sourced by the port multiplied by the voltage drop across the device (difference between V_{CC} and the output voltage).

9.2.1.2 Minimizing I_{CC} When I/Os Control LEDs

When the I/Os are used to control LEDs, normally they are connected to V_{CC} through a resistor as shown in Figure 33. For a P-port configured as an input, I_{CC} increases as V_I becomes lower than V_{CC}. The LED is a diode, with threshold voltage V_T, and when a P-port is configured as an input the LED is off but V_I is a V_T drop below V_{CC}.

For battery-powered applications, it is essential that the voltage of P-ports controlling LEDs is greater than or equal to V_{CC} when the P-ports are configured as input to minimize current consumption. Figure 34 shows a high-value resistor in parallel with the LED. Figure 35 shows V_{CC} less than the LED supply voltage by at least V_T. Both of these methods maintain the I/O V_I at or above V_{CC} and prevents additional supply current consumption when the P-port is configured as an input and the LED is off.

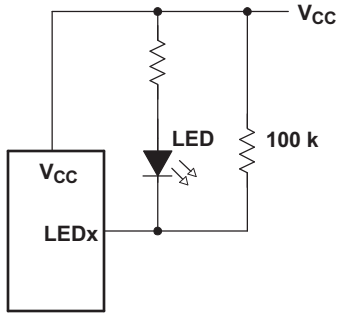


Figure 34. High-Value Resistor in Parallel With LED

Typical Application (continued)

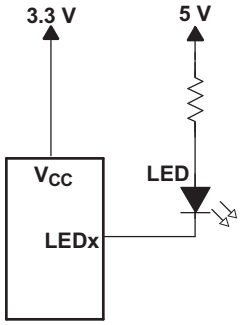


Figure 35. Device Supplied by a Lower Voltage

9.2.2 Detailed Design Procedure

The pull-up resistors, R_P, for the SCL and SDA lines need to be selected appropriately and take into consideration the total capacitance of all slaves on the I^2C bus. The minimum pull-up resistance is a function of V_{CC}, $V_{OL,(max)}$, and I_{OL} as shown in Equation 5.

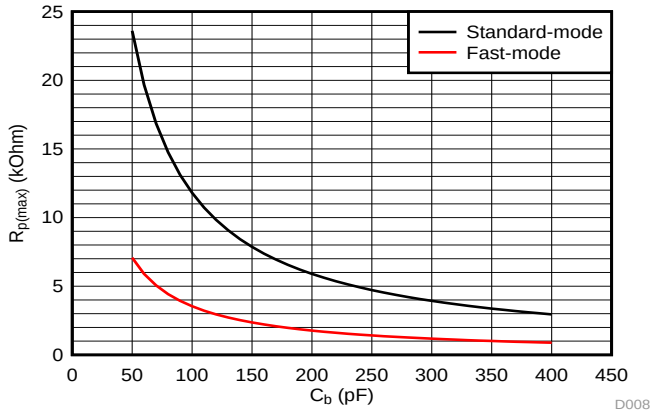
$$R_{p(min)} = \frac{V_{CC} - V_{OL(max)}}{I_{OL}} \quad (5)$$

The maximum pull-up resistance is a function of the maximum rise time, t_r (300 ns for fast-mode operation, f_{SCL} = 400 kHz) and bus capacitance, C_b as shown in Equation 6.

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (6)$$

The maximum bus capacitance for an I^2C bus must not exceed 400 pF for standard-mode or fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the TCA9534A, C_i for SCL or C_{io} for SDA, the capacitance of wires, connections, traces, and the capacitance of additional slaves on the bus.

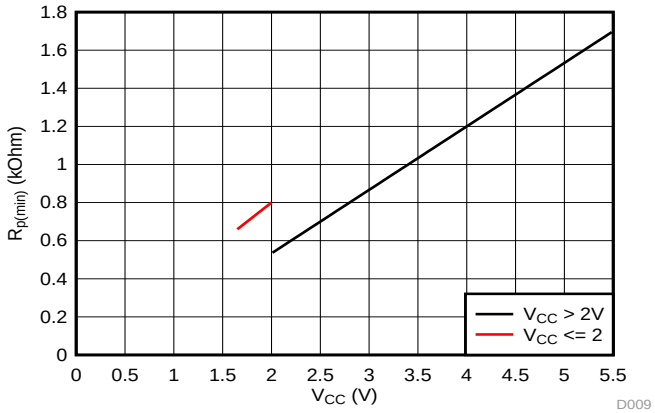
9.2.3 Application Curves



Standard-mode (f_{SCL} = 100 kHz, t_r = 1 µs)

Fast-mode (f_{SCL} = 400 kHz, t_r = 300 ns)

Figure 36. Maximum Pull-Up resistance ($R_{p(max)}$) vs Bus Capacitance (C_b)



V_{OL} = 0.2*V_{CC}, I_{OL} = 2 mA when V_{CC} ≤ 2 V

V_{OL} = 0.4 V, I_{OL} = 3 mA when V_{CC} > 2 V

Figure 37. Minimum Pull-Up Resistance ($R_{p(min)}$) vs Pull-Up Reference Voltage (V_{CC})

10 Power Supply Recommendations

10.1 Power-On Reset Requirements

In the event of a glitch or data corruption, the TCA9534A can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The two types of power-on reset are shown in and Figure 38.

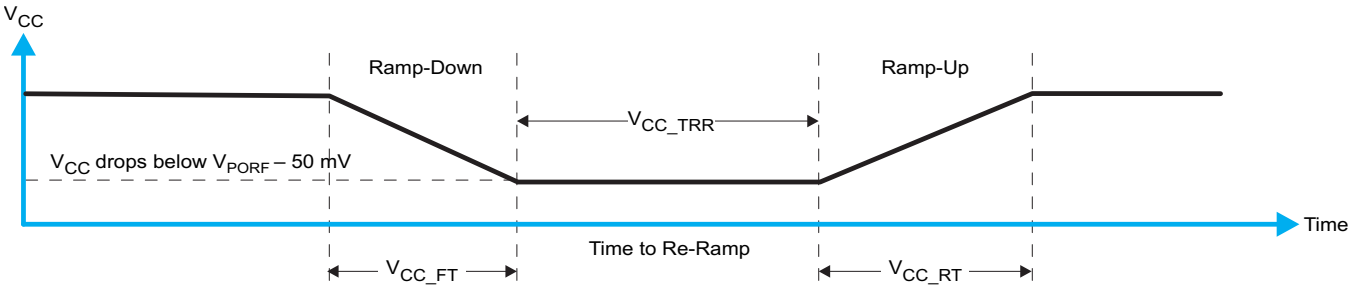


Figure 38. V_{CC} is Lowered Below the POR Threshold, then Ramped Back Up to V_{CC}

Table 8 specifies the performance of the power-on reset feature for the TCA9534A for both types of power-on reset.

Table 8. Recommended Supply Sequencing and Ramp Rates(1)

PARAMETER			MIN	MAX	UNIT
V_{CC_FT}	Fall rate	See Figure 38	1	2000	ms
V_{CC_RT}	Rise rate	See Figure 38	0.1	2000	ms
V_{CC_TRR}	Time to re-ramp (when V_{CC} drops to V_{POR_MIN} – 50 mV or when V_{CC} drops to GND)	See Figure 38	1		µs
V_{CC_GH}	Level that V_{CCP} can glitch down to, but not cause a functional disruption when V_{CCX_GW} = 1 µs	See Figure 39		1.2	V
V_{CC_MV}	The minimum voltage that V_{CC} can glitch down to without causing a reset (V_{CC_GH} must not be violated)	See Figure 39	1.5		V
V_{CC_GW}	Glitch width that does not cause a functional disruption when V_{CCX_GH} = 0.5 × V_{CCx}	See Figure 39		10	µs

(1) All supply sequencing and ramp rate values are measured at T_A = 25°C

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 39 and Table 8 provide more information on how to measure these specifications.

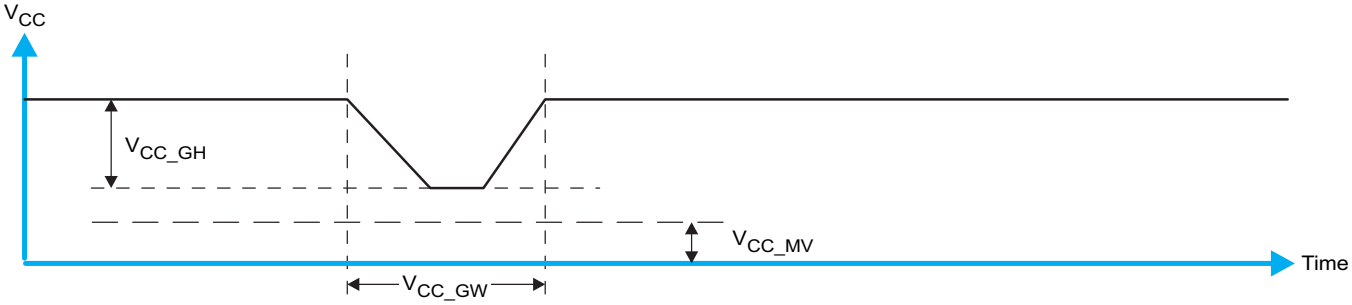


Figure 39. Glitch Width and Glitch Height

V_{POR} is critical to the power-on reset. V_{POR} is the voltage level at which the reset condition is released and all the registers and the I^2C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. Figure 40 and Table 8 provide more details on this specification.

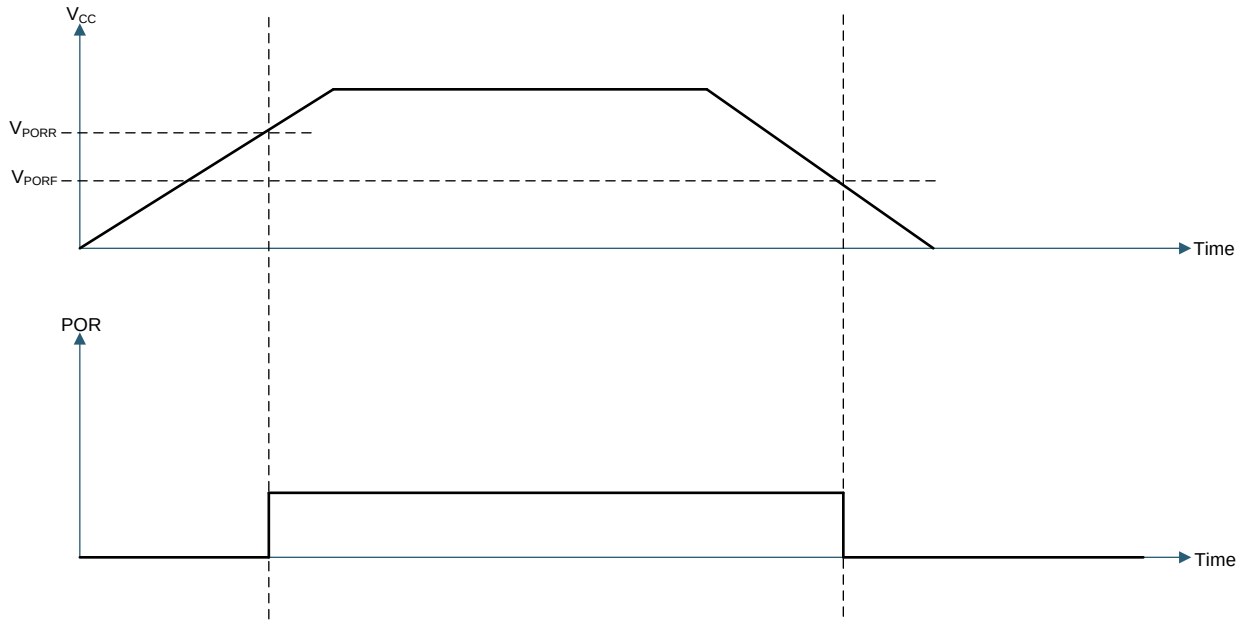


Figure 40. V_{POR}

11 Layout

11.1 Layout Guidelines

For printed circuit board (PCB) layout of the TCA9534A, common PCB layout practices must be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I^2C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. By-pass and de-coupling capacitors are commonly used to control the voltage on the VCC pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple. These capacitors must be placed as close to the TCA9534A as possible. These best practices are shown in Figure 41.

For the layout example provided in Figure 41, it is possible to fabricate a PCB with only 2 layers by using the top layer for signal routing and the bottom layer as a split plane for power (V_{CC}) and ground (GND). However, a 4 layer board is preferable for boards with higher density signal routing. On a 4 layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which needs to attach to V_{CC} or GND and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board, but this technique is not demonstrated in Figure 41.

11.2 Layout Example

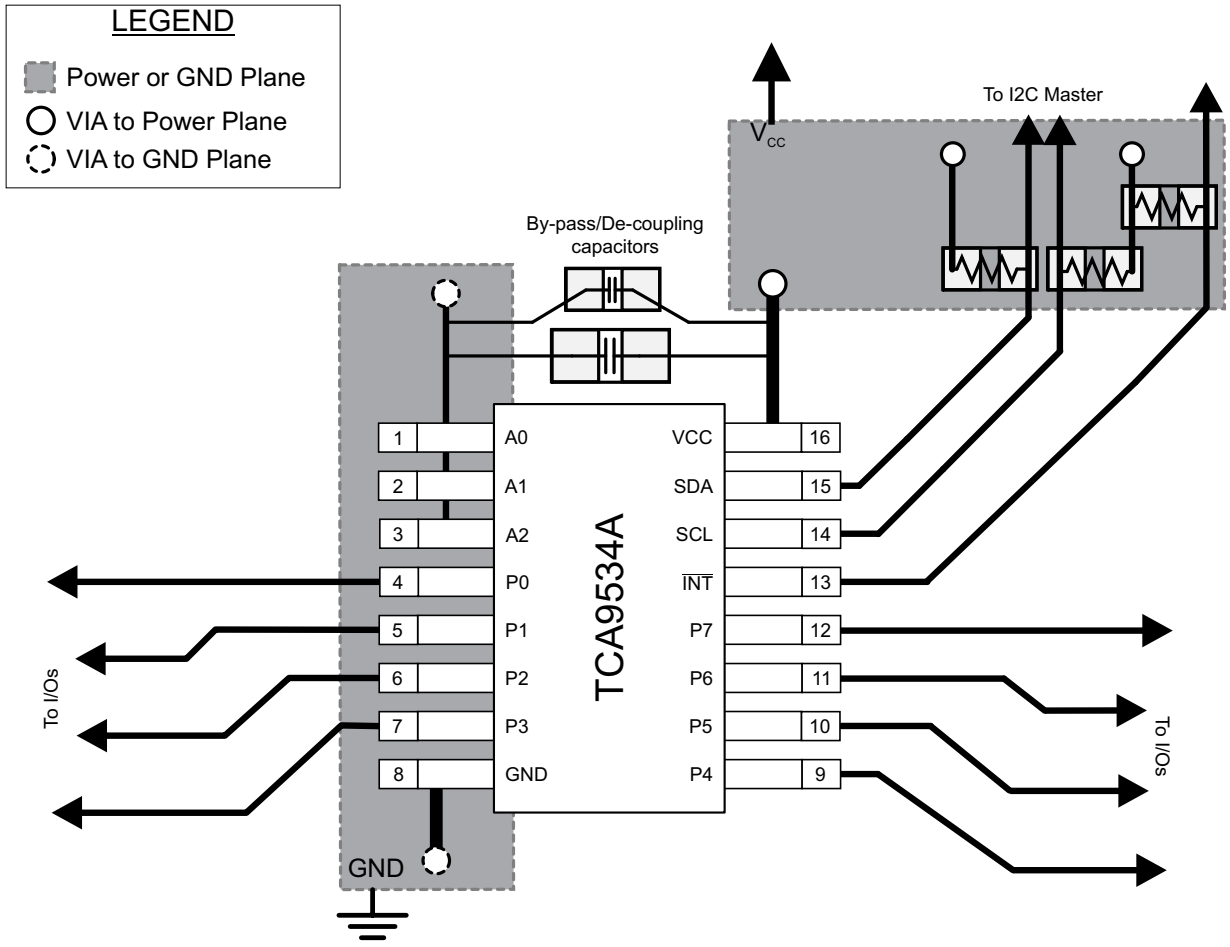


Figure 41. TCA9534A Layout

12 器件和文档支持

12.1 相关文档

请参阅如下相关文档：

- *《I2C 总线上拉电阻器计算》*
- *《I2C 总线在采用中继器时的最高时钟频率》*
- *《逻辑器件简介》*
- *《理解 I2C 总线》*
- *《IO 扩展器 EVM 用户指南》*
- *《为新设计挑选合适的 I2C 器件》*

12.2 接收文档更新通知

如需接收文档更新通知，请访问 ti.com 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

12.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA9534ADWR	ACTIVE	SOIC	DW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TCA9534A	Samples
TCA9534ADWT	ACTIVE	SOIC	DW	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TCA9534A	Samples
TCA9534APWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	PW534A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

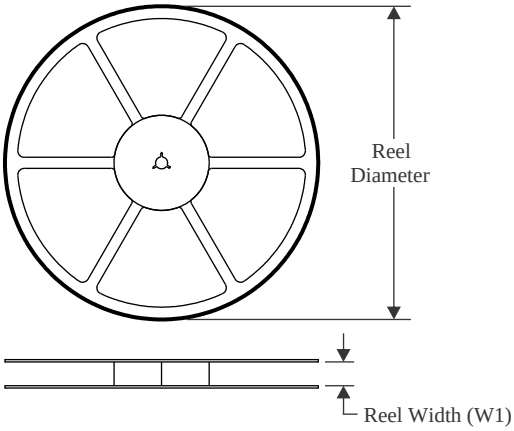
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

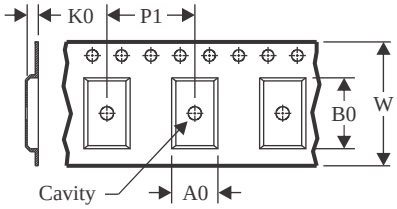
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

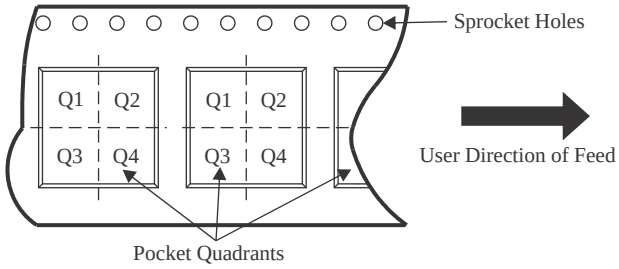


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

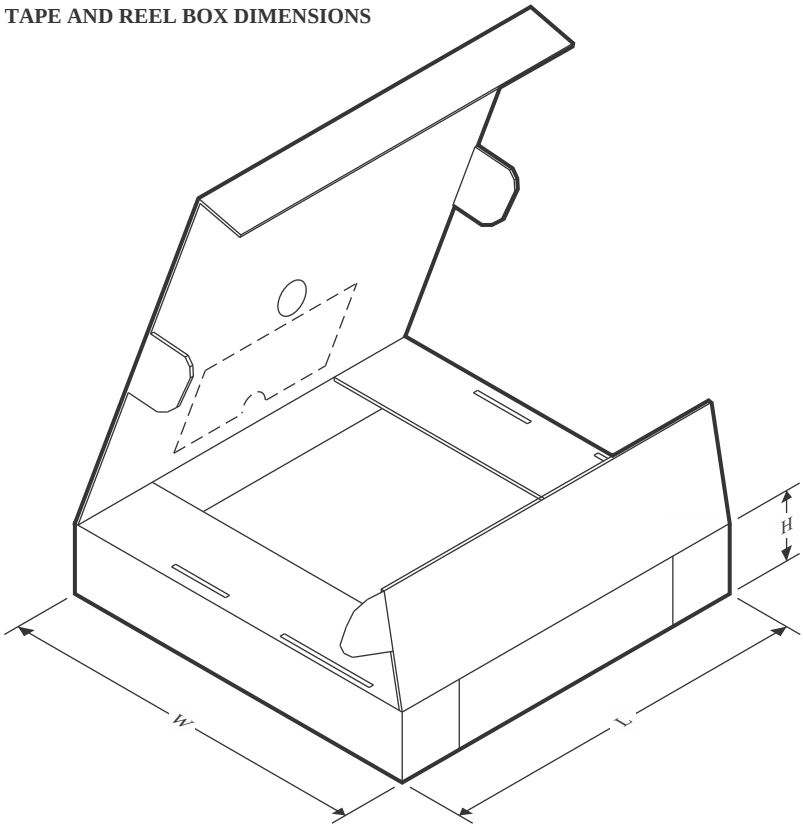
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA9534ADWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
TCA9534APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

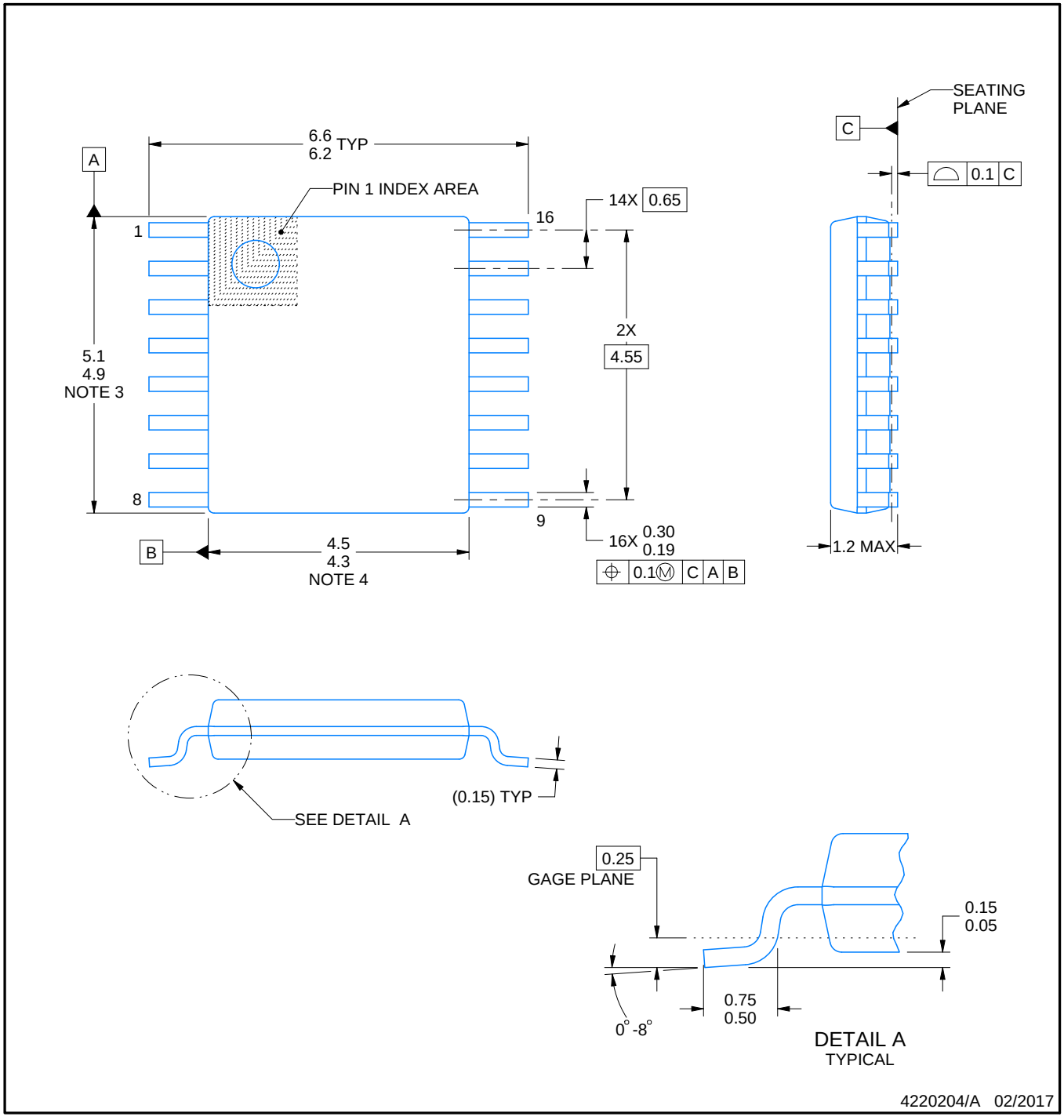
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA9534ADWR	SOIC	DW	16	2000	350.0	350.0	43.0
TCA9534APWR	TSSOP	PW	16	2000	356.0	356.0	35.0

PACKAGE OUTLINE

PW0016A

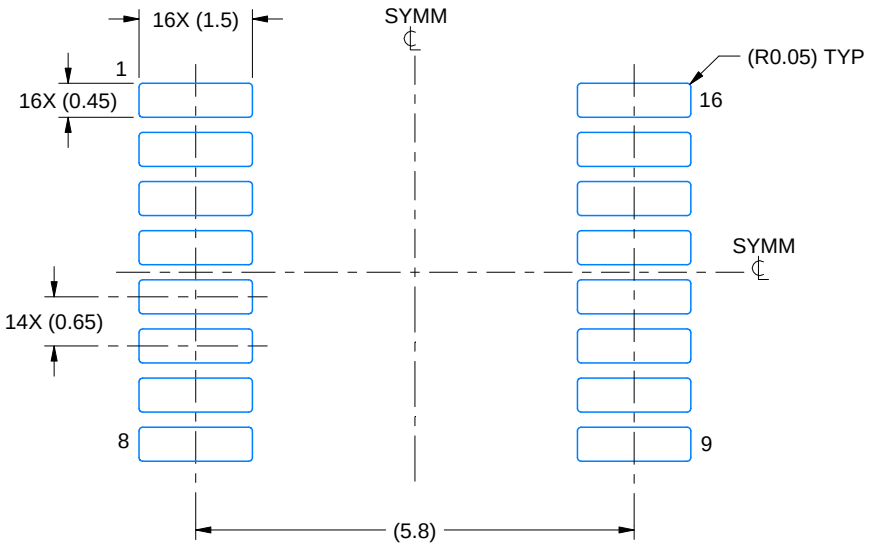
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

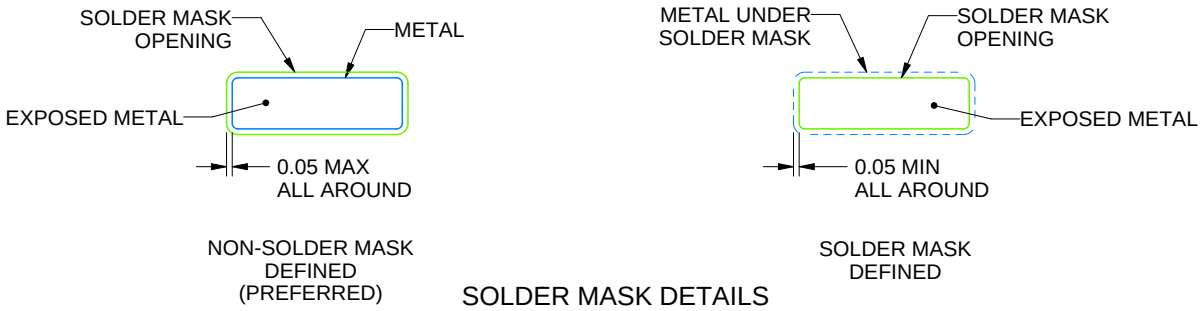


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

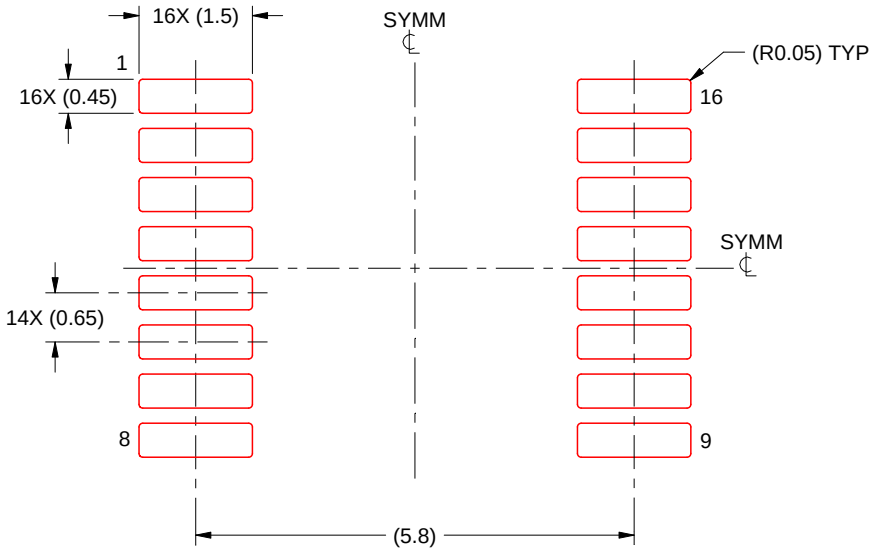


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

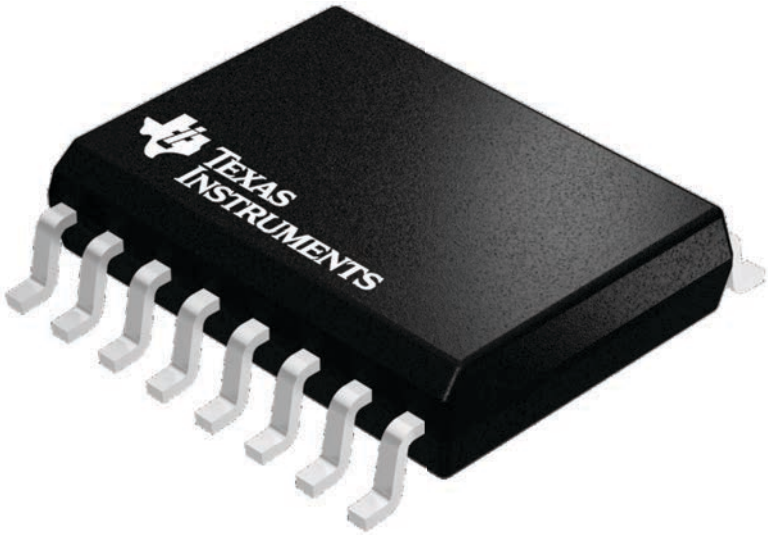
DW 16

SOIC - 2.65 mm max height

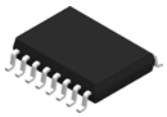
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

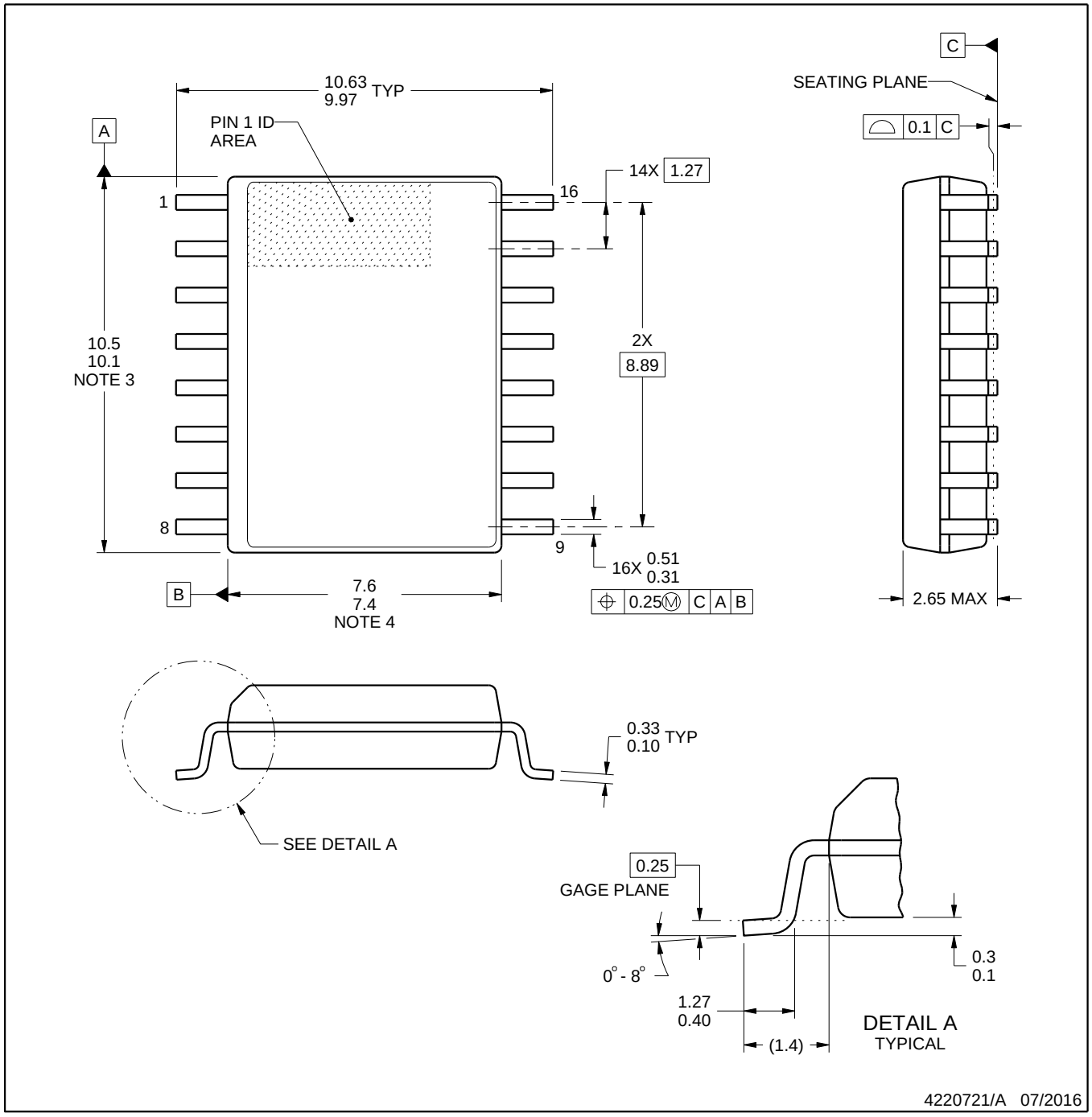


PACKAGE OUTLINE

DW0016A

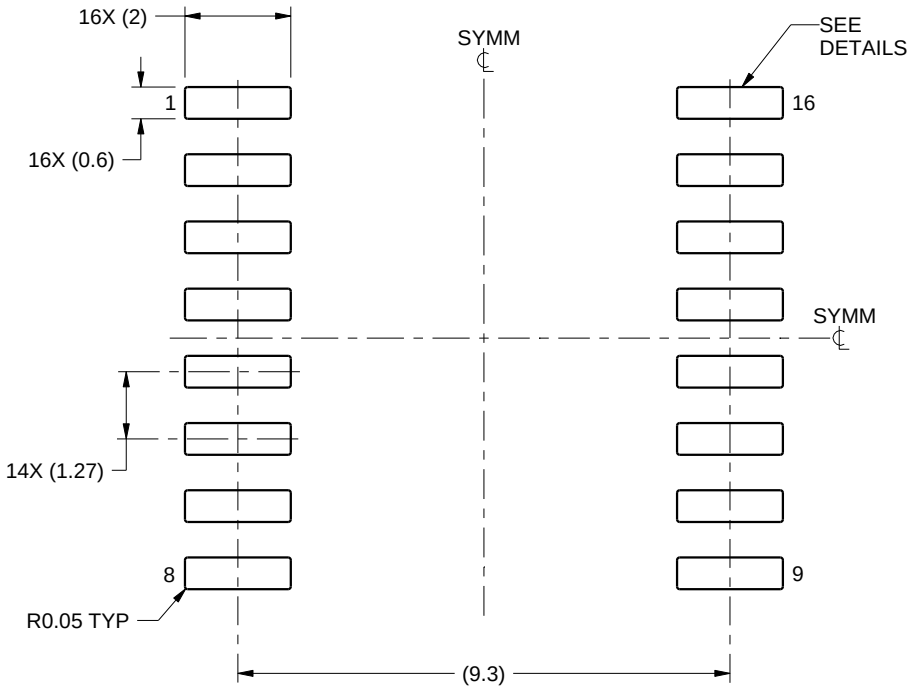
SOIC - 2.65 mm max height

SOIC

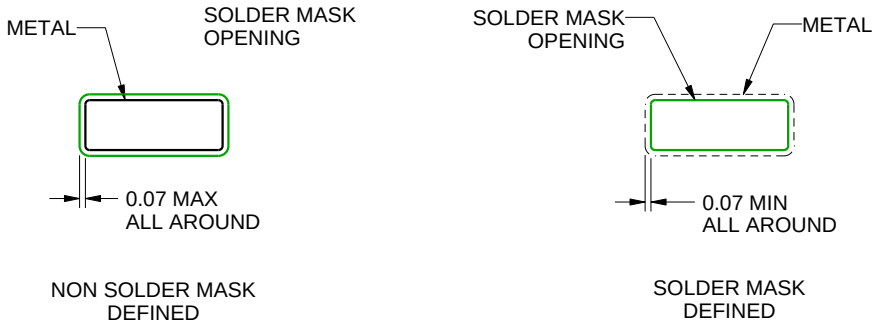


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

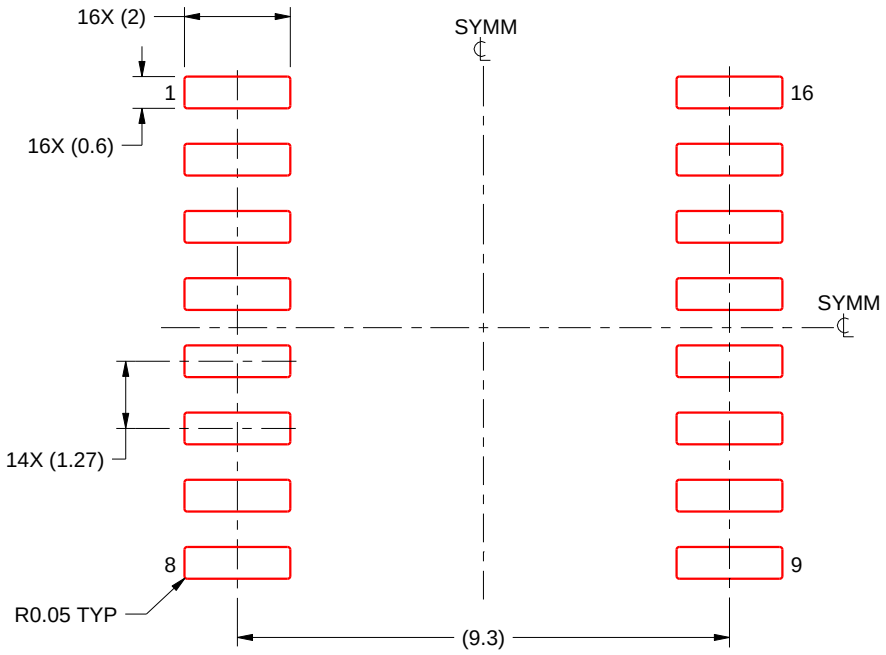


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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