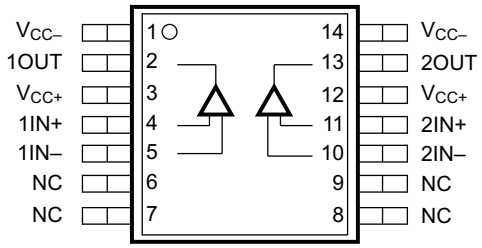
250-mA DUAL DIFFERENTIAL LINE DRIVER

FEATURES

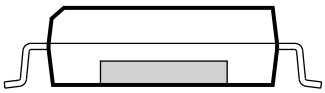
- **ADSL, HDSL and VDSL Differential Line Driver**
- **200-mA Output Current Minimum Into 50-Ω Load**
- **High Speed**
  - **210-MHz Bandwidth (–3-dB) at 50-Ω Load**
  - **300-MHz Bandwidth (–3-dB) at 100-Ω Load**
  - **1900-V/µs Slew Rate, G = 5**
- **Low Distortion**
  - **–69-dB Third-Order Harmonic Distortion at f = 1 MHz, 50-Ω Load, and $V_{O(PP)}$ = 20 V**
- **Independent Power Supplies for Low Crosstalk**
- **Wide Supply Range ±5 V to ±15 V**
- **Thermal-Shutdown and Short-Circuit Protection**
- **Evaluation Module Available**

Thermally Enchanced TSSOP (PWP)
PowerPAD™ Package
(Top View)



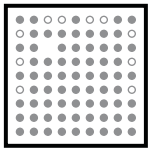
NC – No internal connection

(Side View)



Cross Section View Showing Thermal Pad

MicroStar™ Junior (GQE) Package
(Top View)



(Side View)

P0067-01

DESCRIPTION

The THS6022 contains two high-speed drivers capable of providing 200-mA output current (minimum) into a 50-Ω load. These drivers can be configured differentially to drive a 50-V p-p output signal over low-impedance lines. The drivers are current feedback amplifiers, designed for the high slew rates necessary to support low total harmonic distortion (THD) in xDSL applications. The THS6022 is ideally suited for asymmetrical digital subscriber line (ADSL) at the remote terminal, high-data-rate digital subscriber line (HDSL), and very high-data-rate digital subscribe line (VDSL), where it supports the high-peak voltage and current requirements of these applications. Separate power supply connections for each driver are provided to minimize crosstalk.

HIGH-SPEED xDSL LINE DRIVER/RECEIVER FAMILY

DEVICE	DRIVER	RECEIVER	DESCRIPTION
THS6002	√	√	Dual differential line drivers and receivers
THS6012	√		500-mA dual differential line driver
THS6022	√		250-mA dual differential line driver
THS6032	√		Low-power ADSL central office line driver
THS6062		√	Low-noise ADSL receiver

HIGH-SPEED xDSL LINE DRIVER/RECEIVER FAMILY (continued)

DEVICE	DRIVER	RECEIVER	DESCRIPTION
THS7002		√	Low-noise programmable gain ADSL receiver

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

The THS6022 is packaged in the patented PowerPAD™ package. This package provides outstanding thermal characteristics in a small-footprint package that is fully compatible with automated surface-mount assembly procedures. The exposed thermal pad on the underside of the package is in direct contact with the die. By simply soldering the pad to the PWB copper and using other thermal outlets, the heat is conducted away from the junction.

AVAILABLE OPTIONS

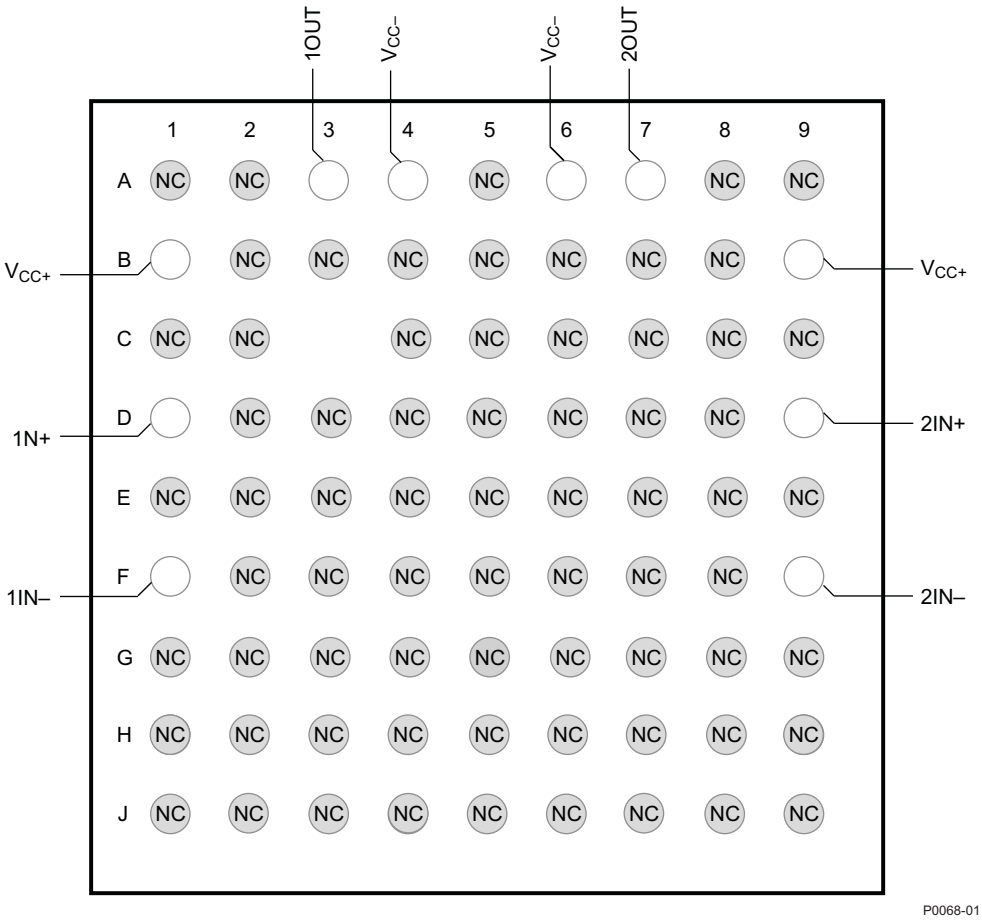
T_A	PACKAGED DEVICE		
	PowerPAD™ PLASTIC SMALL OUTLINE(1) (PWP)	MicroStar Junior™ (GQE)	EVALUATION MODULE
0°C to 70°C	THS6022CPWP	THS6022CGQE	THS6022EVM
–40°C to 85°C	THS6022IPWP	THS6022IGQE	–

(1) The PWP packages are available taped and reeled. Add an R suffix to the device type (e.g., THS6022CPWPR)

TERMINAL FUNCTIONS

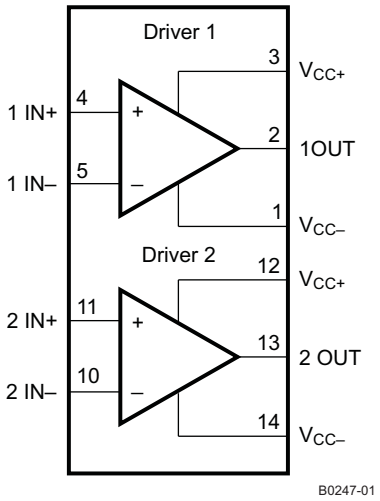
TERMINAL		
NAME	PWP PACKAGE TERMINAL NO.	GQE PACKAGE TERMINAL NO.
1OUT	2	A3
1IN–	5	F1
1IN+	4	D1
2OUT	13	A7
2IN–	10	F9
2IN+	11	D9
V_{CC+}	3, 12	B1, B9
$V_{CC–}$	1, 14	A4, A6
NC	6, 7, 8, 9	NA

MicroStar™Junior (GQE) Package
(Top View)



NOTE: Shaded terminals are used for thermal connection to the ground plane.

Functional Block Diagram



ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
V_{CC+} to V_{CC-}	Supply voltage	33	V
V_I	Input voltage	$\pm V_{CC}$	V
I_O	Output current	400	mA
V_{ID}	Differential input voltage	6	V
	Continuous total power dissipation at (or below) T_A = 25°C	3.3	W
T_A	Operating free air temperature	–40 to 85	°C
T_{stg}	Storage temperature	–65 to 125	°C
	Lead temperature, 1,6 mm (1/16 inch) from case for 10 seconds	300	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC+} and V_{CC-}	Supply voltage	Split supply	±4.5		±16	V
		Single supply	9		32	
T_A	Operating free-air temperature	C suffix	0		70	°C
		I suffix	–40		85	

ELECTRICAL CHARACTERISTICS

V_{CC} = ±15 V, R_L = 50 Ω, R_F = 1 kΩ, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
Dynamic Performance								
BW	Small-signal bandwidth (–3 dB)	V_O = 200 mV, G = 1	V_{CC} = ±15 V	R_F = 787 Ω		210		MHz
			V_{CC} = ±5 V	R_F = 910 Ω		150		
		VO = 200 mV, G = 2	V_{CC} = ±15 V	R_F = 787 Ω		590		
			V_{CC} = ±5 V	R_F = 910 Ω		715		
		V_O = 100 mV, G = 1	V_{CC} = ±15 V	R_F = 750 Ω		300		
			V_{CC} = ±5 V	R_F = 910 Ω		210		
		V_O = 100 mV, G = 2	V_{CC} = ±15 V	R_F = 620 Ω		260		
			V_{CC} = ±5 V	R_F = 680 Ω		180		
	Bandwidth for 0.1-dB flatness	R_L = 50 Ω, G = 2	V_{CC} = ±15 V	R_F = 590 Ω		115		
			V_{CC} = ±5 V	R_F = 715 Ω		70		
		R_L = 100 Ω, G = 2	V_{CC} = ±15 V	R_F = 620 Ω		140		
			V_{CC} = ±5 V	R_F = 680 Ω		80		
SR	Slew rate (1)	V_{CC} = ±15 V,	$V_{O(PP)}$ = 20 V,	G = 5		1900		V/µs
		V_{CC} = ±5 V,	$V_{O(PP)}$ = 5 V,	G = 2		950		
t_S	Settling time to 0.1%	0-V to 10-V step,	G = 2,	R_L = 1 kΩ		70		ns
	Full-power bandwidth (2)	V_{CC} = ±15 V,	V_O = 20 $V_{(PP)}$			30		MHz
		V_{CC} = ±5 V,	V_O = 4 $V_{(PP)}$			75		

(1) Slew rate is measured from an output level range of 25% to 75%.
(2) Full power bandwidth = slew rate/2πV_{peak}

ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = ±15 V, R_L = 50 Ω, R_F = 1 kΩ, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
Noise/Distortion Performance								
THD	Total harmonic distortion	V_{CC} = ±5 V, G = 2	f = 500 kHz	$V_{O(PP)}$ = 20 V		–69		dBc
				$V_{O(PP)}$ = 2 V		–80		
			f = 1 MHz	$V_{O(PP)}$ = 20 V		–66		
				$V_{O(PP)}$ = 2 V		–75		
		V_{CC} = ±5 V, $V_{O(PP)}$ = 2 V, G = 2	R_L = 25 Ω	f = 500 kHz		–71		
				f = 1 MHz		–65		
			R_L = 50 Ω	f = 500 kHz		–78		
				f = 1 MHz		–72		
I_n	Input noise current, positive (IN+)	V_{CC} = ±5 V or ±15 V	G = 2	f = 10 kHz		11.5		pA/√Hz
	Input noise current, negative (IN–)					16		
A_D	Differential gain error	R_L = 150 Ω, G = 2,	NTSC, 40 IRE Mod.	V_{CC} = ±5 V		0.03%		
				V_{CC} = ±15 V		0.04%		
φ_D	Differential phase error	R_L = 150 Ω, G = 2,	NTSC, 40 IRE Mod.	V_{CC} = ±5 V		0.08°		
				V_{CC} = ±15 V		0.06°		
	Crosstalk	V_I = 200 mV,	f = 1 MHz			–64		dB
V_n	Input voltage noise	V_{CC} = ±5 V or ±15 V,	f = 10 kHz,	G = 2, single-ended		1.7		nV/√Hz
DC Performance (3)								
V_{IO}	Input offset voltage	V_{CC} = ±5 V or ±15 V		T_A = 25°C		1	5	mV
				T_A = full range			7	
	Input offset voltage drift	V_{CC} = ±5 V or ±15 V,		T_A = full range			20	µV/°C
	Differential input offset voltage	V_{CC} = ±5 V or ±15 V		T_A = 25°C		0.5	4	mV
				T_A = full range			5	
	Differential input offset voltage drift	V_{CC} = ±5 V or ±15 V,		T_A = full range			10	µV/°C
I_{IB}	Input bias current, negative	V_{CC} = ±5 V or ±15 V		T_A = 25°C		1	9	µA
				T_A = full range			12	
	Input bias current, positive			T_A = 25°C		5	10	
				T_A = full range			12	
	Input bias current, differential			T_A = 25°C		1.5	8	
				T_A = full range			11	
	Open-loop transresistance	V_{CC} = ±5				1		MΩ
		V_{CC} = ±15 V				4		
Input Characteristics (3)								
V_{ICR}	Common-mode input voltage range	V_{CC} = ±5			±3.5	±3.6		V
		V_{CC} = ±15			±13.3	±13.4		
CMRR	Common-mode rejection ratio	V_{CC} = ±5 V or ±15 V, T_A = full range			62	73		dB
	Differential common-mode rejection ratio					100		
r_i	Input resistance,	+ input				1.5		MΩ
	Input resistance,	– input				15		Ω
C_i	Input capacitance					1.4		pF

(3) Full range is 0°C to 70°C for the THS6022C, and –40°C to 85°C for the THS6022I.

ELECTRICAL CHARACTERISTICS (continued)

V_{CC} = ±15 V, R_L = 50 Ω, R_F = 1 kΩ, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
Output Characteristics (4)								
V_O	Output voltage swing	single-ended	R_L = 50 Ω	V_{CC} = ±5	±3	±3.2		V
				V_{CC} = ±15	±12	±12.6		
		differential	R_L = 100 Ω	V_{CC} = ±5	±6	±6.6		
				V_{CC} = ±15	±24.6	±25.2		
I_O	Output current (5)	V_{CC} = ±5 V,	R_L = 5 Ω			250		mA
		V_{CC} = ±15,	R_L = 50 Ω		200	250		
I_{OS}	Short-circuit output current (6)					400		mA
R_O	Output resistance	Open-loop				13		Ω
Power Supply (4)								
V_{CC}	Power supply operating range	Split supply			±4.5		±16.5	V
		Single supply			9		33	
I_{CC}	Quiescent current (each driver)		V_{CC} = ±5	T_A = 25°C		6	8	mA
				T_A = full range			10	
			V_{CC} = ±15	T_A = 25°C		7.2	9	
				T_A = full range			11	
PSRR	Power-supply rejection ratio		V_{CC} = ±5	T_A = 25°C	–68	–76		dB
				T_A = full range	–65			
			V_{CC} = ±15	T_A = 25°C	–64	–75		dB
				T_A = full range	–62			

(4) Full range is 0°C to 70°C for the THS6022C, and –40°C to 85°C for the THS6022I.
(5) Slew rate is measured from an output level range of 25% to 75%.
(6) A heat sink is required to keep the junction temperature below absolute maximum when an output is heavily loaded or shorted. See the absolute maximum ratings and Thermal Information section.

PARAMETER MEASUREMENT INFORMATION

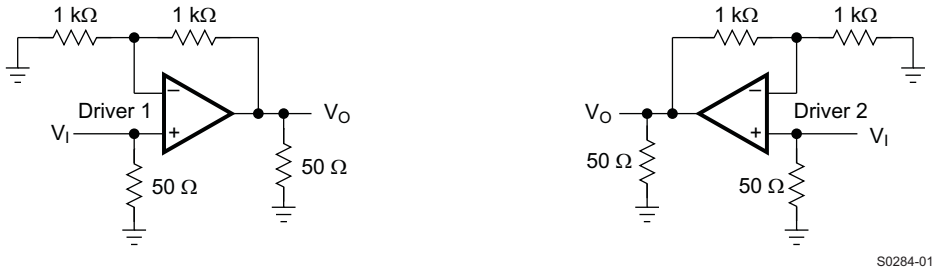


Figure 1. Input-to-Output Crosstalk Test Circuit

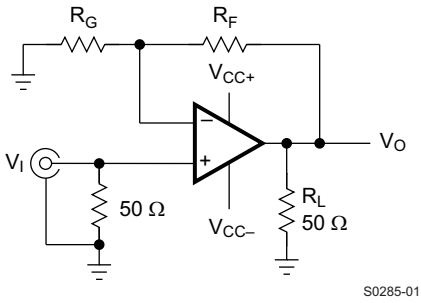


Figure 2. Test Circuit, Gain = 1 + (RF/RG)

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
$V_{O(PP)}$	Peak-to-peak output voltage	vs Load resistance	3
	Maximum peak-to-peak output voltage swing	vs Free-air temperature	4
V_{IO}	Input offset voltage	vs Free-air temperature	5
I_{IB}	Input bias current	vs Free-air temperature	6
	Positive input bias current	vs Common-mode input voltage	7
CMRR	Common-mode rejection ratio	vs Free-air temperature	8
	Input-to-output crosstalk	vs Frequency	9
PSRR	Power supply rejection ratio	vs Free-air temperature	10
	Closed-loop output impedance	vs Frequency	11
I_{CC}	Supply current	vs Free-air temperature	12
SF	Slew rate	vs Output step	13, 14
V_n	Input voltage noise	vs Frequency	15
I_n	Input current noise	vs Frequency	15
	Output amplitude	vs Frequency	16, 17, 19–32
	Closed-loop output phase	vs Frequency	18
	Small and large frequency response		33–36
	Single-ended output distortion	vs Peak-to-peak output voltage	37, 38
	Harmonic distortion	vs Frequency	39, 40
	Differential gain	Number of 150-Ω loads	41, 42
	Differential phase	Number of 150-Ω loads	43, 44
	400-mV output step response		45, 47
	20-V step response		46
	4-V step response		48

PEAK-TO-PEAK OUTPUT VOLTAGE vs LOAD RESISTANCE

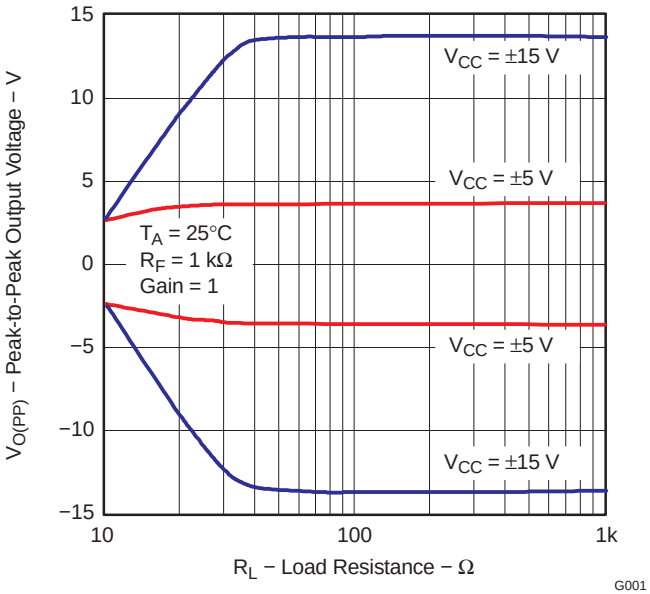


Figure 3.

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE SWING vs FREE-AIR TEMPERATURE

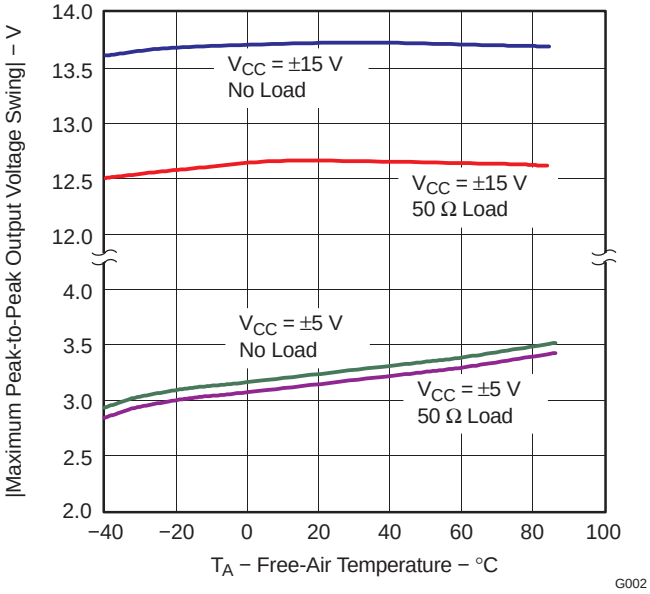


Figure 4.

INPUT OFFSET VOLTAGE vs FREE-AIR TEMPERATURE

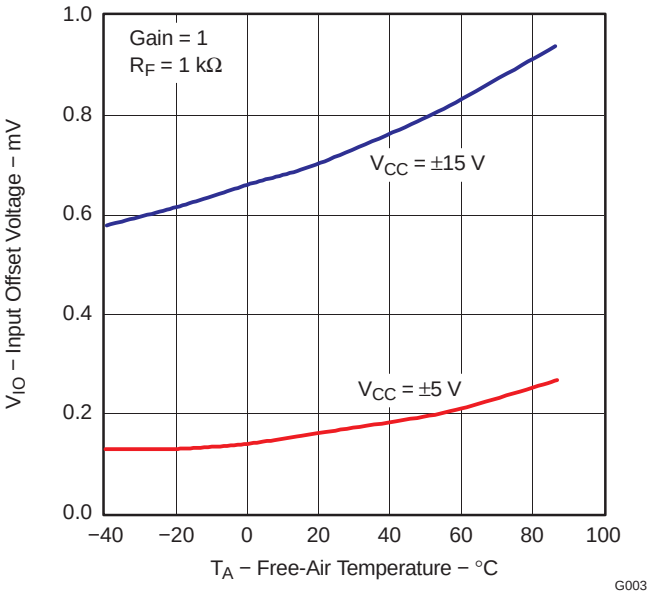


Figure 5.

INPUT BIAS CURRENT vs FREE-AIR TEMPERATURE

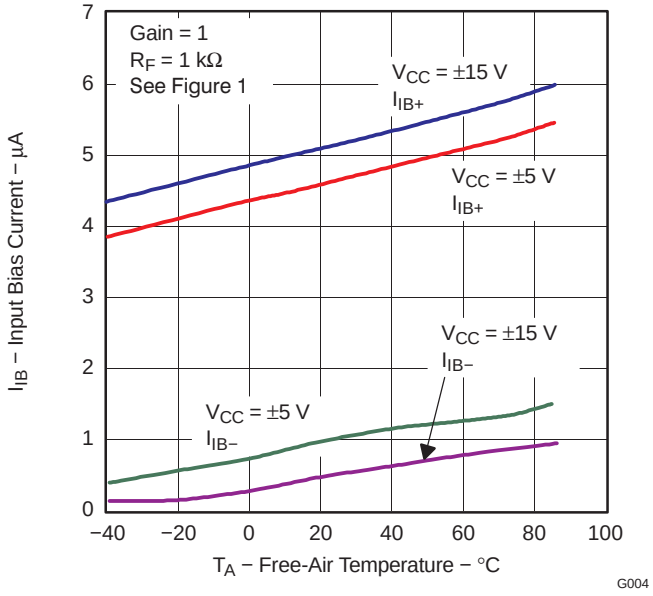


Figure 6.

POSITIVE INPUT BIAS CURRENT vs COMMON-MODE INPUT VOLTAGE

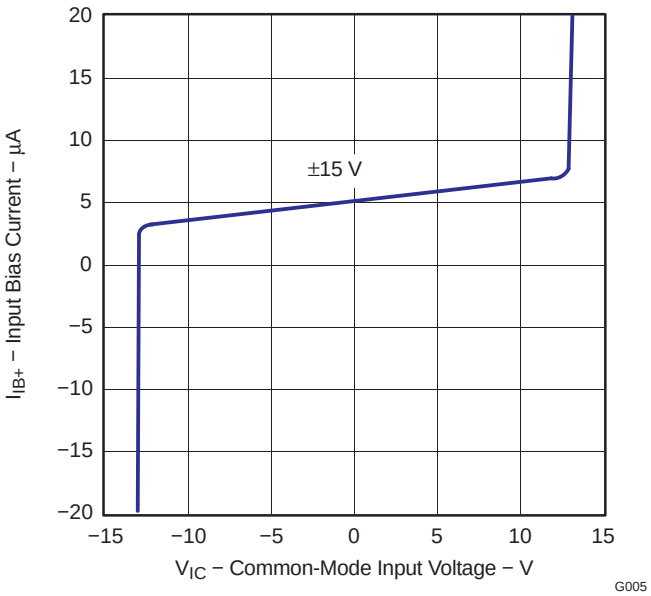


Figure 7.

COMMON-MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

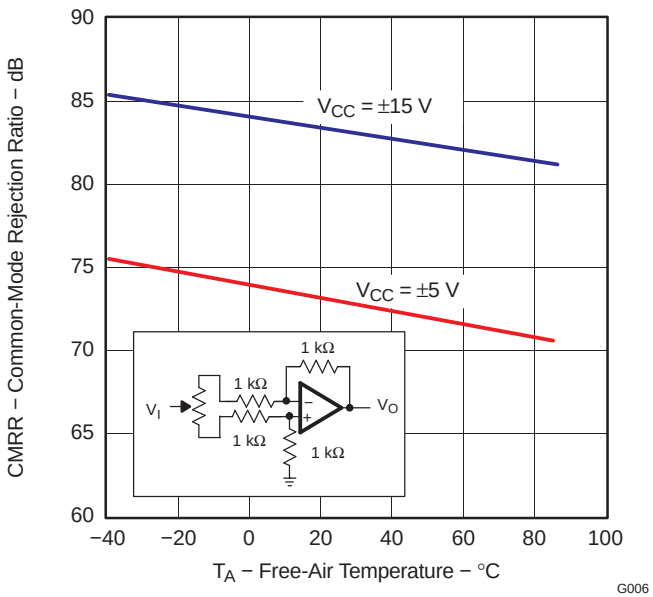


Figure 8.

INPUT-TO-OUTPUT CROSSTALK vs FREQUENCY

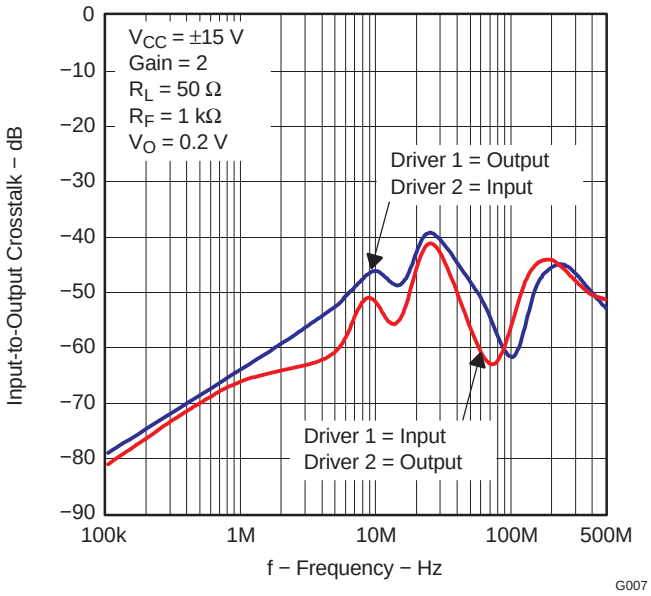


Figure 9.

POWER SUPPLY REJECTION RATIO vs FREE-AIR TEMPERATURE

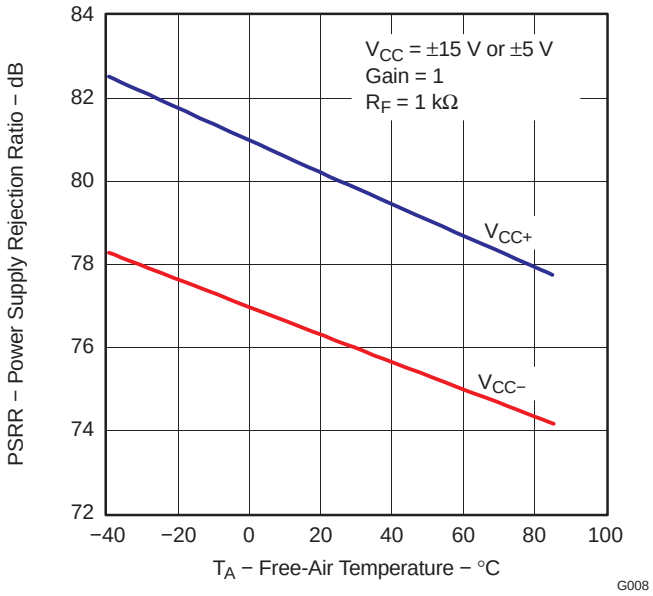


Figure 10.

CLOSED-LOOP OUTPUT IMPEDANCE vs FREQUENCY

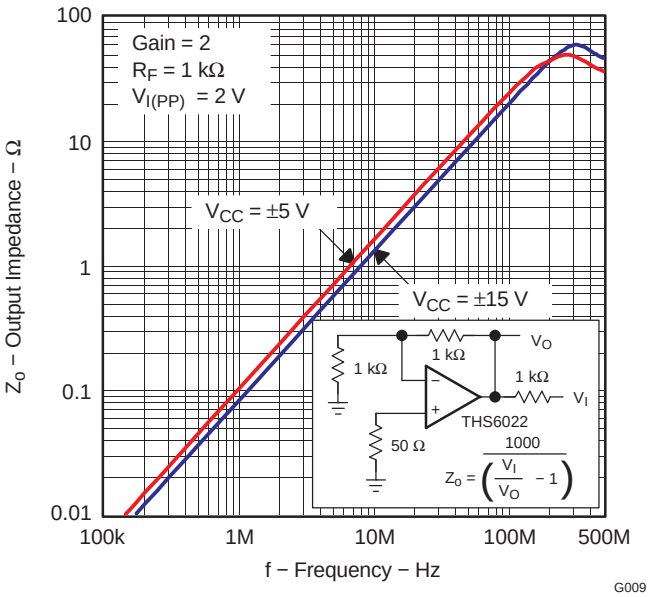


Figure 11.

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

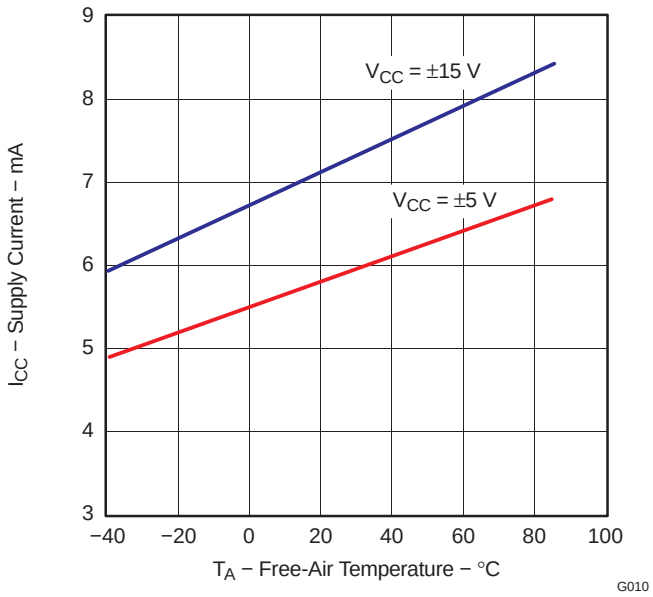


Figure 12.

SLEW RATE vs OUTPUT STEP

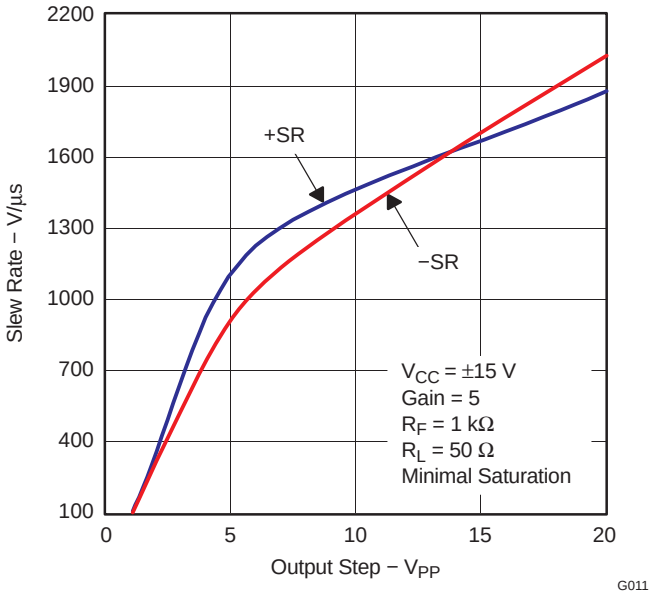


Figure 13.

SLEW RATE vs OUTPUT STEP

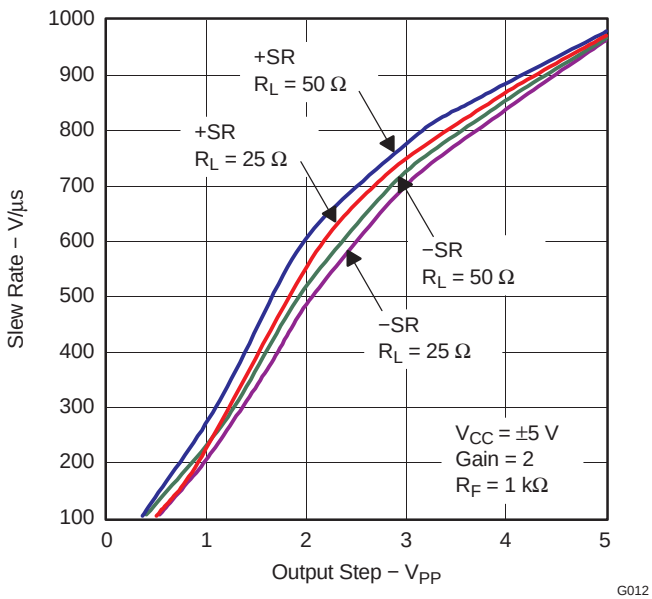


Figure 14.

INPUT VOLTAGE AND CURRENT NOISE vs FREQUENCY

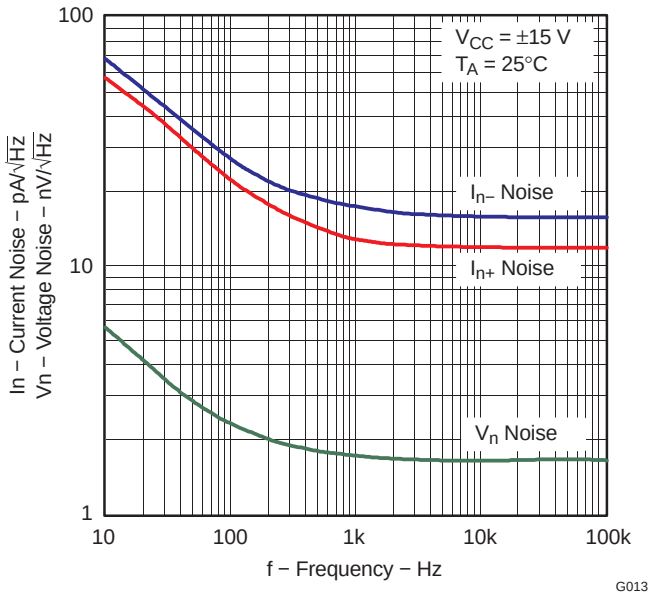


Figure 15.

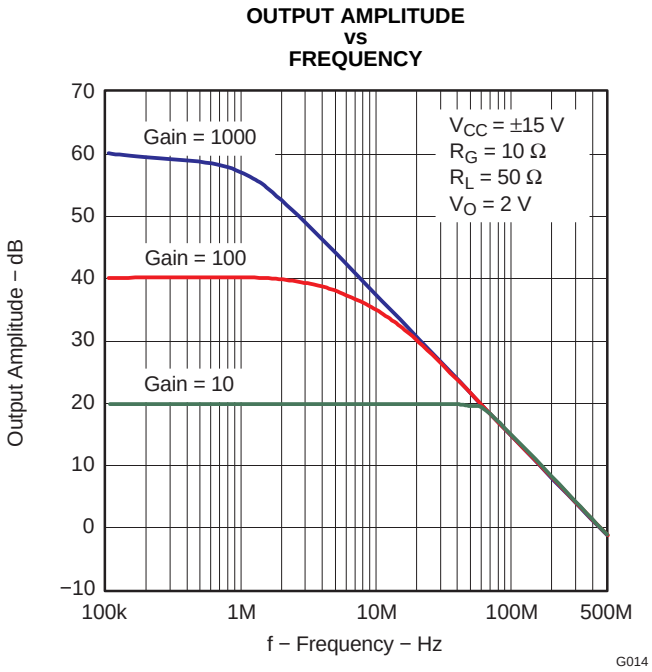


Figure 16.

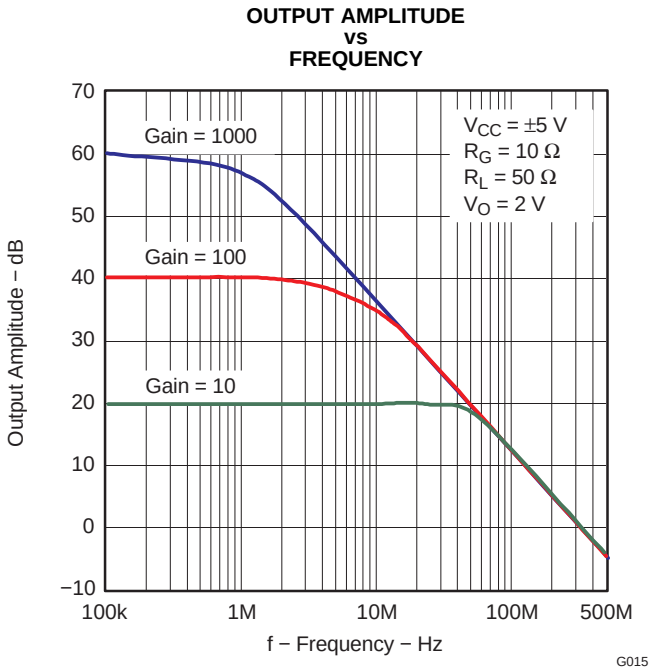


Figure 17.

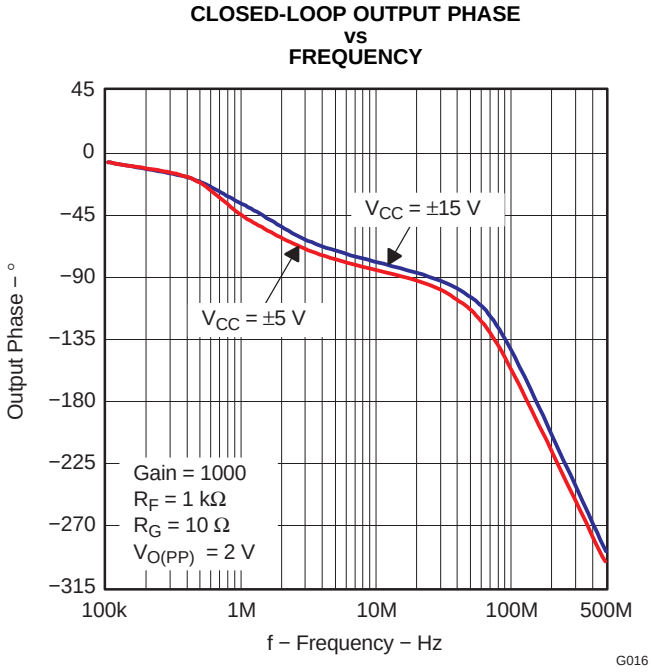


Figure 18.

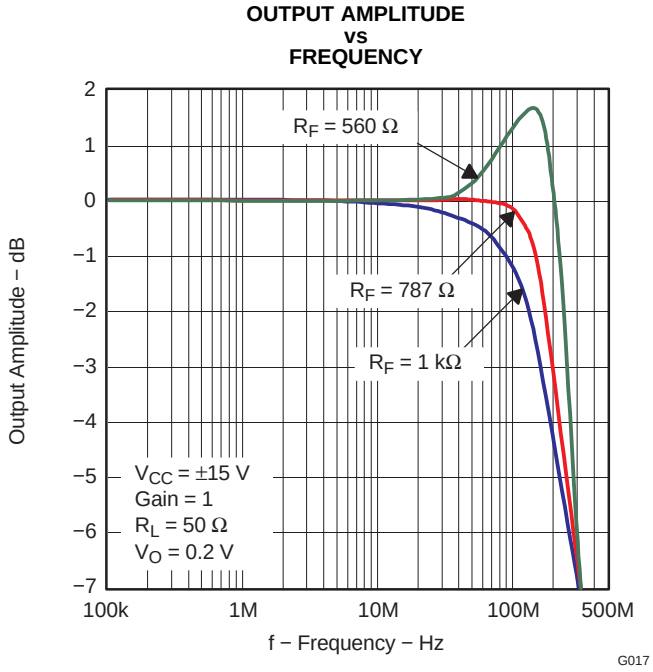


Figure 19.

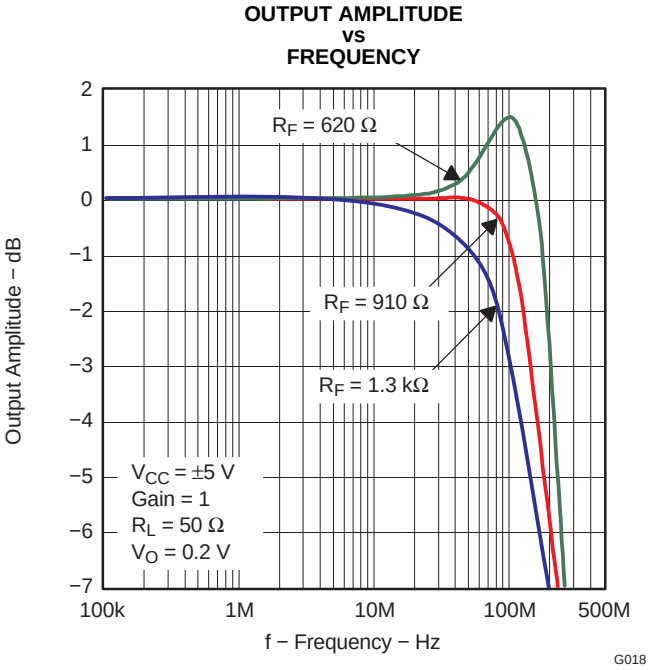


Figure 20.

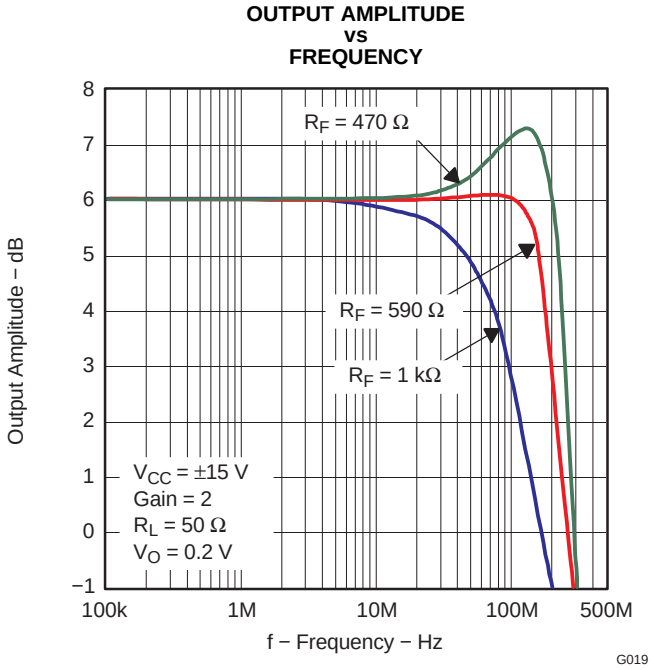
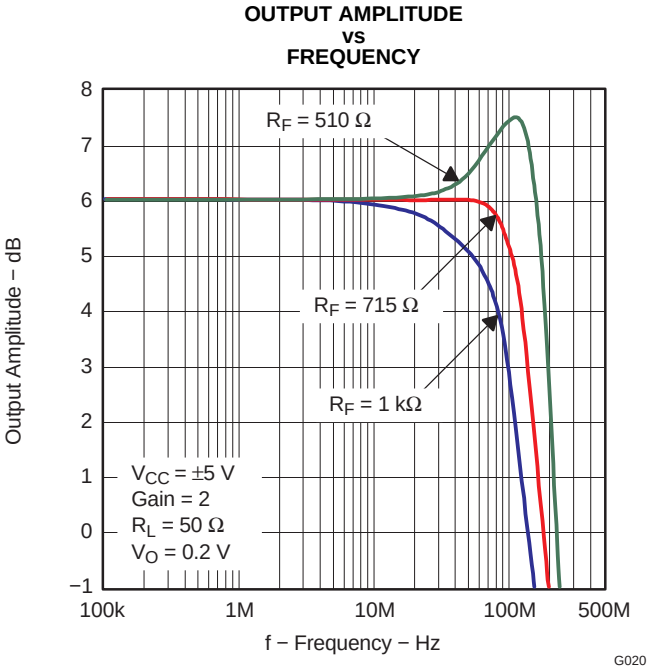


Figure 21.



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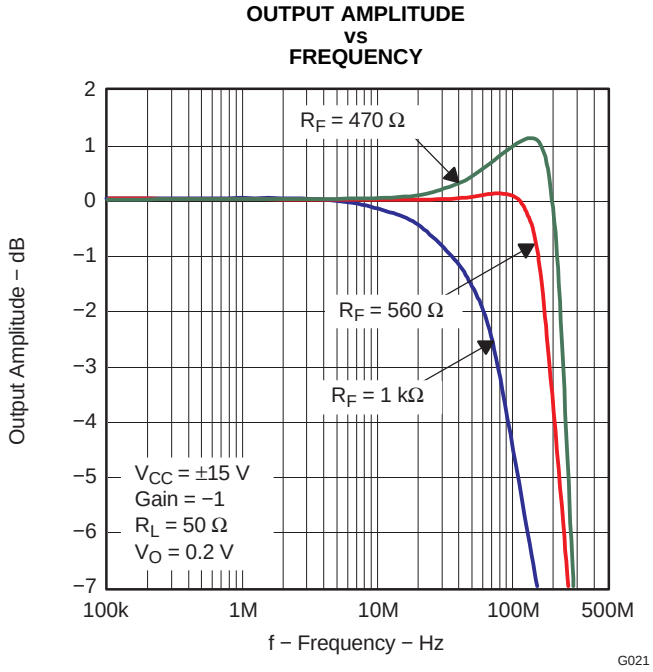

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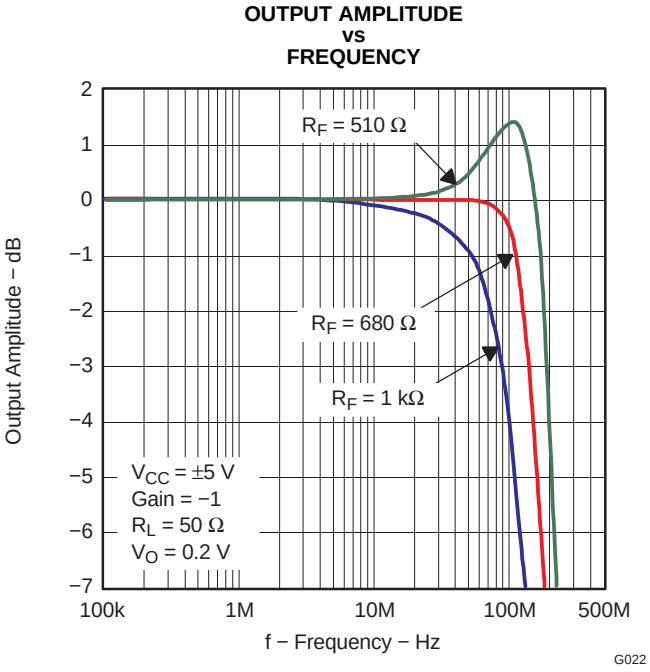

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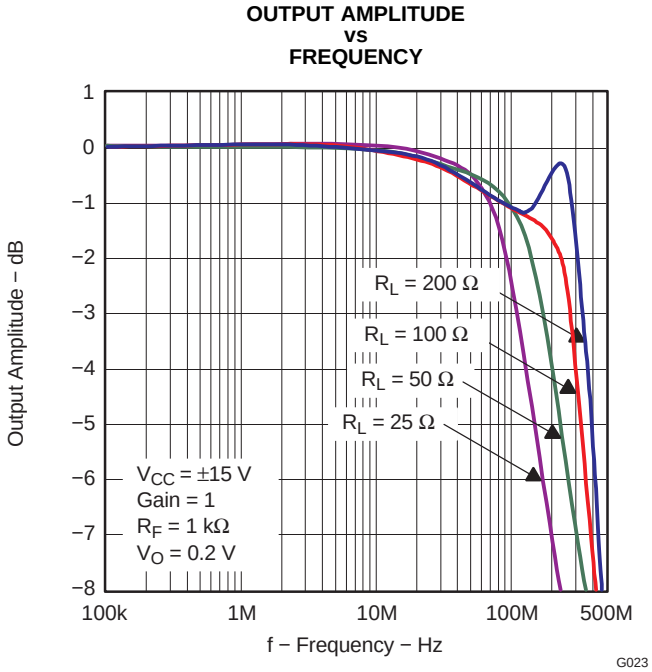

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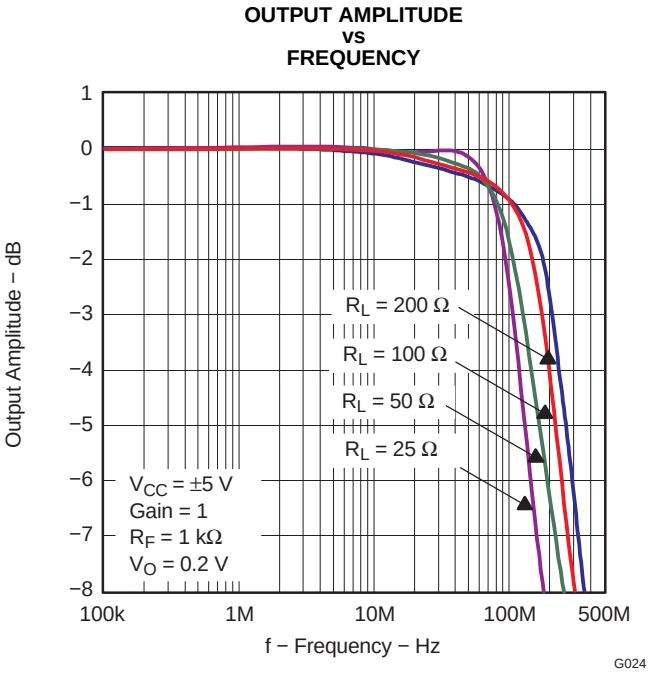

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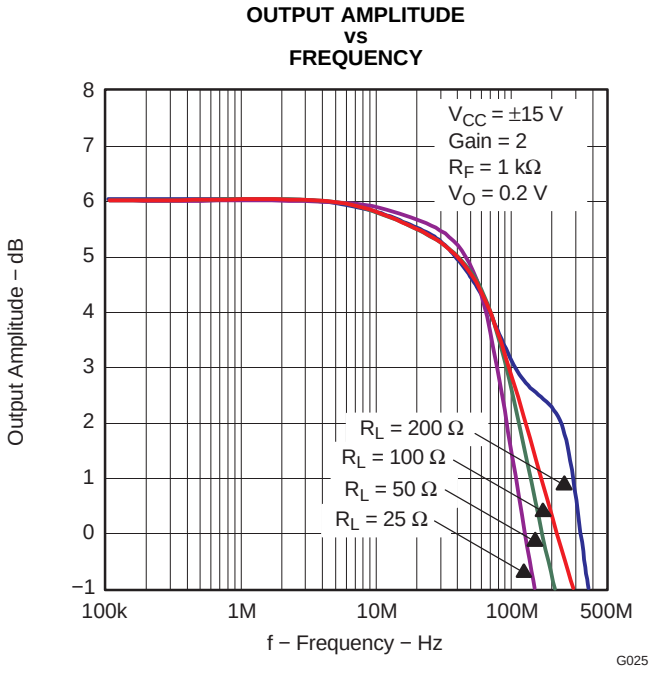

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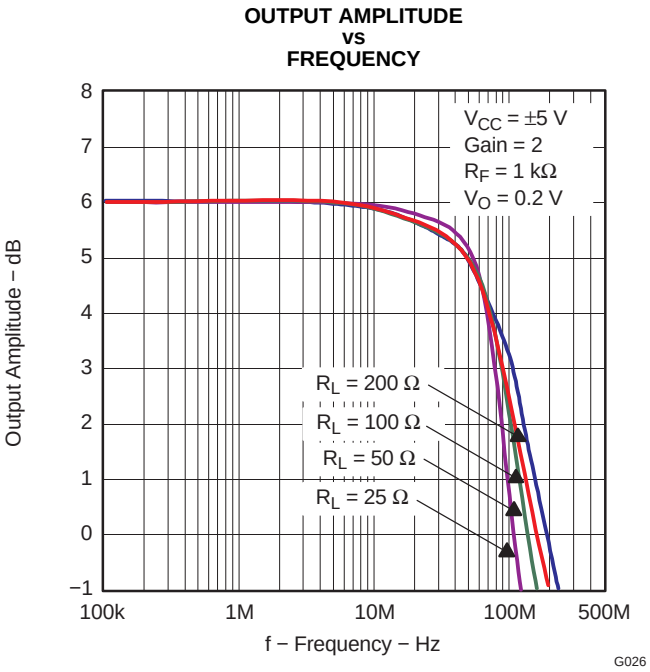

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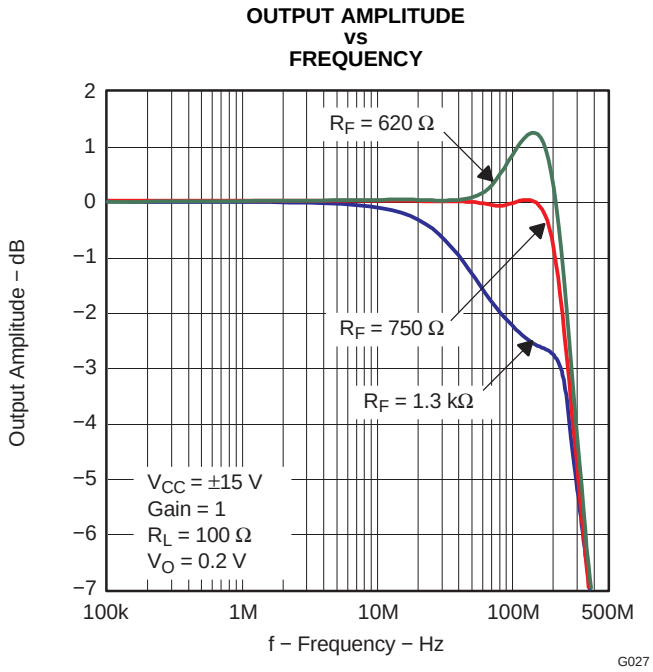

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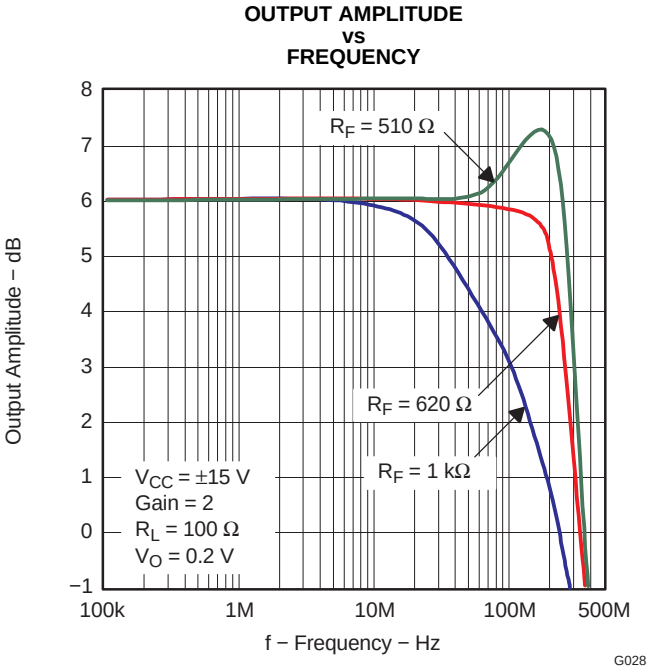

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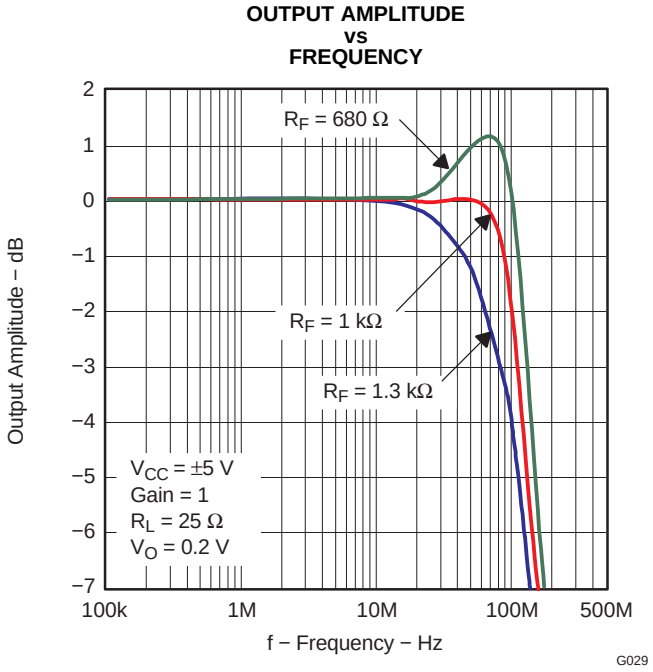

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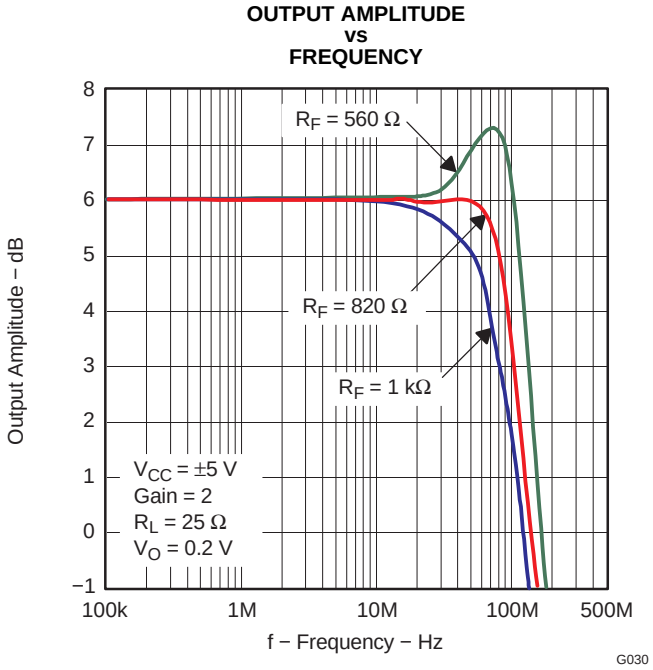

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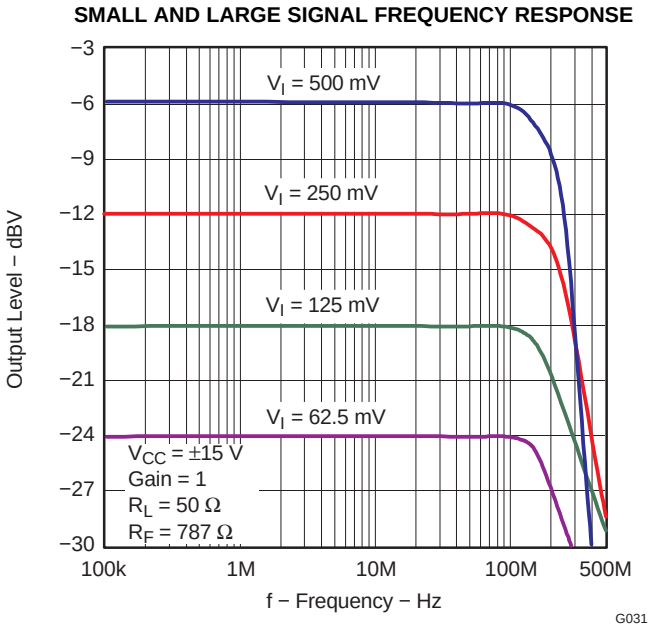

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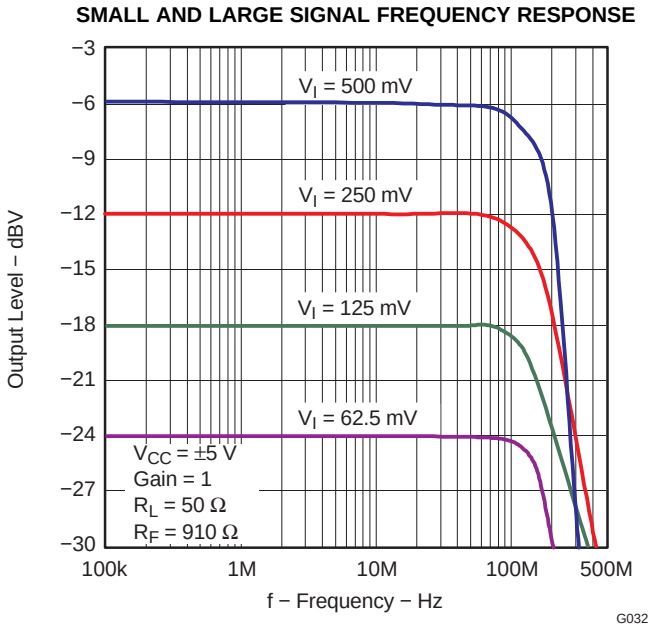


Figure 34.

SMALL AND LARGE SIGNAL FREQUENCY RESPONSE

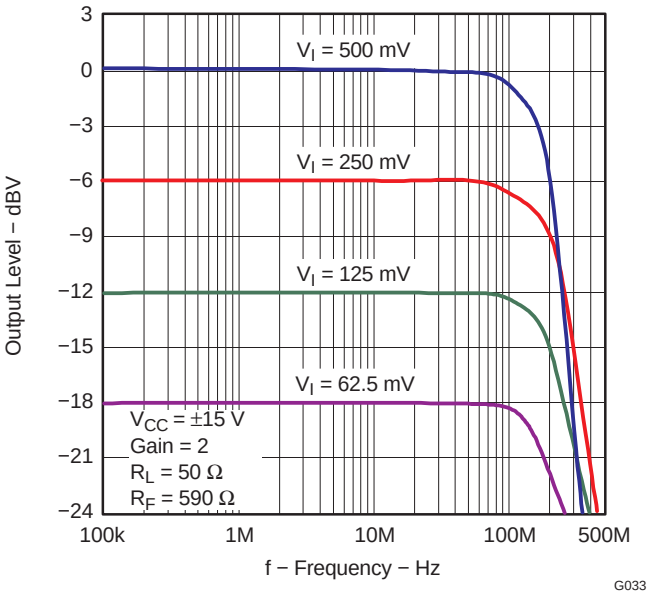


Figure 35.

SMALL AND LARGE SIGNAL FREQUENCY RESPONSE

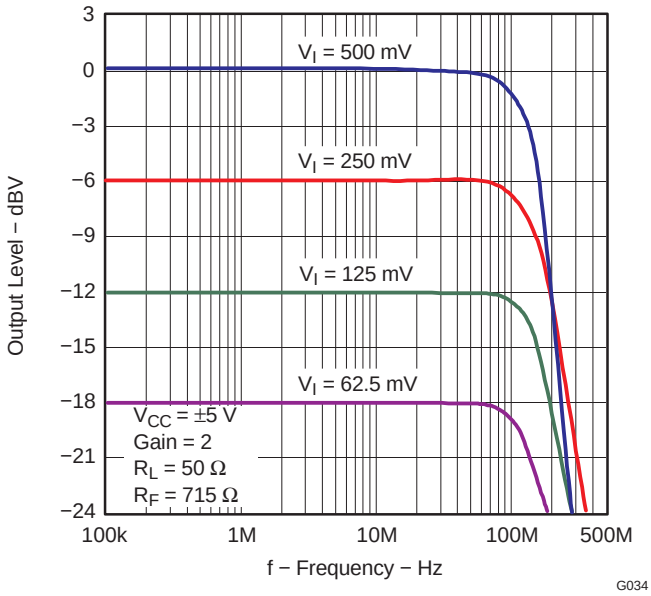


Figure 36.

SINGLE-ENDED OUTPUT DISTORTION
vs
PEAK-TO-PEAK OUTPUT VOLTAGE

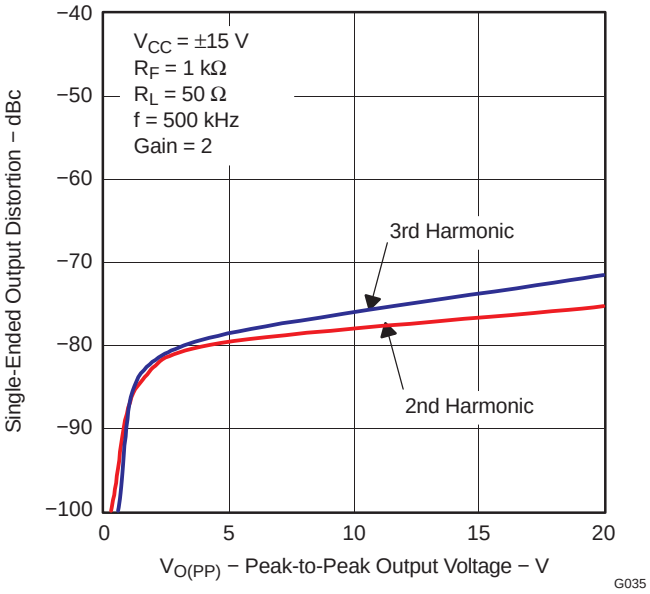
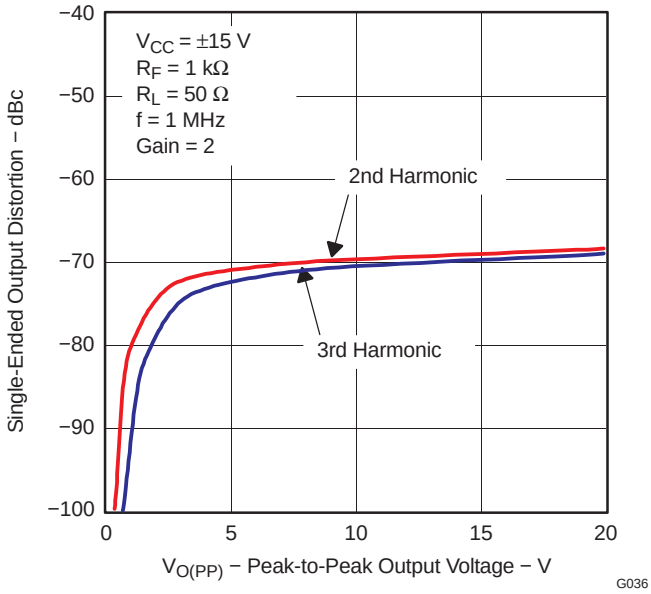


Figure 37.

SINGLE-ENDED OUTPUT DISTORTION
vs
PEAK-TO-PEAK OUTPUT VOLTAGE



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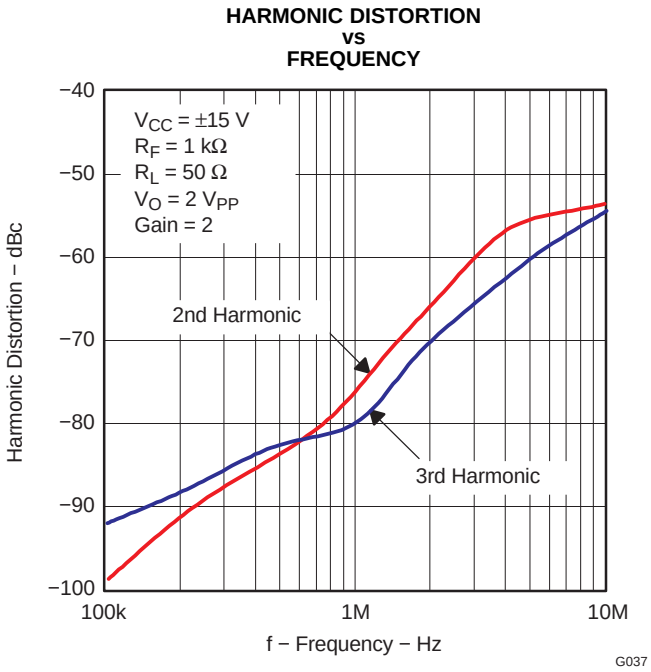

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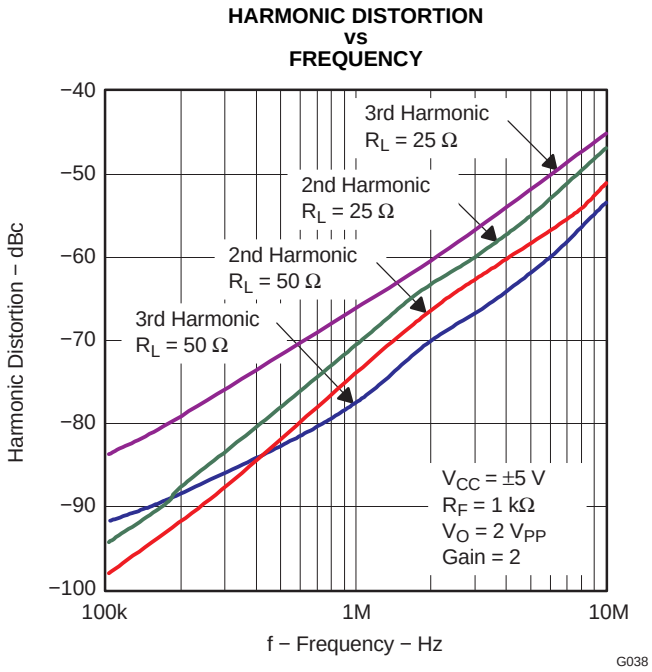
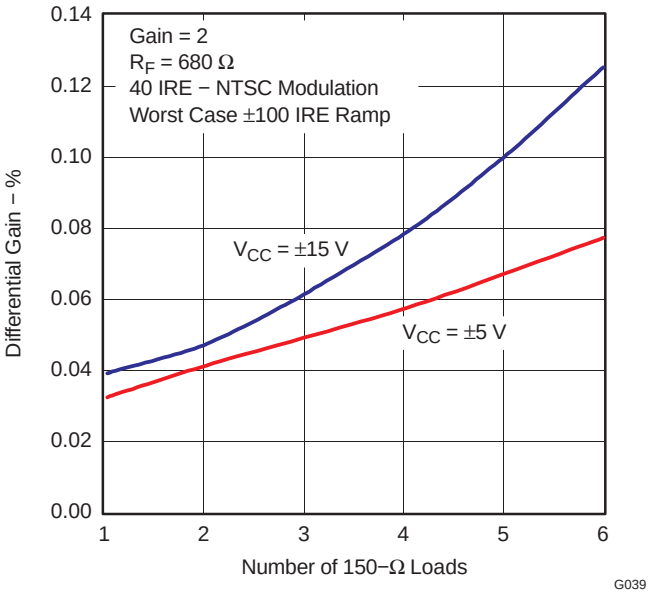


Figure 40.



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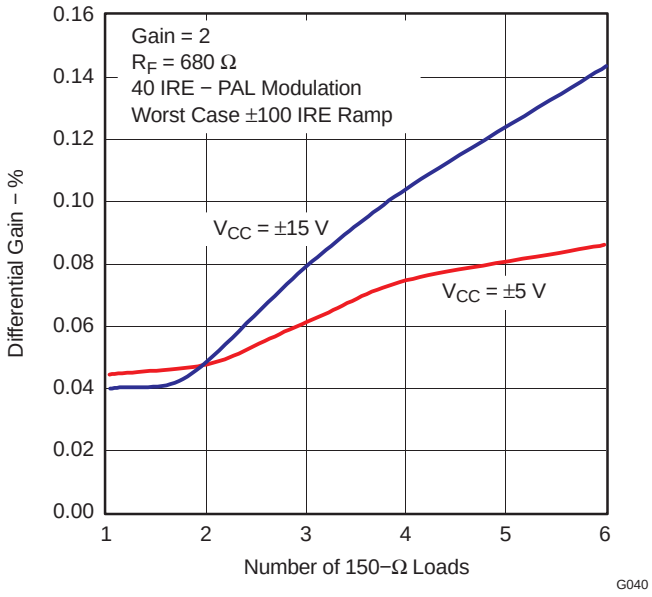


Figure 42.

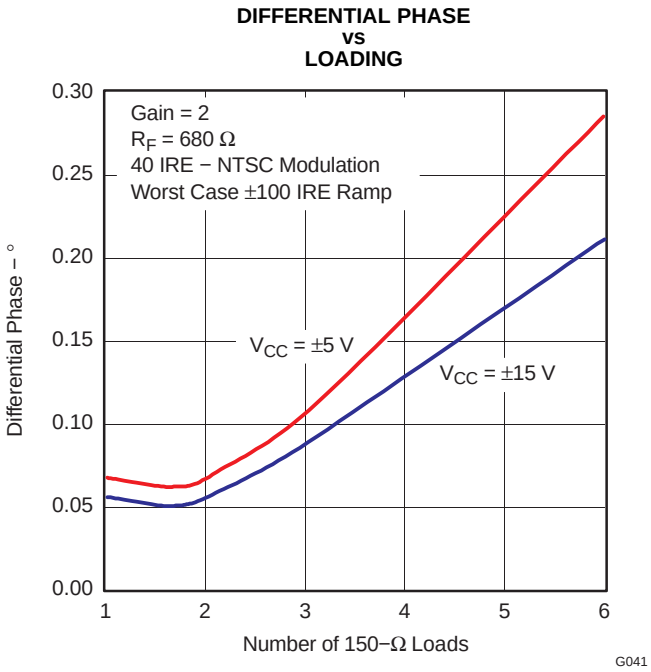
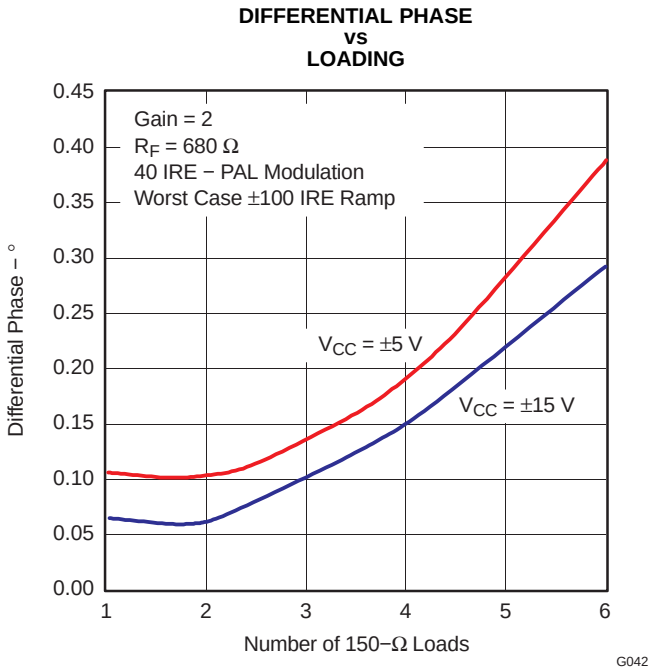


Figure 43.



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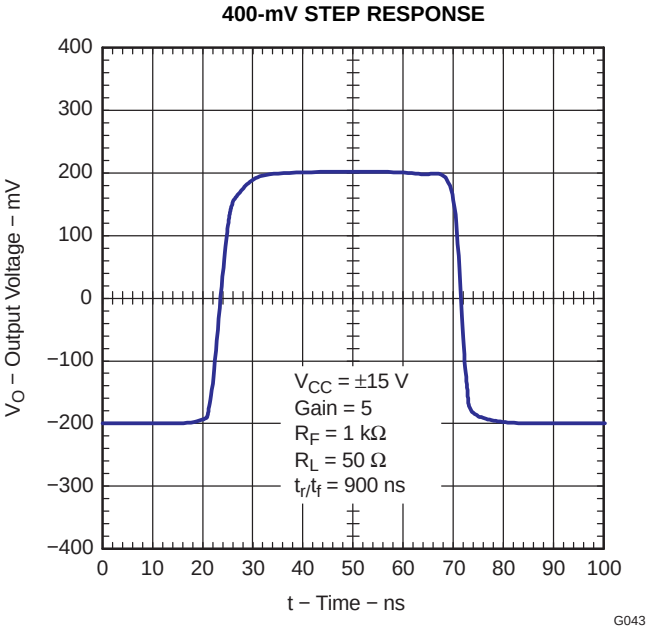

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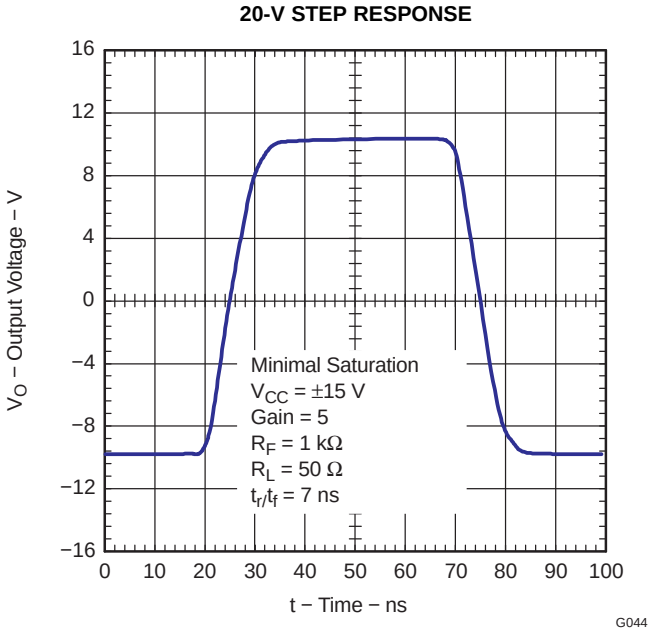

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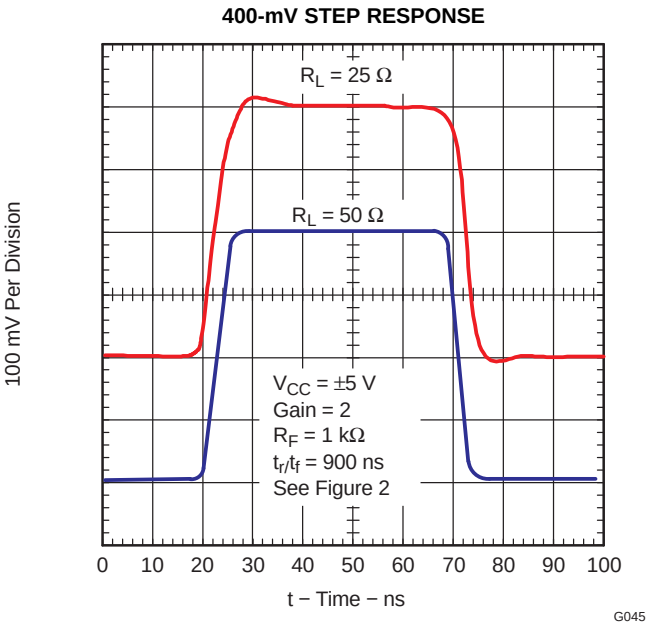


Figure 47.

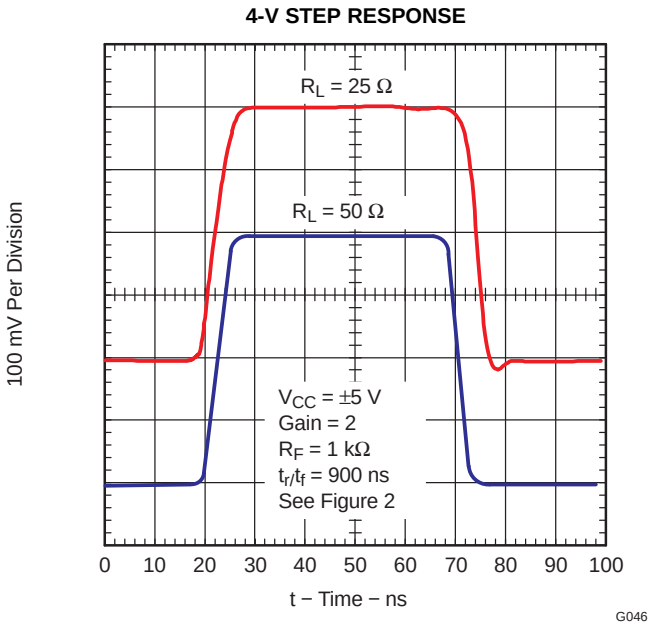
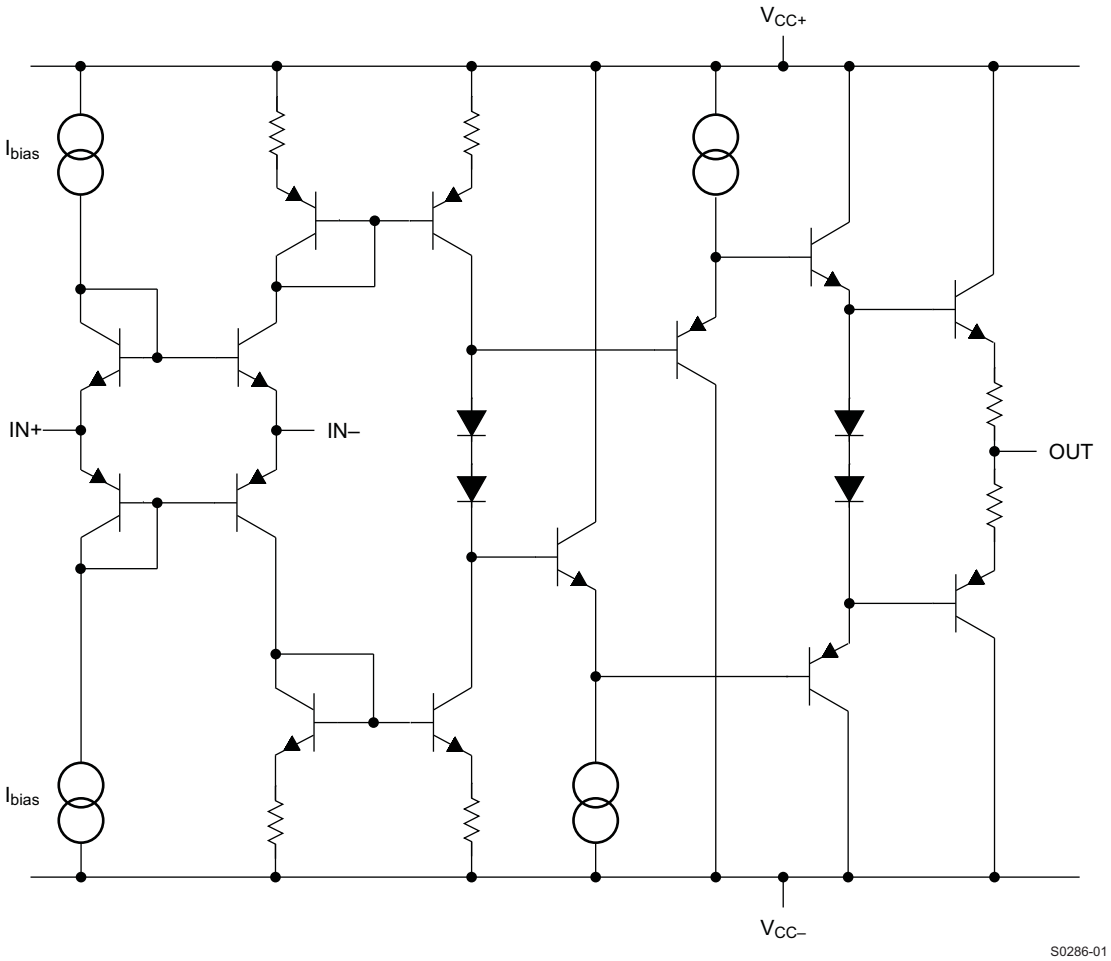


Figure 48.

APPLICATION INFORMATION

Simplified Schematic



The THS6022 contains two independent operational amplifiers. These amplifiers are current feedback topology amplifiers made for high-speed operation. They have been specifically designed to deliver the full power requirements of ADSL and therefore can deliver output currents of at least 200 mA at full output voltage.

The THS6022 is fabricated using Texas Instruments 30-V complementary bipolar process, HVBiCOM. This process provides excellent isolation and high slew rates that result in excellent crosstalk and extremely low distortion.

Independent Power Supplies

Each amplifier of the THS6022 has its own power supply pins. This was specifically done to solve a problem that often occurs when multiple devices in the same package share common power pins. This problem is crosstalk between the individual devices caused by currents flowing in common connections. Whenever the current required by one device flows through a common connection shared with another device, this current, in conjunction with the impedance in the shared line, produces an unwanted voltage on the power supply. Proper power-supply decoupling and good device power-supply rejection helps to reduce this unwanted signal. What is left is crosstalk.

However, with independent power-supply pins for each device, the effects of crosstalk through common impedance in the power supplies are more easily managed. This is because it is much easier to achieve low common impedance on the PCB with copper etch than it is to achieve low impedance within the package with either bond wires or metal traces on silicon.

APPLICATION INFORMATION (continued)

Power Supply Restrictions

Although the THS6022 is specified for operation from power supplies of ±5 V to ±15 V (or singled-ended power supply operation from 10 V to 30 V), and each amplifier has its own power supply pins, several precautions must be taken to assure proper operation.

- The power supplies for each amplifier must be the same value. For example, if the driver 1 uses ±15 volts, then the driver 2 must also use ±15 volts. Using ±15 volts for one amplifier and ±5 volts for another amplifier is not allowed.
- To save power by powering down one of the amplifiers in the package, the following rules must be followed.
  - The amplifier designated driver 1 must always receive power. This is because the internal startup circuitry uses the power from the driver 1 device.
  - The $-V_{CC}$ pins from both drivers must always be at the same potential.
  - Individual amplifiers are powered down by simply opening the V_{CC+} connection.

The THS6022 incorporates a standard class A-B output stage. This means that some of the quiescent current is directed to the load as the load current increases. So under heavy load conditions, accurate power dissipation calculations are best achieved through actual measurements. For small loads, however, internal power dissipation for each amplifier in the THS6022 can be approximated by the following formula:

$$P_D \cong \left(2\, V_{CC}\, I_{CC}\right) + \left(V_{CC} - V_O\right) \times \left(\frac{V_O}{R_L}\right)$$

where:

P_D = Power dissipation for one amplifier

V_{CC} = Split supply voltage

I_{CC} = Supply current for that particular amplifier

V_O = RMS output voltage of amplifier

R_L = Load resistance

To find the total THS6022 power dissipation, we simply sum up both amplifier power dissipation results. Generally, the worst-case power dissipation occurs when the output voltage is one-half the V_{CC} voltage. One last note, which is often overlooked: the feedback resistor (R_F) is also a load to the output of the amplifier and should be taken into account for low value feedback resistors.

Device Protection Features

The THS6022 has two built-in features that protect the device against improper operation. The first protection mechanism is output current limiting. Should the output become shorted to ground, the output current is automatically limited to the value given in the data sheet. While this protects the output against excessive current, the device internal power dissipation increases due to the high current and large voltage drop across the output transistors. Continuous output shorts are not recommended and could damage the device. Additionally, connection of the amplifier output to one of the supply rails ($\pm V_{CC}$) can cause failure of the device and is not recommended.

The second built-in protection feature is thermal shutdown. Should the internal junction temperature rise above approximately 180°C, the device automatically shuts down. Such a condition could exist with improper heat sinking or if the output is shorted to ground. When the abnormal condition is fixed, the internal thermal shutdown circuit automatically turns the device back on.

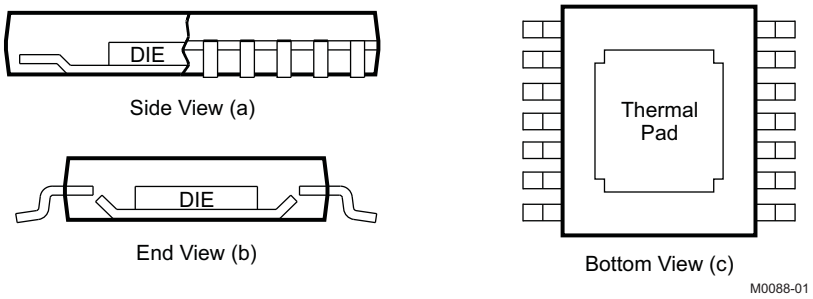
Thermal Information

The THS6022 is packaged in a thermally-enhanced PWP package, which is a member of the PowerPAD family of packages. This package is constructed using a downset leadframe upon which the die is mounted [see Figure 49(a) and Figure Figure 49(b)]. This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package [see Figure 49(c)]. Because this thermal pad has direct thermal contact with the die, excellent thermal performance can be achieved by providing a good thermal path away from the thermal pad.

APPLICATION INFORMATION (continued)

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad can also be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat dissipating device. This is discussed in more detail in the *PCB Design Considerations* section of this document.

The PowerPAD package represents a design breakthrough, combining the small area and ease of the surface mount assembly method to eliminate the previously difficult mechanical methods of heatsinking.



The thermal pad is electrically isolated from all terminals in the package.

Figure 49. Views of Thermally Enhanced PWP Package

Recommended Feedback and Gain Resistor Values

As with all current feedback amplifiers, the bandwidth of the THS6022 is an inversely proportional function of the value of the feedback resistor. This can be seen from Figure 19 through Figure 32. The recommended resistors for the optimum frequency response are shown in Table 1. These should be used as a starting point and once optimum values are found, 1% tolerance resistors should be used to maintain frequency response characteristics. Because there is a finite amount of output resistance of the operational amplifier, load resistance can play a major part in frequency response. This is especially true with these drivers, which tend to drive low-impedance loads. This can be seen in Figure 10 and Figure 25 through Figure 28. As the load resistance increases, the output resistance of the amplifier becomes less dominant at high frequencies. To compensate for this, the feedback resistor should change. For most applications, a feedback resistor value of 1 kΩ is recommended, which is a good compromise between bandwidth and phase margin that yields a very stable amplifier.

Table 1. Recommended Feedback (R_F) Values for Optimum Frequency Response

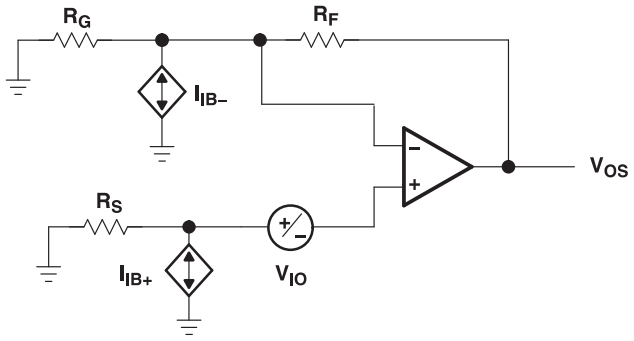
GAIN	V_{CC} = ±15 V		V_{CC} = ±15 V		
	R_L = 50 Ω	R_L = 100 Ω	R_L = 25 Ω	R_L = 50 Ω	R_L = 100 Ω
1	787 Ω	750 Ω	1 kΩ	910 Ω	820 Ω
2	590 Ω	590 Ω	820 Ω	715 Ω	680 Ω
–1	560 Ω	–	–	680 Ω	–

Consistent with current-feedback amplifiers, increasing the gain is best accomplished by changing the gain resistor, not the feedback resistor. This is because the bandwidth of the amplifier is dominated by the feedback resistor value and internal dominant-pole capacitor. The ability to control the amplifier gain independently of the bandwidth constitutes a major advantage of current-feedback amplifiers over conventional voltage feedback amplifiers. Therefore, once a frequency response is found suitable to a particular application, adjust the value of the gain resistor to increase or decrease the overall amplifier gain.

Finally, it is important to realize the effects of the feedback resistance on distortion. Increasing the resistance decreases the loop gain and increases the distortion. It is also important to know that decreasing load impedance increases total harmonic distortion (THD). Typically, the third-order harmonic distortion increases more than the second-order harmonic distortion. This is illustrated in Figure 40.

Offset Voltage

The output offset voltage, (V_{OO}) is the sum of the input offset voltage (V_{IO}) and both input bias currents (I_{IB}) times the corresponding gains. The following schematic and formula can be used to calculate the output offset voltage:



$$V_{OS} = \left(\pm V_{IO} \pm I_{IB+} R_S\right)\left(1 + \frac{R_F}{R_G}\right) \pm I_{IB-} R_F$$

Figure 50. Output Offset Voltage Model

Noise Calculations and Noise Figure

Noise can cause errors on very small signals. This is especially true for amplifying small signals. The noise model for current-feedback amplifiers (CFB) is the same as for voltage-feedback amplifiers (VFB). The only difference between the two is that the CFB amplifiers generally specify different current noise parameters for each input, whereas VFB amplifiers usually only specify one noise-current parameter. The noise model is shown in Figure 51. This model includes all of the noise sources as follows:

- e_n = Amplifier internal voltage noise (nV/$\sqrt{Hz}$)
- IN+ = Noninverting current noise (pA/$\sqrt{Hz}$)
- IN– = Inverting current noise (pA/$\sqrt{Hz}$)
- e_{Rx} = Thermal voltage noise associated with each resistor (e_{Rx} = 4 kTR$_x$)

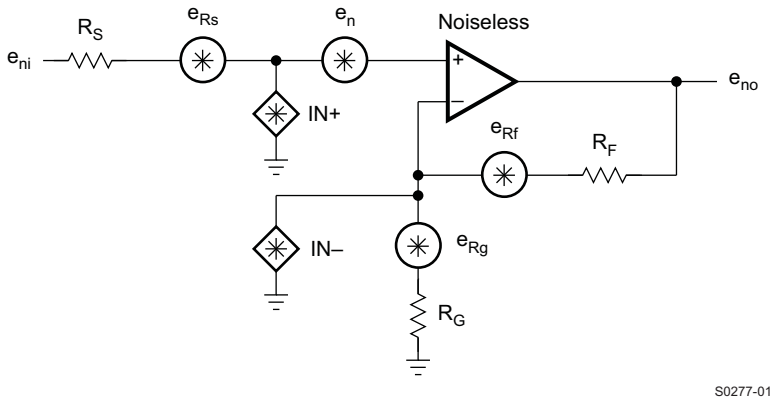


Figure 51. Noise Model

The total equivalent input noise density (e_{ni}) is calculated by using the following equation:

$$e_{ni} = \sqrt{(e_n)^2 + \left(IN+ \times R_S\right)^2 + \left(IN- \times \left(R_F \parallel R_G\right)\right)^2 + 4\,kTR_S + 4\,kT\left(R_F \parallel R_G\right)}$$

where:

k = Boltzmann's constant = 1.380658×10^{-23}

T = Temperature in degrees Kelvin (273 + °C)

$R_F \parallel R_G$ = Parallel resistance of R_F and R_G

To get the equivalent output noise of the amplifier, just multiply the equivalent input noise density (e_{ni}) by the overall amplifier gain (A_V).

$$e_{no} = e_{ni}\,A_V = e_{ni}\left(1 + \frac{R_F}{R_G}\right) \text{ (Noninverting Case)}$$

As the previous equations show, to keep noise at a minimum, small-value resistors should be used. As the closed-loop gain is increased (by reducing R_G), the input noise is reduced considerably because of the parallel resistance term. This leads to the general conclusion that the most dominant noise sources are the source resistor (R_S) and the internal amplifier noise voltage (e_n). Because noise is summed in a root-mean-squares method, noise sources smaller than 25% of the largest noise source can be effectively ignored. This can greatly simplify the formula and make noise calculations much easier to calculate.

This brings up another noise measurement usually preferred in RF applications, the noise figure (NF). Noise figure is a measure of noise degradation caused by the amplifier. The value of the source resistance must be defined and is typically 50 Ω in RF applications.

$$NF = 10\log\left[\frac{e_{ni}^2}{\left(e_{Rs}\right)^2}\right]$$

Because the dominant noise components are generally the source resistance and the internal amplifier noise voltage, we can approximate noise figure as:

$$NF = 10\log\left[1 + \frac{\left[\left(e_n\right)^2 + \left(IN+ \times R_S\right)^2\right]}{4\,kTR_S}\right]$$

Figure 52 shows the noise figure graph for the THS6022.

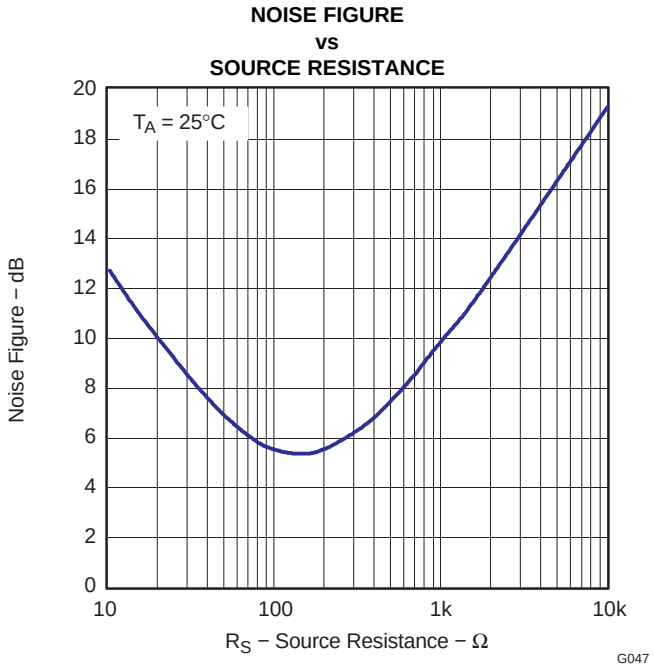


Figure 52. Noise Figure vs Source Resistance

Slew Rate

The slew rate performance of a current-feedback amplifier like the THS6022 is affected by many different factors. Some of these factors are external to the device, such as amplifier configuration and PCB parasitics, and others are internal to the device, such as available currents and node capacitance. Understanding some of these factors should help the PCB designer arrive at a more optimum circuit with fewer problems.

Whether the THS6022 is used in an inverting amplifier configuration or a noninverting configuration can impact the output slew rate. Slew rate performance in the inverting configuration is generally faster than the noninverting configuration. This is because in the inverting configuration, the input terminals of the amplifier are at a virtual ground and do not significantly change voltage as the input changes. Consequently, the time to charge any capacitance on these input nodes is less than for the noninverting configuration, where the input nodes actually do change in voltage an amount equal to the size of the input step. In addition, any PCB parasitic capacitance on the input nodes degrades the slew rate further simply because there is more capacitance to charge. If the supply voltage (V_{CC}) to the amplifier is reduced, slew rate decreases because there is less current available within the amplifier to charge the capacitance on the input nodes as well as other internal nodes. Also, as the load resistance decreases, the slew rate typically decreases due to the increasing internal currents, which slow down the transitions (see Figure 13 and Figure 14).

Internally, the THS6022 has other factors that impact the slew rate. The amplifier's behavior during the slew rate transition varies slightly depending upon the rise time of the input. This is because of the way the input stage handles faster and faster input edges. Slew rates (as measured at the amplifier output) of less than about 1300 V/µs are processed by the input stage in a very linear fashion. Consequently, the output waveform smoothly transitions between initial and final voltage levels. This is shown in Figure 53. For slew rates greater than 1300 V/µs, additional slew-enhancing transistors present in the input stage begin to turn on to support these faster signals. The result is an amplifier with extremely fast slew rate capabilities. Figure 54 shows waveforms for these faster slew rates. The additional aberrations present in the output waveform with these faster slewing input signals are due to the brief saturation of the internal current mirrors. This phenomenon, which typically lasts less than 20 ns, is considered normal operation and is not detrimental to the device in any way. If for any reason this type of response is not desired, then increasing the feedback resistor or slowing down the input signal slew rate reduces the effect.

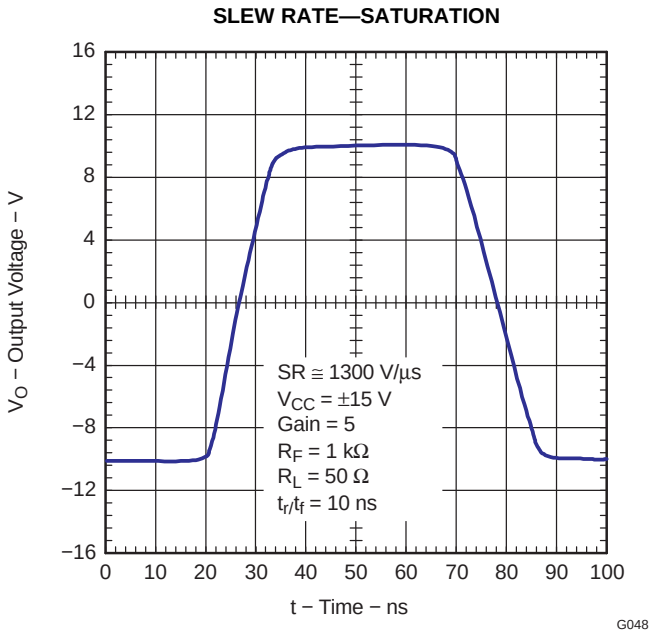


Figure 53.

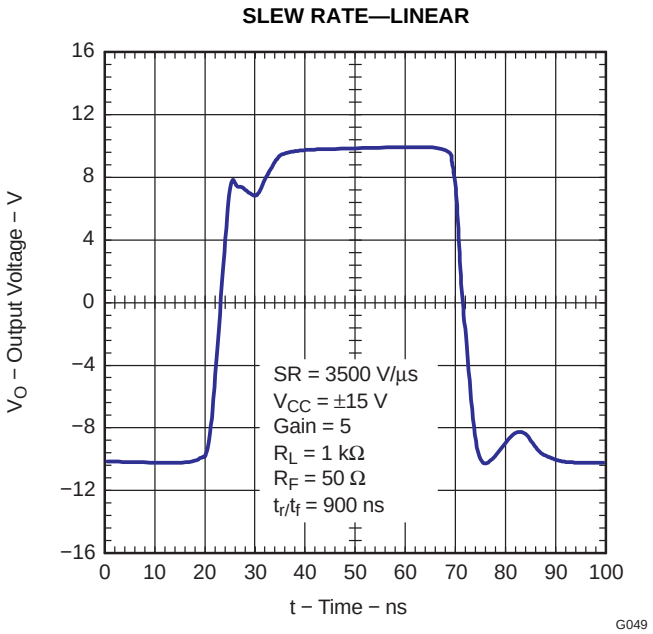


Figure 54.

Driving a Capacitive Load

Driving capacitive loads with high-performance amplifiers is not a problem as long as certain precautions are taken. The first is to realize that the THS6022 has been internally compensated to maximize its bandwidth and slew-rate performance. When the amplifier is compensated in this manner, capacitive loading directly on the output decreases the device phase margin, leading to high-frequency ringing or oscillations. Therefore, for capacitive loads of greater than 10 pF, it is recommended that a resistor be placed in series with the output of the amplifier, as shown in Figure 55. A minimum value of 15 Ω should work well for most applications. For example, in 75-Ω transmission systems, setting the series resistor value to 75 Ω both isolates any capacitance loading and provides the proper line impedance matching at the source end.

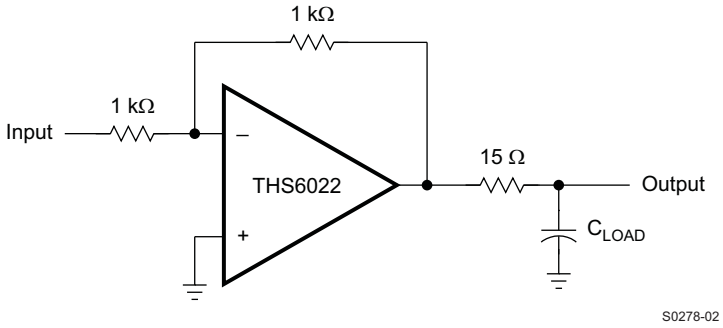


Figure 55. Driving a Capacitive Load

PCB Design Considerations

Proper PCB design techniques in two areas are important to assure proper operation of the THS6022. These areas are high-speed layout techniques and thermal-management techniques. Because the THS6022 is a high-speed part, the following guidelines are recommended.

- Ground plane—It is essential that a ground plane be used on the board to provide all components with a low-inductance ground connection. Although a ground connection directly to a terminal of the THS6022 is not necessarily required, it is recommended that the thermal pad of the package be tied to ground. This serves two functions. It provides a low-inductance ground to the device substrate to minimize internal crosstalk, and it provides the path for heat removal.
- Input stray capacitance—To minimize potential problems with amplifier oscillation, the capacitance at the inverting input of the amplifiers must be kept to a minimum. To do this, PCB trace runs to the inverting input must be as short as possible, the ground plane must be removed under any etch runs connected to the inverting input, and external components should be placed as close as possible to the inverting input. This is especially true in the noninverting configuration. An example of this can be seen in Figure 56, which shows what happens when a 1-pF capacitor is added to the inverting input terminal in the noninverting configuration. The bandwidth increases dramatically at the expense of peaking. This is because some of the error current is flowing through the stray capacitor instead of the inverting node of the amplifier. While the device is in the inverting mode, stray capacitance at the inverting input has a minimal effect. This is because the inverting node is at a virtual ground and the voltage does not fluctuate nearly as much as in the noninverting configuration. This can be seen in Figure 57, where a 27-pF capacitor adds only 0.5 dB of peaking. In general, as the gain of the system increases, the output peaking due to this capacitor decreases. While this can initially appear to be a faster and better system, overshoot and ringing are more likely to occur under fast transient conditions. So, proper analysis of adding a capacitor to the inverting input node should always be performed for stable operation.

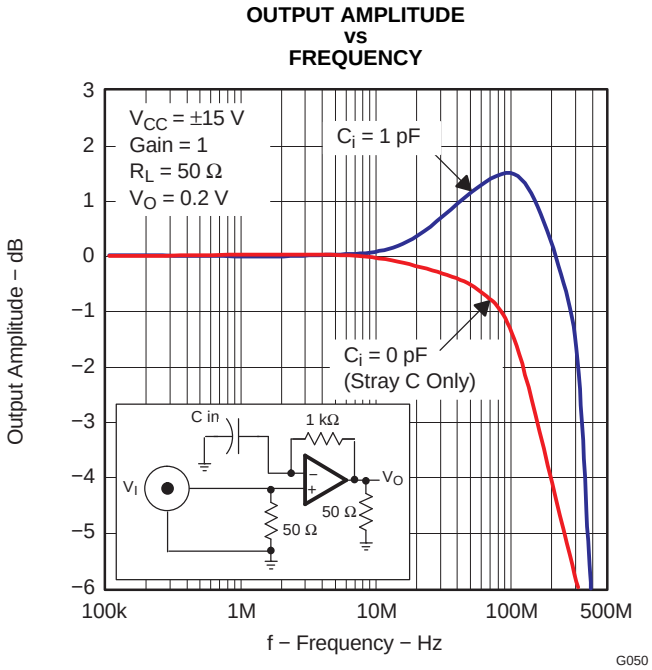


Figure 56.

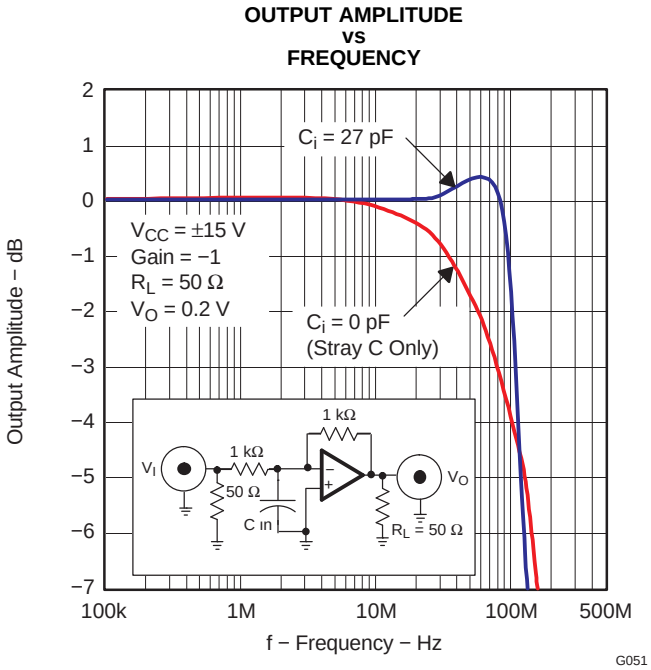


Figure 57.

- Proper power supply decoupling—Use a minimum of a 6.8-μF tantalum capacitor in parallel with a 0.1-μF ceramic capacitor on each supply terminal. It may be possible to share the tantalum among several amplifiers depending on the application, but a 0.1-μF ceramic capacitor should always be used on the supply terminal of every amplifier. In addition, the 0.1-μF capacitor should be placed as close as possible to the supply terminal. As this distance increases, the inductance in the connecting etch makes the capacitor less effective. The designer should strive for distances of less than 0.1 inch (2.55 mm) between the device power terminal and the ceramic capacitors.

Because of its power dissipation, proper thermal management of the THS6022 is required. Although there are many ways to properly heatsink this device, the following steps illustrate one recommended approach for a multilayer PCB with an internal ground plane. See Figure 58 for the following steps.

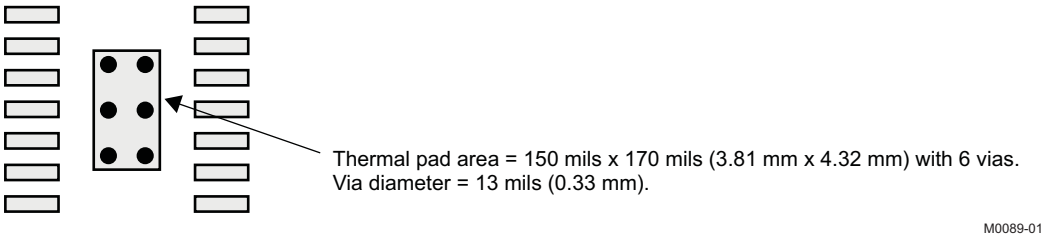


Figure 58. PowerPAD PCB Etch and Via Pattern Minimum Requirements

1. Place six holes in the area of the thermal pad. These holes should be 13 mils (0.33 mm) in diameter. They are kept small so that solder wicking through the holes is not a problem during reflow.
2. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area. This will help dissipate the heat generated from the THS6022. These additional vias may be larger than the 13-mil (0.33-mm) diameter vias directly under the thermal pad. They can be larger because they are not in the thermal-pad area to be soldered; therefore, wicking is generally not a problem.
3. Connect all holes to the internal ground plane.
4. When connecting these holes to the ground plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This makes the soldering of vias that have plane connections easier. However, in this application, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the THS6022 package should make their connection to the internal ground plane with a complete connection around the entire circumference of the plated-through hole.
5. The top-side solder mask should leave exposed the terminals of the package and the thermal pad area with its six holes. The bottom-side solder mask should cover the six holes of the thermal pad area. This prevents solder from being pulled away from the thermal pad area during the reflow process.
6. Apply solder paste to the exposed thermal pad area and all of the operational amplifier terminals.
7. With these preparatory steps in place, the THS6022 is simply placed in position and run through the solder reflow operation as any standard surface-mount component. This results in a part that is properly installed.

The actual thermal performance achieved with the THS6022 in its PowerPAD package depends on the application. In the example above, if the size of the internal ground plane is approximately 3 inches $\times$ 3 inches (7.62 mm $\times$ 7.62 mm), then the expected thermal coefficient, θ_{JA}, is about 37.5°C/W. For a given θ_{JA}, the maximum power dissipation is shown in Figure 60 and is calculated by the following formula:

$$P_D = \left(\frac{T_{MAX} - T_A}{\theta_{JA}} \right)$$

where:

P_D = Maximum power dissipation of THS6022 (watts)
T_{MAX} = Absolute maximum junction temperature (150°C)
T_A = Ambient free-air temperature (°C)
$\theta_{JA} = \theta_{JC} + \theta_{CA}$
θ_{JC} = Thermal coefficient from junction to case (2.07°C/W)
θ_{CA} = Thermal coefficient from case to ambient air

More-complete details of the thermal pad installation process and thermal management techniques can be found in the *PowerPAD Thermally Enhanced Package* application report (SLMA002).

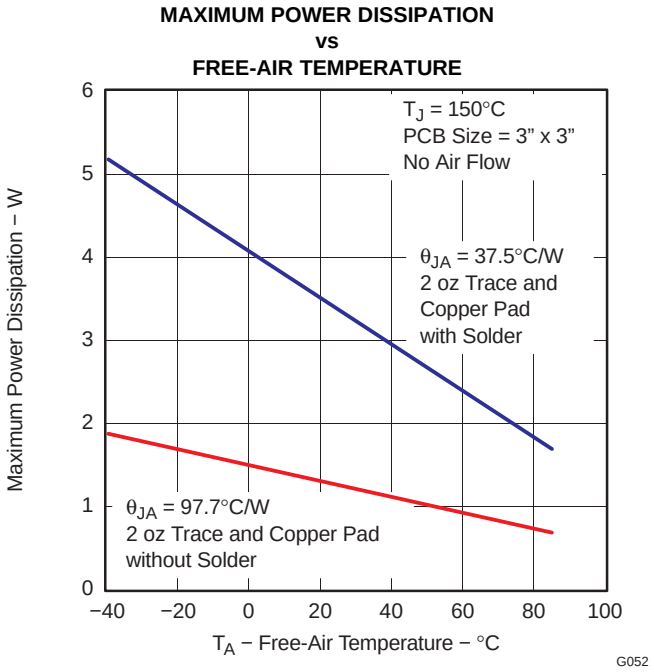


Figure 59.

ADSL

The THS6022 was primarily designed as a line driver and line receiver for ADSL (asymmetrical digital subscriber line). The driver output stage has been sized to provide full ADSL power levels of 13 dBm onto the telephone lines. Although actual driver output peak voltages and currents vary with each particular ADSL application, the THS6022 is specified for a minimum full output current of 200 mA at its full output voltage of approximately 12 V. This performance meets the demanding needs of ADSL at the client side end of the telephone line. A typical ADSL schematic is shown in Figure 60

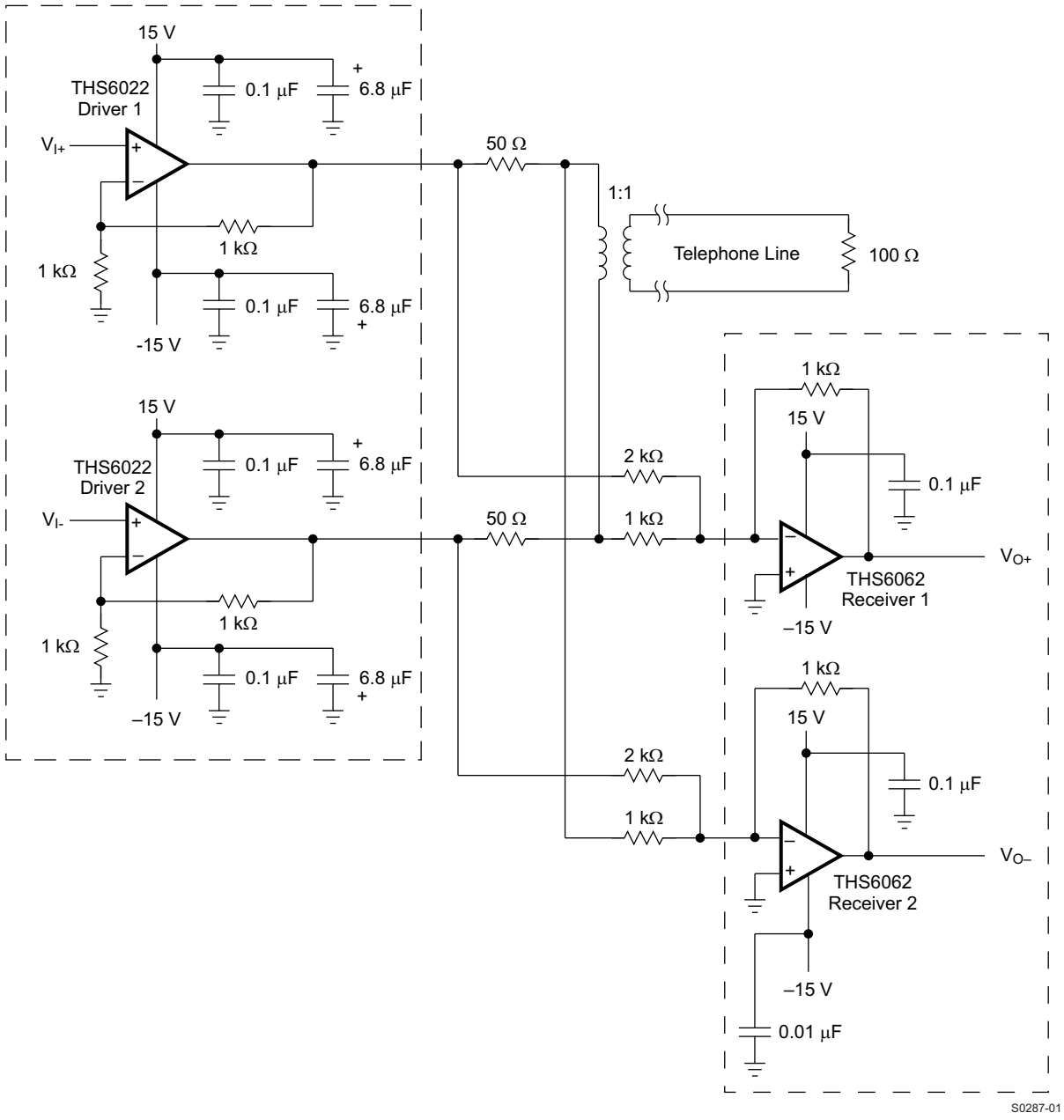


Figure 60. THS6022 ADSL Application

The ADSL transmit band consists of 255 separate carrier frequencies each with its own modulation and amplitude level. With such an implementation, it is imperative that signals put onto the telephone line have as low a distortion as possible. This is because any distortion either interferes directly with other ADSL carrier frequencies or it creates intermodulation products that interfere with ADSL carrier frequencies.

The THS6022 has been specifically designed for ultralow distortion by careful circuit implementation and by taking advantage of the superb characteristics of the complementary bipolar process. Driver single-ended distortion measurements are shown in Figure 37 through Figure 40. It is commonly known that in the differential driver configuration, the second-order harmonics tend to cancel out. Thus, the dominant total harmonic distortion (THD) is primarily due to the third-order harmonics. Additionally, distortion should be reduced as the feedback resistance drops. This is because the bandwidth of the amplifier increases, which allows the amplifier to react faster to any nonlinearities in the closed-loop system.

Another significant point is the fact that distortion decreases as the impedance load increases. This is because the output resistance of the amplifier becomes less significant as compared to the output load resistance. This is illustrated in Figure 40.

One problem that has been receiving a lot of attention in the ADSL area is power dissipation. One way to substantially reduce power dissipation is to lower the power supply voltages. This is because the RMS voltage of an ADSL remote terminal signal is 1.35-V RMS. But to meet ADSL requirements, the drivers must have a voltage RMS-to-peak crest factor of 5.6 in order to keep the bit-error probability rate below 10^{-7}. Hence, the power supply voltages must be high enough to accomplish the peak output voltage of 1.35 V $\times$ 5.6 = 7.6 V(PEAK). If ±15-V power supplies are used for the THS6022 drivers in the circuit shown in Figure 61, the power dissipation of the THS6022 is approximately 600 mW. This is assuming that part of the quiescent current is diverted back to the load, which typically happens in a class-AB amplifier. But if the power supplies are dropped down to ±12 V, then the power dissipation drops to approximately 460 mW. This is a 23% reduction of power, which ultimately lowers the temperature of the drivers and increases efficiency.

Another way to reduce power dissipation in the drivers is to increase the transformer ratio. The drawback in doing this is that it increases the loading on the drivers and reduces the signals being received from the central office. If this can be overcome, then a power reduction in the drivers results. By going to a 1:2 transformer ratio, the power supply voltages can drop to ±6 V. The driver output voltage has now been reduced to 675 mV RMS. But the loading on the output of the drivers drops to 25 Ω. The power dissipated is now approximately 360 mW, a reduction of 22% over the previous example. But, the received signal is now 1/2 of the previous example. This must be dealt with by requiring low-noise receivers. There are always trade offs when it comes to dealing with power, so proper analysis of the system should always be considered.

General Configurations

A common error for the first-time CFB user is to create a unity-gain buffer amplifier by shorting the output directly to the inverting input. A CFB amplifier in this configuration oscillates and is not recommended. The THS6022, like all CFB amplifiers, must have a feedback resistor for stable operation. Additionally, placing capacitors directly from the output to the inverting input is not recommended. This is because, at high frequencies, a capacitor has a very low impedance. This results in an unstable amplifier and should not be considered when using a current-feedback amplifier. Because of this, integrators and simple low-pass filters, which are easily implemented on a VFB amplifier, must be designed slightly differently. If filtering is required, simply place an RC-filter at the noninverting terminal of the operational-amplifier (see Figure 62).

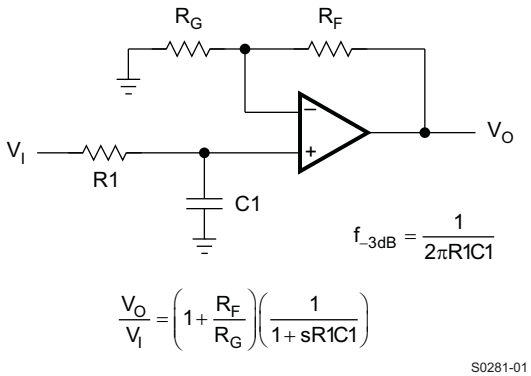


Figure 61. Single-Pole Low-Pass Filter

If a multiple-pole filter is required, the use of a Sallen-Key filter can work very well with CFB amplifiers. This is because the filtering elements are not in the negative feedback loop and stability is not compromised. Because of their high slew-rates and high bandwidths, CFB amplifiers can create very accurate signals and help minimize distortion. An example is shown in Figure 63

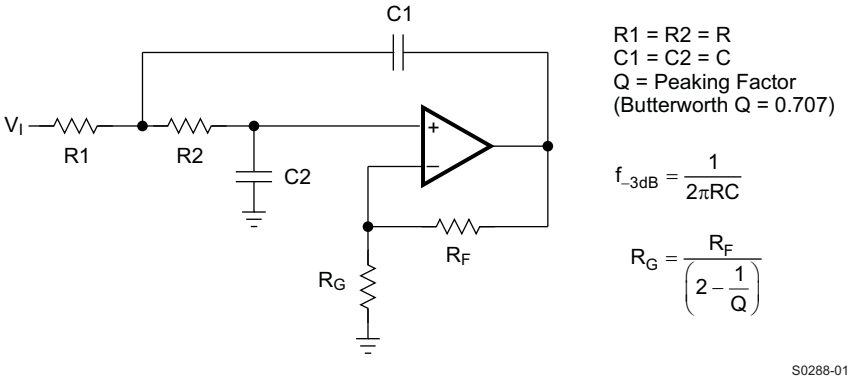


Figure 62. Two-Pole Low-Pass Sallen-Key Filter

There are two simple ways to create an integrator with a CFB amplifier. The first one, shown in Figure 64, adds a resistor in series with the capacitor. This is acceptable because at high frequencies, the resistor is dominant and the feedback impedance never drops below the resistor value. The second one, shown in Figure 65, uses positive feedback to create the integration. Caution is advised because oscillations can occur because of the positive feedback.

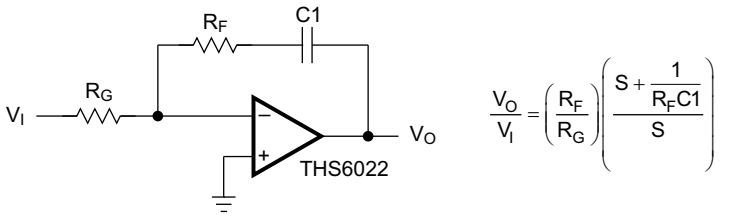


Figure 63. Inverting CFB Integrator

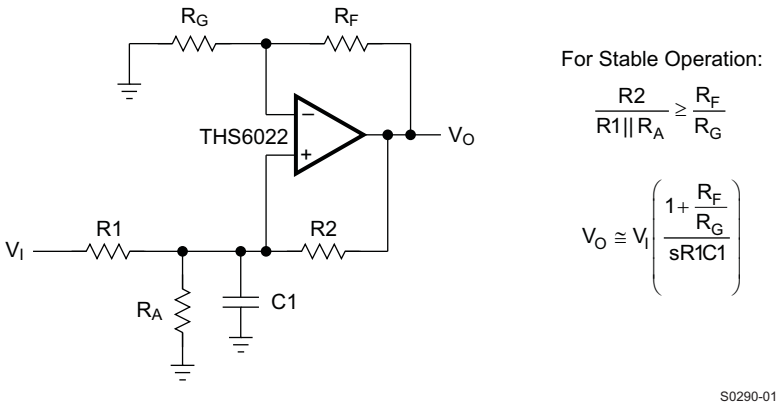


Figure 64. Noninverting CFB Integrator

Another good use for the THS6022 amplifiers is as very good video distribution amplifiers. One characteristic of distribution amplifiers is the fact that the differential phase (DP) and the differential gain (DG) are compromised as the number of lines increases and the closed-loop gain increases. Be sure to use termination resistors throughout the distribution system to minimize reflections and capacitive loading.

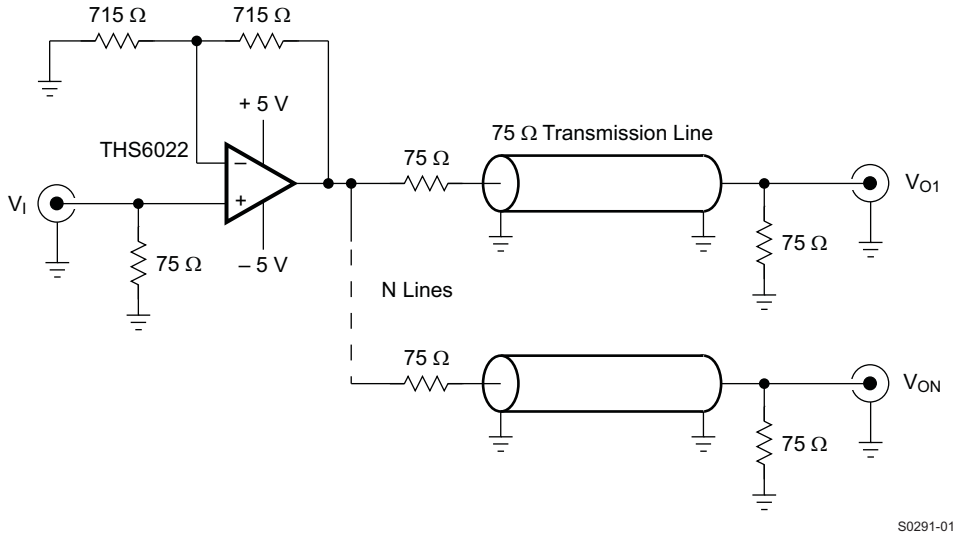


Figure 65. Video Distribution Amplifier Application

Evaluation Board

An evaluation board is available for the THS6022 (literature number SLOP133). This board has been configured for proper thermal management of the THS6022. The circuitry has been designed for a typical ADSL application as shown previously in this document. For more detailed information, see the *THS6022 250-mA Dual Differential Drivers Evaluation Module* user's guide (SLOV035). To order the evaluation board, contact your local TI sales office or distributor.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS6022CPWP	ACTIVE	HTSSOP	PWP	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	HS6022C	Samples
THS6022CPWPR	ACTIVE	HTSSOP	PWP	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	HS6022C	Samples
THS6022IPWP	ACTIVE	HTSSOP	PWP	14	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	HS6022I	Samples
THS6022IPWPR	ACTIVE	HTSSOP	PWP	14	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR		HS6022I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

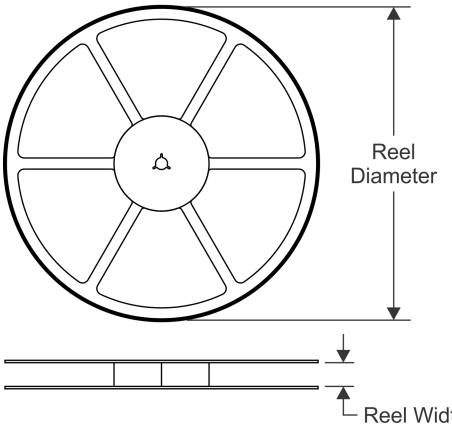
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

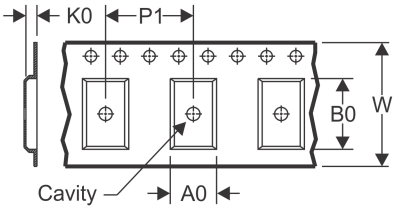
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

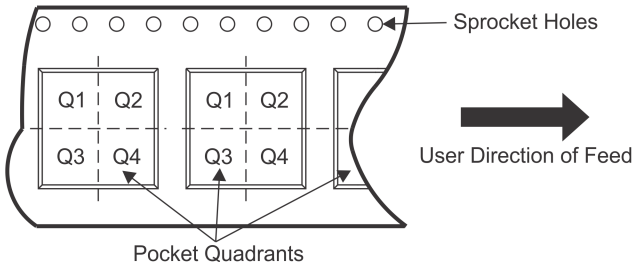


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

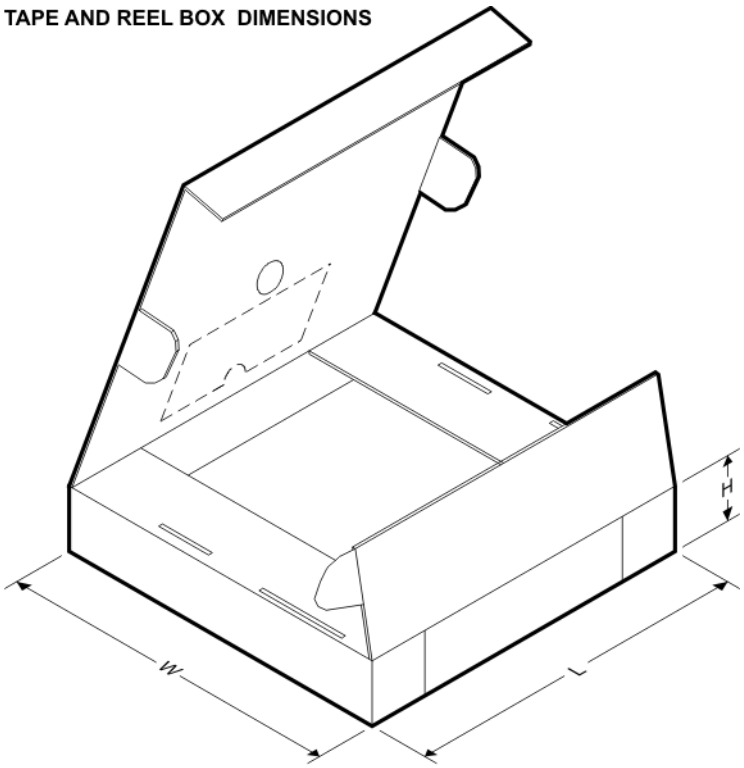
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
THS6022CPWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
THS6022IPWPR	HTSSOP	PWP	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

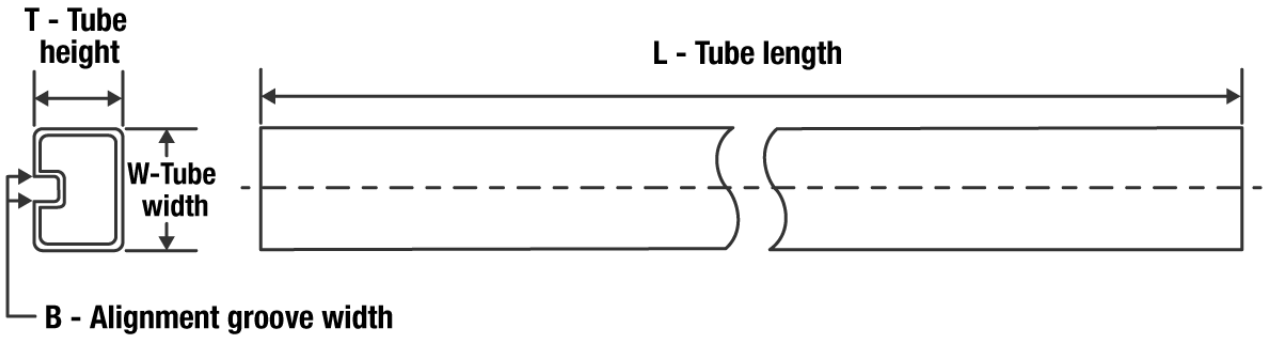
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
THS6022CPWPR	HTSSOP	PWP	14	2000	350.0	350.0	43.0
THS6022IPWPR	HTSSOP	PWP	14	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
THS6022CPWP	PWP	HTSSOP	14	90	530	10.2	3600	3.5
THS6022IPWP	PWP	HTSSOP	14	90	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

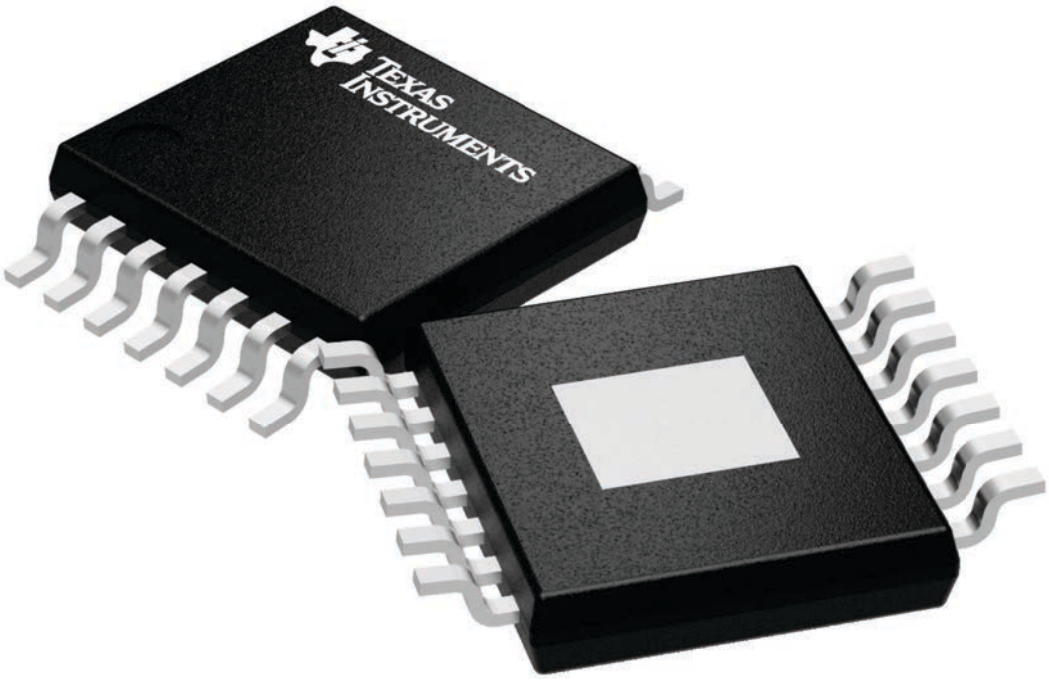
PWP 14

PowerPAD TSSOP - 1.2 mm max height

4.4 x 5.0, 0.65 mm pitch

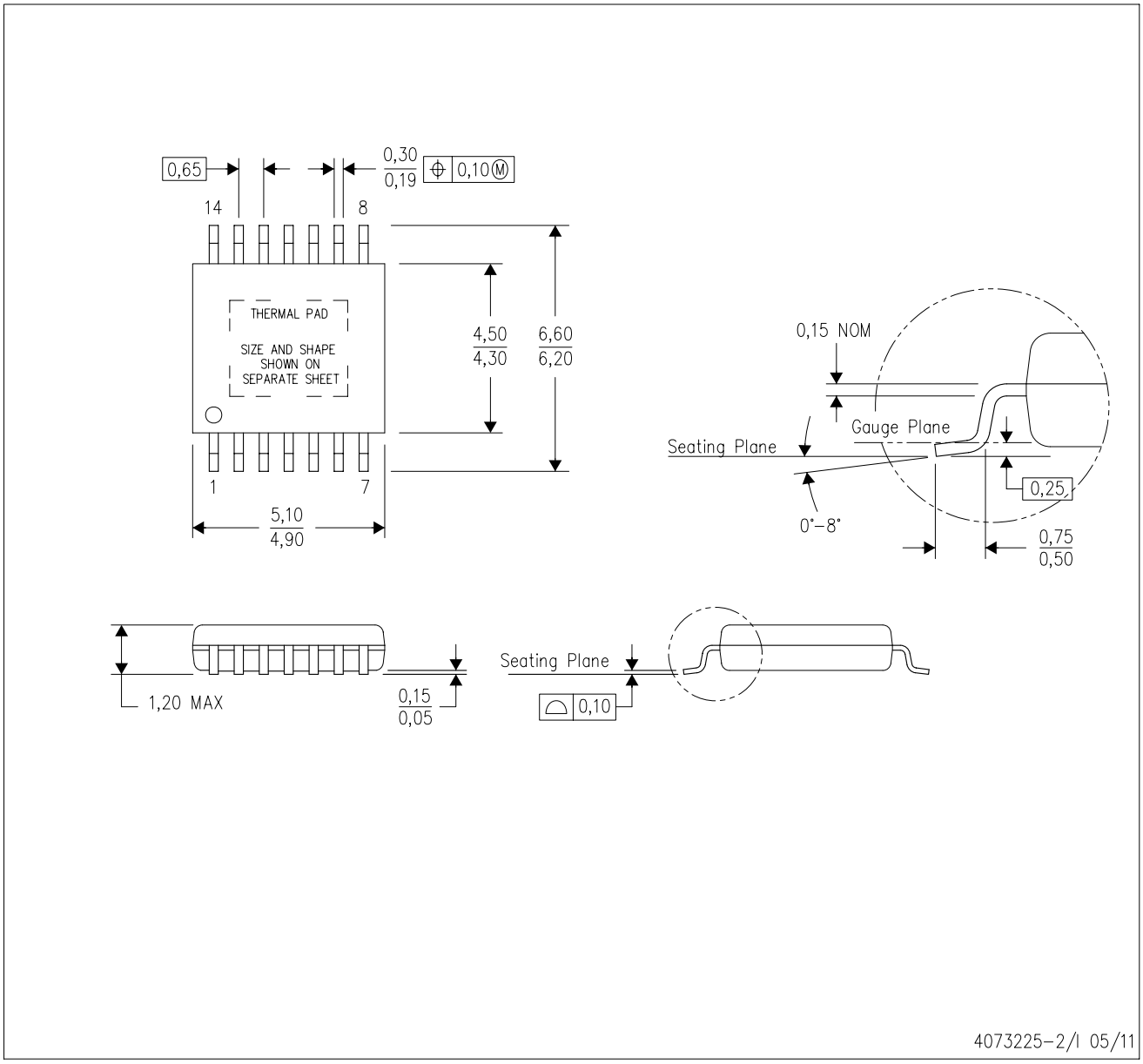
PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224995/A

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

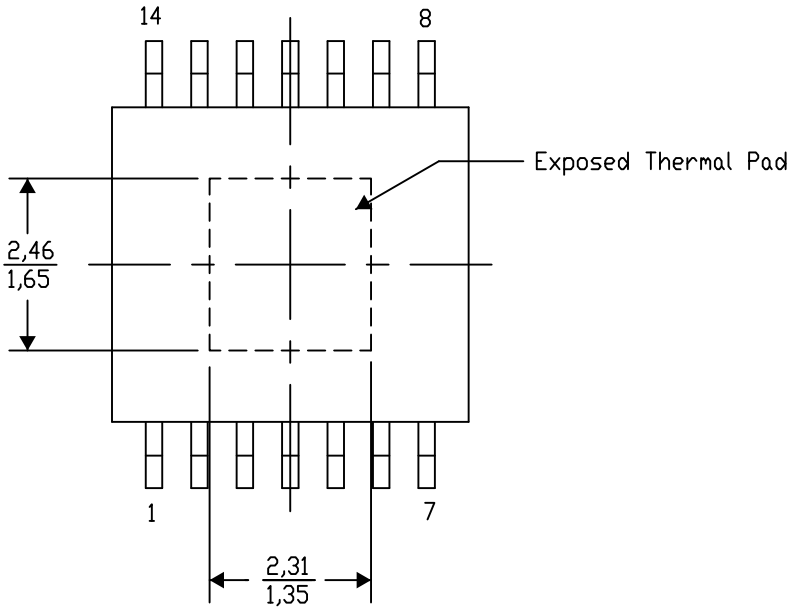
PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

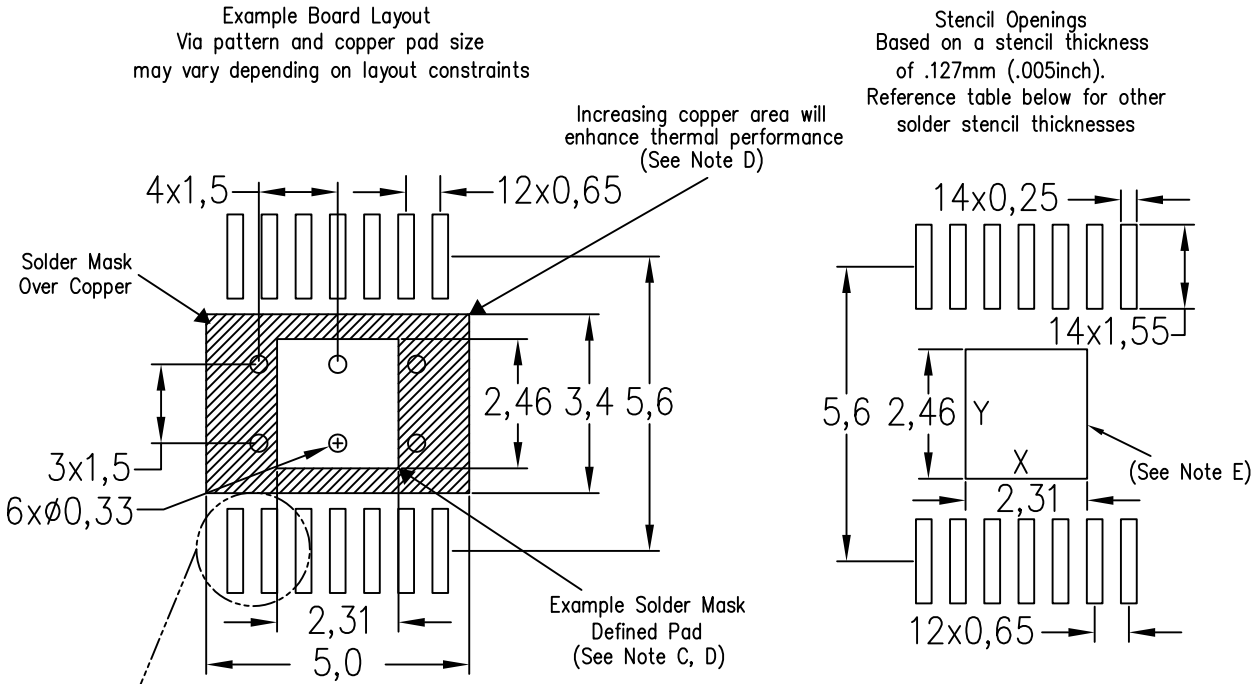
Exposed Thermal Pad Dimensions

4206332–2/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE

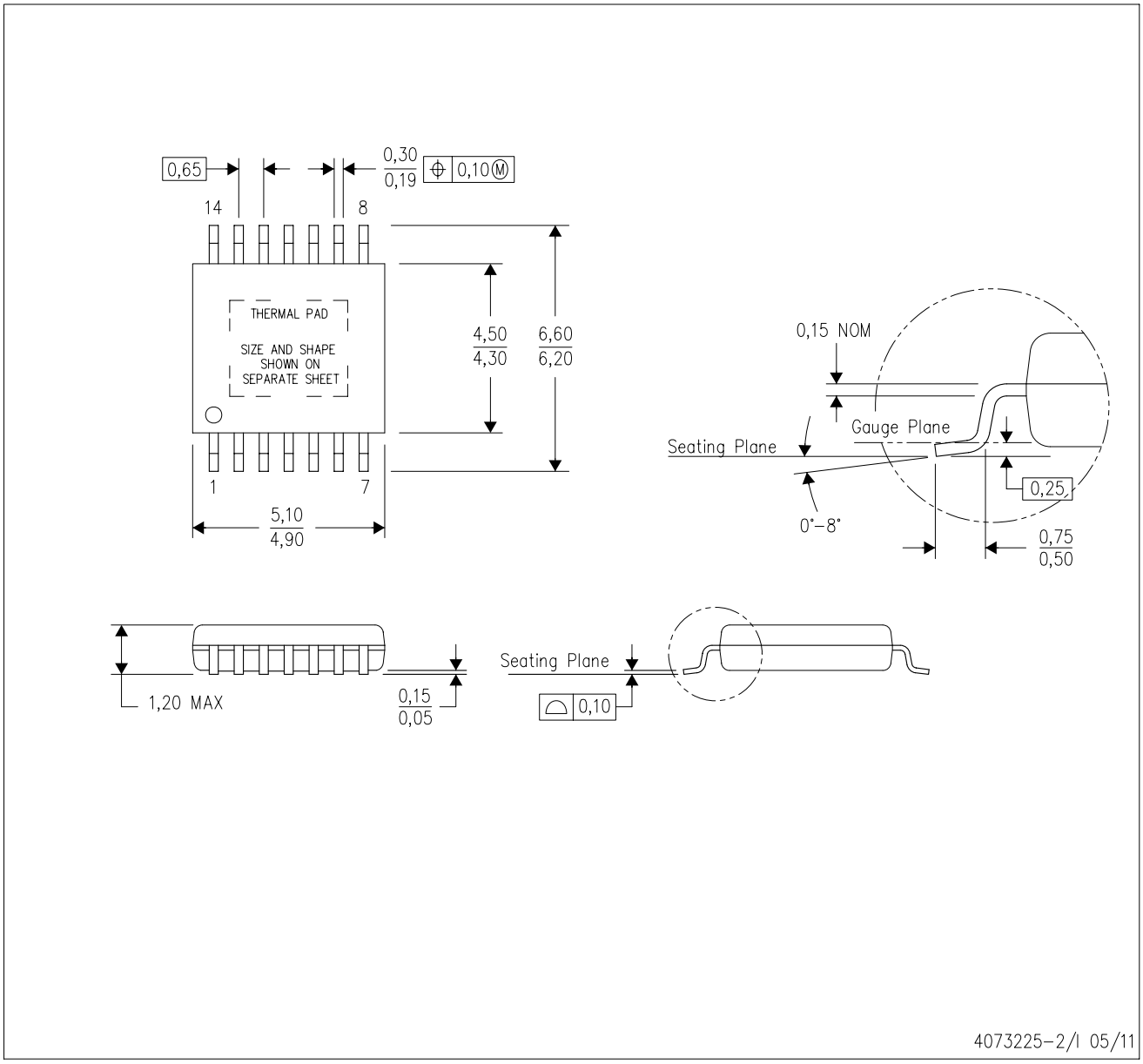


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

4207609–2/W 09/15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

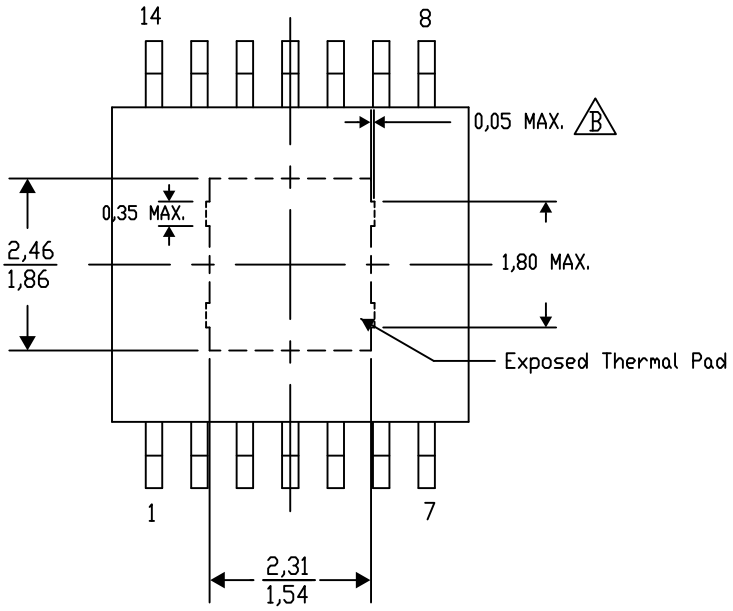
PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332–44/AO 01/16

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

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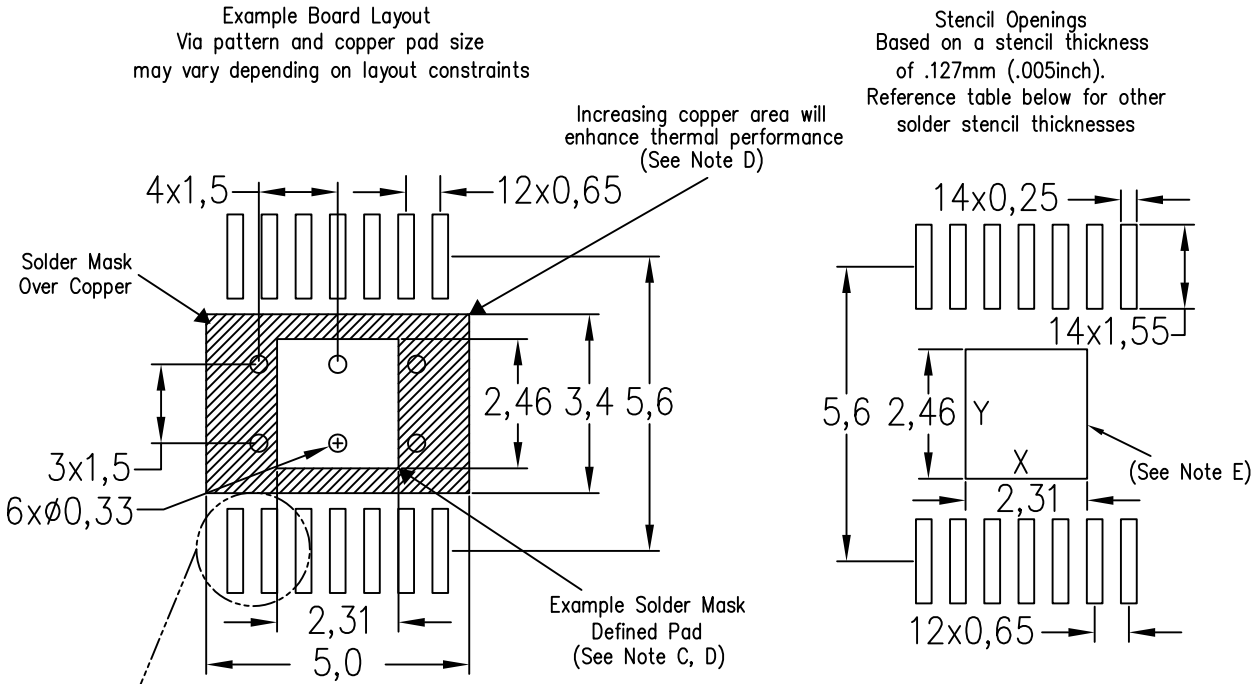
PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

4207609–2/W 09/15

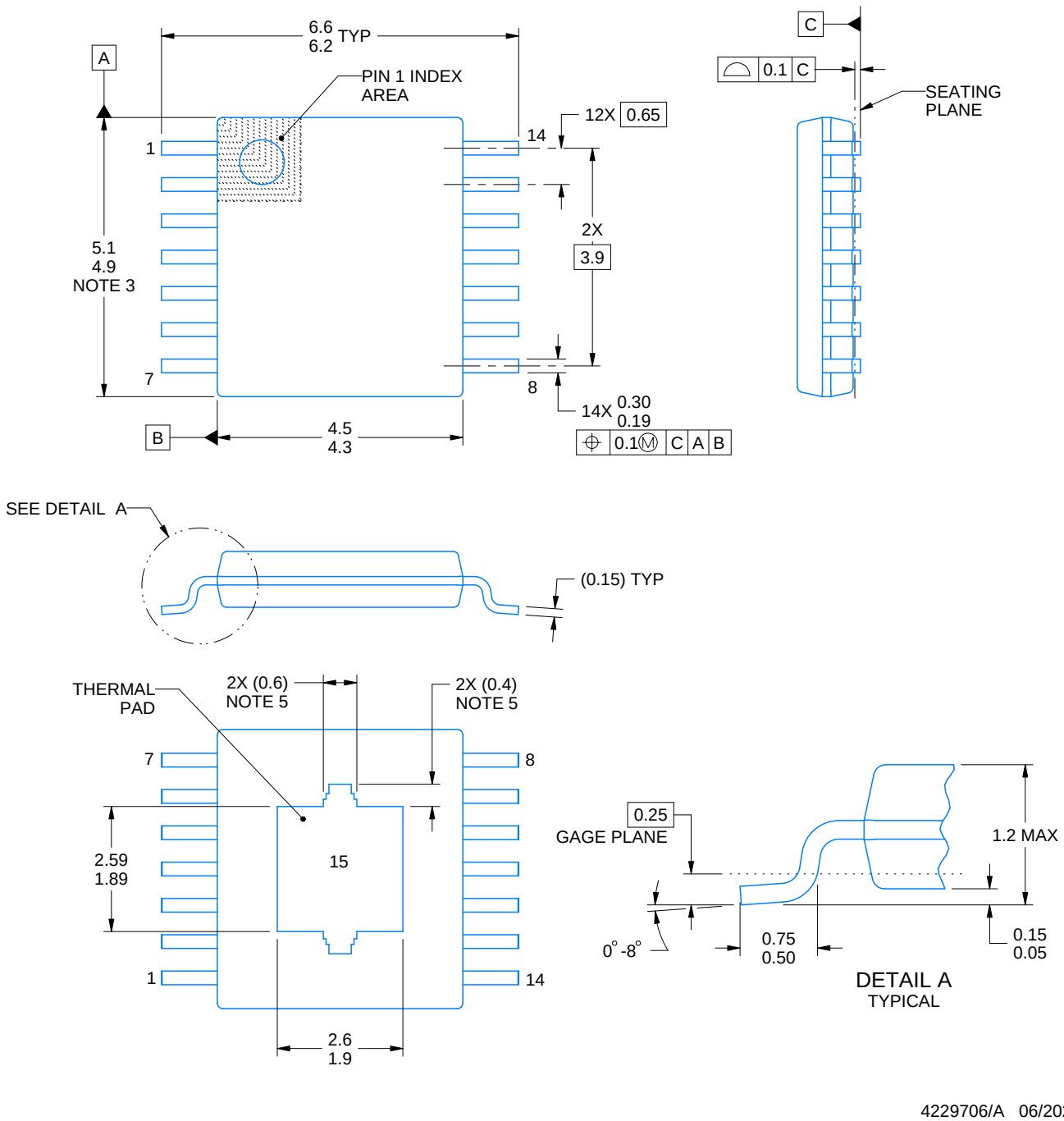
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PWP0014K

PowerPAD™ TSSOP - 1.2 mm max height

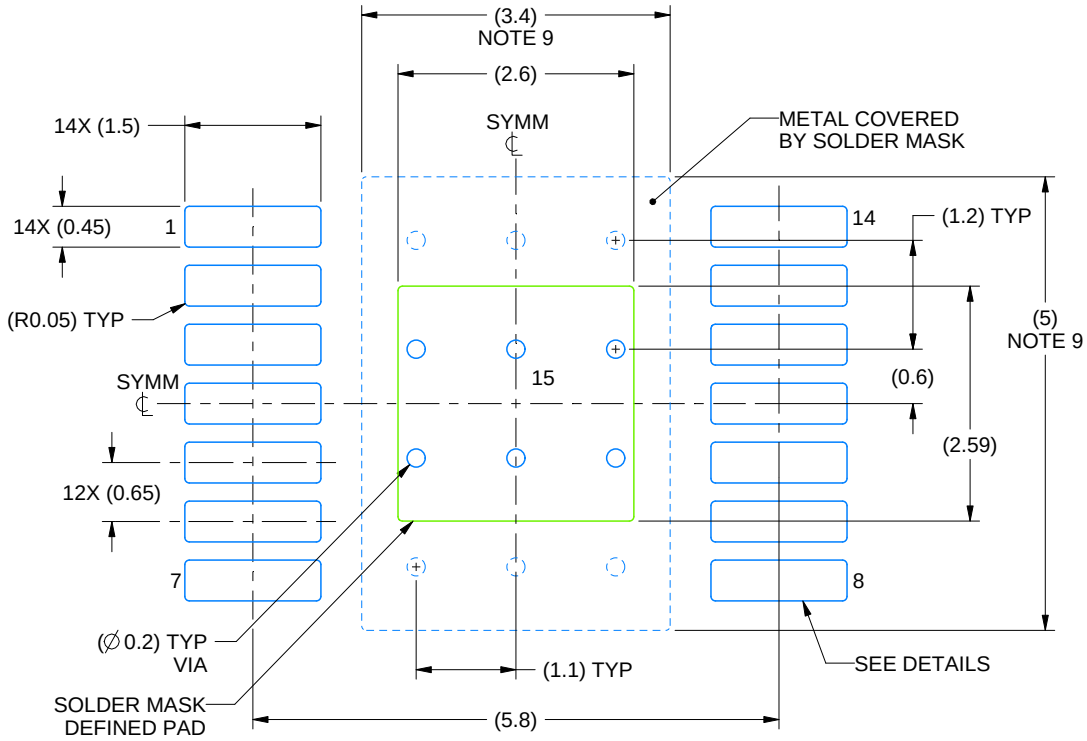
SMALL OUTLINE PACKAGE



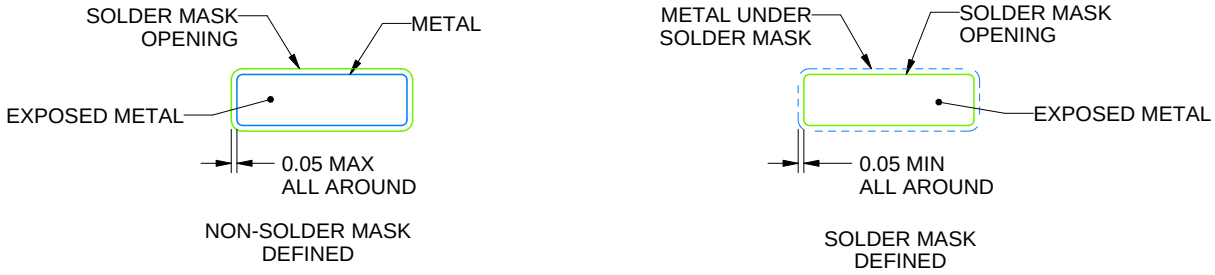
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

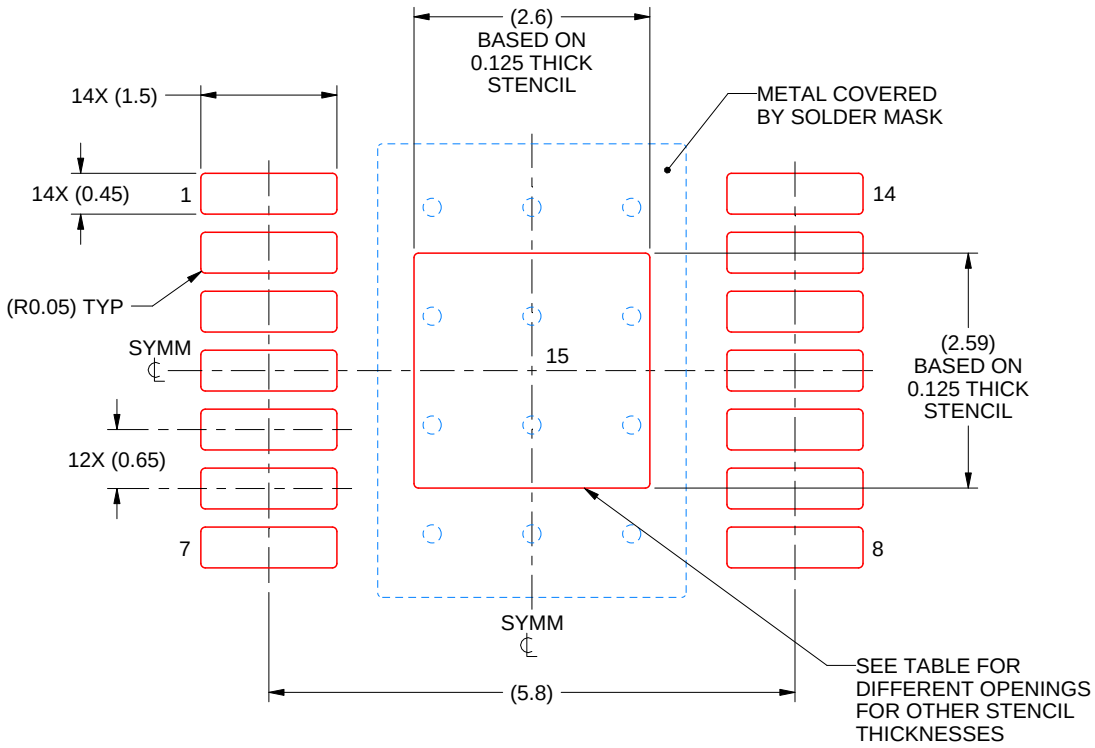


SOLDER MASK DETAILS

4229706/A 06/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.91 X 2.90
0.125	2.60 X 2.59 (SHOWN)
0.15	2.37 X 2.36
0.175	2.20 X 2.19

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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