TL103W Dual Operational Amplifiers With Internal Reference

1 Features

- Operational Amplifier
  - Low Offset Voltage Max of:
    - TL103WA…3 mV (25°C) and 5 mV (Full Temperature)
    - TL103W…4 mV (25°C) and 5 mV (Full Temperature)
  - Low Supply Current…350 μA/Channel (Typ)
  - Unity Gain Bandwidth…0.9 MHz (Typ)
  - Input Common-Mode Range Includes GND
  - Large Output-Voltage Swing… 0 V to V_{CC} – 1.5 V
  - Wide Supply-Voltage Range…3 V to 32 V
  - 2.5-kV ESD Protection (HBM)
- Voltage Reference
  - Fixed 2.5-V Reference
  - Tight Tolerance Max of:
    - TL103WA…0.4% (25°C) and 0.8% (Full Temperature)
    - TL103W . . . 0.7% (25°C) and 1.4% (Full Temperature)
  - Low Temperature Drift…7 mV (Typ) Over Operating Temperature Range
  - Wide Sink-Current Range . . . 0.5 mA (Typ) to 100 mA
  - Output Impedance…0.2 Ω (Typ)

2 Applications

- Battery Chargers
- Switch-Mode Power Supplies
- Linear Voltage Regulation
- Data-Acquisition Systems

3 Description

The TL103W and TL103WA combine the building blocks of a dual operational amplifier and a fixed voltage reference – both of which often are used in the control circuitry of both switch-mode and linear power supplies. OP AMP1 has its noninverting input internally tied to a fixed 2.5-V reference, while OP AMP2 is independent, with both inputs uncommitted.

For the A grade, especially tight voltage regulation can be achieved through low offset voltages for both operational amplifiers (typically 0.5 mV) and tight tolerances for the voltage reference (0.4% at 25°C and 0.8% over operating temperature range).

The TL103W and TL103WA are characterized for operation from –40°C to 105°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TL103W TL103WA	SOIC (8)	4.90 mm x 3.91 mm
	WSON (8)	4.00 mm x 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit

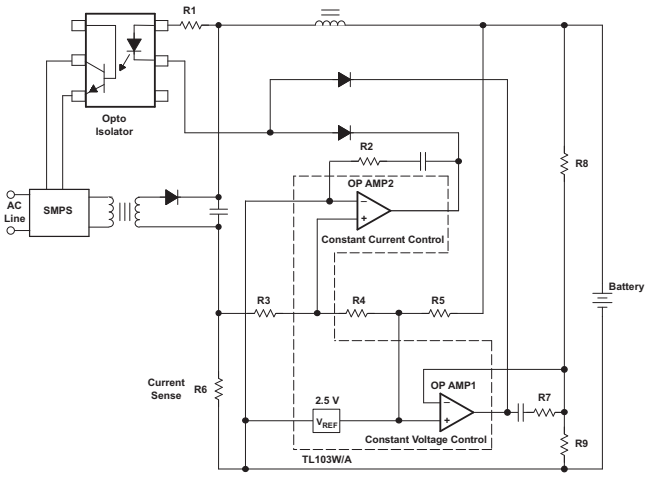

Figure 1. TL103W/A in a Constant-Current and Constant-Voltage Battery Charger

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision L (February 2016) to Revision M **Page**

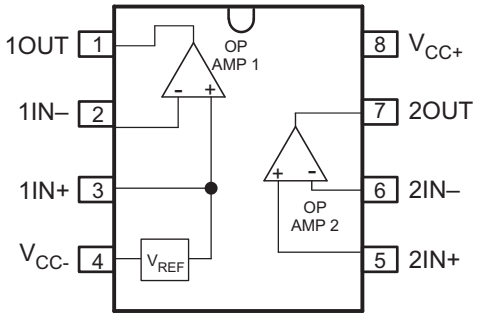
- Changed positive and negative terminals OP AMP 2 in the D Package image of *Pin Configuration and Functions* ... 3

Changes from Revision K (October 2010) to Revision L **Page**

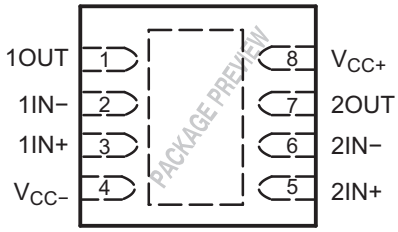
- Added the *Device Information* table, *Pin Configuration and Functions*, *ESD Ratings*, *Thermal Information*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections ... 1
- Changed *Features* From: 2 kV ESD Protection (HBM) To: 2.5-kV ESD Protection (HBM) ... 1
- Changed the Zener diode component to V_{REF} in the *Typical Application Circuit* ... 1
- Changed the Zener diode component to V_{REF} in the D Package of *Pin Configuration and Functions* ... 3

5 Pin Configuration and Functions

D Package
8 Pin (SOIC)
Top View



DRJ Package
8 Pin (WSON)
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	D	DRJ		
1OUT	1	1	O	Opamp 1 output
1IN–	2	2	I	Opamp 1 inverting input
1IN+	3	3	I	Opamp 1 non-inverting input and Shunt reference cathode terminal
$V_{CC–}$	4	4	I	Negative Supply Voltage
2IN+	5	5	O	Opamp 2 output
2IN–	6	6	I	Opamp 2 inverting input
2OUT	7	7	I	Opamp 2 non-inverting input
V_{CC+}	8	8	I	Positive Supply Voltage

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage		36	V
V_{ID}	Operational amplifier input differential voltage		36	V
V_I	Operational amplifier input voltage range	–0.3	36	V
I_{KA}	Voltage reference cathode current		100	mA
T_J	Maximum junction temperature		150	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Supply voltage	3	32	V
I_K	Cathode current	1	100	mA
T_A	Operating free-air temperature	–40	105	°C

6.4 Thermal Information

THERMAL METRIC(1)		TL103W / TL103W D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 OP AMP1, Operational Amplifier With Noninverting Input Connected to the Internal V_{REF} Electrical Characteristics

V_{CC+} = 5 V, V_{CC} = GND, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TL103W	V_{icm} = 0 V	25°C		1	4	mV
				Full range			5	
		TL103WA	V_{icm} = 0 V	25°C		0.5	3	
				Full range			5	
αV_{IO}	Input offset-voltage drift			25°C		7		µV/°C
I_{IB}	Input bias current (negative input)			25°C		20		nA
A_{VD}	Large-signal voltage gain		V_{CC+} = 15 V, R_L = 2 kΩ, V_{icm} = 0 V	25°C		100		V/mV
k_{SVR}	Supply-voltage rejection ratio		V_{CC+} = 5 V to 30 V, V_{icm} = 0 V	25°C	65	100		dB
$I_{O(source)}$	Output source current		V_{CC+} = 15 V, V_O = 2 V, V_{id} = 1 V	25°C	20	40		mA
I_{SC}	Short circuit to GND		V_{CC+} = 15 V	25°C		40	60	mA
$I_{O(sink)}$	Output sink current		V_{CC+} = 15 V, V_O = 2 V, V_{id} = –1 V	25°C	10	12		mA
			V_{CC+} = 15 V, V_O = 0.2 V, V_{id} = –1 V		12	50		µA
V_{OH}	High-level output voltage		V_{CC} = 30 V, R_L = 2 kΩ	25°C	26	27		V
				Full range	26			
			V_{CC} = 30 V, R_L = 10 kΩ	25°C	27	28		
				Full range	27			
V_{OL}	Low-level output voltage		R_L = 10 kΩ	25°C		5	20	mV
				Full range			20	
SR	Slew rate at unity gain		V_{CC+} = 15 V, C_L = 100 pF, R_L = 2 kΩ, V_I = 0.5 V to 2 V, unity gain	25°C	0.2	0.4		V/µs
GBW	Gain bandwidth product		V_{CC+} = 30 V, V_I = 10 mV, C_L = 100 pF, R_L = 2 kΩ, f = 100 kHz	25°C	0.5	0.9		MHz
THD	Total harmonic distortion		V_{CC+} = 30 V, V_O = 2 V_{pp}, C_L = 100 pF, R_L = 2 kΩ, f = 1 kHz, A_V = 20 dB	25°C		0.02%		

6.6 OP AMP2, Independent Operational Amplifier, Electrical Characteristics

V_{CC+} = 5 V, V_{CC} = GND, V_O = 1.4 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	TL103W	V_{icm} = 0 V	25°C		1	4	mV
				Full range			5	
		TL103WA	V_{icm} = 0 V	25°C		0.5	3	
				Full range			5	
αV_{IO}	Input offset voltage drift			25°C		7		µV/°C
I_{IO}	Input offset current			25°C		2	75	nA
				Full range			150	
I_{IB}	Input bias current			25°C		20	150	nA
				Full range			200	
A_{VD}	Large-signal voltage gain		V_{CC+} = 15 V, R_L = 2 kΩ, V_O = 1.4 V to 11.4 V	25°C	50	100		V/mV
				Full range	25			
k_{SVR}	Supply-voltage rejection ratio		V_{CC+} = 5 V to 30 V	25°C	65	100		dB
V_{ICR}	Input common-mode voltage range		V_{CC+} = 30 V (1)	25°C	0		V_{CC+} – 1.5	V
				Full range	0		V_{CC+} – 2	
CMRR	Common-mode rejection ratio			25°C	70	85		dB
				Full range	60			
$I_{O(source)}$	Output source current		V_{CC+} = 15 V, V_O = 2 V, V_{id} = 1 V	25°C	20	40		mA
I_{SC}	Short circuit to GND		V_{CC+} = 15 V	25°C		40	60	mA
$I_{O(sink)}$	Output sink current		V_{CC+} = 15 V, V_O = 2 V, V_{id} = –1 V	25°C	10	12		mA
			V_{CC+} = 15 V, V_O = 0.2 V, V_{id} = –1 V		12	50		µA
V_{OH}	High-level output voltage		V_{CC} = 30 V, R_L = 2 kΩ	25°C	26	27		V
				Full range	26			
			V_{CC} = 30 V, R_L = 10 kΩ	25°C	27	28		
				Full range	27			
V_{OL}	Low-level output voltage		R_L = 10 kΩ	25°C		5	20	mV
				Full range			20	
SR	Slew rate at unity gain		V_{CC+} = 15 V, C_L = 100 pF, R_L = 2 kΩ, V_I = 0.5 V to 3 V, unity gain	25°C	0.2	0.4		V/µs
GBW	Gain bandwidth product		V_{CC+} = 30 V, V_I = 10 mV, C_L = 100 pF, R_L = 2 kΩ, f = 100 kHz	25°C	0.5	0.9		MHz
THD	Total harmonic distortion		V_{CC+} = 30 V, V_O = 2 V_{pp}, C_L = 100 pF, R_L = 2 kΩ, f = 1 kHz, A_V = 20 dB	25°C		0.02%		
V_n	Equivalent input noise voltage		V_{CC} = 30 V, R_S = 100 Ω, f = 1 kHz	25°C		50		nV/√Hz

(1) The input common-mode voltage of either input should not be allowed to go below –0.3 V. The upper end of the common-mode voltage range is V_{CC+} – 1.5 V, but either input can go to V_{CC+} + 0.3 V (but ≤36 V) without damage.

6.7 Voltage Reference, Electrical Characteristics

PARAMETER			TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{REF}	Reference voltage	TL103W	I_K = 10 mA	25°C	2.482	2.5	2.518	V
				Full range	2.465		2.535	
		TL103WA	I_K = 10 mA	25°C	2.49	2.5	2.51	
				Full range	2.48		2.52	
ΔV_{REF}	Reference input voltage deviation over temperature range		$V_{KA} = V_{REF}$, I_K = 10 mA	Full range		7	30	mV
I_{min}	Minimum cathode current for regulation		$V_{KA} = V_{REF}$	25°C		0.5	1	mA
$\lvert z_{ka} \rvert$	Dynamic impedance(1)		$V_{KA} = V_{REF}$, ΔI_K = 1 mA to 100 mA, f < 1 kHz	25°C		0.2	0.5	Ω

(1) The dynamic impedance is defined as $|z_{ka}| = \frac{\Delta V_{KA}}{\Delta I_K}$.

6.8 Total Device, Electrical Characteristics

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
I_{CC}	Total supply current, excluding cathode-current reference	V_{CC+} = 5 V, No load	Full range		0.7	1.2	mA
		V_{CC+} = 30 V, No load				2	

7 Device and Documentation Support

7.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TL103W	Click here	Click here	Click here	Click here	Click here
TL103WA	Click here	Click here	Click here	Click here	Click here

7.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

7.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

7.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

7.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

7.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

8 Mechanical, Packaging, and Orderable Information

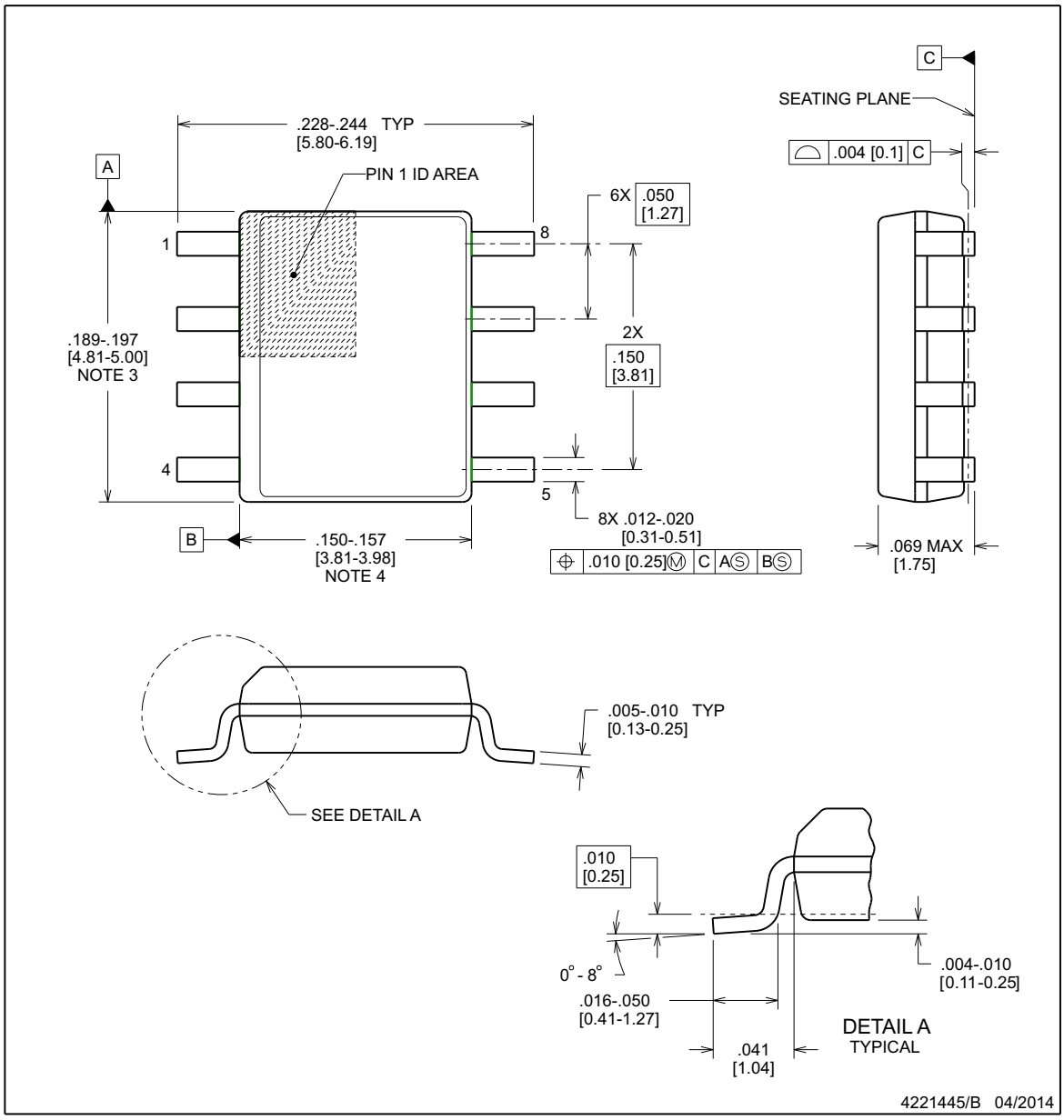
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

D0008B

SOIC - 1.75 mm max height

SOIC



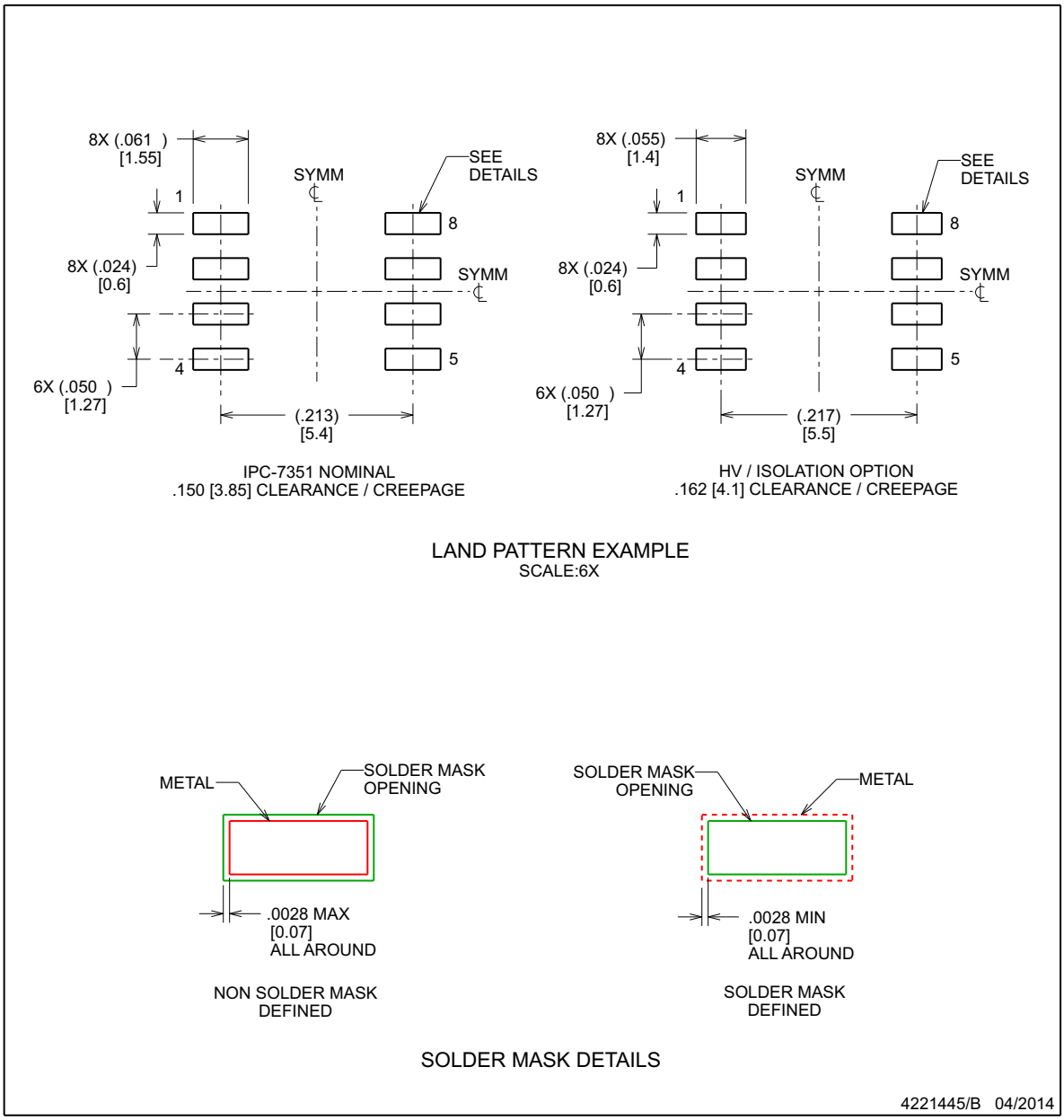
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15], per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008B SOIC - 1.75 mm max height

SOIC



NOTES: (continued)

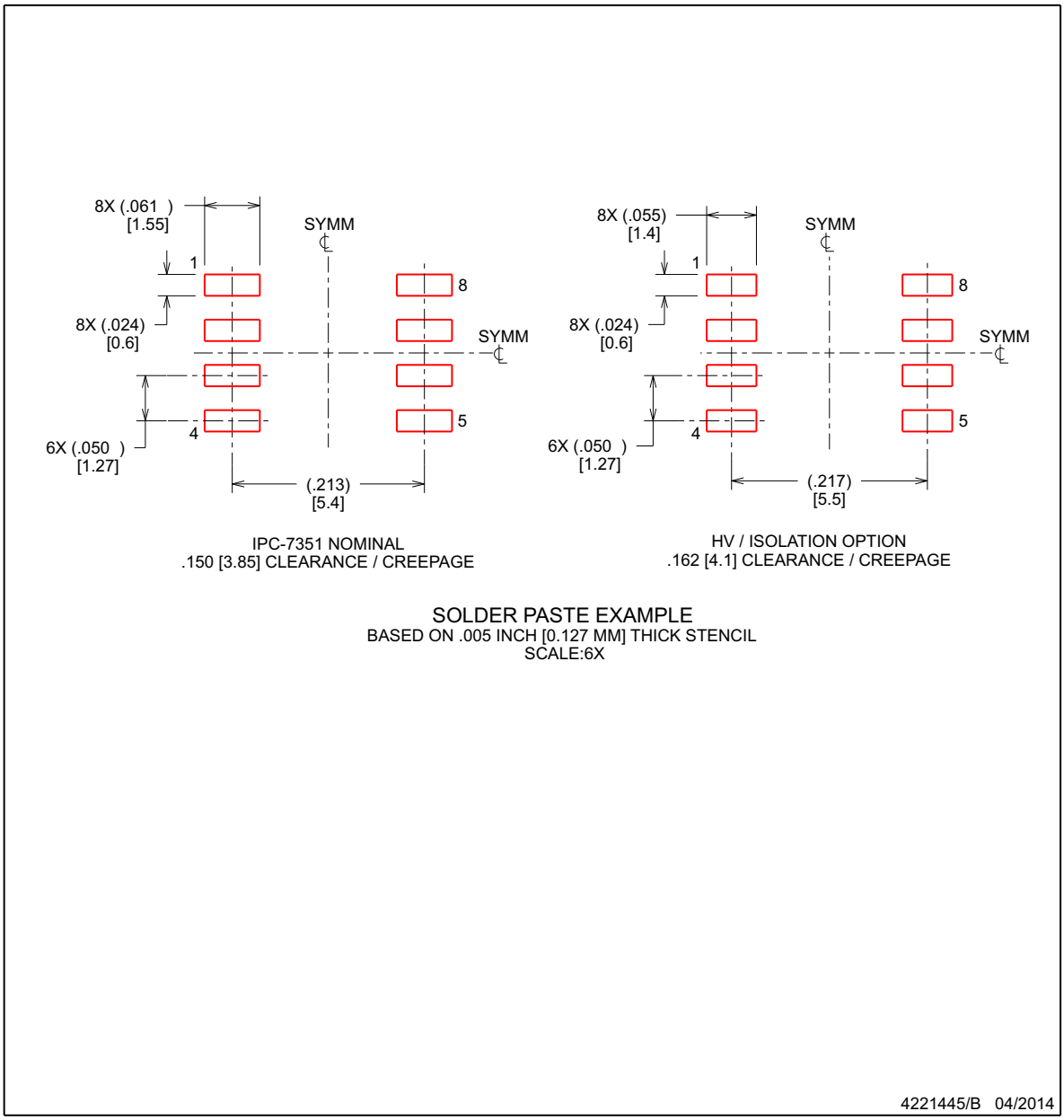
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008B

SOIC - 1.75 mm max height

SOIC



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL103WAID	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103WA	
TL103WAIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103WA	Samples
TL103WID	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103W	
TL103WIDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	Z103W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

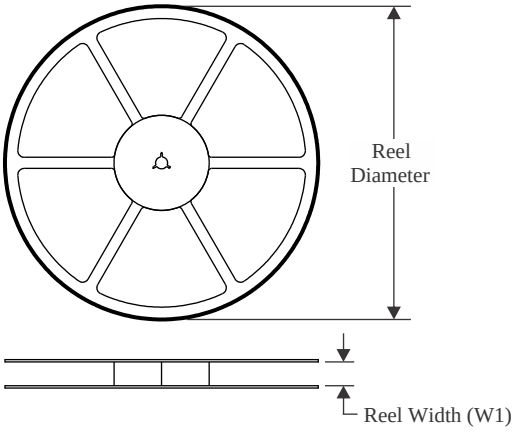
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

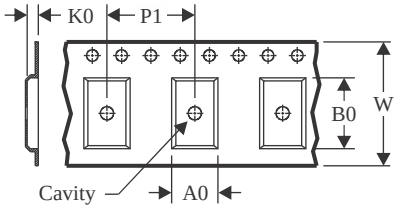
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

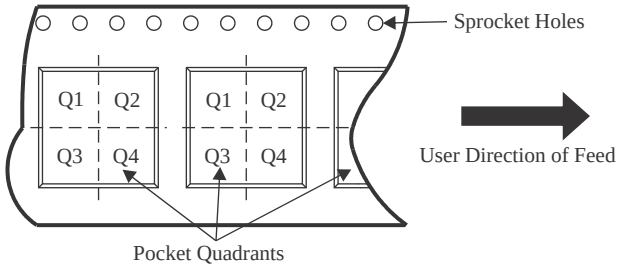


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

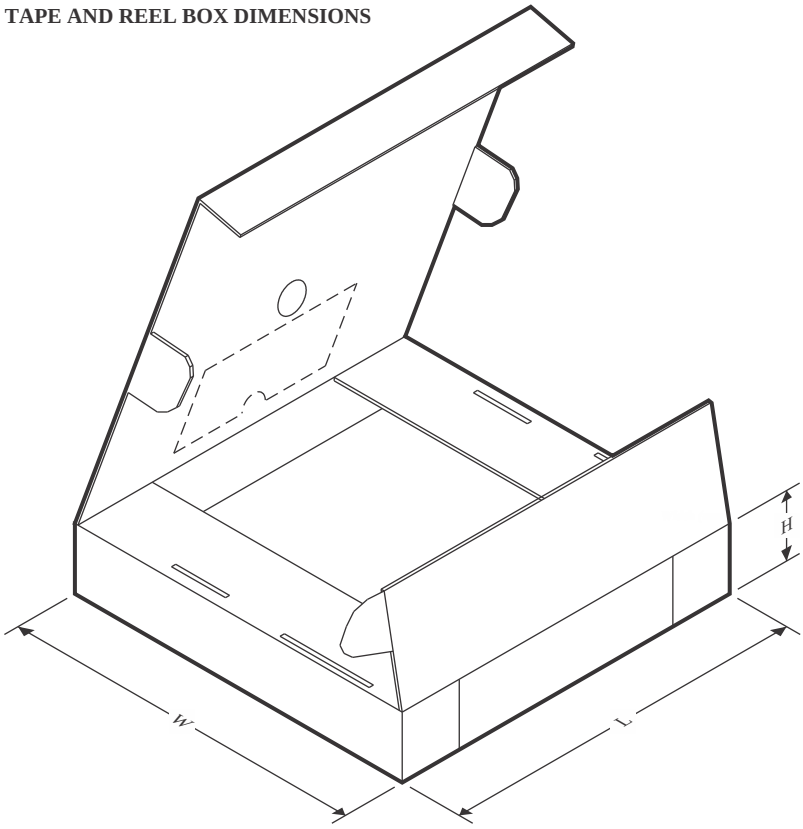
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL103WAIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL103WIDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

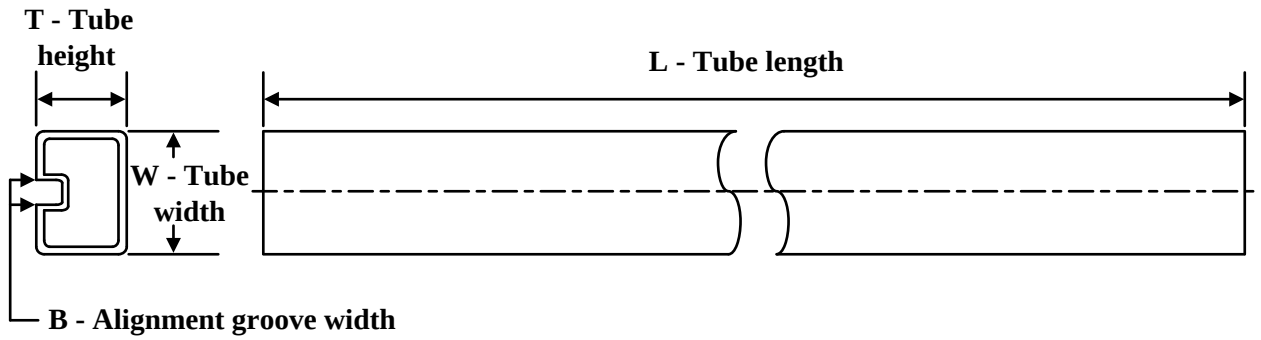
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL103WAIDR	SOIC	D	8	2500	340.5	336.1	25.0
TL103WIDR	SOIC	D	8	2500	340.5	336.1	25.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL103WAID	D	SOIC	8	75	507	8	3940	4.32
TL103WID	D	SOIC	8	75	507	8	3940	4.32

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