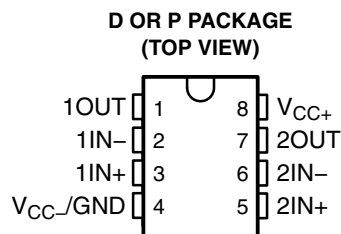


- Wide Gain-Bandwidth Product . . . 4 MHz
- High Slew Rate . . . 13 V/ $\mu$ s
- Fast Settling Time . . . 1.1  $\mu$ s to 0.1%
- Wide-Range Single-Supply Operation . . . 4 V to 36 V
- Wide Input Common-Mode Range Includes Ground ( $V_{CC-}$ )
- Low Total Harmonic Distortion . . . 0.02%
- Large-Capacitance Drive Capability . . . 10,000 pF
- Output Short-Circuit Protection



### description/ordering information

Quality, low-cost, bipolar fabrication with innovative design concepts is employed for the TL3472 operational amplifier. This device offers 4 MHz of gain-bandwidth product, 13-V/ $\mu$ s slew rate, and fast settling time, without the use of JFET device technology. Although the TL3472 can be operated from split supplies, it is particularly suited for single-supply operation because the common-mode input voltage range includes ground potential ( $V_{CC-}$ ). With a Darlington transistor input stage, this device exhibits high input resistance, low input offset voltage, and high gain. The all-npn output stage, characterized by no dead-band crossover distortion and large output voltage swing, provides high-capacitance drive capability, excellent phase and gain margins, low open-loop high-frequency output impedance, and symmetrical source/sink ac frequency response. This low-cost amplifier is an alternative to the MC33072 and the MC34072 operational amplifiers.

### ORDERING INFORMATION

| $T_A$          | PACKAGE† |              | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|----------|--------------|-----------------------|------------------|
| 0°C to 70°C    | PDIP (P) | Tube of 25   | TL3472CP              | TL3472CP         |
|                | SOIC (D) | Tube of 50   | TL3472CD              | 3472C            |
|                |          | Reel of 2500 | TL3472CDR             |                  |
| -40°C to 105°C | PDIP (P) | Tube of 25   | TL3472IP              | TL3472IP         |
|                | SOIC (D) | Tube of 50   | TL3472ID              | Z3472            |
|                |          | Reel of 2500 | TL3472IDR             |                  |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

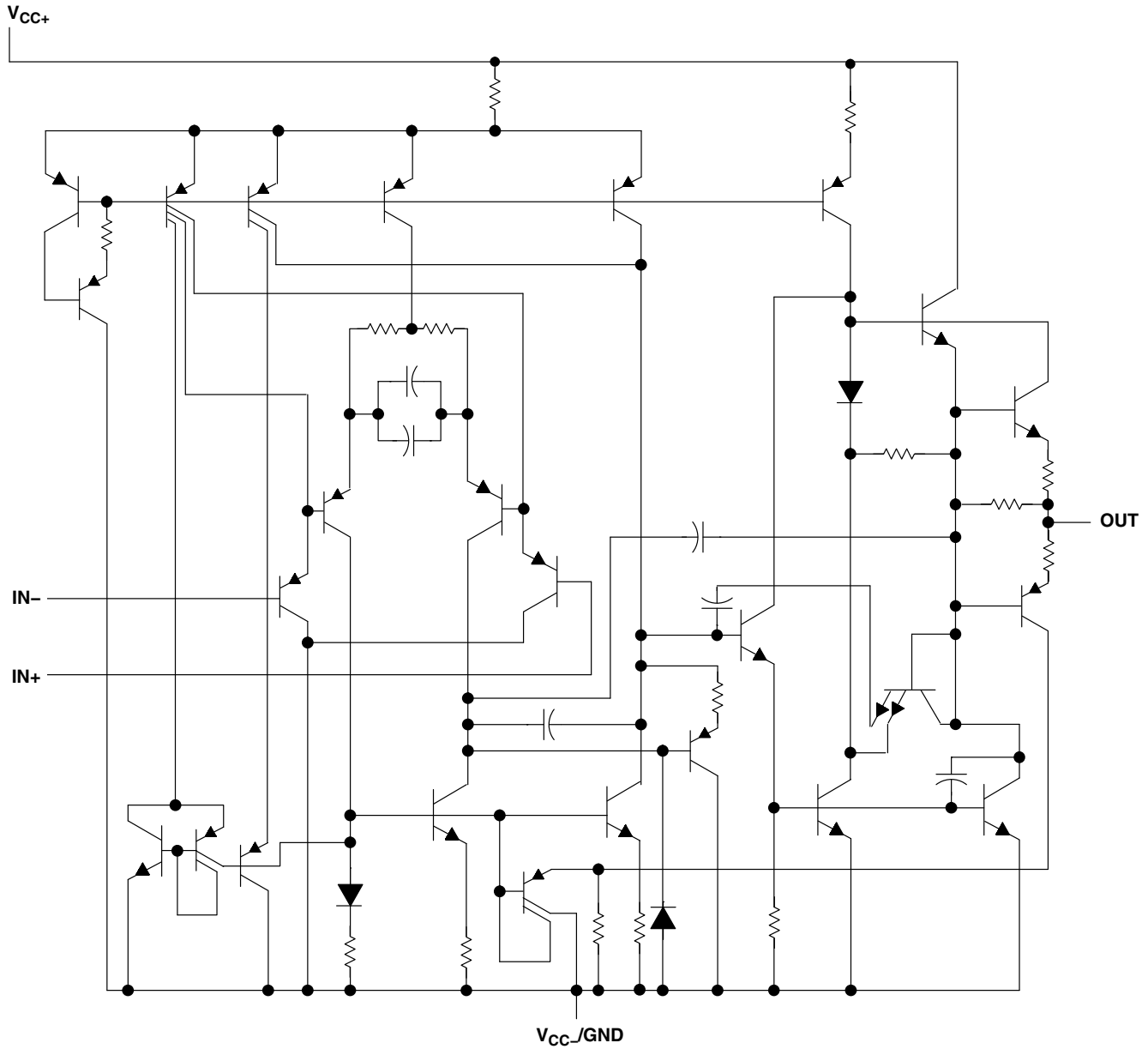
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# TL3472 HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIER

SLOS200G – OCTOBER 1997 – REVISED JULY 2003

## schematic (each amplifier)



# TL3472

## HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIER

SLOS200G – OCTOBER 1997 – REVISED JULY 2003

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

|   |                |
|---|----------------|
| Supply voltage (see Note 1): $V_{CC+}$ .....                                  | 18 V           |
| $V_{CC-}$ .....   | -18 V          |
| Differential input voltage, $V_{ID}$ (see Note 2) .....                       | $\pm 36$ V     |
| Input voltage, $V_I$ (any input) .....  | $V_{CC\pm}$    |
| Input current, $I_I$ (each input) .....                                       | $\pm 1$ mA     |
| Output current, $I_O$ .....   | $\pm 80$ mA    |
| Total current into $V_{CC+}$ .....  | 80 mA          |
| Total current out of $V_{CC-}$ .....  | 80 mA          |
| Duration of short-circuit current at (or below) 25°C (see Note 3) .....       | Unlimited      |
| Package thermal impedance, $\theta_{JA}$ (see Notes 4 and 5): D package ..... | 97°C/W         |
| P package .....   | 85°C/W         |
| Operating virtual junction temperature, $T_J$ .....                           | 150°C          |
| Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds .....            | 260°C          |
| Storage temperature range, $T_{stg}$ .....                                    | -65°C to 150°C |

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, except differential voltages, are with respect to the midpoint between  $V_{CC+}$  and  $V_{CC-}$ .
  2. Differential voltages are at the noninverting input with respect to the inverting input. Excessive input current can flow when the input is less than  $V_{CC-} - 0.3$  V.
  3. The output can be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
  4. Maximum power dissipation is a function of  $T_J(\text{max})$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(\text{max}) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can impact reliability.
  5. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions

|             |                                | MIN                    | MAX | UNIT |    |
|-------------|--------------------------------|------------------------|-----|------|----|
| $V_{CC\pm}$ | Supply voltage                 | 4                      | 36  | V    |    |
| $V_{IC}$    | Common-mode input voltage      | $V_{CC} = 5$ V         | 0   | 2.8  | V  |
|             |                                | $V_{CC\pm} = \pm 15$ V | -15 | 12.8 |    |
| $T_A$       | Operating free-air temperature | TL3472C                | 0   | 70   | °C |
|             |                                | TL3472I                | -40 | 105  |    |



# TL3472

## HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIER

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### electrical characteristics at specified free-air temperature, $V_{CC\pm} = \pm 15$ V (unless otherwise noted)

| PARAMETER   | TEST CONDITIONS  | $T_A$               | MIN         | TYP†        | MAX  | UNIT                         |
|---|--|---------------------|-------------|-------------|------|------------------------------|
| $V_{IO}$ Input offset voltage   | $V_{IC} = 0$ ,<br>$V_O = 0$ ,<br>$R_S = 50 \Omega$           | $V_{CC} = 5$ V      | 25°C        | 1.5         | 10   | mV                           |
|   |  | $V_{CC} = \pm 15$ V | 25°C        | 1.0         | 10   |                              |
|   |  |                     | Full range‡ |             |      |                              |
| $\alpha_{V_{IO}}$ Temperature coefficient of input offset voltage             | $V_{IC} = 0$ ,<br>$V_O = 0$ ,<br>$R_S = 50 \Omega$           | $V_{CC} = \pm 15$ V | Full range‡ | 10          |      | $\mu\text{V}/^\circ\text{C}$ |
| $I_{IO}$ Input offset current   |  | $V_{CC} = \pm 15$ V | 25°C        | 6           | 75   | nA                           |
|   |  |                     | Full range‡ |             | 300  |                              |
| $I_{IB}$ Input bias current   |  | $V_{CC} = \pm 15$ V | 25°C        | 100         | 500  | nA                           |
|   | Full range‡  |                     |             | 700         |      |                              |
| $V_{ICR}$ Common-mode input voltage range                                     | $R_S = 50 \Omega$  | 25°C                |             | -15 to 12.8 |      | V                            |
|   |  | Full range‡         |             | -15 to 12.8 |      |                              |
| $V_{OH}$ High-level output voltage  | $V_{CC+} = 5$ V, $V_{CC-} = 0$ , $R_L = 2$ k $\Omega$        | 25°C                | 3.7         | 4           | V    |                              |
|   | $R_L = 10$ k $\Omega$  | 25°C                | 13.6        | 14          |      |                              |
|   | $R_L = 2$ k $\Omega$   | Full range‡         | 13.4        |             |      |                              |
| $V_{OL}$ Low-level output voltage   | $V_{CC+} = 5$ V, $V_{CC-} = 0$ , $R_L = 2$ k $\Omega$        | 25°C                | 0.1         | 0.3         | V    |                              |
|   | $R_L = 10$ k $\Omega$  | 25°C                | -14.7       | -14.3       |      |                              |
|   | $R_L = 2$ k $\Omega$   | Full range‡         | -13.5       |             |      |                              |
| $A_{VD}$ Large-signal differential voltage amplification                      | $V_O = \pm 10$ V, $R_L = 2$ k $\Omega$                       | 25°C                | 25          | 100         | V/mV |                              |
|   |  | Full range‡         | 20          |             |      |                              |
| $I_{OS}$ Short-circuit output current   | Source: $V_{ID} = 1$ V, $V_O = 0$                            | 25°C                | -10         | -34         | mA   |                              |
|   | Sink: $V_{ID} = -1$ V, $V_O = 0$                             |                     | 20          | 27          |      |                              |
| CMRR Common-mode rejection ratio  | $V_{IC} = V_{ICR}(\text{min})$ , $R_S = 50 \Omega$           | 25°C                | 65          | 97          | dB   |                              |
| $k_{SVR}$ Supply-voltage rejection ratio ( $\Delta V_{CC\pm}/\Delta V_{IO}$ ) | $V_{CC\pm} = \pm 13.5$ V to $\pm 16.5$ V, $R_S = 100 \Omega$ | 25°C                | 70          | 97          | dB   |                              |
| $I_{CC}$ Supply current (per channel)   | $V_O = 0$ , No load  | 25°C                | 3.5         | 4.5         | mA   |                              |
|   |  | Full range‡         | 4.5         | 5.5         |      |                              |
|   |  | 25°C                | 3.5         | 4.5         |      |                              |

† All typical values are at  $T_A = 25^\circ\text{C}$ .

‡ Full range is  $0^\circ\text{C}$  to  $70^\circ\text{C}$  for the TL3472C device and  $-40^\circ\text{C}$  to  $105^\circ\text{C}$  for the TL3472I device.



# TL3472

## HIGH-SLEW-RATE, SINGLE-SUPPLY OPERATIONAL AMPLIFIER

SLOS200G – OCTOBER 1997 – REVISED JULY 2003

**operating characteristics,  $V_{CC\pm} = \pm 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$**

| PARAMETER |                                | TEST CONDITIONS   |                       | MIN | TYP  | MAX | UNIT                         |
|-----------|--------------------------------|---|-----------------------|-----|------|-----|------------------------------|
| SR+       | Positive slew rate             | $V_I = -10\text{ V to } 10\text{ V}$ ,<br>$R_L = 2\text{ k}\Omega$ , $C_L = 300\text{ pF}$                | $A_V = 1$             | 8   | 10   |     | $\text{V}/\mu\text{s}$       |
| SR-       | Negative slew rate             |   | $A_V = -1$            |     | 13   |     | $\text{V}/\mu\text{s}$       |
| $t_s$     | Settling time                  | $A_{VD} = -1$ , 10-V step   | To 0.1%               |     | 1.1  |     | $\mu\text{s}$                |
|           |                                |   | To 0.01%              |     | 2.2  |     |                              |
| $V_n$     | Equivalent input noise voltage | $f = 1\text{ kHz}$ ,  | $R_S = 100\ \Omega$   |     | 49   |     | $\text{nV}/\sqrt{\text{Hz}}$ |
| $I_n$     | Equivalent input noise current | $f = 1\text{ kHz}$  |                       |     | 0.22 |     | $\text{pA}/\sqrt{\text{Hz}}$ |
| THD       | Total harmonic distortion      | $V_{O(PP)} = 2\text{ V to } 20\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $A_{VD} = 10$ , $f = 10\text{ kHz}$ |                       |     | 0.02 |     | %                            |
| GBW       | Gain-bandwidth product         | $f = 100\text{ kHz}$  |                       | 3   | 4    |     | MHz                          |
| BW        | Power bandwidth                | $V_{O(PP)} = 20\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $A_{VD} = 1$ , THD = 5.0%                          |                       |     | 160  |     | kHz                          |
| $\phi_m$  | Phase margin                   | $R_L = 2\text{ k}\Omega$  | $C_L = 0$             |     | 70   |     | deg                          |
|           |                                |   | $C_L = 300\text{ pF}$ |     | 50   |     |                              |
|           | Gain margin                    | $R_L = 2\text{ k}\Omega$  | $C_L = 0$             |     | 12   |     | dB                           |
|           |                                |   | $C_L = 300\text{ pF}$ |     | 4    |     |                              |
| $r_i$     | Differential input resistance  | $V_{IC} = 0$  |                       |     | 150  |     | $\text{M}\Omega$             |
| $C_i$     | Input capacitance              | $V_{IC} = 0$  |                       |     | 2.5  |     | $\text{pF}$                  |
|           | Channel separation             | $f = 10\text{ kHz}$   |                       |     | 101  |     | dB                           |
| $z_o$     | Open-loop output impedance     | $f = 1\text{ MHz}$ ,  | $A_V = 1$             |     | 20   |     | $\Omega$                     |



**PACKAGING INFORMATION**

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| TL3472CD         | LIFEBUY       | SOIC         | D               | 8    | 75          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | 3472C                   |         |
| TL3472CDR        | ACTIVE        | SOIC         | D               | 8    | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | 0 to 70      | 3472C                   | Samples |
| TL3472CP         | ACTIVE        | PDIP         | P               | 8    | 50          | RoHS & Green    | NIPDAU                               | N / A for Pkg Type   | 0 to 70      | TL3472CP                | Samples |
| TL3472ID         | LIFEBUY       | SOIC         | D               | 8    | 75          | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 105   | Z3472                   |         |
| TL3472IDR        | ACTIVE        | SOIC         | D               | 8    | 2500        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 105   | Z3472                   | Samples |
| TL3472IP         | ACTIVE        | PDIP         | P               | 8    | 50          | RoHS & Green    | NIPDAU                               | N / A for Pkg Type   | -40 to 105   | TL3472IP                | Samples |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF TL3472 :**

- Automotive : [TL3472-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device    | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TL3472CDR | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |
| TL3472IDR | SOIC         | D               | 8    | 2500 | 330.0              | 12.4               | 6.4     | 5.2     | 2.1     | 8.0     | 12.0   | Q1            |



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device    | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------|--------------|-----------------|------|------|-------------|------------|-------------|
| TL3472CDR | SOIC         | D               | 8    | 2500 | 340.5       | 336.1      | 25.0        |
| TL3472IDR | SOIC         | D               | 8    | 2500 | 340.5       | 336.1      | 25.0        |

**TUBE**


\*All dimensions are nominal

| Device   | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|----------|--------------|--------------|------|-----|--------|--------|--------|--------|
| TL3472CD | D            | SOIC         | 8    | 75  | 506.6  | 8      | 3940   | 4.32   |
| TL3472CD | D            | SOIC         | 8    | 75  | 507    | 8      | 3940   | 4.32   |
| TL3472CP | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |
| TL3472ID | D            | SOIC         | 8    | 75  | 506.6  | 8      | 3940   | 4.32   |
| TL3472ID | D            | SOIC         | 8    | 75  | 507    | 8      | 3940   | 4.32   |
| TL3472IP | P            | PDIP         | 8    | 50  | 506    | 13.97  | 11230  | 4.32   |



D0008A

# PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

# EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE  
 EXPOSED METAL SHOWN  
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE  
BASED ON .005 INCH [0.125 MM] THICK STENCIL  
SCALE:8X

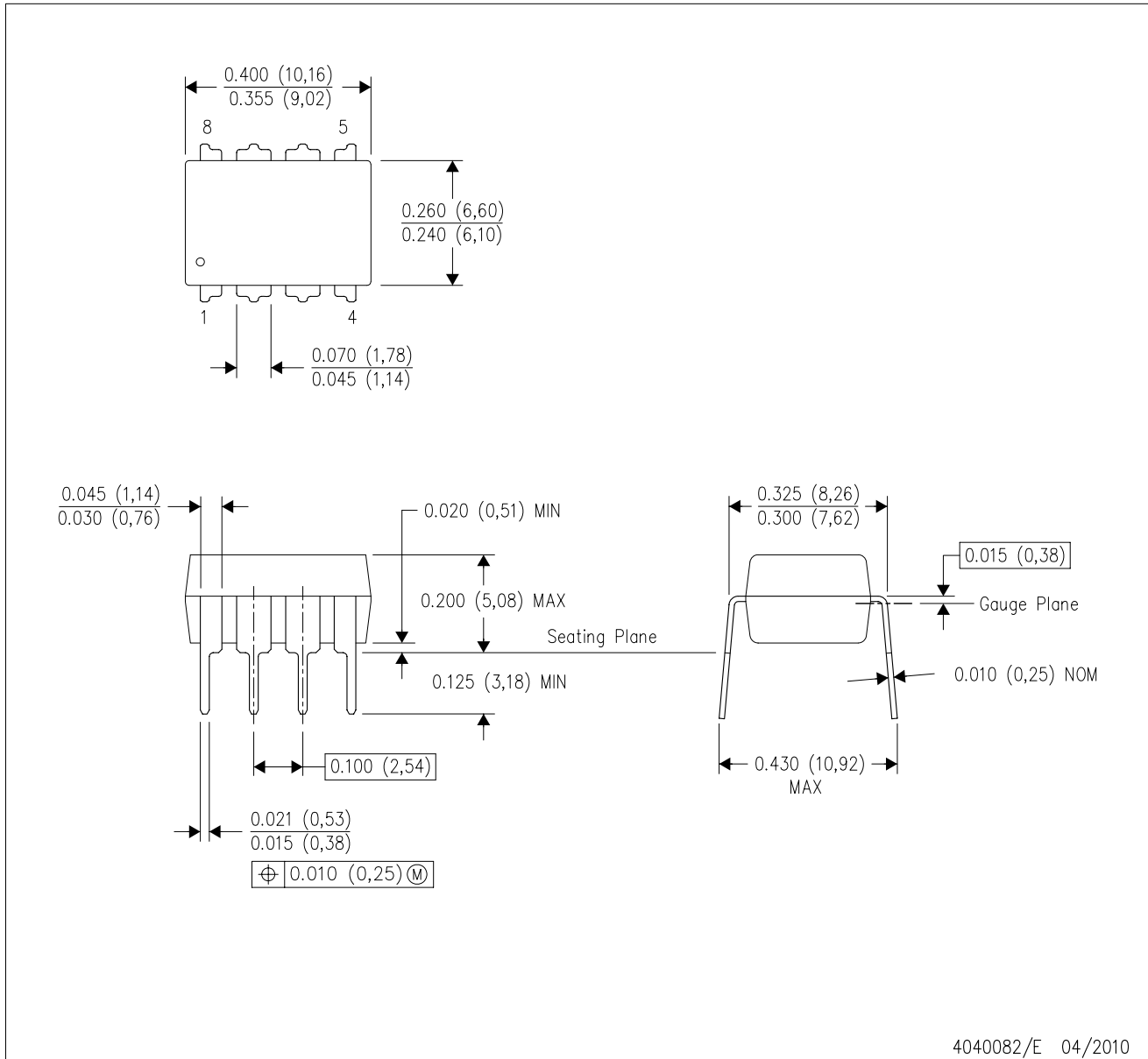
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

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