具有 4 通道分组式延迟的 16 通道、恒定电流 LED 驱动器

查询样品: TLC59282

特性

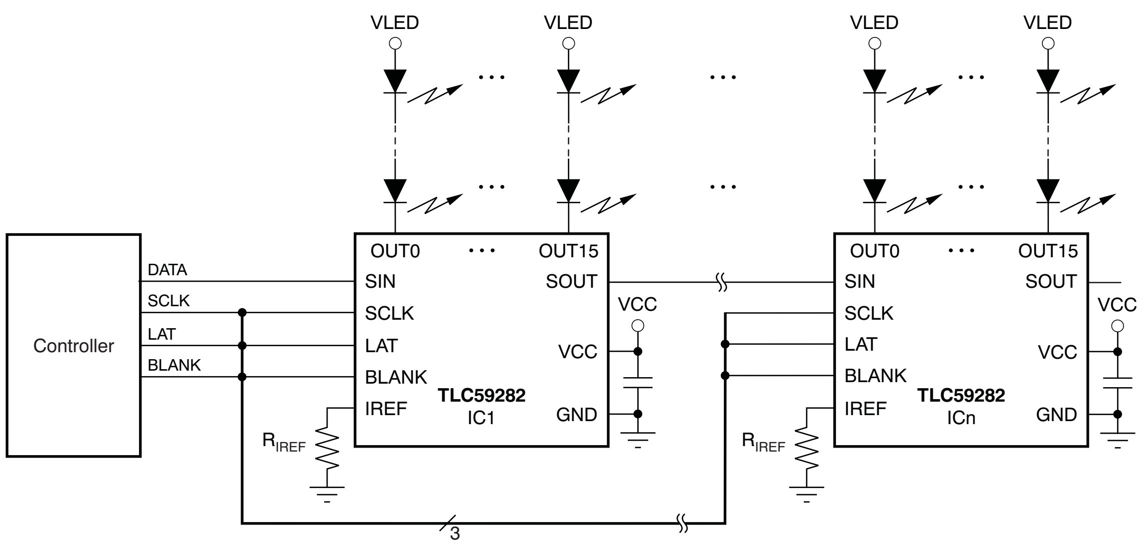
- 具有开/关控制功能的 16 通道、恒定吸收电流输出
- 功能（恒定电流吸收）：
  35mA (V_{CC} ≤ 3.6V)，45mA (V_{CC} > 3.6V)
- LED 电源电压高达 17V
- V_{CC}= 3V 至 5.5V
- 恒定电流准确度:
  - 通道间 = ±0.6% （典型值），±2% （最大值）
  - 器件间 = ±1%（典型值），±3%（最大值）
- 低饱和电压: 在 20 mA (典型值)时，0.31 V
  - T_A = +25℃, 一个通道开启
- CMOS 逻辑电平 I/O
- 数据传输速率： 35 MHz
- 消隐脉冲宽度： 30 ns
- 用于降噪的 4 通道分组式延迟
- 工作温度： －40℃ 至 ＋85℃

应用

- 视频显示器
- 消息板
- 照明

说明

TLC59282 是一款 16 通道、恒定吸收电流驱动器。 每个通道可利用一种与 3.3V 或 5V CMOS 逻辑电平相兼容 （取决于工作 VCC） 的简单串行通信协议进行独立控制。 当串行数据缓冲器被加载时，LATCH 上的一个上升沿将把数据传送至 LEDx 输出端。 BLANK 引脚可用于在加电及输出数据锁存过程中关断所有的 OUTn 输出，以防止在此期间进行无用的图像显示。 所有 16 个通道的恒定电流值均由单个外部电阻器设定。 可以将多个 TLC59282 级联起来，以利用同一个处理器来控制额外的 LED。



典型应用电路（多重菊花链 TLC59282s）

English Data Sheet: SBVS152

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TLC59282	SSOP-24/QSOP-24	TLC59282DBQR	Tape and Reel, 2500
		TLC59282DBQ	Tube, 50
TLC59282	QFN-24	TLC59282RGER	Tape and Reel, 3000
		TLC59282RGE	Tape and Reel, 250

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Over operating free-air temperature range, unless otherwise noted.

PARAMETER			TLC59282	UNIT
V_{CC}	Supply voltage		–0.3 to +6	V
I_{OUT}	Output current (dc)	OUT0 to OUT15	50	mA
V_{IN}	Input voltage range	SIN, SCLK, LAT, BLANK, IREF	–0.3 to V_{CC} + 0.3	V
V_{OUT}	Output voltage range	SOUT	–0.3 to V_{CC} + 0.3	V
		OUT0 to OUT15	–0.3 to +18	V
$T_{J(MAX)}$	Operating junction temperature		+150	°C
T_{STG}	Storage temperature range		–55 to +150	°C
	ESD rating	Human body model (HBM)	4000	V
		Charged device model (CDM)	1000	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) All voltage values are with respect to network ground terminal.

THERMAL INFORMATION

THERMAL METRIC(1)		TLC59282		UNITS
		DBQ	RGE	
		24 PINS	24 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	73.2	46.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	44.6	48.6	
θ_{JB}	Junction-to-board thermal resistance	38.9	23.0	
ψ_{JT}	Junction-to-top characterization parameter	12.3	1.2	
ψ_{JB}	Junction-to-board characterization parameter	39.7	22.9	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	6.3	

(1) 有关传统和新的热度量的更多信息，请参阅 *IC* 封装热度量 应用报告 SPRA953。

RECOMMENDED OPERATING CONDITIONS

At T_A= –40°C to +85°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLC59282 MIN	NOM	MAX	UNIT
DC Characteristics: V_{CC} = 3 V to 5.5 V						
V_{CC}	Supply voltage		3		5.5	V
V_O	Voltage applied to output	OUT0 to OUT15			17	V
V_{IH}	High-level input voltage		0.7 × V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage		GND		0.3 × V_{CC}	V
I_{OH}	High-level output current	SOUT			–1	mA
I_{OL}	Low-level output current	SOUT			1	mA
I_{OLC}	Constant output sink current	OUT0 to OUT15, 3 V ≤ V_{CC} < 3.6 V	2		35	mA
		OUT0 to OUT15, 3.6 V ≤ V_{CC} < 5.5 V	2		45	mA
T_A	Operating free-air temperature range		–40		+85	°C
T_J	Operating junction temperature range		–40		+125	°C
AC Characteristics: V_{CC} = 3 V to 5.5 V						
$f_{CLK\ (SCLK)}$	Data shift clock frequency	SCLK			35	MHz
T_{WH0}	Pulse duration	SCLK	10			ns
T_{WL0}		SCLK	10			ns
T_{WH1}		LAT	20			ns
T_{WH2}		BLANK	60			ns
T_{WL2}		BLANK	30			ns
T_{SU0}	Setup time	SIN–SCLK↑	4			ns
T_{SU1}		LAT↓–SCLK↑	10			ns
T_{H0}	Hold time	SIN–SCLK↑	4			ns
T_{H1}		LAT↓–SCLK↑	10			ns

ELECTRICAL CHARACTERISTICS

At V_{CC} = 3 V to 5.5 V and T_A = –40°C to +85°C. Typical values at V_{CC} = 3.3 V and T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLC59282 MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA at SOUT	V_{CC} – 0.4		V_{CC}	V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA at SOUT			0.4	V
I_{IN}	Input current	V_{IN} = V_{CC} or GND at SIN and SCLK	–1		1	µA
I_{CC0}	Supply current (V_{CC})	SIN/SCLK/LAT = low, BLANK = high, V_{OUTn} = 1 V, R_{IREF} = open		0.1	1	mA
I_{CC1}		SIN/SCLK/LAT = low, BLANK = high, V_{OUTn} = 1 V, R_{IREF} = 3 kΩ (I_{OUT} = 16.8 mA target)		4.5	6	mA
I_{CC2}		All OUTn = ON, SIN/SCLK/LAT/BLANK = low, V_{OUTn} = 1 V, R_{IREF} = 3 kΩ		7	15	mA
I_{CC3}		All OUTn = ON, SIN/SCLK/LAT/BLANK = low, V_{OUTn} = 1 V, R_{IREF} = 1.5 kΩ (I_{OUT} = 33.6mA target)		16	34	mA
I_{OLC}	Constant output current	All OUTn = ON, V_{OUTn} = V_{OUTfix} = 1 V, R_{IREF} = 1.5 kΩ at OUT0 to OUT15 (see Figure 6), T_A = +25°C	32.1	33.7	35.3	mA
I_{OLKG}	Output leakage current	OUTn = OFF, V_{OUTn} = V_{OUTfix} = 17 V, BLANK = high, R_{IREF} = 1.5 kΩ at OUT0 to OUT15 (see Figure 6)			0.1	µA
ΔI_{OLC0}	Constant-current error (channel-to-channel)(1)	All OUTn = ON, V_{OUTn} = V_{OUTfix} = 1 V, R_{IREF} = 1.5 kΩ at OUT0 to OUT15		±0.6	±2	%
ΔI_{OLC1}	Constant-current error (device-to-device)(2)	All OUTn = ON, V_{OUTn} = V_{OUTfix} = 1 V, R_{IREF} = 1.5 kΩ at OUT0 to OUT15, T_A = +25°C		±1	±3	%
ΔI_{OLC2}	Line regulation(3)	All OUTn = ON, V_{OUTn} = V_{OUTfix} = 1 V, R_{IREF} = 1.5 kΩ at OUT0 to OUT15, V_{CC} = 3 V to 5.5 V		±0.5	±1	%/V
ΔI_{OLC3}	Load regulation(4)	All OUTn = ON, V_{OUTn} = 1 V to 3V, V_{OUTfix} = 1 V, R_{IREF} = 1.5 kΩ		±1	±3	%/V
V_{IREF}	Reference voltage output	R_{IREF} = 1.5 kΩ, T_A = +25°C	1.18	1.205	1.23	V
R_{PUP}	Pull-up resistor	BLANK	250	500	750	kΩ
R_{PDWN}	Pull-down resistor	LAT	250	500	750	kΩ

(1) The deviation of each output from the average of OUT0–OUT15 constant-current. Deviation is calculated by the formula:

$$\Delta (\%) = \left(\frac{I_{OUTn}}{\frac{(I_{OUT0} + I_{OUT1} + \ldots + I_{OUT14} + I_{OUT15})}{16}} - 1 \right) \times 100$$

(2) The deviation of the OUT0–OUT15 constant-current average from the ideal constant-current value. Deviation is calculated by the following formula:

$$\Delta (\%) = \left(\frac{\frac{(I_{OUT0} + I_{OUT1} + \ldots I_{OUT14} + I_{OUT15})}{16} - (\text{Ideal Output Current})}{\text{Ideal Output Current}} \right) \times 100$$

Ideal current is calculated by the formula:

$$I_{OUT(IDEAL)} = 41.9 \times \left(\frac{1.205}{R_{IREF}} \right)$$

(3) Line regulation is calculated by this equation:

$$\Delta (\%/V) = \left(\frac{(I_{OUTn} \text{ at } V_{CC} = 5.5\text{ V}) - (I_{OUTn} \text{ at } V_{CC} = 3\text{ V})}{(I_{OUTn} \text{ at } V_{CC} = 3\text{ V})} \right) \times \frac{100}{5.5\text{ V} - 3\text{ V}}$$

(4) Load regulation is calculated by the equation:

$$\Delta (\%/V) = \left(\frac{(I_{OUTn} \text{ at } V_{OUTn} = 3\text{ V}) - (I_{OUTn} \text{ at } V_{OUTn} = 1\text{ V})}{(I_{OUTn} \text{ at } V_{OUTn} = 1\text{ V})} \right) \times \frac{100}{3\text{ V} - 1\text{ V}}$$

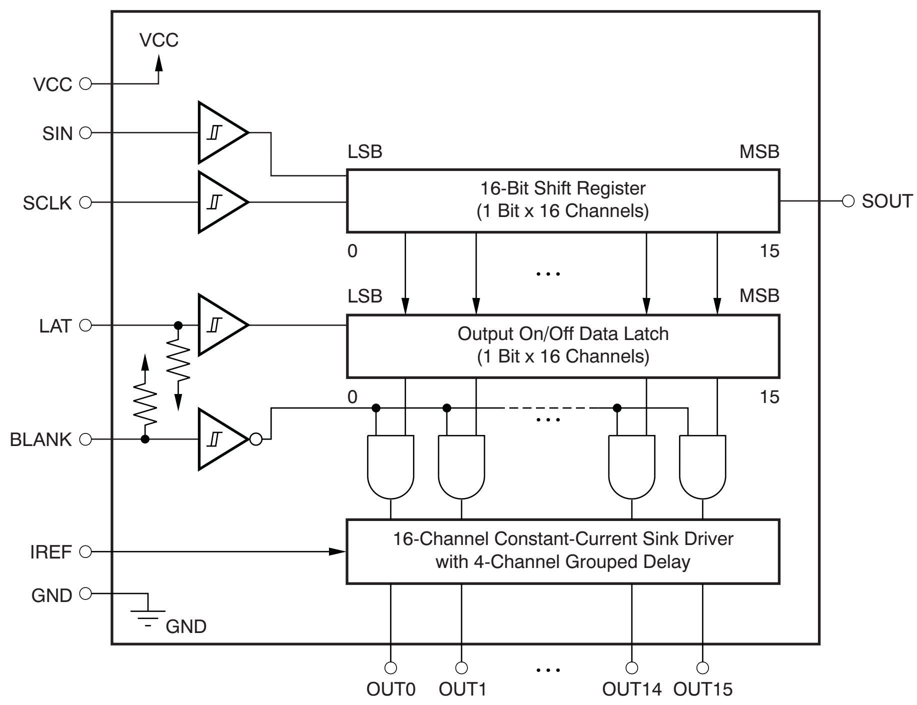
SWITCHING CHARACTERISTICS

At V_{CC} = 3 V to 5.5 V, T_A = –40°C to +85°C, C_L = 15 pF, R_L = 130 Ω, R_{IREF} = 1.5 kΩ, and V_{LED} = 5.5 V. Typical values at V_{CC} = 3.3 V and T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLC59282 MIN	TLC59282 TYP	TLC59282 MAX	UNIT
t_{R0}	Rise time	SOUT (see Figure 5)		5	12	ns
t_{R1}	Rise time	OUTn (see Figure 4)		10	30	ns
t_{F0}	Fall time	SOUT (see Figure 5)		5	12	ns
t_{F1}	Fall time	OUTn (see Figure 4)		10	30	ns
t_{D0}	Propagation delay time	SCLK↑ to SOUT↑↓		8	20	ns
t_{D1}	Propagation delay time	LAT↑ or BLANK↑↓ to OUT0/OUT7/OUT8/OUT15 on/off		18	36	ns
t_{D2}	Propagation delay time	LAT↑ or BLANK↑↓ to OUT1/OUT6/OUT9/OUT14 on/off		38	69	ns
t_{D3}	Propagation delay time	LAT↑ or BLANK↑↓ to OUT2/OUT5/OUT10/OUT13 on/off		58	102	ns
t_{D4}	Propagation delay time	LAT↑ or BLANK↑↓ to OUT3/OUT4/OUT11/OUT12 on/off		78	135	ns
t_{ON_ERR}	Output on-time error (1)	On/off latch data = all '1', 30 ns BLANK low level one-shot pulse input	–15		15	ns

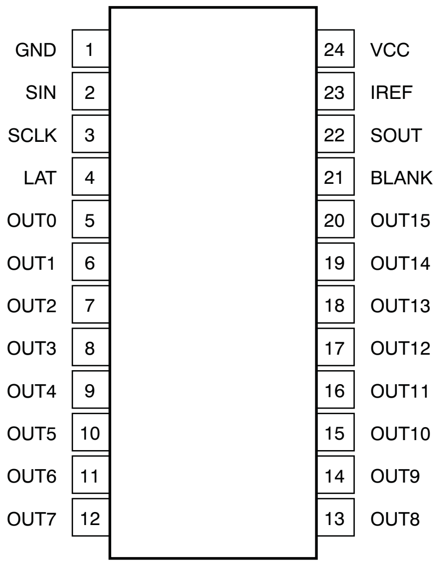
(1) Output on-time error (t_{ON_ERR}) is calculated by the formula: t_{ON_ERR} (ns) = t_{OUT_ON} – BLANK low level one-shot pulse width (T_{WL2}). t_{OUT_ON} indicates the actual on-time of the constant-current output.

FUNCTIONAL BLOCK DIAGRAM

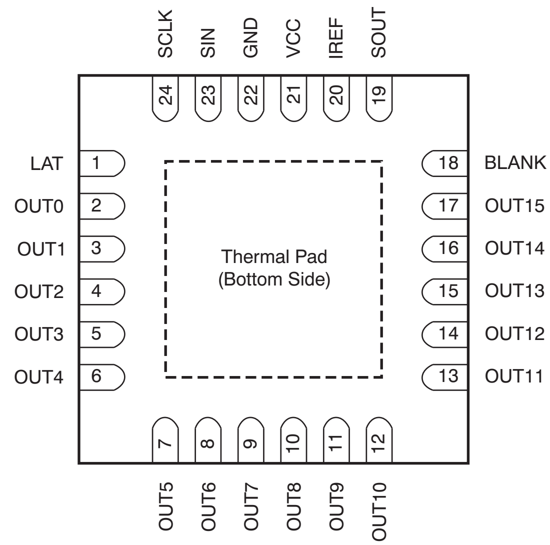


DEVICE INFORMATION

SSOP-24/QSOP-24
DBQ PACKAGE
(TOP VIEW)



QFN-24
RGE PACKAGE
(TOP VIEW)



NOTE: Thermal pad is not connected to GND internally. The thermal pad must be connected to GND via the PCB pattern.

TERMINAL FUNCTIONS

TERMINAL				
NAME	**DBQ**	**RGE**	**I/O**	**DESCRIPTION**
SIN	2	23	I	Serial data input for driver on/off control; Schmitt buffer input. When SIN is high, data '1' are written into the LSB of the 16-bit shift register at the SCLK rising edge.
SCLK	3	24	I	Serial data shift clock; Schmitt buffer input. All data in the 16-bit shift register are shifted toward the MSB by 1-bit synchronization of SCLK.
LAT	4	1	I	Level triggered latch; Schmitt buffer input. The data in the 16-bit shift register continue to transfer to the output on/off data latch while LAT is high. Therefore, if the data in the 16-bit shift register are changed when LAT is high, the data in the data latch are also changed. The data in the data latch are held when LAT is low. This pin is internally pulled down to GND with a 500 kΩ (typ) resistor.
BLANK	21	18	I	Blank, all outputs; Schmitt buffer input. When BLANK is high, all constant-current outputs (OUT0–OUT15) are forced off. When BLANK is low, all constant-current outputs are controlled by the data in the output on/off data latch. This pin is internally pulled up to V_{CC} with a 500 kΩ (typ) resistor.
IREF	23	20	I/O	Constant-current value setting, OUT0–OUT15 sink constant-current is set to desired value by connection to an external resistor between IREF and GND.
SOUT	22	19	O	Serial data output. This output is connected to the MSB of the 16-bit shift register. SOUT data changes at the rising edge of SCLK.
OUT0	5	2	O	Constant-current output. Each output can be tied together with others to increase the constant-current. Different voltages can be applied to each output.
OUT1	6	3	O	Constant-current output
OUT2	7	4	O	Constant-current output
OUT3	8	5	O	Constant-current output
OUT4	9	6	O	Constant-current output
OUT5	10	7	O	Constant-current output
OUT6	11	8	O	Constant-current output
OUT7	12	9	O	Constant-current output
OUT8	13	10	O	Constant-current output
OUT9	14	11	O	Constant-current output
OUT10	15	12	O	Constant-current output
OUT11	16	13	O	Constant-current output
OUT12	17	14	O	Constant-current output
OUT13	18	15	O	Constant-current output
OUT14	19	16	O	Constant-current output
OUT15	20	17	O	Constant-current output
VCC	24	21	—	Power-supply voltage
GND	1	22	—	Power ground

PARAMETER MEASUREMENT INFORMATION

PIN EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

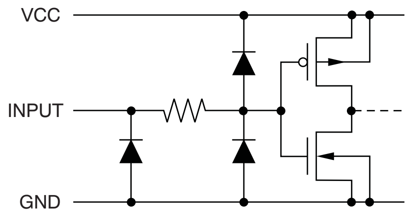


Figure 1. SIN, SCLK, LAT, BLANK

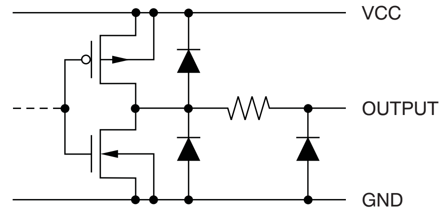


Figure 2. SOUT

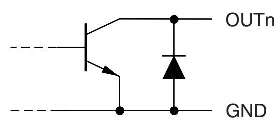
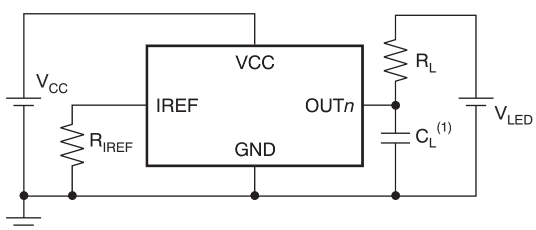


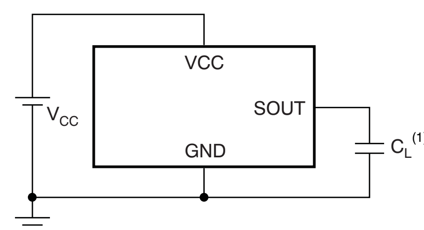
Figure 3. OUT0 Through OUT15

TEST CIRCUITS



(1) C_L includes measurement probe and jig capacitance.

Figure 4. Rise Time and Fall Time Test Circuit for OUTn



(1) C_L includes measurement probe and jig capacitance.

Figure 5. Rise Time and Fall Time Test Circuit for SOUT

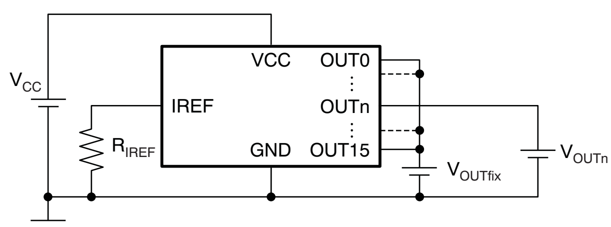
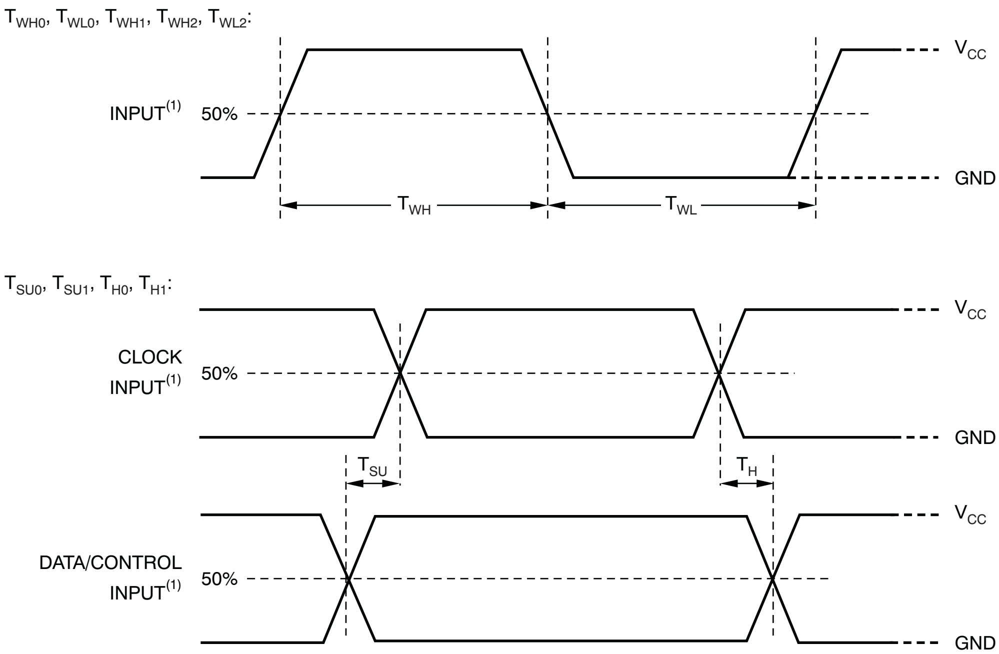


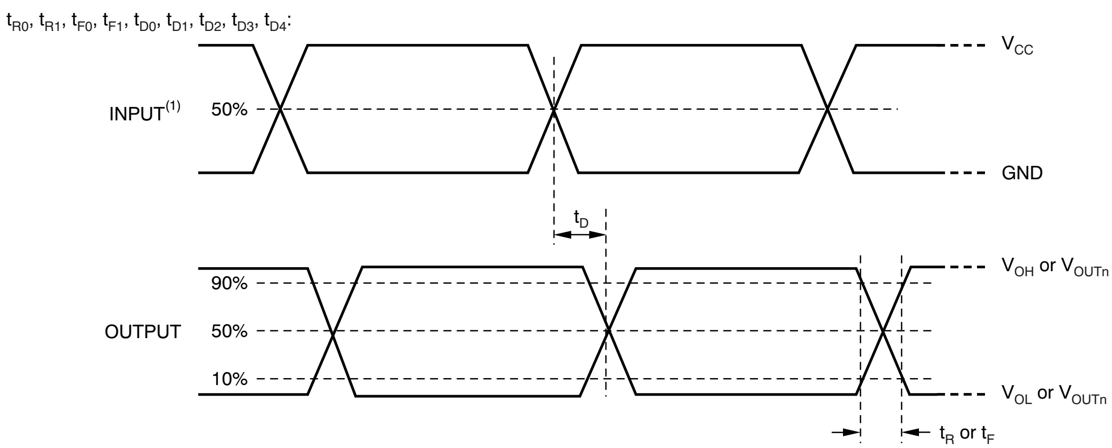
Figure 6. Constant-Current Test Circuit for OUTn

TIMING DIAGRAMS



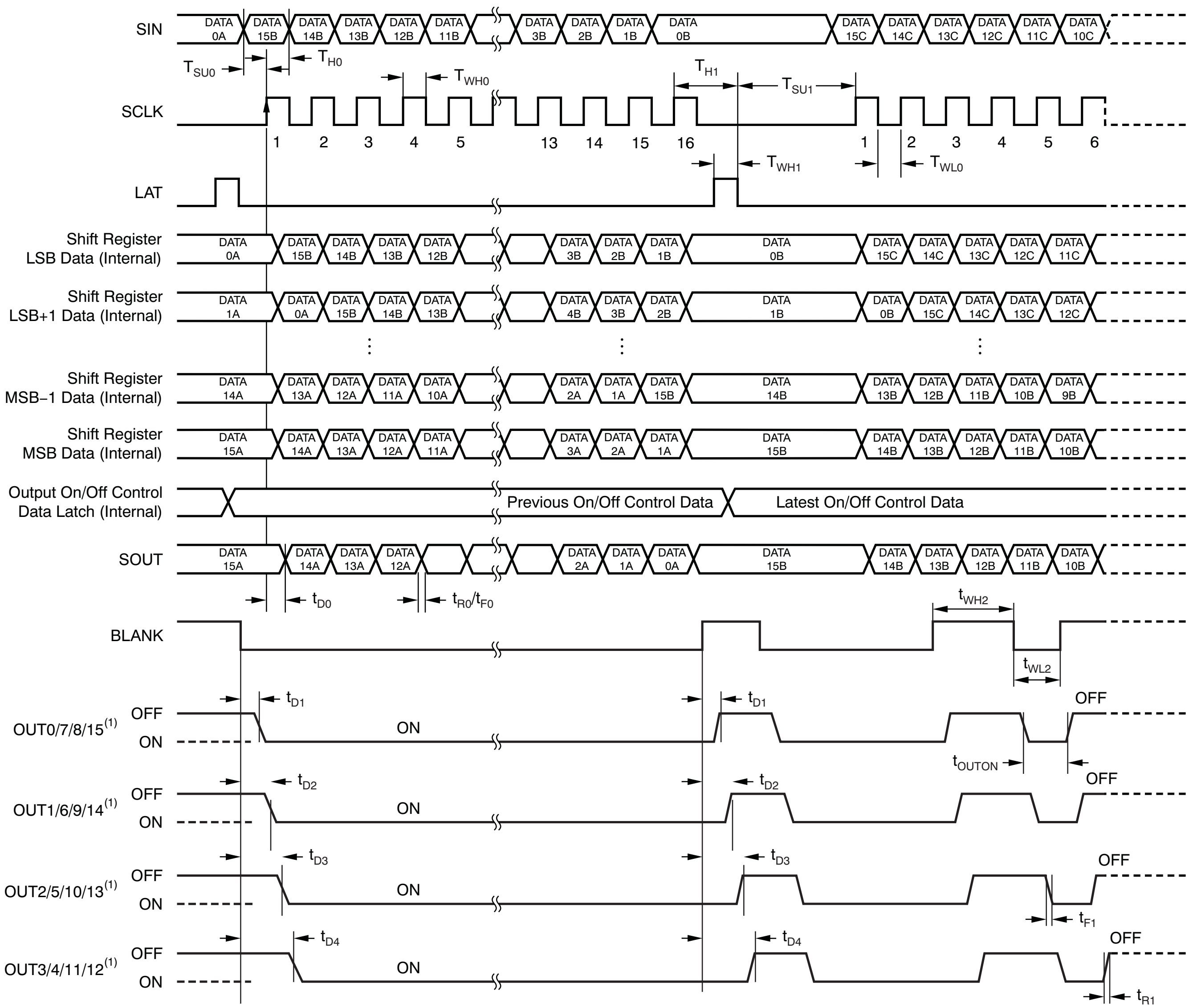
(1) Input pulse rise and fall time is 1 ns to 3 ns.

Figure 7. Input Timing



(1) Input pulse rise and fall time is 1 ns to 3 ns.

Figure 8. Output Timing



(1) Output on/off data = FFFFh.

(2) $t_{ON\_ERR} = t_{OUTON} - T_{WL2}$.

Figure 9. Timing Diagram

TYPICAL CHARACTERISTICS

At V_{CC} = 3.3 V and T_A = +25°C, unless otherwise noted.

REFERENCE RESISTOR vs OUTPUT CURRENT

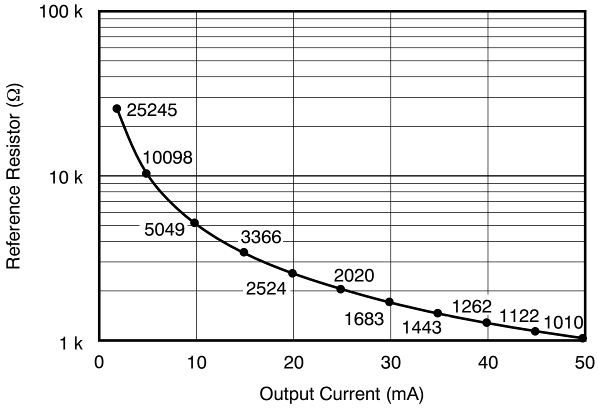


Figure 10.

OUTPUT CURRENT vs OUTPUT VOLTAGE

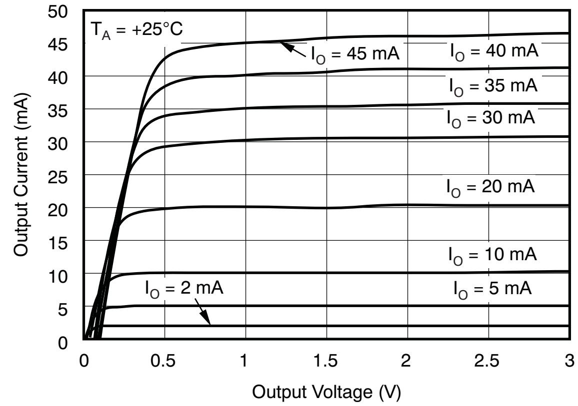


Figure 11.

OUTPUT CURRENT vs OUTPUT VOLTAGE

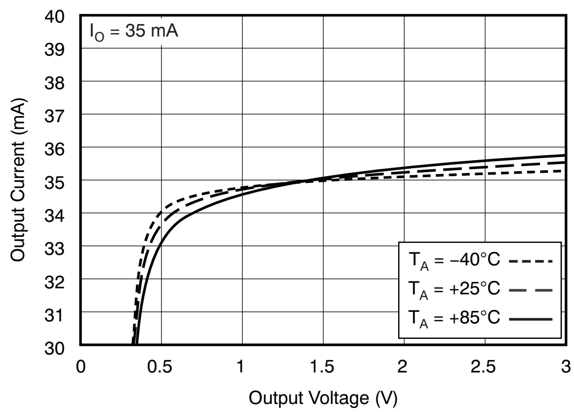


Figure 12.

ΔI_{OLC} vs AMBIENT TEMPERATURE

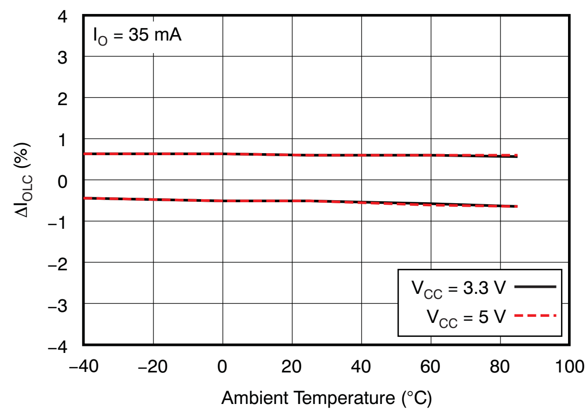


Figure 13.

ΔI_{OLC} vs OUTPUT CURRENT

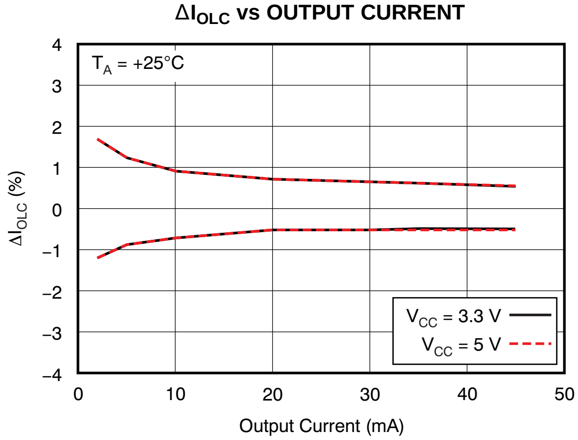


Figure 14.

CONSTANT-CURRENT OUTPUT VOLTAGE WAVEFORM

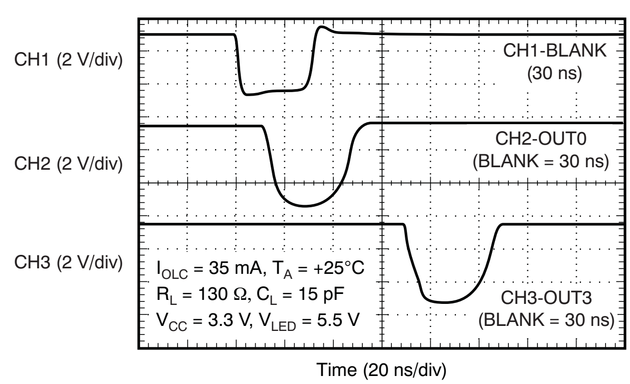


Figure 15.

DETAILED DESCRIPTION

SETTING FOR THE CONSTANT SINK CURRENT VALUE

The constant-current values are determined by an external resistor (R_{IREF}) placed between IREF and GND. The resistor (R_{IREF}) value is calculated by Equation 1.

$$R_{IREF}\ (k\Omega) = \frac{V_{IREF}\ (V)}{I_{OLC}\ (mA)} \times 41.9$$

Where:

V_{IREF} = the internal reference voltage on the IREF pin (typically 1.205 V) (1)

I_{OLC} must be set in the range of 2 mA to 35 mA when V_{CC} is less than 3.6 V. Also, when V_{CC} is equal to 3.6 V or greater, I_{OLC} must be set in the range of 2 mA to 45 mA. The constant sink current characteristic for the external resistor value is shown in Figure 10. Table 1 describes the constant-current output versus external resistor value.

Table 1. Constant-Current Output versus External Resistor Value

I_{OLC} (mA, Typical)	R_{IREF} (kΩ)
45 (V_{CC} > 3.6 V only)	1.12
40 (V_{CC} > 3.6 V only)	1.26
35	1.44
30	1.68
25	2.02
20	2.52
15	3.37
10	5.05
5	10.1
2	25.2

CONSTANT-CURRENT DRIVER ON/OFF CONTROL

When BLANK is low, the corresponding output is turned on if the data in the on/off control data latch are '1' and remains off if the data are '0'. When BLANK is high, all outputs are forced off. This control is shown in Table 2.

Table 2. On/Off Control Data Truth Table

OUTPUT ON/OFF DATA	CONSTANT-CURRENT OUTPUT STATUS
0	Off
1	On

When the IC is initially powered on, the data in the 16-bit shift register and output on/off data latch are not set to the respective default value. Therefore, the output on/off data must be written to the data latch before turning the constant-current output on. BLANK should be at a high level when powered on because the constant-current may be turned on as a result of random data in the output on/off data latch.

The output on/off data corresponding to any unconnected OUTn outputs should be set to '0' before turning on the remaining outputs. Otherwise, the supply current (I_{CC}) increases while the LEDs are on.

REGISTER CONFIGURATION

The TLC59282 has a 16-bit shift register and an output on/off data latch. Both the shift register and data latch are 16 bits long and are used to turn the constant-current outputs on and off. Figure 16 shows the shift register and data latch configuration. The data at the SIN pin are shifted in to the LSB of the 16-bit shift register at the rising edge of the SCLK pin; SOUT data change at the rising edge of SCLK.

The output on/off data in the 16-bit shift register continue to transfer to the output on/off data latch while LAT is high. Therefore, if the data in the 16-bit shift register are changed when LAT is high, the data in the data latch are also changed. The data in the data latch are held when LAT is low. When the IC initially powers on, the data in the output on/off shift register and latch are not set to the default values; on/off control data must be written to the on/off control data latch before turning the constant-current output on. BLANK should be high when the IC is powered on because the constant-current may be turned on at that time as a result of random values in the on/off data latch. All constant-current outputs are forced off when BLANK is high. The OUTn on/off are controlled by the data in the output on/off data latch. The timing diagram and truth table for writing data are shown in Figure 17 and Table 3.

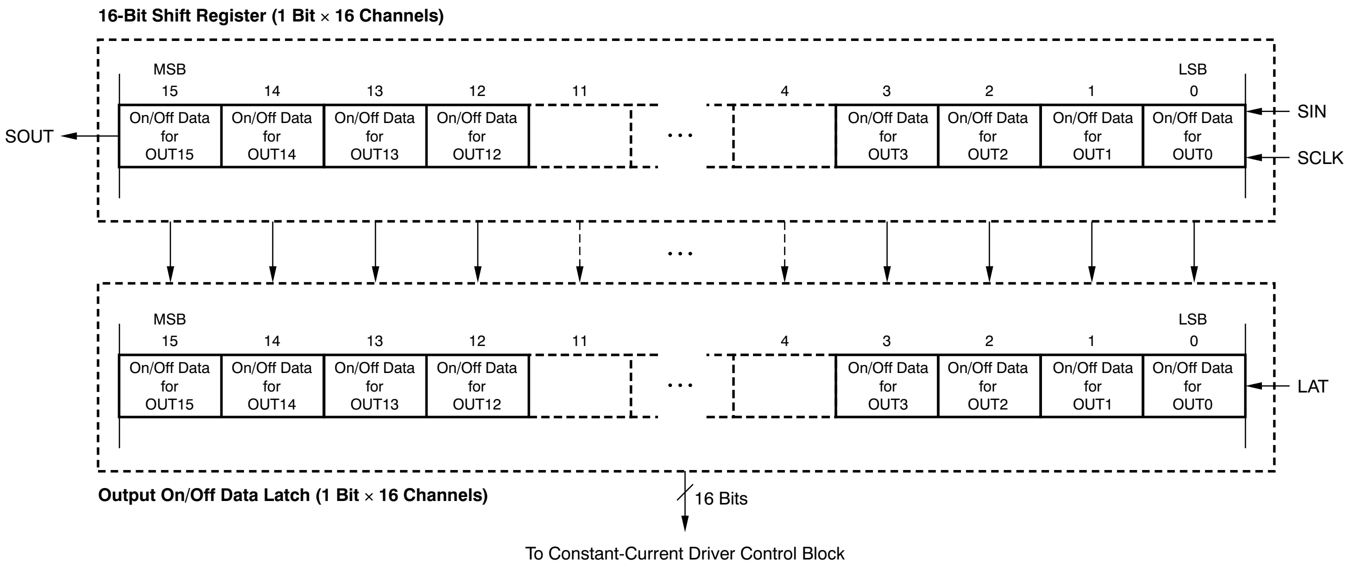


Figure 16. 16-Bit Shift Register and Output On/Off Data Latch Configuration

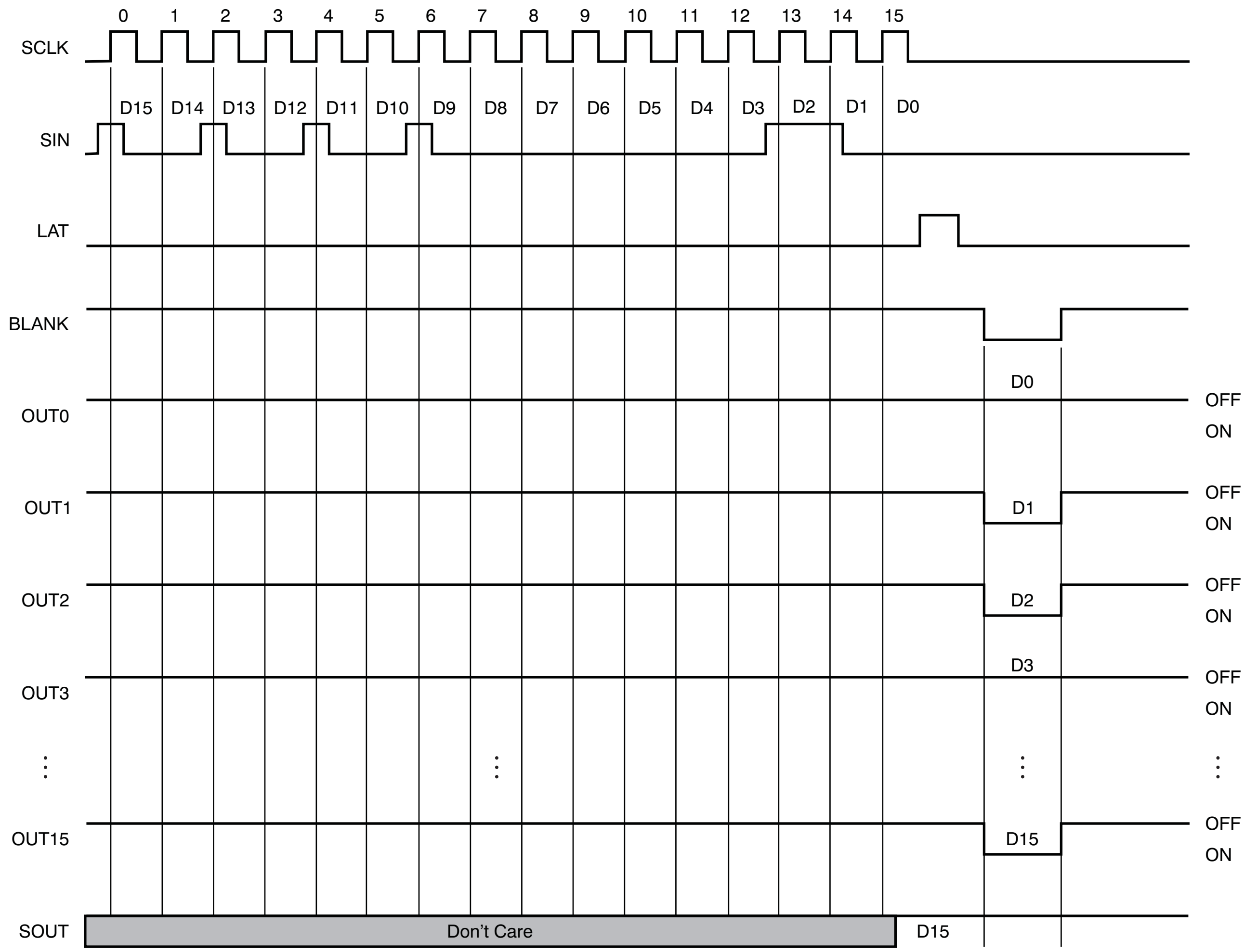


Figure 17. Operation Timing Diagram

Table 3. Truth Table in Operation

SCLK	LAT	BLANK	SIN	OUT0…OUT7…OUT15	SOUT
↑	High	Low	Dn	Dn…Dn – 7…Dn – 15	Dn – 15
↑	Low	Low	Dn + 1	No change	Dn – 14
↑	High	Low	Dn + 2	Dn + 2…Dn – 5…Dn – 13	Dn – 13
↓	—	Low	Dn + 3	Dn + 2…Dn – 5…Dn – 13	Dn – 13
↓	—	High	Dn + 3	Off	Dn – 13

NOISE REDUCTION

Large surge currents may flow through the IC and the board if all 16 outputs turn on or off simultaneously. These large current surges could induce detrimental noise and electromagnetic interference (EMI) into other circuits. The TLC59282 independently turns on or off the outputs for each color group with a 20 ns (typ) delay time; see Figure 9. The output current sinks are grouped into four groups. The first group that is turned on/off are OUT0/7/8/15; the second group that is turned on/off are OUT1/6/9/14; the third group that is turned on/off are OUT2/5/10/13; and the fourth group is OUT3/4/11/12. Both turn-on and turn-off are delayed. However, the state of each output is controlled by the data in the output on-off data latch and BLANK level.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (July 2011) to Revision C **Page**

Changes from Revision A (December 2010) to Revision B **Page**

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC59282DBQ	ACTIVE	SSOP	DBQ	24	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC59282	Samples
TLC59282DBQR	ACTIVE	SSOP	DBQ	24	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC59282	Samples
TLC59282RGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 59282	Samples
TLC59282RGET	ACTIVE	VQFN	RGE	24	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TLC 59282	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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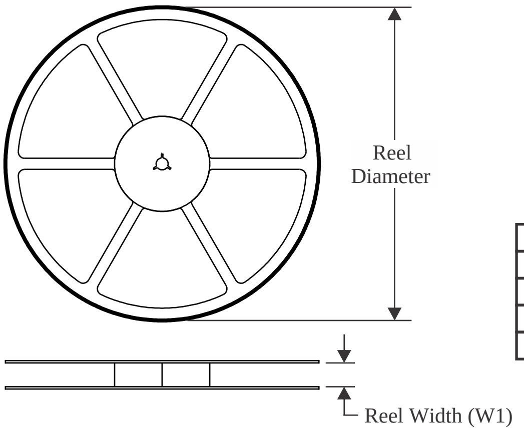
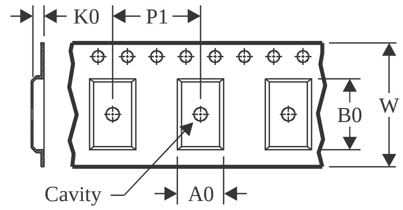
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

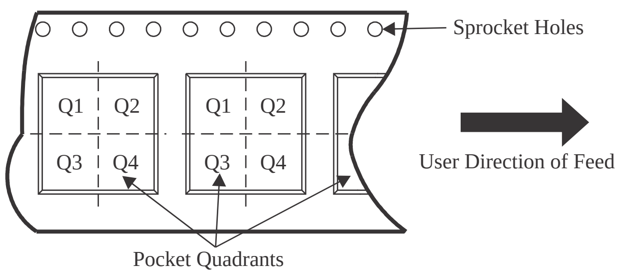


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

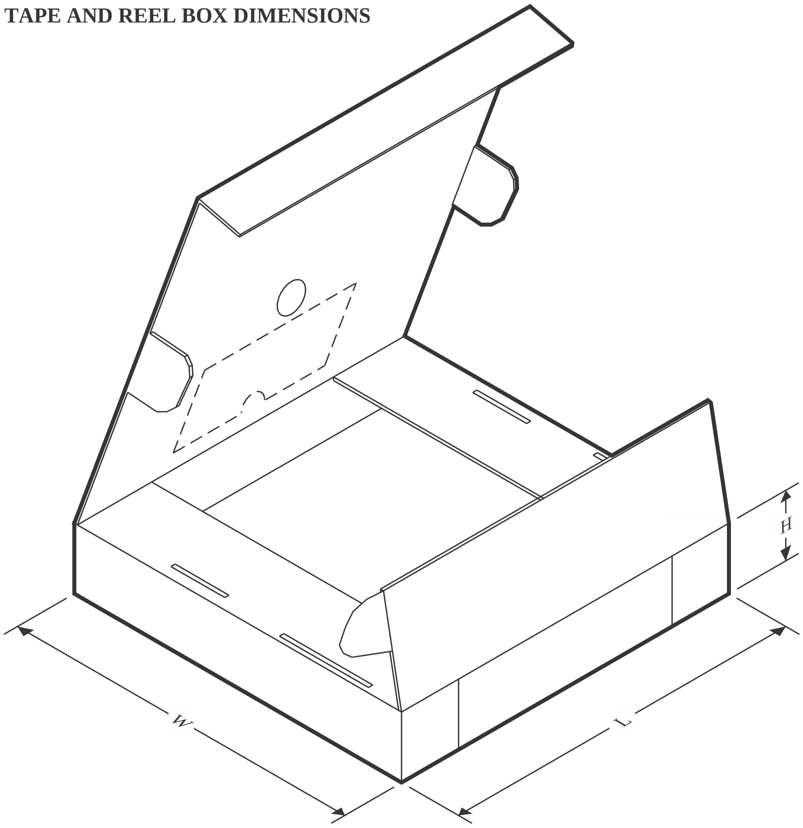
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC59282DBQR	SSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC59282RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TLC59282RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

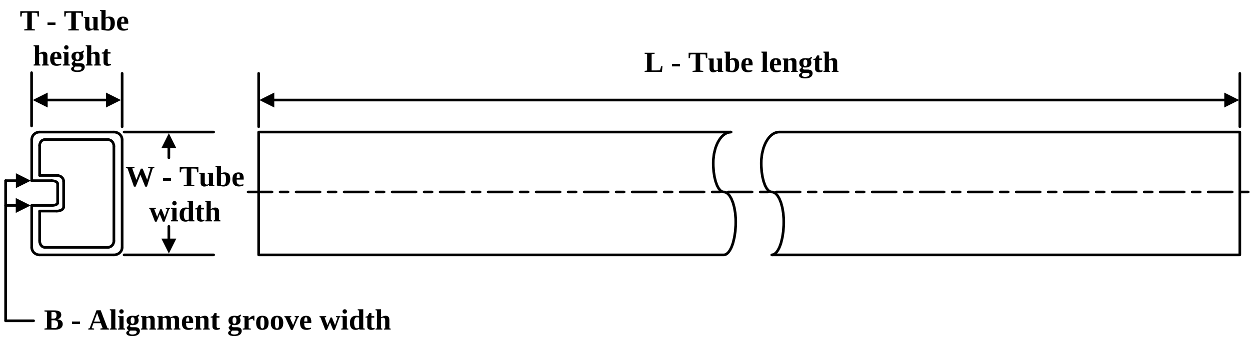
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

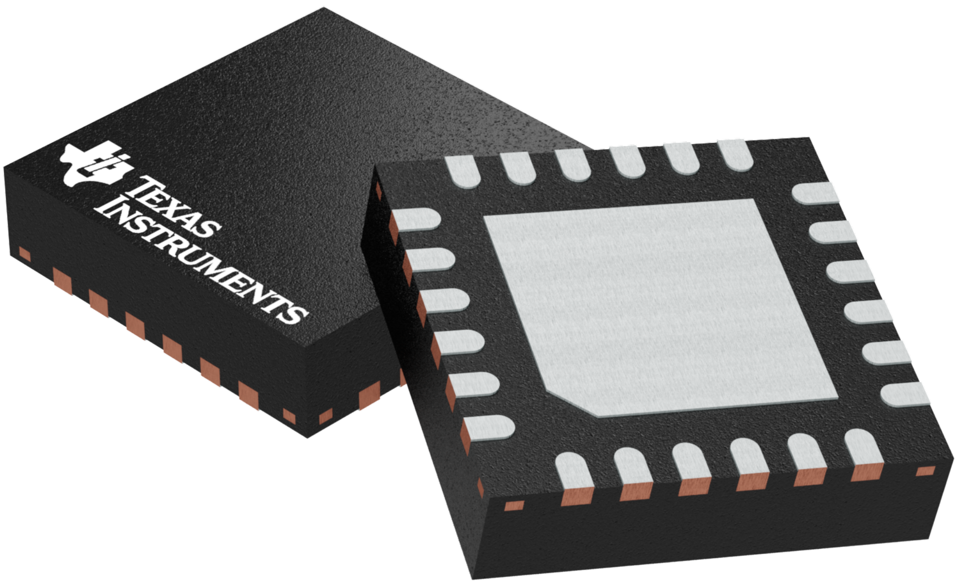
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC59282DBQR	SSOP	DBQ	24	2500	367.0	367.0	38.0
TLC59282RGER	VQFN	RGE	24	3000	356.0	356.0	35.0
TLC59282RGET	VQFN	RGE	24	250	210.0	185.0	35.0

TUBE

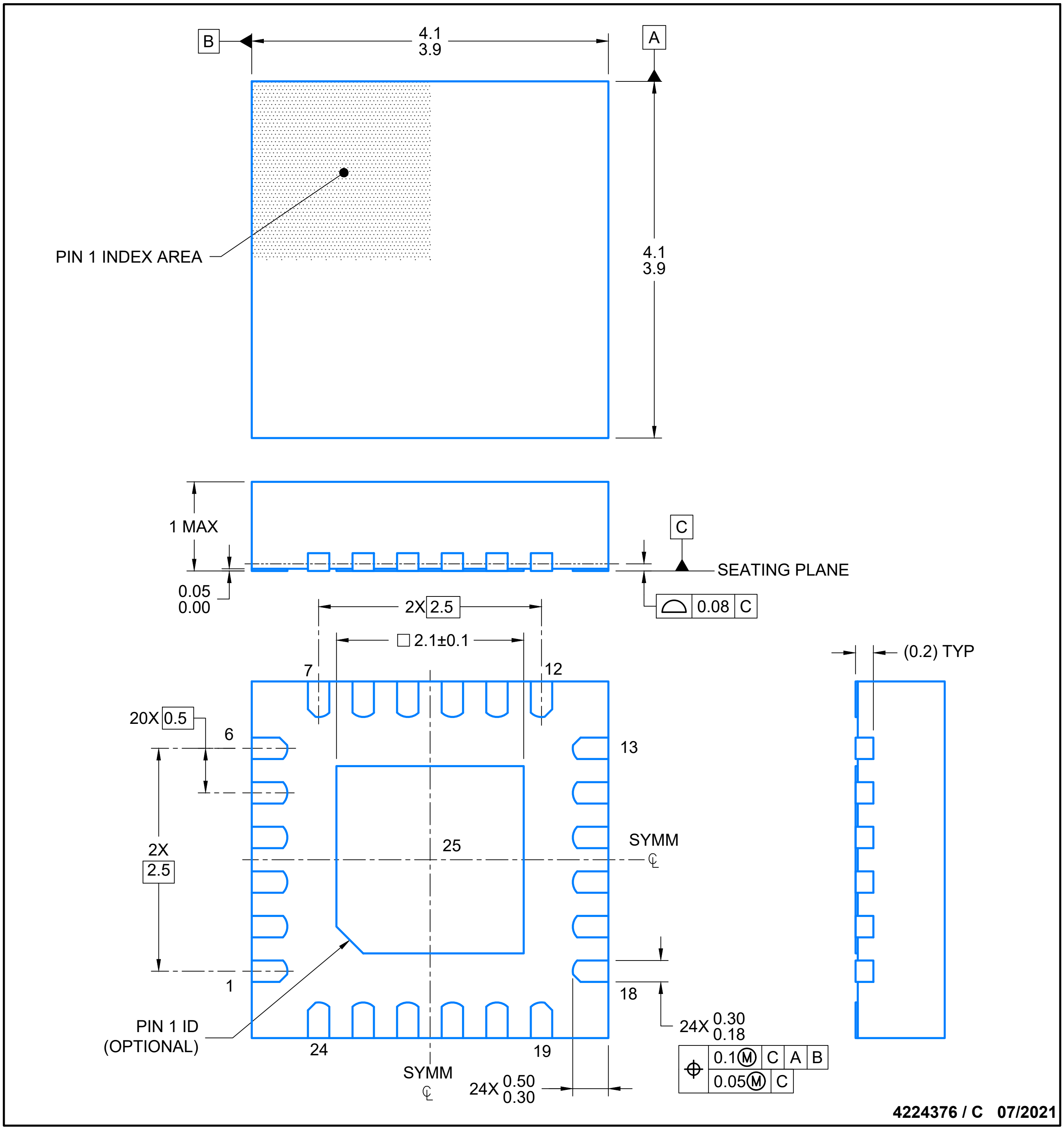


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC59282DBQ	DBQ	SSOP	24	50	506.6	8	3940	4.32

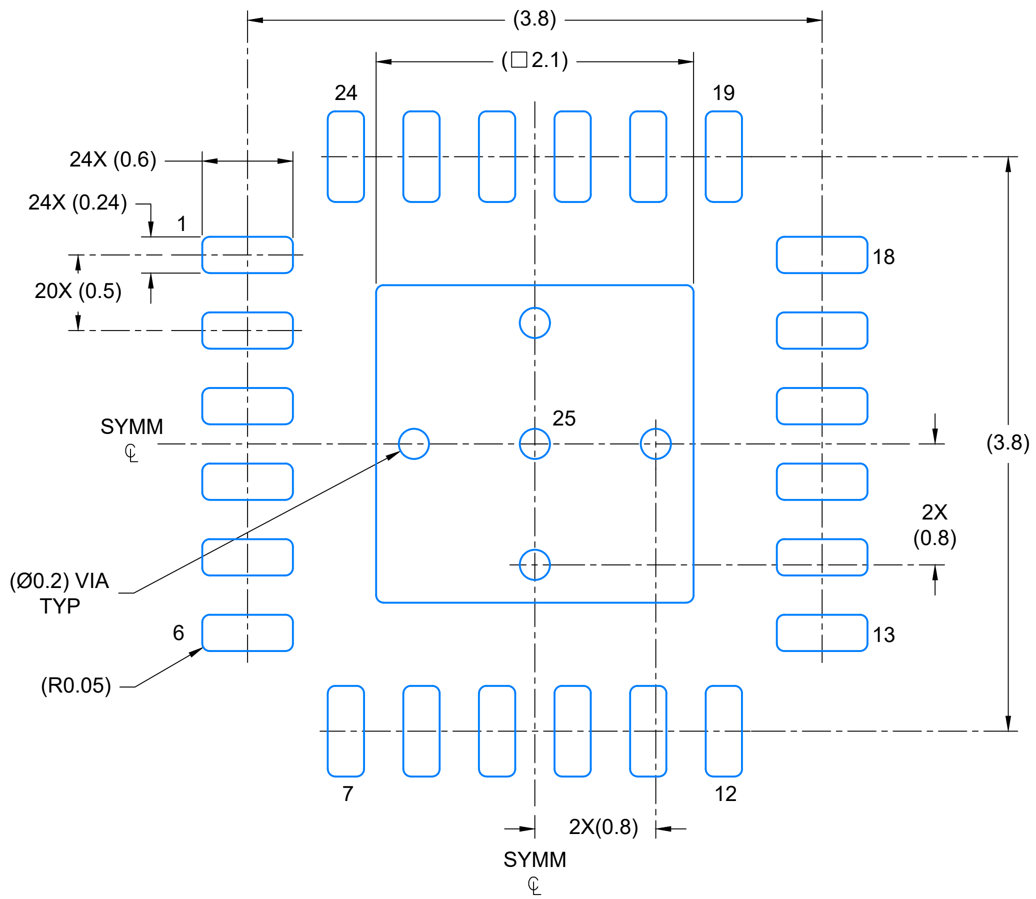


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

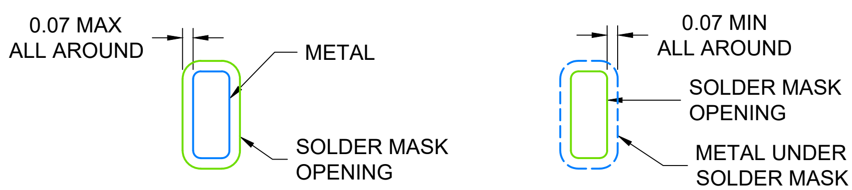


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE: 20X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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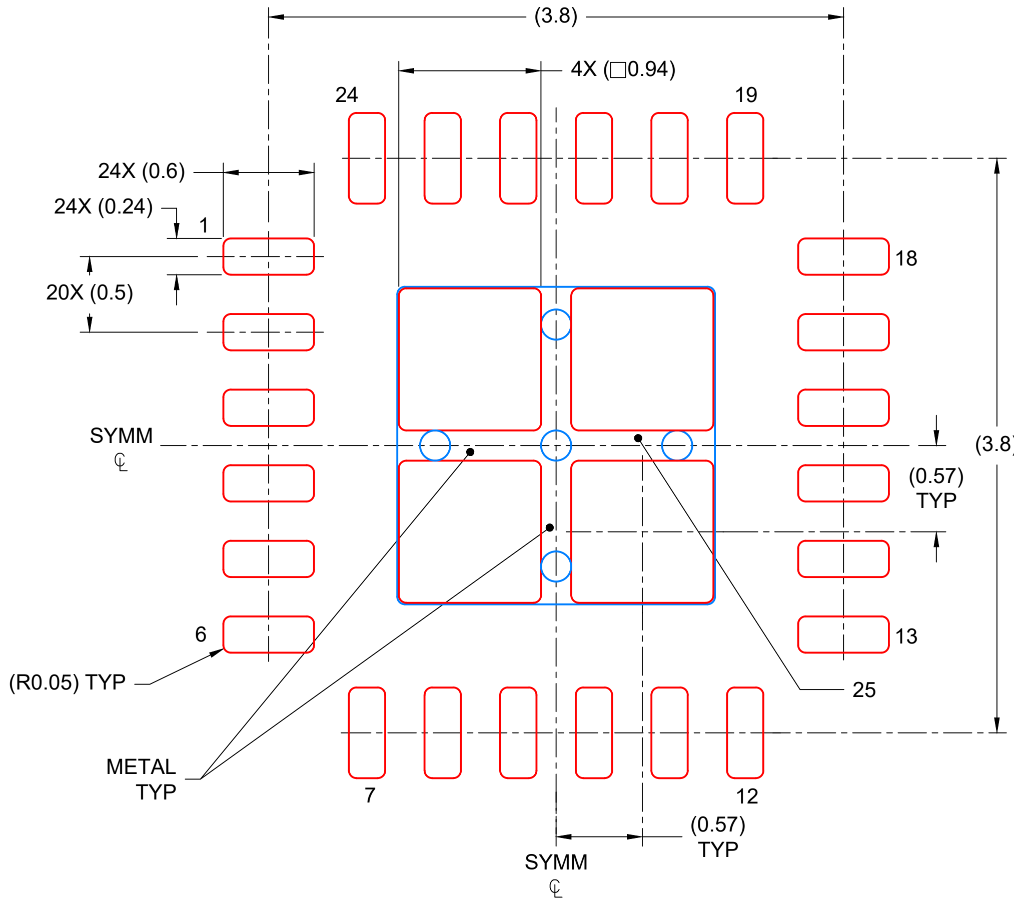
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 20X

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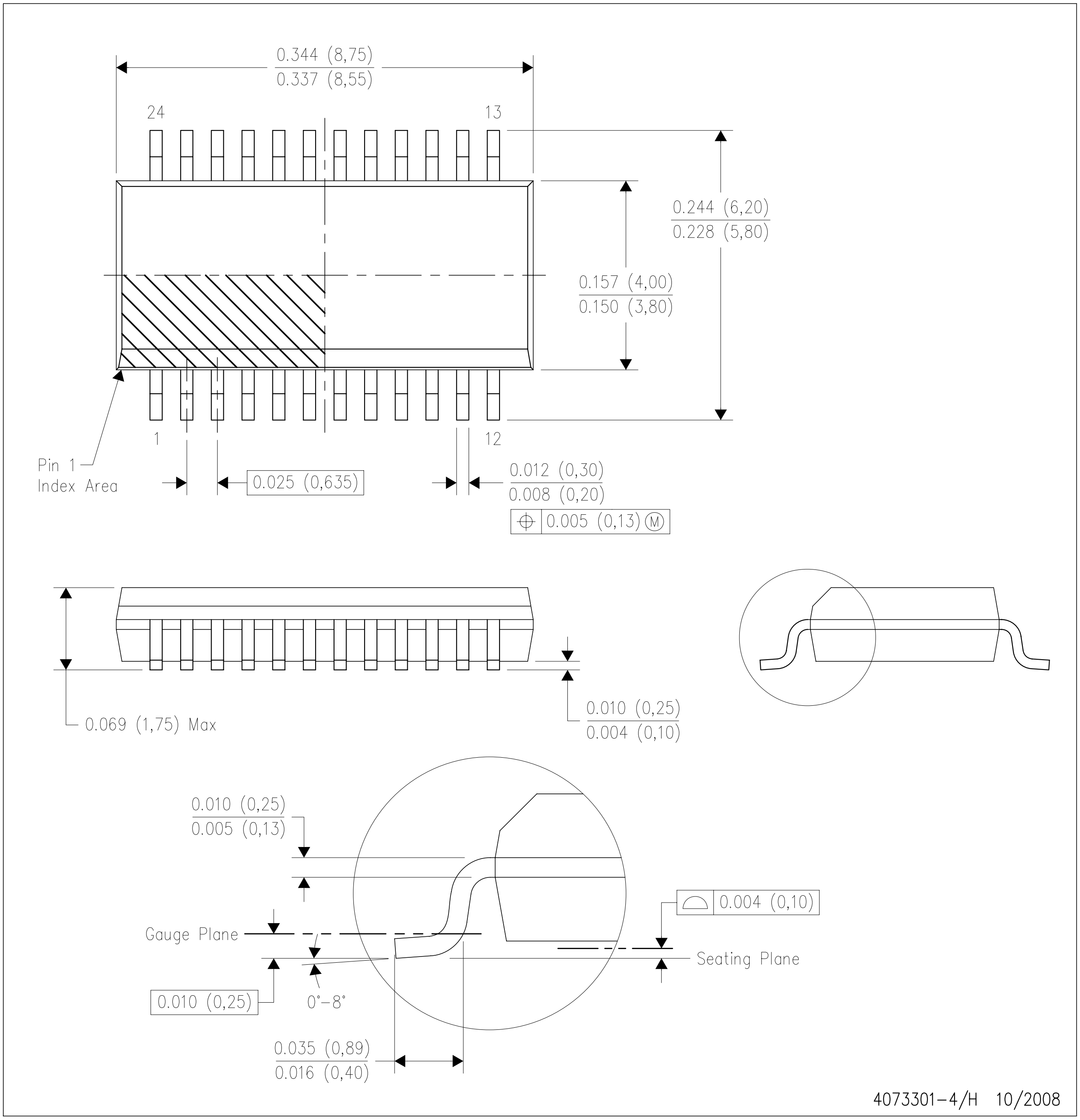
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

DBQ (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
- D. Falls within JEDEC MO–137 variation AE.

重要声明和免责声明

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265