TLV717P 适用于便携式设备且具有折返电流限值的 150mA 低压降稳压器

1 特性

- 超低压降：电流为 150mA 时，压降为 215mV
- 精度：0.5%（典型值）
- 低 I_Q：35µA
- 可提供固定输出电压：
  1.2V 至 5V
- 高电源抑制比 (PSRR)：
  - 1kHz 时为 70dB
  - 1MHz 时为 50dB
- 搭配 0.1µF 有效输出电容使用时可保持稳定
- 折返电流限制
- 封装：1mm x 1mm DQN

(1) 可提供电压选项的完整列表请参阅此文档末尾的封装选项附录。

(2) 更多信息，请参见*Input and Output Capacitor Requirements*。

2 应用

- 个人电脑 (PC) 和笔记本电脑
- 智能手机
- 便携式电子设备和电池供电类设备
- 电子销售点

3 说明

TLV717P 系列低压降线性稳压器 (LDO) 具有较低的静态电流，并且线路和负载瞬态性能出色，适用于功耗敏感型 应用。此系列器件可提供典型值为 0.5% 的精度。

当负载电阻减小时，TLV717P 系列可提供折返电流以降低输出电流。电流折返初始典型值为 350mA；输出短路电流限值的典型值为 40mA。

此外，这些器件还能在采用仅 0.1µF 的有效输出电容时保持稳定。这一特性允许使用具有较高偏置电压和温度降额的成本有效电容器。这些器件在不产生输出负载的情况下可调节至特定的精度。

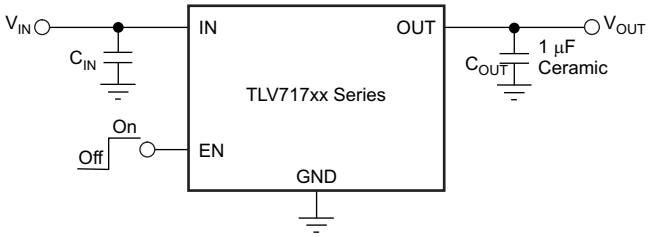
TLV717P 系列采用 1mm × 1mm DQN 封装，非常适合手持式 应用。TLV717P 提供了一个有源下拉电路，用于使输出负载快速放电。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TLV717P	X2SON (4)	1.00mm x 1.00mm

(1) 要了解所有可用封装，请参见数据表末尾的可订购产品附录。

典型应用电路



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (February 2012) to Revision B **Page**

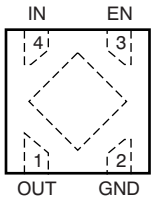
- 已删除 TLV717xx 的所有实例；已替换为通用部件号“TLV717P” 1
- 已更新*应用*. 1
- 已添加 *ESD 额定值表，特性 描述* 部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 1
- Changed T_J = –25°C to T_J = 25°C in the conditions statement in *Absolute Maximum Ratings* 4
- Changed T_A to T_J throughout *Electrical Characteristics* 5
- Changed T_A to T_J in the conditions statement in *Typical Characterisitcs* 6
- Changed T_A to T_J in the conditions statement in *Typical Characterisitcs* 7
- Changed T_A to T_J in the conditions statement in *Typical Characterisitcs* 8
- Changed junction temperature range from –40°C to 125°C to –40°C to 85°C in *Overview* 9
- Deleted TLV717xx functional block diagram 9

Changes from Original (October 2011) to Revision A **Page**

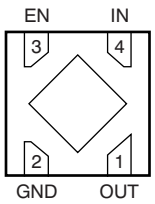
- 已更改 文档状态从 产品预览 改为 生产数据 1

5 Pin Configuration and Functions

DQN Package
4-Pin X2SON
Top View



DQN Package
4-Pin X2SON
Bottom View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	3	I	Enable pin. Driving EN over 1.2 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode.
GND	2	—	Ground pin
IN	4	I	Input pin. A small capacitor is recommended from this pin to ground to assure stability. See the *Input and Output Capacitor Requirements* section in the *Application and Implementation* for more details.
OUT	1	O	Regulated output voltage pin. A small 1-µF ceramic capacitor is recommended from this pin to ground to assure stability. See the *Input and Output Capacitor Requirements* section in the *Application and Implementation* for more details.
Thermal pad	—	—	Connect to GND for improved thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

At T_J = 25°C, unless otherwise noted. All voltages are with respect to GND.(1)

		MIN	MAX	UNIT
Voltage	Input range, V_{IN}	–0.3	6	V
	Enable range, V_{EN}	–0.3	V_{IN} + 0.3	
	Output range, V_{OUT}	–0.3	6	
Current	Maximum output, I_{OUT}	Internally limited		
Output short-circuit duration		Indefinite		
Continuous total power dissipation, P_{DISS}		See *Thermal Information*		
Temperature	Junction, T_J	–55	150	°C
	Storage junction, T_{stg}	–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage	1.7	5.5	V
V_{OUT}	Output voltage	1.2	5	V
I_{OUT}	Output current	0	150	mA
V_{EN}	Enable pin voltage	0	V_{IN}	V
T_J	Junction temperature	–40	85	°C

6.4 Thermal Information

THERMAL METRIC		TLV717P DQN (X2SON) 4 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	393.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	140.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	330	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	329	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	147.5	°C/W

6.5 Electrical Characteristics

At operating temperature range (T_J = –40°C to 85°C), T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.7 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range			1.7		5.5	V
V_{OUT}	Output voltage range			1.2		5	V
I_{OUT}	Output current			150			mA
	DC output accuracy	T_J = +25°C			0.5%		
		V_{OUT} ≥ 1.2 V, –40°C ≤ T_J ≤ +85°C		–1.5%		1.5%	
		V_{OUT} ≤ 1.2 V				25	mV
$\Delta V_O/V_{IN}$	Line regulation	$V_{OUT(NOM)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V			1	5	mV
$\Delta V_O/I_{OUT}$	Load regulation	0 mA ≤ I_{OUT} ≤ 150 mA			10	20	mV
V_{DO}	Dropout voltage	V_{IN} = 0.98 × $V_{OUT(NOM)}$, I_{OUT} = 150 mA	1.2 V ≤ V_{OUT} < 1.5 V		330	500	mV
			1.5 V ≤ V_{OUT} < 1.8 V		330	450	
			1.8 V ≤ V_{OUT} ≤ 5 V		215	350	
I_{GND}	Ground pin current	I_{OUT} = 0 mA			35	55	µA
I_{SHDN}	Shutdown current	V_{EN} ≤ 0.4 V, 2 V ≤ V_{IN} ≤ 4.5 V			0.1	0.5	µA
PSRR	Power-supply rejection ratio	V_{IN} = 3.3 V, V_{OUT} = 2.8 V, I_{OUT} = 30 mA	f = 10 Hz		70		dB
			f = 100 Hz		70		
			f = 1 kHz		65		
			f = 10 kHz		60		
			f = 100 kHz		43		
V_{NOISE}	Output noise voltage	BW = 100 Hz to 100 kHz, V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA			55		μV_{RMS}
t_{STR}	Start-up time	C_{OUT} = 1 µF, I_{OUT} = 150 mA			100		µs
I_{SC}	Short current limit	V_{IN} = min ($V_{OUT(NOM)}$ + 1 V, 5.5 V), V_{OUT} = 0 V			40		mA
V_{HI}	Enable high (enabled)			0.9		V_{IN}	V
V_{LO}	Enable low (disabled)			0		0.4	V
I_{EN}	EN pin current	EN = 5.5 V			0.01		µA
$R_{PULLDOWN}$	Pulldown resistor				120		Ω
UVLO	Undervoltage lockout	V_{IN} rising			1.6		V

6.6 Typical Characteristics

At operating temperature range (T_J = –40°C to 85°C), T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.7 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF, unless otherwise noted.

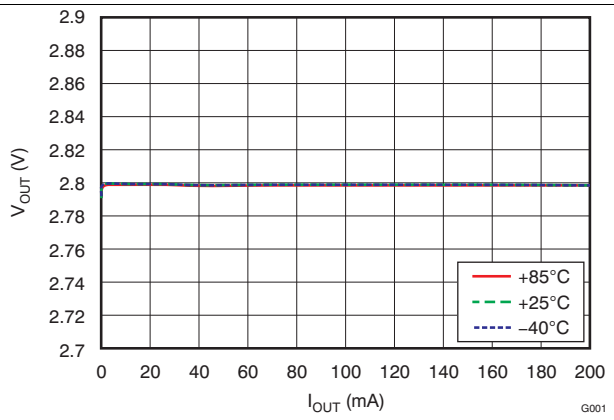


Figure 1. Load Regulation

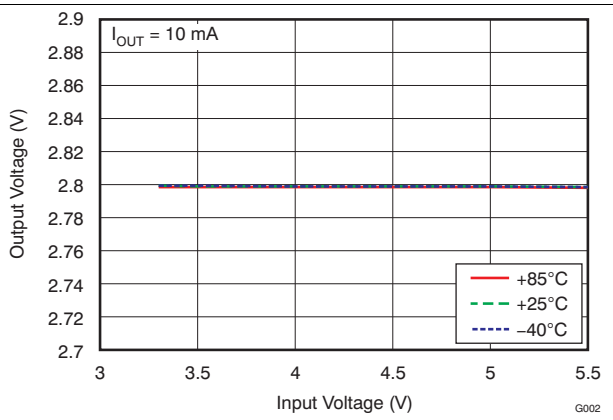


Figure 2. Line Regulation

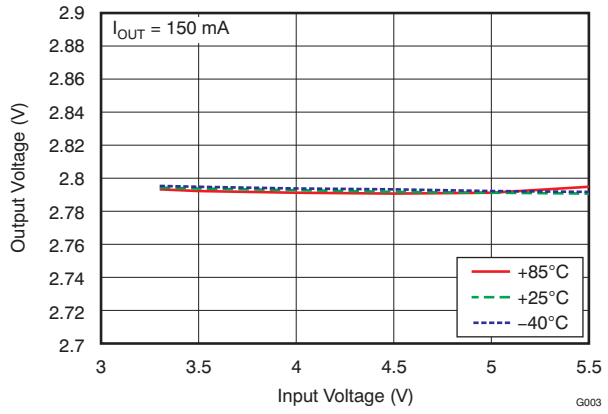


Figure 3. Line Regulation

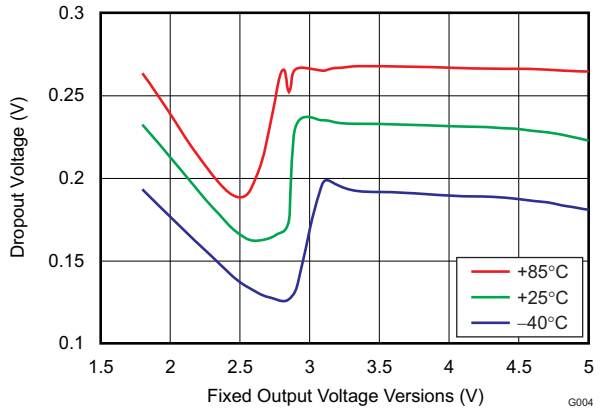


Figure 4. Dropout Voltage vs Fixed Output Voltage Versions

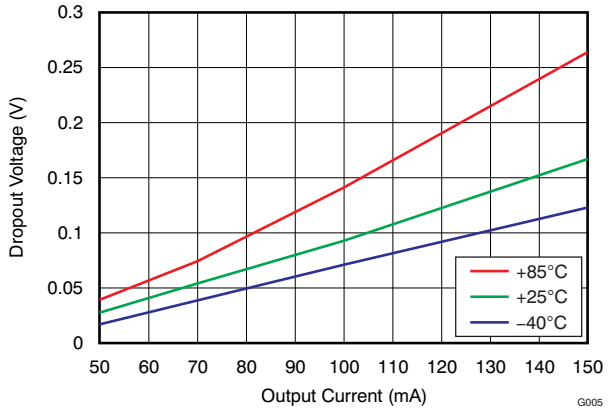


Figure 5. Dropout Voltage vs Output Current

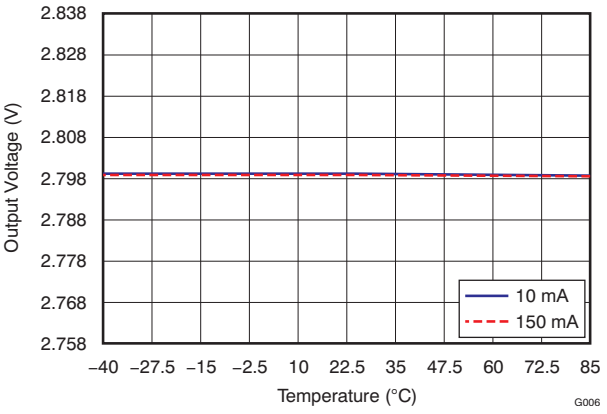


Figure 6. Output Voltage vs Temperature

Typical Characteristics (continued)

At operating temperature range (T_J = –40°C to 85°C), T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.7 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF, unless otherwise noted.

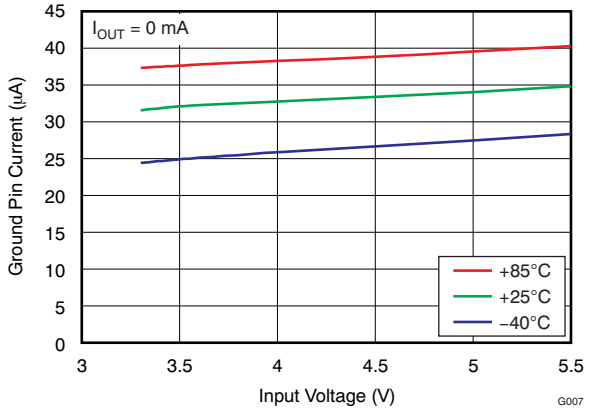


Figure 7. Ground Pin Current vs Input Voltage

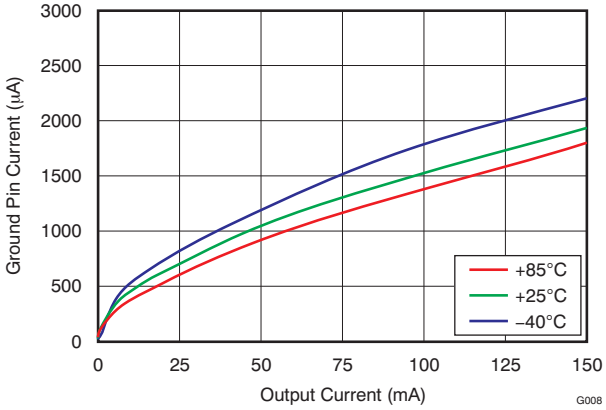


Figure 8. Ground Pin Current vs Output Current

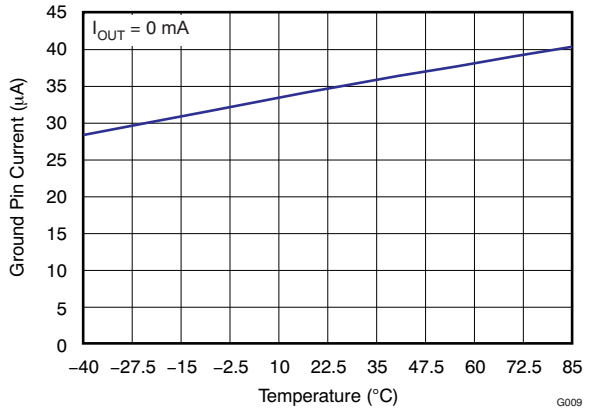


Figure 9. Ground Pin Current vs Temperature

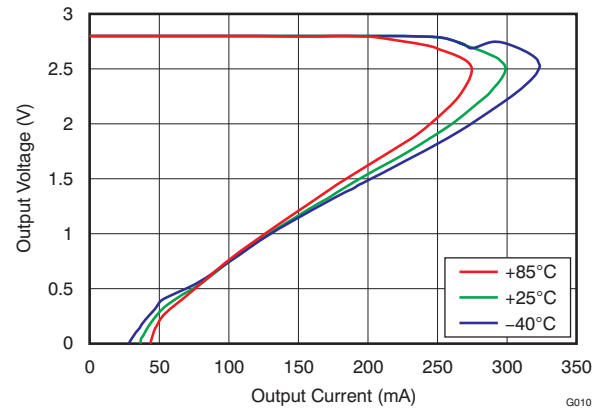


Figure 10. Output Voltage vs Output Current

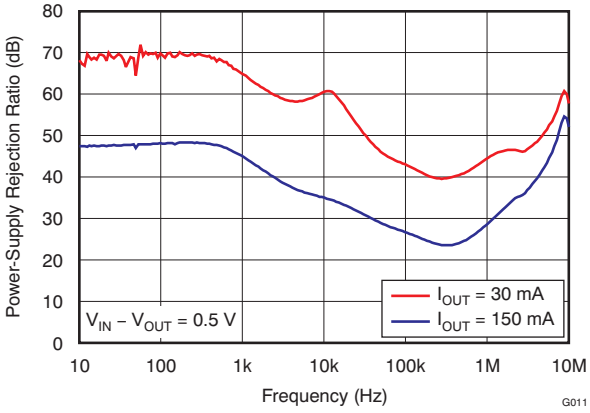


Figure 11. TLV71728PSRR vs Frequency

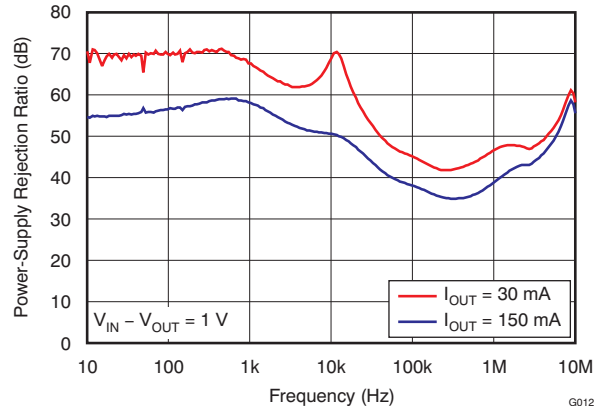


Figure 12. TLV71728PSRR vs Frequency

Typical Characteristics (continued)

At operating temperature range (T_J = –40°C to 85°C), T_J = 25°C, V_{IN} = $V_{OUT(NOM)}$ + 0.5 V or 1.7 V (whichever is greater), I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1 µF, unless otherwise noted.

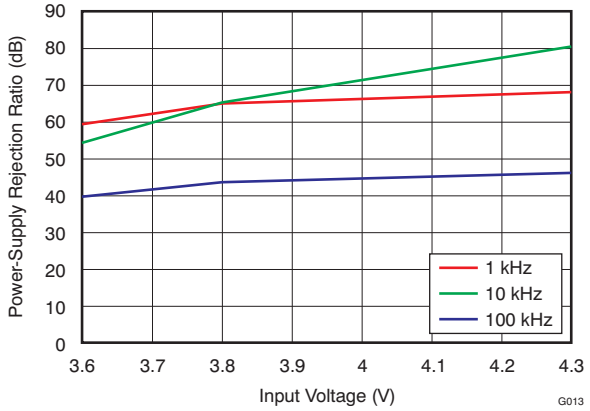


Figure 13. PSRR vs Input Voltage

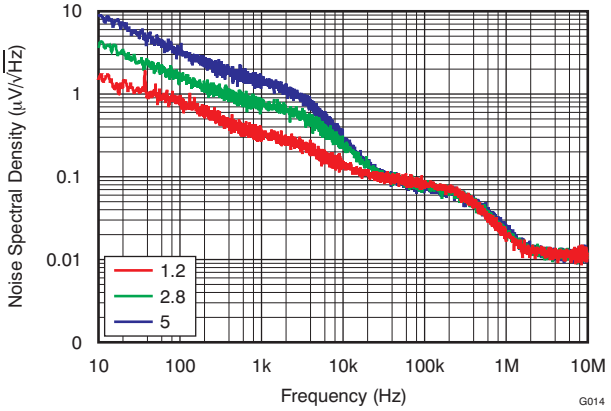


Figure 14. Output Spectral Noise Density vs Frequency

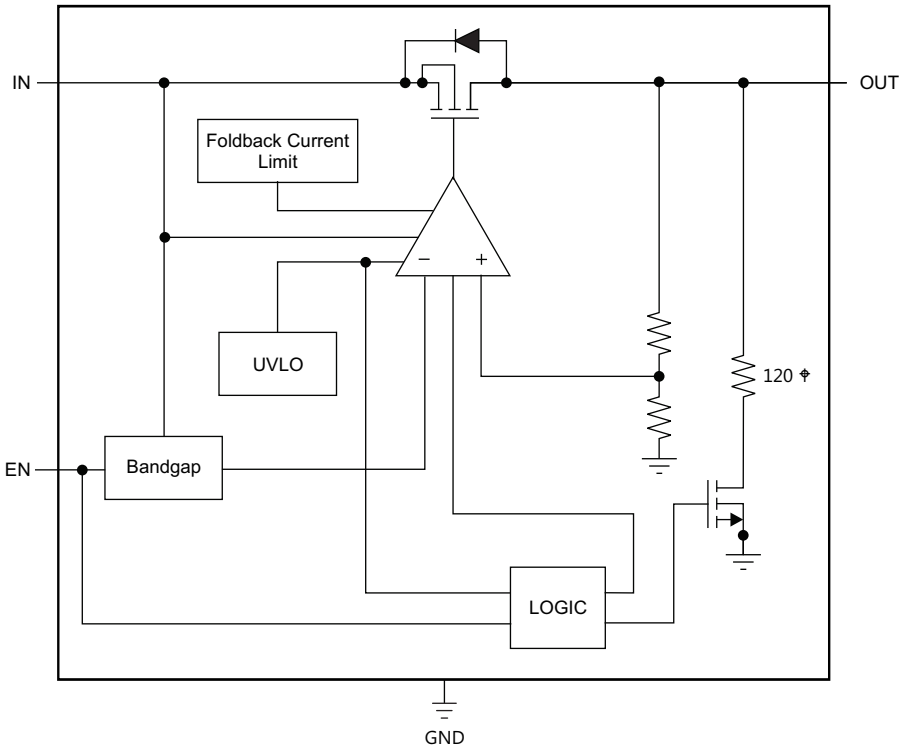
7 Detailed Description

7.1 Overview

The TLV717P belongs to a new family of next-generation value low-dropout (LDO) regulators. These devices consume low quiescent current and deliver excellent line and load transient performance. These characteristics, combined with low noise, very good PSRR with little (V_{IN} – V_{OUT}) headroom, make this family of devices ideal for RF portable applications.

This family of regulators offers current foldback. Device operating junction temperature is –40°C to 85°C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Internal Current Limit

The TLV717P has an internal foldback current limit that helps to protect the regulator during fault conditions. The current supplied by the device is gradually throttled down as the output voltage decreases. When the output is shorted, the LDO supplies a typical current of 40 mA. Output voltage is not regulated when the device is in current limit, and is $V_{OUT} = I_{LIMIT} \times R_{LOAD}$. The advantage of foldback current limit is that the I_{LIMIT} value is less than the fixed current limit. Therefore, the power that the PMOS pass transistor dissipates [($V_{IN} – V_{OUT}$) × I_{LIMIT}] is much less.

The TLV717P PMOS pass element has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

Feature Description (continued)

7.3.2 Shutdown

The enable pin (EN) is active high. The device is enabled when the voltage at the EN pin goes above 0.9 V. This relatively lower voltage value required to turn the LDO on can be exploited to power the LDO with a GPIO of recent processors whose GPIO logic 1 voltage level is lower than traditional microcontrollers. The device is turned off when the EN pin is held at less than 0.4 V. When shutdown capability is not required, EN can be connected to the IN pin.

7.3.3 Undervoltage Lockout (UVLO)

The TLV717P uses an undervoltage lockout circuit (UVLO = 1.6 V) to keep the output shut off until the internal circuitry operates properly.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage has previously exceeded the UVLO rising voltage and has not decreased below the UVLO falling threshold.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage has previously exceeded the enable rising threshold voltage and not decreased below the enable falling threshold.
- The output current is less than the current limit.

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is the same the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout may result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The input voltage is less than the UVLO falling voltage, or has not yet exceeded the UVLO rising threshold.
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.

When the device is disabled, the active pulldown resistor discharges the output.

Table 1 lists the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER		
	V_{IN}	V_{EN}	I_{OUT}
Normal mode	$V_{IN} > V_{OUT}(nom) + V_{DO}$ and $V_{IN} > UVLO_{RISE}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{LIM}$
Dropout mode	$UVLO_{RISE} < V_{IN} < V_{OUT}(nom) + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{LIM}$
Disabled mode (any true condition disables the device)	$V_{IN} < UVLO_{FALL}$	$V_{EN} < V_{EN(LO)}$	—

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TLV717P is a low-dropout regulator (LDO) with low quiescent current that delivers excellent line and load transient performance. This LDO regulator offers a foldback current limit. The operating junction temperature of this device series is –40°C to 85°C.

8.2 Typical Application

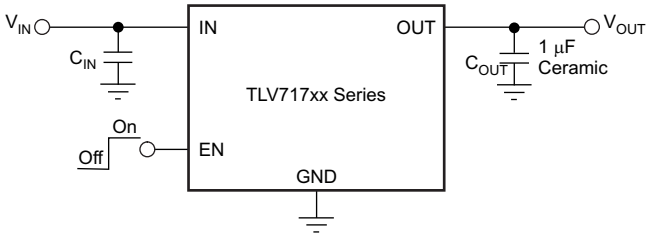


Figure 15. Typical Application Circuit

8.2.1 Design Requirements

Table 2 lists the parameters for this application.

Table 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	3.8 V
Output voltage	2.8 V ±1%
Output current	30 to 150 mA

8.2.2 Detailed Design Procedure

8.2.2.1 Input and Output Capacitor Requirements

TI recommends X5R- and X7R-type ceramic capacitors because they have minimal variation in value and equivalent series resistance (ESR) over temperature. The TLV717P is designed to be stable with an effective capacitance of 0.1 µF or larger at the output, though TI recommends a 1-µF ceramic capacitor for typical applications. Thus, the device is stable with capacitors of other dielectric types as well, as long as the effective capacitance under operating bias voltage and temperature is greater than 0.1 µF. This effective capacitance refers to the capacitance that the LDO detects under operating bias voltage and temperature conditions; that is, the capacitance after taking both bias voltage and temperature derating into consideration. In addition to allowing the use of cheaper dielectrics, this capability of being stable with 0.1-µF effective capacitance also enables the use of smaller footprint capacitors that have higher derating in size- and space-constrained applications. Using a 0.1-µF rated capacitor at the LDO output does not ensure stability because the effective capacitance under the specified operating conditions would be less than 0.1 µF. Maximum ESR should be less than 200 mΩ.

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1-µF to 1-µF, low ESR capacitor across the IN and GND pins of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast, rise-time load transients are anticipated, or if the device is not located close to the power source. If source impedance is more than 2 Ω, a 0.1-µF input capacitor may be necessary to ensure stability.

8.2.2.2 Dropout Voltage

The TLV717P uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves like a resistor in dropout. As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout.

8.2.2.3 Transient Response

As with any regulator, increasing the size of the output capacitor reduces over- and undershoot magnitude but increases the duration of the transient response.

8.2.3 Application Curves

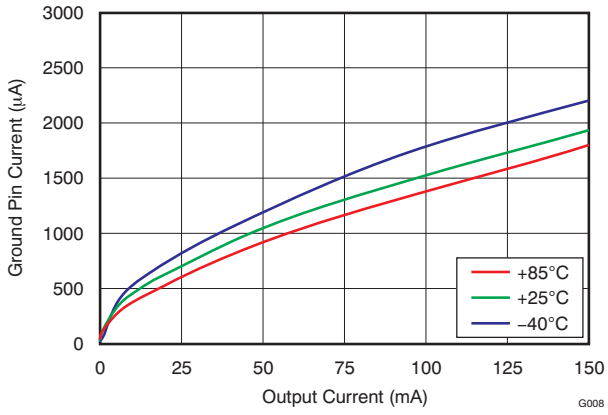


Figure 16. Ground Pin Current vs Output Current

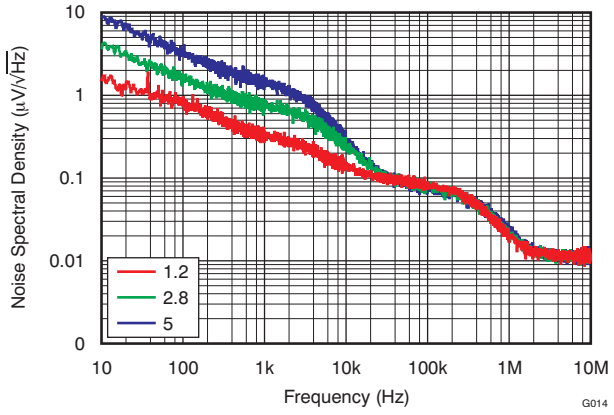


Figure 17. Output Spectral Noise Density vs Frequency

9 Power Supply Recommendations

Connect a low-output impedance power supply directly to the IN pin of the TLV717P. Inductive impedances between the input supply and the IN pin can create significant voltage excursions at the IN pin during start-up or load transient events. If inductive impedances are unavoidable, use an input capacitor.

10 Layout

10.1 Layout Guidelines

Input and output capacitors should be placed as close to the device pins as possible. To improve AC performance (such as PSRR, output noise, and transient response), TI recommends designing the board with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the device GND pin. In addition, the output capacitor ground connection should be connected directly to the device GND pin. High ESR capacitors may degrade PSRR performance.

10.2 Layout Example

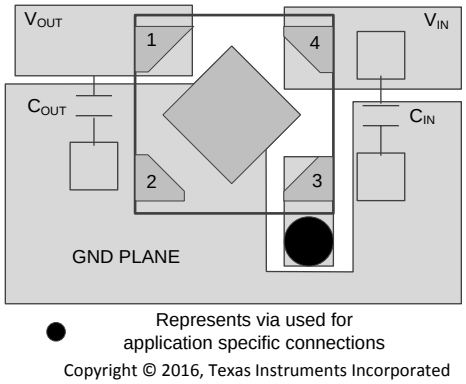


Figure 18. Recommended Layout Example

10.3 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed-circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to ambient air. Performance data for JEDEC-low and high-K boards are given in *Thermal Information*. Using heavier copper increases the effectiveness in removing heat from the device. The addition, plated through-holes to heat-dissipating layers also improves heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current and the voltage drop across the output pass element, as shown in Equation 1.

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT} \quad (1)$$

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 评估模块

评估模块 (EVM) 可与 TLV717P 配套使用，协助评估初始电路性能。SLVU553 详细介绍了 TLV71733PEVM-072 的设计套件和评估模块。

EVM 可通过德州仪器 (TI) 网站上的 TLV717P 产品文件夹获取，也可直接从 TI 网上商店购买。

11.1.2 器件命名规则

表 **3.** 器件命名规则(1)

产品	V_{OUT}
TLV717**xx(x)Pyyyz**	**XX(X)** 是标称输出电压。对于分辨率为 100mV 的输出电压，订货编号中使用两位数字；否则，使用三位数字（例如，28 = 2.8V；475 = 4.75 V）。 **P** 表示有源输出放电功能。TLV717P 系列的所有器件在禁用时都可以使输出进行有源放电。 **YYY** 为封装标识符。 **Z** 为封装数量。R 表示 3000 片，T 表示 250 片。

(1) 要获得最新的封装和订货信息，请参见本文档末尾的封装选项附录，或者访问器件产品文件夹（www.ti.com）。

11.2 文档支持

11.2.1 相关文档

《TLV71733PEVM-072 评估模块用户指南》，SLVU553

11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械封装和可订购信息

以下页中包括机械封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV71712PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	UX	Samples
TLV71712PDQNR3	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	UX	Samples
TLV71712PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	UX	Samples
TLV71713PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VC	Samples
TLV71713PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VC	Samples
TLV71715PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	UY	Samples
TLV71715PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	UY	Samples
TLV717185PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VN	Samples
TLV717185PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VN	Samples
TLV71718PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	UZ	Samples
TLV71718PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	UZ	Samples
TLV71721PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AR	Samples
TLV71721PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AR	Samples
TLV71725PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VA	Samples
TLV71725PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VA	Samples
TLV71727PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AS	Samples
TLV71727PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AS	Samples
TLV717285PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM		VE	Samples
TLV717285PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VE	Samples
TLV71728PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VD	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV71728PDQNR3	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VD	Samples
TLV71728PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VD	Samples
TLV71729PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VI	Samples
TLV71729PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VI	Samples
TLV71730PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VF	Samples
TLV71730PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VF	Samples
TLV71733PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VG	Samples
TLV71733PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VG	Samples
TLV71736PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VH	Samples
TLV71736PDQNT	ACTIVE	X2SON	DQN	4	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	VH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

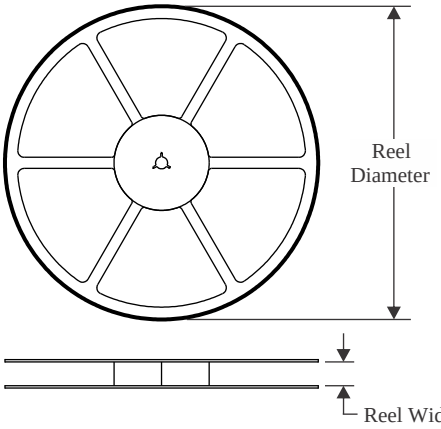
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

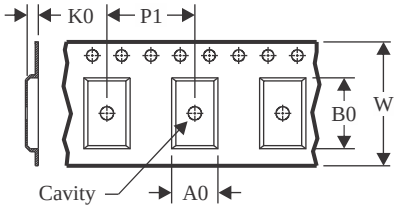
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

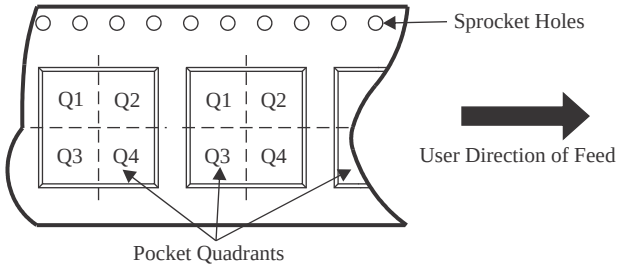


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

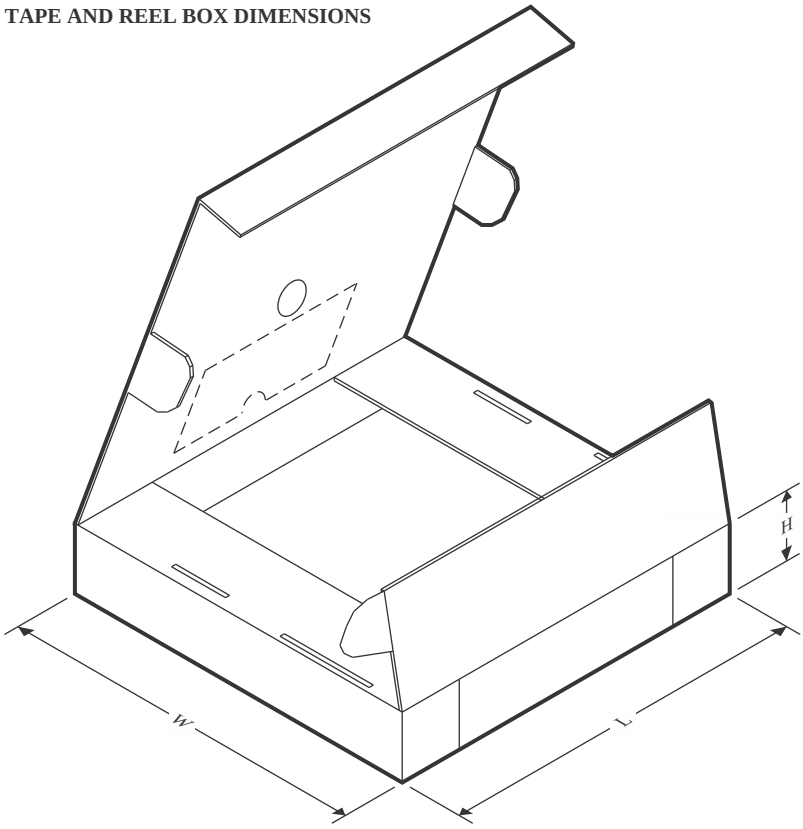


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV71712PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71712PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71712PDQNR3	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	2.0	8.0	Q3
TLV71712PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71712PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71713PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71713PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71713PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71715PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71715PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71715PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71715PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV717185PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV717185PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV71718PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV71718PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV71721PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71721PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71721PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71721PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71725PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71725PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71725PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71725PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71727PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV71727PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV717285PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV717285PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV717285PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV717285PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71728PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71728PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71728PDQNR3	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	2.0	8.0	Q3
TLV71728PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71728PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71729PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV71729PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV71730PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71730PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71730PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71733PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV71733PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV71736PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2
TLV71736PDQNR	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71736PDQNT	X2SON	DQN	4	250	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q2
TLV71736PDQNT	X2SON	DQN	4	250	180.0	8.4	1.16	1.16	0.63	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV71712PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV71712PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71712PDQNR3	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71712PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV71712PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV71713PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71713PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV71713PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV71715PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV71715PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71715PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV71715PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV717185PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV717185PDQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV71718PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV71718PDQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV71721PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV71721PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV71721PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV71721PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV71725PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV71725PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71725PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV71725PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV71727PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV71727PDQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV717285PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV717285PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV717285PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV717285PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV71728PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71728PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV71728PDQNR3	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71728PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV71728PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV71729PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV71729PDQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV71730PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71730PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0
TLV71730PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV71733PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV71733PDQNT	X2SON	DQN	4	250	210.0	185.0	35.0
TLV71736PDQNR	X2SON	DQN	4	3000	183.0	183.0	20.0
TLV71736PDQNR	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV71736PDQNT	X2SON	DQN	4	250	184.0	184.0	19.0
TLV71736PDQNT	X2SON	DQN	4	250	183.0	183.0	20.0

GENERIC PACKAGE VIEW

DQN 4 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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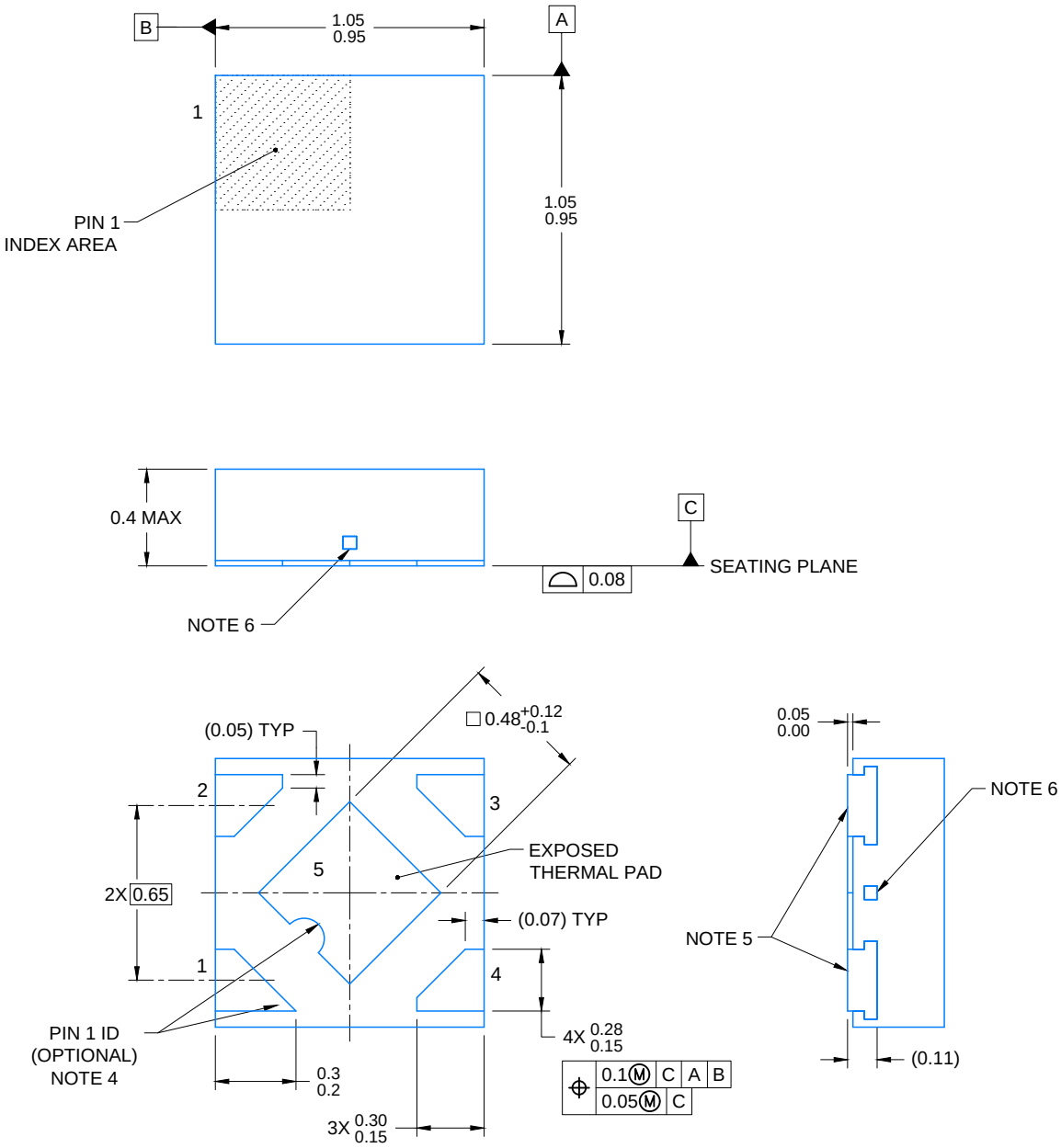
PACKAGE OUTLINE

DQN0004A

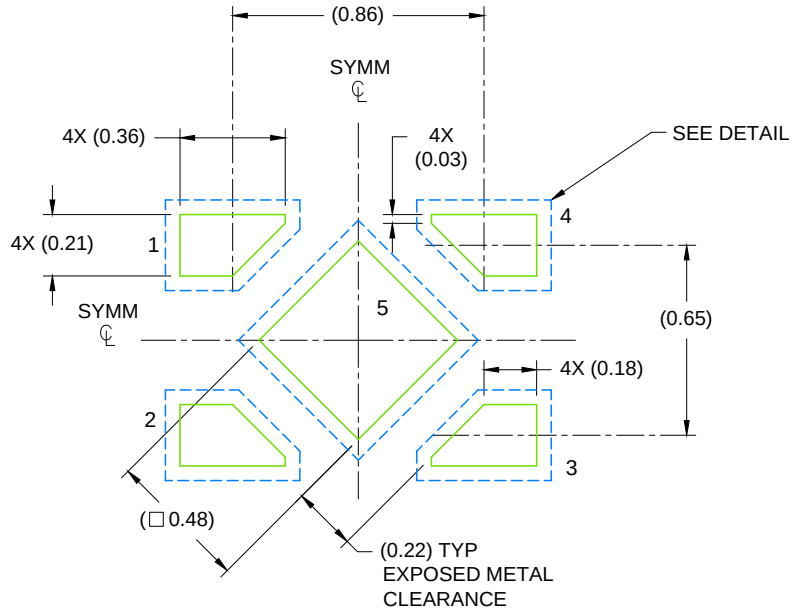
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



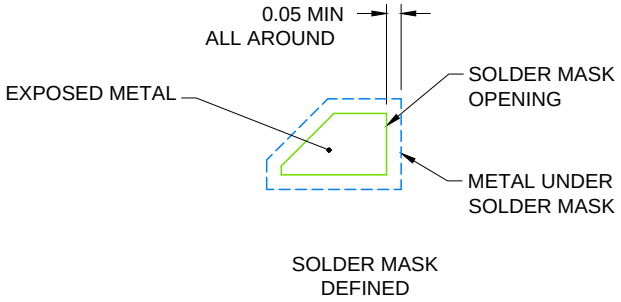
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.
5. Shape of exposed side leads may differ.
6. Number and location of exposed tie bars may vary.



LAND PATTERN EXAMPLE

SCALE: 40X



SOLDER MASK DETAIL

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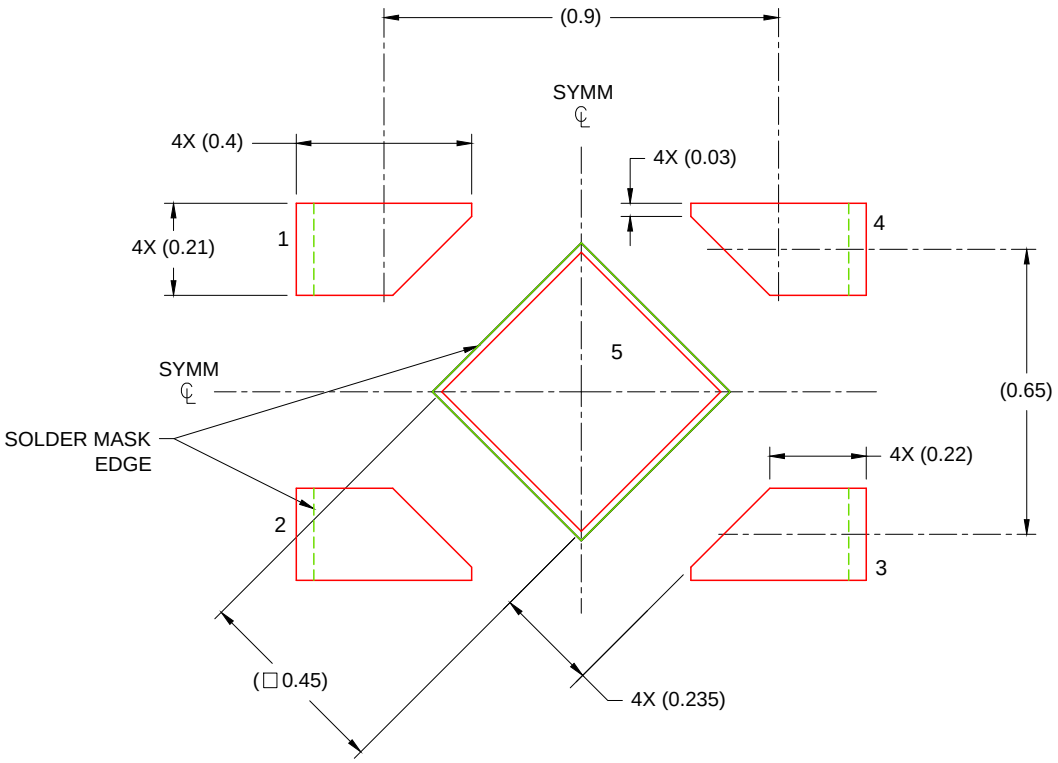
NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
8. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1mm THICK STENCIL

EXPOSED PAD
88% PRINTED SOLDER COVERAGE BY AREA
SCALE: 60X

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

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