TLV743P 300mA 低压差稳压器

1 特性

- 输入电压范围：1.4V 至 5.5V
- 使用 1μF 陶瓷输出电容器实现稳定运行
- 折返过流保护
- 封装：
  - SOT-23 (5)
  - X2SON (4)
- 极低压差：125mV/300mA (3.3V_{OUT})
- 精度：1%（典型值）、1.4%（最大值）
- 低 I_Q：34μA
- 可提供固定输出电压：
  1V 至 3.3V
- 高电源抑制比 (PSRR)：1kHz 频率时为 50dB
- 有源输出放电

2 应用

- 平板电脑
- 智能手机
- 笔记本和台式计算机
- 便携式工业和消费类产品
- 无线局域网 (WLAN) 和其他 PC 附加卡
- 摄像机模块

3 说明

TLV743P 低压差线性稳压器 (LDO) 是一款超小型低静态电流 LDO，可提供 300mA 拉电流，具有良好的线路和负载瞬态性能。此器件提供了 1% 的典型精度。

TLV743P 器件旨在使用 1μF 的小型输出电容器实现稳定运行。TLV743P 器件可在器件加电和使能期间提供折返电流控制。该功能对于电池供电型器件尤为重要。

TLV743P 提供了有源下拉电路，用于在器件处于禁用状态时对输出负载进行快速放电。

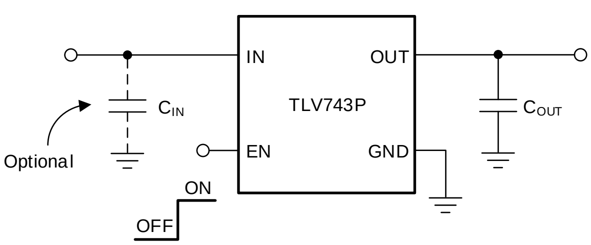
TLV743P 采用标准 DBV (SOT-23) 和 DQN (X2SON) 封装。

器件信息[(1)]

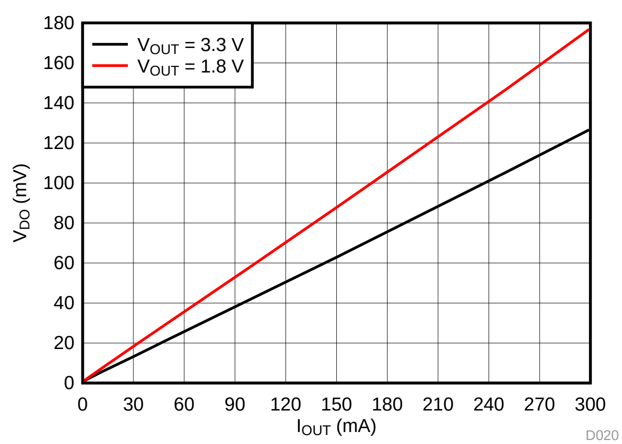
器件型号	封装	封装尺寸（标称值）
TLV743P	SOT-23 (5)	2.90mm × 1.60mm
	X2SON (4)	1.00mm x 1.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的封装选项附录。

典型应用电路



压降电压与输出电流间的关系



目录

4 修订历史记录

Changes from Revision B (March 2018) to Revision C	**Page**
• Changed description of EN pin in *Pin Functions* table	4
• Deleted typical specification from $V_{EN(HI)}$ and $V_{EN(LO)}$ parameters	6
• Added maximum specification to I_{LIM} parameter	7
• 已添加 condition to *1-V Load Regulation vs I_{OUT} and Temperature* figure	8
• 已添加 condition to *1.8-V Load Regulation vs I_{OUT} and Temperature* figure	8
• 已添加 condition to *3.3-V Load Regulation vs I_{OUT} and Temperature* figure	8
• 已添加 condition to *1.2-V Dropout Voltage vs I_{OUT} and Temperature* figure	9
• 已添加 condition to *1.8-V Dropout Voltage vs I_{OUT} and Temperature* figure	9
• 已添加 condition to *3.3-V Dropout Voltage vs I_{OUT} and Temperature* figure	9
• 已添加 *and Output Enable* to title and changed first paragraph of *Shutdown and Output Enable* section	14
• 已添加 DBV package to *Maximum Ambient Temperature vs Device Power Dissipation* figure and text reference	17
• 已添加 将 (3) 添加到*器件命名规则* 表	20

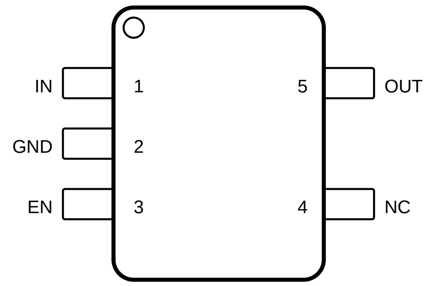
Changes from Revision A (January 2018) to Revision B	**Page**
• 已更改 将 X2SON 封装从预览更改为生产数据（有效）	1

Changes from Original (July 2017) to Revision A	**Page**
• 已添加 X2SON 封装至*特性* 列表	1
• 已添加 将 DQN (X2SON) 封装添加至*说明* 部分	1
• 已添加 将 X2SON 封装添加至*器件信息* 表	1
• Added DQN (X2SON) package pinout drawing and pin functions table to *Pin Configuration and Functions* section	4
• Deleted thermal pad from DBV pinout drawing and *Pin Functions* table	4
• Changed format of I/O column contents and order of packages in *Pin Functions* table	4
• Added DQN (X2SON) thermal information to *Thermal Information* table	5
• 已更改 condition text for 图 31	17

- 已添加 X2SON layout example image to *Layout Examples* section 19

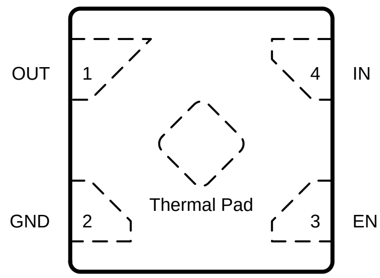
5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



Not to scale

DQN Package
4-Pin X2SON With Exposed Thermal Pad
Top View



Not to scale

Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOT-23	X2SON		
EN	3	3	I	Enable pin. Drive EN greater than $V_{EN(LO)}$ to turn on the regulator. Drive EN less than $V_{EN(LO)}$ to put the LDO into shutdown mode.
GND	2	2	—	Ground pin
IN	1	4	I	Input pin. A small capacitor is recommended from this pin to ground. See *Input and Output Capacitor Selection* for more details.
NC	4		—	No internal connection
OUT	5	1	O	Regulated output voltage pin. For best transient response, use a small 1-µF ceramic capacitor from this pin to ground. See *Input and Output Capacitor Selection* for more details.
Thermal pad	—	Thermal pad	—	The thermal pad is electrically connected to the GND node. Connect to the GND plane for improved thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted); all voltages are with respect to GND(1)

		MIN	MAX	UNIT
Voltage	V_{IN}	–0.3	6	V
	V_{EN}	–0.3	V_{IN} + 0.3	
	V_{OUT}	–0.3	3.6	
Current	I_{OUT}	Internally limited		A
Output short-circuit duration		Indefinite		
Temperature	Operating junction, T_J	–40	150	°C
	Storage, T_{stg}	–65	160	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input range	1.4		5.5	V
V_{OUT}	Output range	1		3.3	V
I_{OUT}	Output current	0		300	mA
V_{EN}	Enable range	0		V_{IN}	V
T_J	Junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TLV743P DBV (SOT-23) 5 PINS	TLV743P DQN (X2SON) 4 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	228.4	218.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	151.5	164.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	55.8	164.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	31.4	5.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	54.8	163.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	131.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = V_{OUT}(nom) + 0.5 V or 2 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted). All typical values at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage			1.4		5.5	V
	DC output accuracy	T_J = 25°C		–1%		1%	
		–40°C ≤ T_J ≤ 125°C		–1.4%		1.4%	
UVLO	Undervoltage lockout	V_{IN} rising			1.3	1.4	V
		V_{IN} falling			1.25		
$\Delta V_{O(\Delta VI)}$	Line regulation	ΔVI = $V_{IN(nom)}$ to $V_{IN(nom)}$ + 1			1		mV
$\Delta V_{O(\Delta IO)}$	Load regulation	ΔIO = 1 mA to 300 mA	DBV package		16		mV
					25		
V_{DO}	Dropout voltage(1)	V_{OUT} = 0.98 × $V_{OUT(nom)}$ I_{OUT} = 300 mA	V_{OUT} = 1.1 V –40°C ≤ T_J ≤ 85°C			480	mV
			1.2 V ≤ V_{OUT} < 1.5 V –40°C ≤ T_J ≤ 85°C			420	
			1.5 V ≤ V_{OUT} < 1.8 V –40°C ≤ T_J ≤ 85°C			370	
			1.8 V ≤ V_{OUT} < 2.5 V –40°C ≤ T_J ≤ 85°C			270	
			2.5 V ≤ V_{OUT} < 3.3 V –40°C ≤ T_J ≤ 85°C			260	
			V_{OUT} = 3.3 V –40°C ≤ T_J ≤ 85°C		125	220	
			1.2 V ≤ V_{OUT} < 1.5 V –40°C ≤ T_J ≤ 125°C			450	
			1.5 V ≤ V_{OUT} < 1.8 V –40°C ≤ T_J ≤ 125°C			400	
			1.8 V ≤ V_{OUT} < 2.5 V –40°C ≤ T_J ≤ 125°C			300	
			2.5 V ≤ V_{OUT} < 3.3 V –40°C ≤ T_J ≤ 125°C			290	
			V_{OUT} = 3.3 V –40°C ≤ T_J ≤ 125°C		125	270	
I_{GND}	Ground pin current	I_{OUT} = 0 mA			34	60	µA
I_{SHDN}	Shutdown current	V_{EN} ≤ 0.35 V 2 V ≤ V_{IN} ≤ 5.5 V T_J = 25°C			0.1	1	µA
PSRR	Power-supply rejection ratio	V_{OUT} = 1.8 V I_{OUT} = 300 mA	f = 100 Hz		68		dB
			f = 10 kHz		35		
			f = 100 kHz		28		
V_n	Output noise voltage	Bandwidth = 10 Hz to 100 kHz V_{OUT} = 1.8 V I_{OUT} = 10 mA			120		μV_{RMS}
$V_{EN(HI)}$	EN pin high voltage (enabled)			0.9			V
$V_{EN(LO)}$	EN pin low voltage (disabled)					0.35	V
I_{EN}	EN pin current	V_{EN} = 5.5 V			0.01		µA

(1) Dropout voltage for the TLV743P is not valid at room temperature. The device engages undervoltage lockout (V_{IN} < $UVLO_{FALL}$) before the dropout condition is met.

Electrical Characteristics (continued)

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = V_{OUT}(nom) + 0.5 V or 2 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted). All typical values at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{STR}	Startup time	Time from EN assertion to 98% × V_{OUT}(nom) V_{OUT} = 1 V I_{OUT} = 0 mA		250		µs
		Time from EN assertion to 98% × V_{OUT}(nom) V_{OUT} = 3.3 V I_{OUT} = 0 mA		800		
	Pulldown resistor	V_{IN} = 2.3 V		120		Ω
I_{LIM}	Output current limit		360		700	mA
I_{OS}	Short-circuit current limit	V_{OUT} shorted to GND V_{OUT} = 1 V		150		mA
		V_{OUT} shorted to GND V_{OUT} = 3.3 V		170		
T_{sd}	Thermal shutdown	Shutdown, temperature increasing		160		°C
		Reset, temperature decreasing		140		

6.6 Typical Characteristics

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = V_{OUT}(nom) + 0.5 V or 2 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)

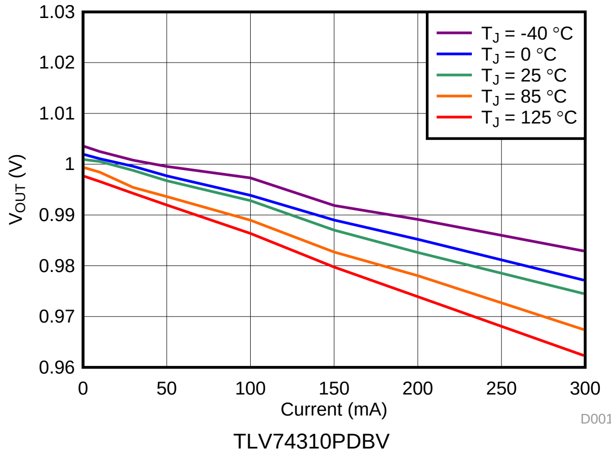


图 1. 1-V Load Regulation vs I_{OUT} and Temperature

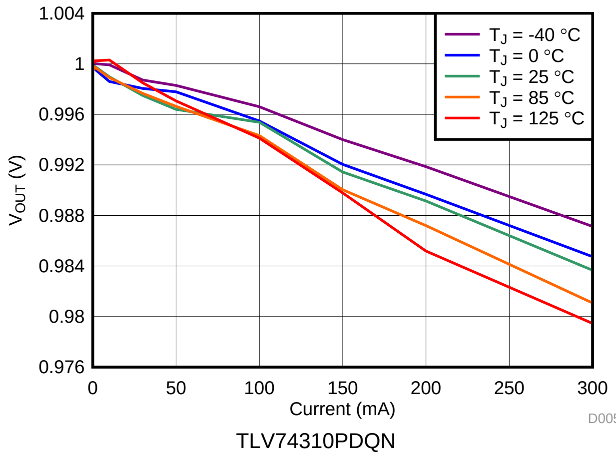


图 2. 1-V Load Regulation vs I_{OUT} and Temperature

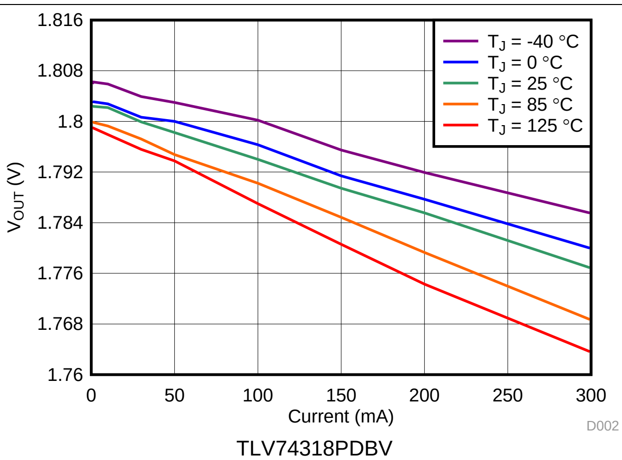


图 3. 1.8-V Load Regulation vs I_O and Temperature

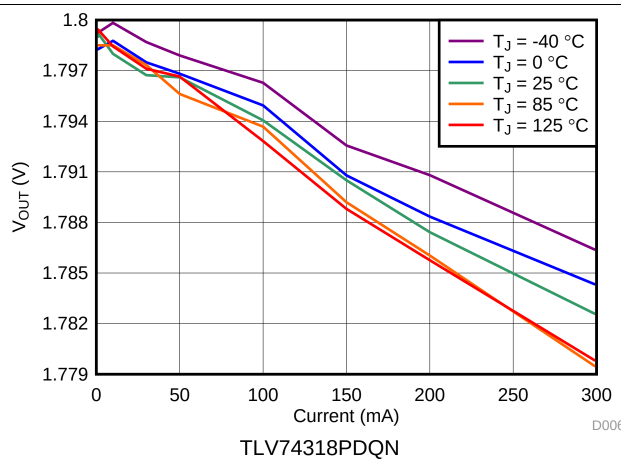


图 4. 1.8-V Load Regulation vs I_{OUT} and Temperature

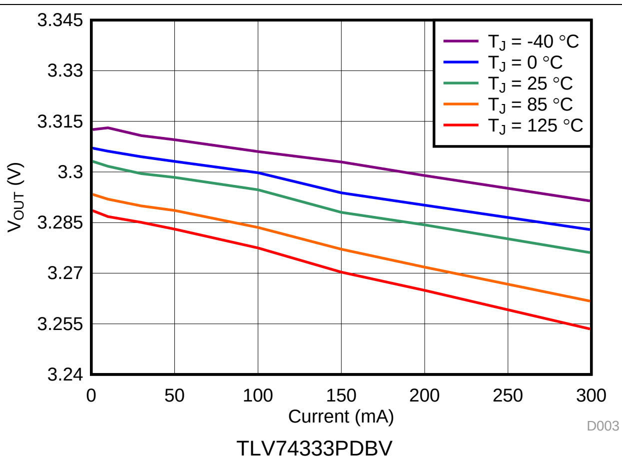


图 5. 3.3-V Load Regulation vs I_{OUT} and Temperature

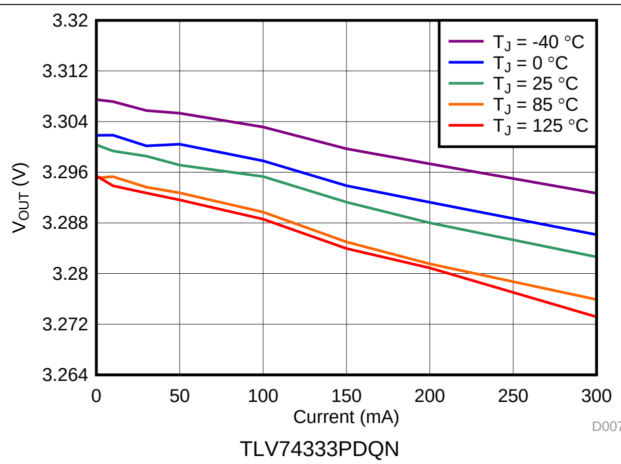


图 6. 3.3-V Load Regulation vs I_{OUT} and Temperature

Typical Characteristics (接下页)

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = V_{OUT}(nom) + 0.5 V or 2 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)

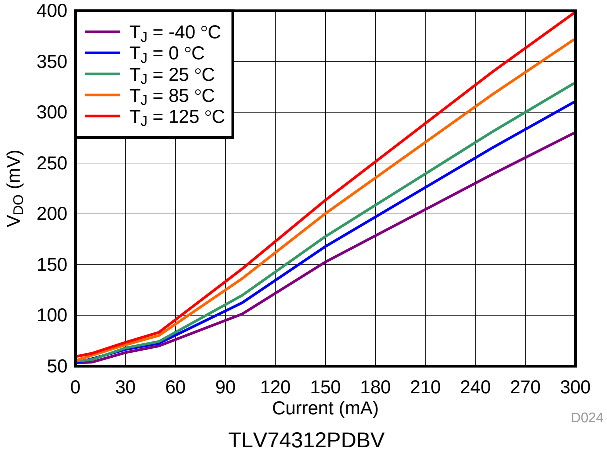


图 7. 1.2-V Dropout Voltage vs I_{OUT} and Temperature

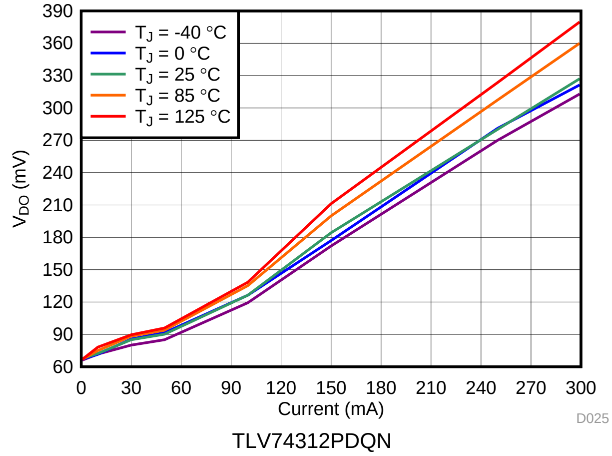


图 8. 1.2-V Dropout Voltage vs I_{OUT} and Temperature

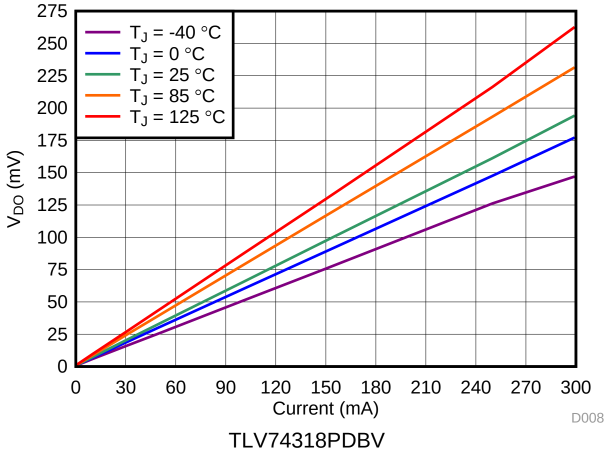


图 9. 1.8-V Dropout Voltage vs I_{OUT} and Temperature

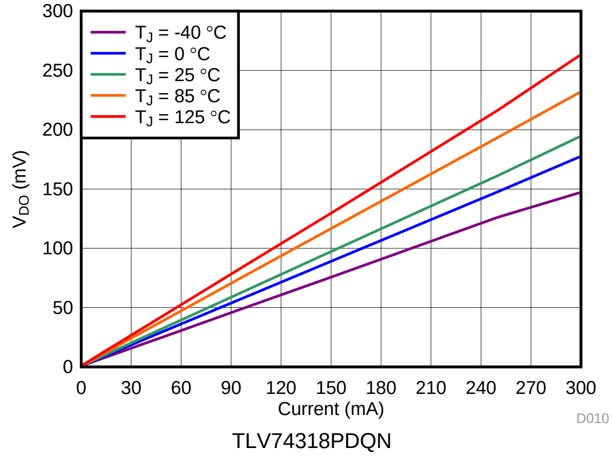


图 10. 1.8-V Dropout Voltage vs I_{OUT} and Temperature

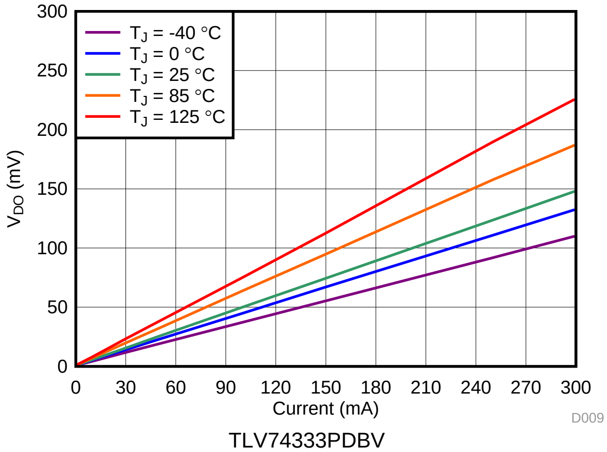


图 11. 3.3-V Dropout Voltage vs I_{OUT} and Temperature

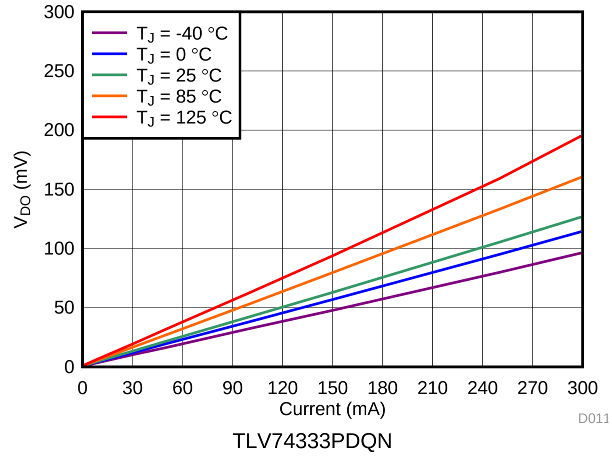


图 12. 3.3-V Dropout Voltage vs I_{OUT} and Temperature

Typical Characteristics (接下页)

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = V_{OUT}(nom) + 0.5 V or 2 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)

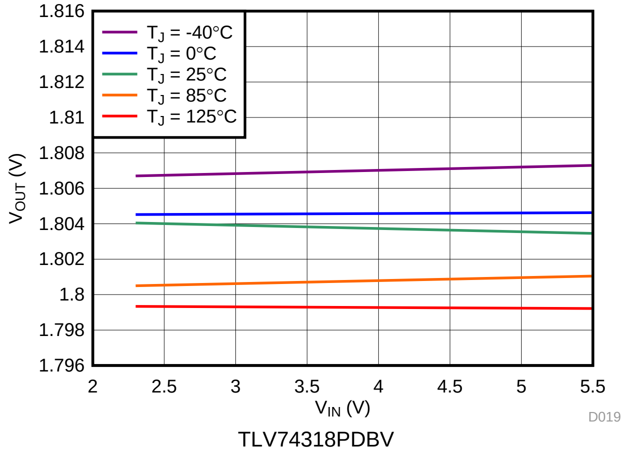


图 13. 1.8-V Regulation vs V_{IN} (Line Regulation) and Temperature

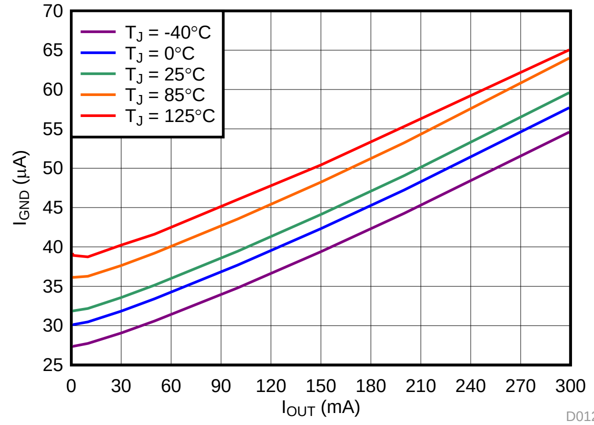


图 14. Ground Pin Current vs I_{OUT} and Temperature

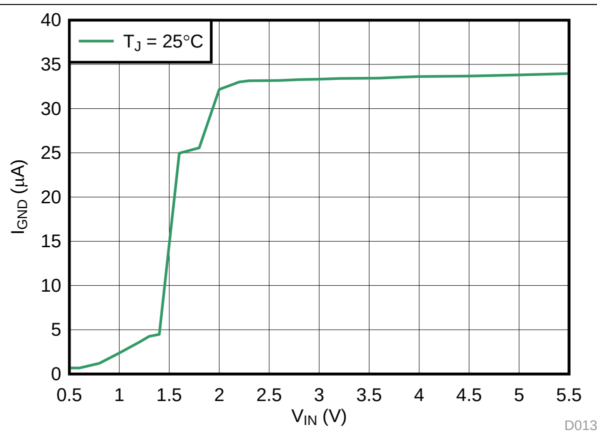


图 15. Ground Pin Current vs V_{IN}

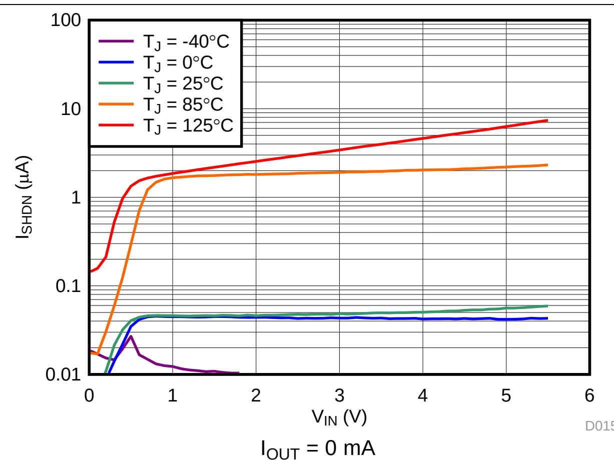


图 16. Shutdown Current vs V_{IN} and Temperature

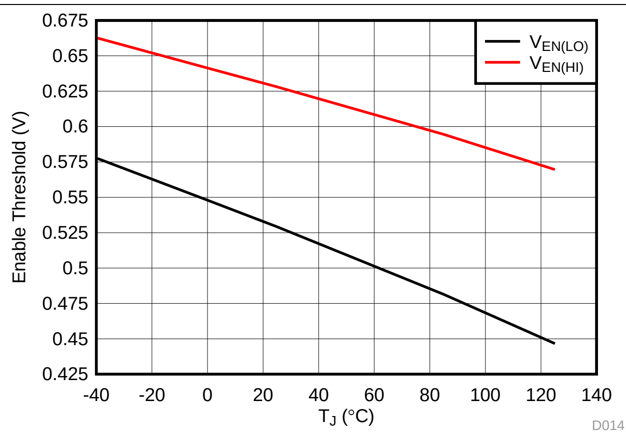


图 17. Enable Threshold vs Temperature

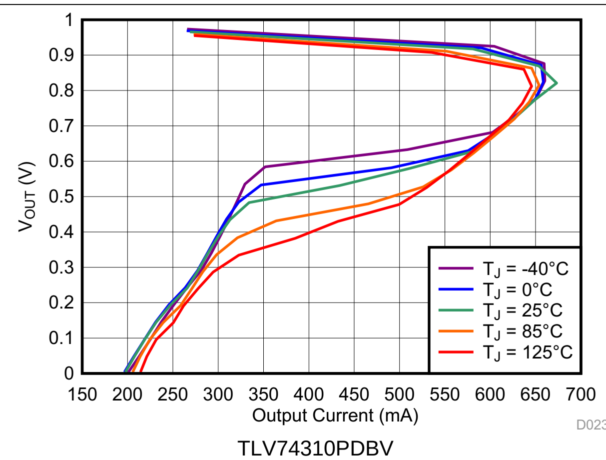
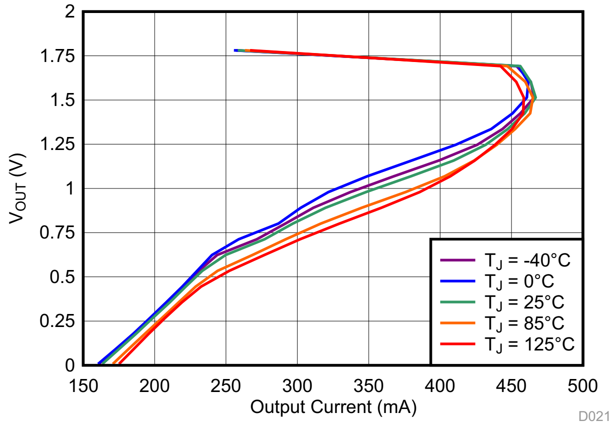


图 18. 1-V Foldback Current Limit vs I_{OUT} and Temperature

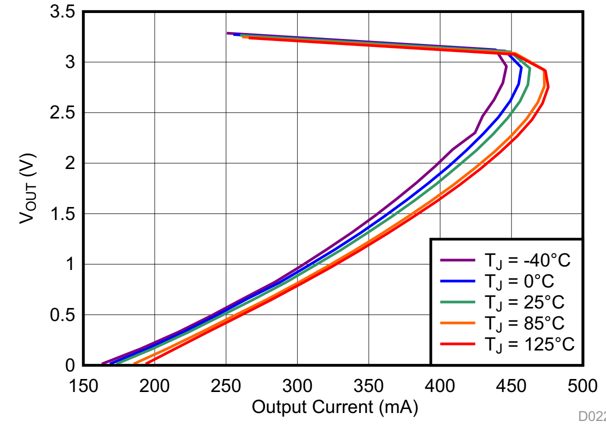
Typical Characteristics (接下页)

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = V_{OUT}(nom) + 0.5 V or 2 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)



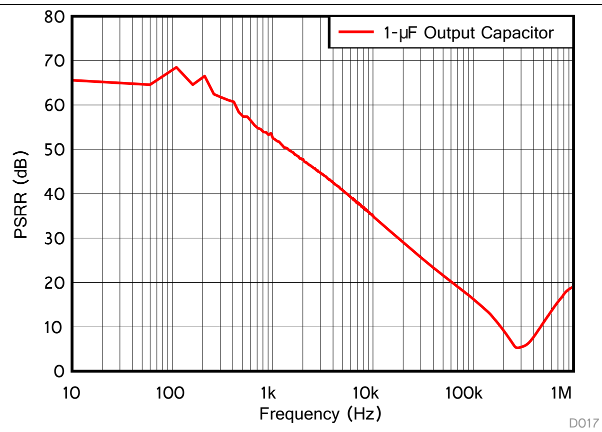
TLV74318PDBV

图 19. 1.8-V Foldback Current Limit vs I_{OUT} and Temperature



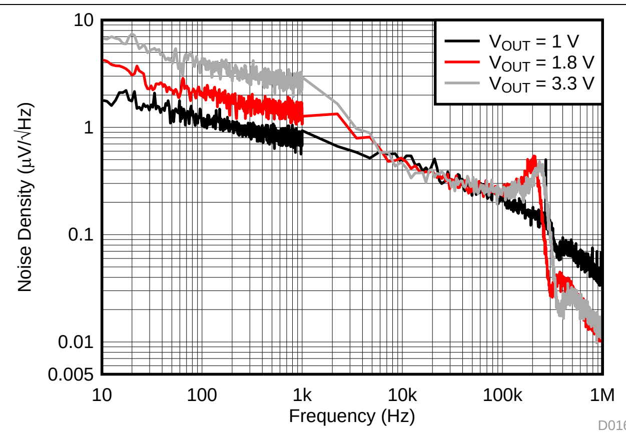
TLV74333PDBV

图 20. 3.3-V Foldback Current Limit vs I_{OUT} and Temperature



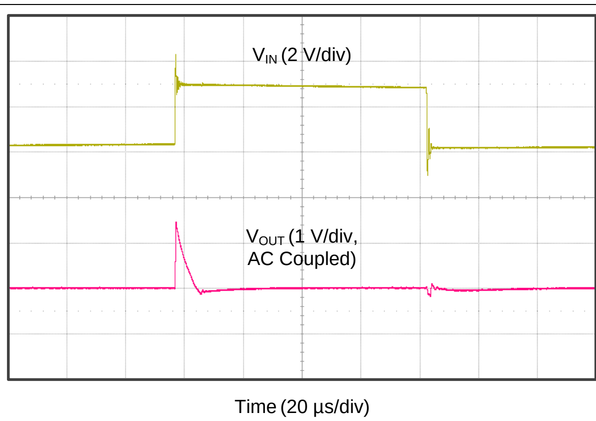
I_{OUT} = 300 mA

图 21. Power-Supply Rejection Ratio vs Frequency



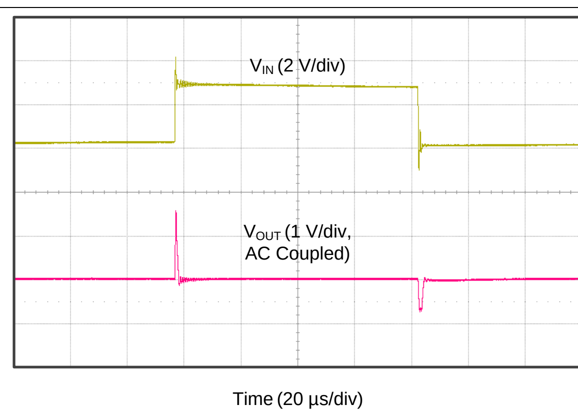
I_{OUT} = 300 mA

图 22. Output Spectral Noise Density



TLV74318PDBV, I_{OUT} = 10 mA, 1-µF output capacitor

图 23. Line Transient

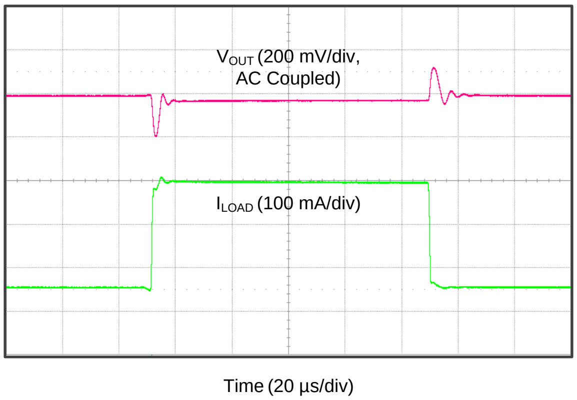


TLV74318PDBV I_{OUT} = 300 mA   1-µF output capacitor

图 24. Line Transient

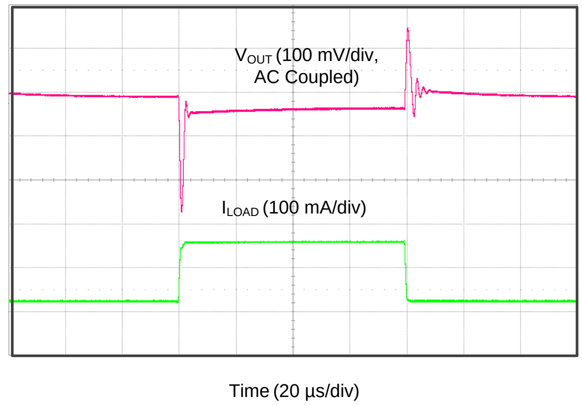
Typical Characteristics (接下页)

at operating temperature range (T_J = –40°C to +125°C), V_{IN} = V_{OUT}(nom) + 0.5 V or 2 V (whichever is greater), I_{OUT} = 1 mA, V_{EN} = V_{IN}, and C_{IN} = C_{OUT} = 1 µF (unless otherwise noted)



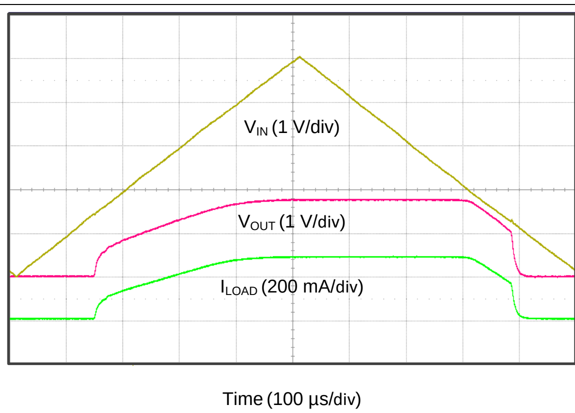
TLV74310 PDBV V_{IN} = 2 V, 1-µF output capacitor, output current slew rate = 0.25 A/µs

图 25. 1-V, 50-mA to 300-mA Load Transient



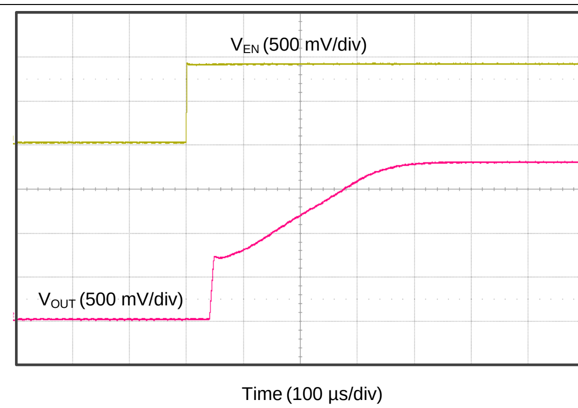
TLV74333PDBV, V_{IN} = 3.8 V,1-µF output capacitor, output current slew rate = 0.25 A/µs

图 26. 3.3 V, 50-mA to 300-mA Load Transient



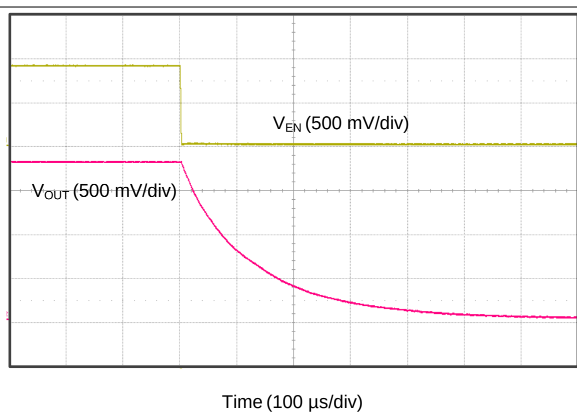
TLV74318PDBV, R_L = 6.2 Ω, V_{EN} = V_{IN}, 1-µF output capacitor

图 27. V_{IN} Power-Up and Power-Down



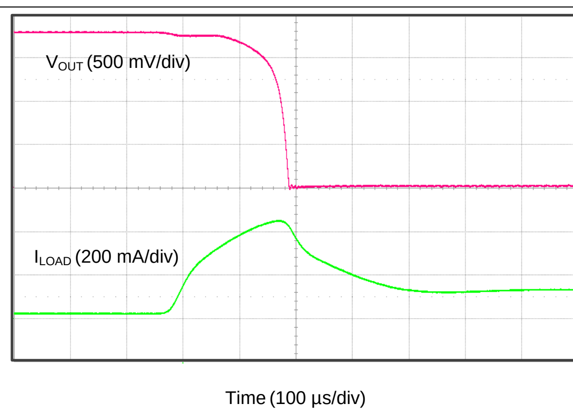
TLV74318PDBV, R_L = 6.2 Ω, 1-µF output capacitor

图 28. Startup with EN



TLV74318PDBV, I_{OUT} = 300 mA, 1-µF output capacitor

图 29. Shutdown Response With Enable



TLV74318PDBV, 1-µF output capacitor

图 30. Foldback Current Limit Response

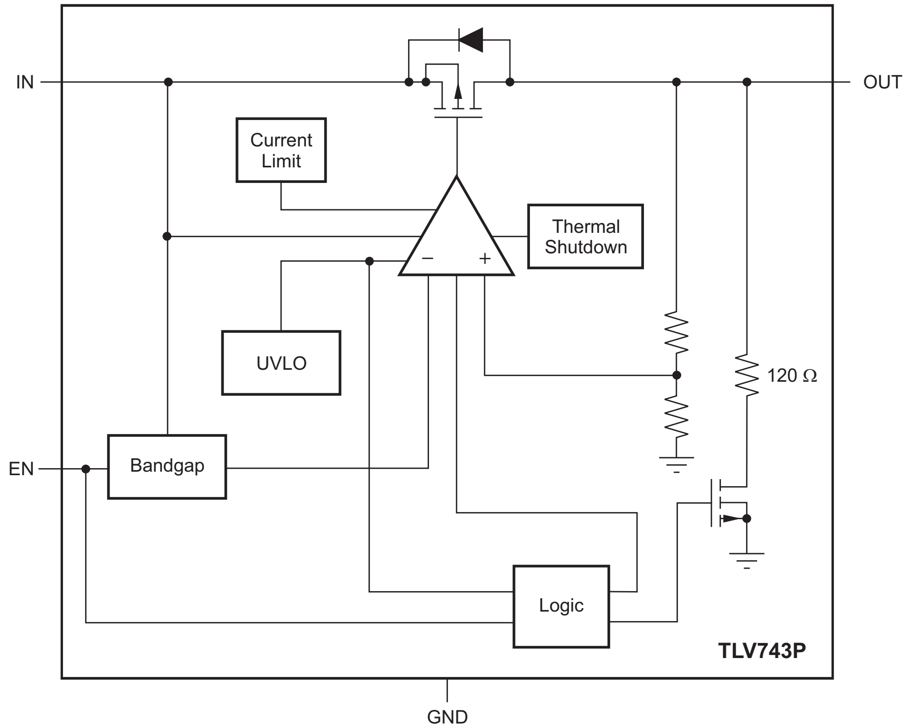
7 Detailed Description

7.1 Overview

The TLV743P device belongs to a new family of next-generation, low-dropout regulators (LDOs). This device consumes low quiescent current and delivers excellent line and load transient performance. These characteristics, combined with low noise, good PSRR with low-dropout voltage, make this device well-suited for portable consumer applications.

This regulator offers foldback current limit, shutdown, and thermal protection. The operating junction temperature for this device is –40°C to +125°C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Undervoltage Lockout (UVLO)

The TLV743P device uses an undervoltage lockout (UVLO) circuit that disables the output until the input voltage is greater than the rising UVLO voltage, $UVLO_{RISE}$. This circuit makes certain that the device does not exhibit any unpredictable behavior when the supply voltage is lower than the operational range of the internal circuitry. During UVLO disable, the output connects to ground with a 120-Ω pulldown resistor.

7.3.2 Shutdown and Output Enable

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed $V_{EN(HI)}$. Turn off the device by forcing the EN pin to drop below $V_{EN(LO)}$. If shutdown capability is not required, connect EN to IN. There is no internal pulldown resistor connected to the EN pin.

The TLV743P device has an internal pulldown MOSFET that connects a 120-Ω resistor to ground when the device is disabled. The discharge time after disabling depends on the output capacitance (C_{OUT}) and the load resistance (R_L) in parallel with the 120-Ω pulldown resistor. The time constant is calculated in 公式 1:

$$t = \frac{120 \times R_L}{120 + R_L} \times C_{OUT} \tag{1}$$

7.3.3 Internal Foldback Current Limit

The TLV743P device has an internal foldback current limit that protects the regulator during fault conditions. The current allowed through the device is reduced as the output voltage falls. When the output is shorted, the LDO supplies a typical current of 150 mA. The output voltage is not regulated when the device is in current limit. In this condition, the output voltage is the product of the regulated current and the load resistance. When the device output is shorted, the PMOS pass transistor dissipates power $[(V_{IN} – V_{OUT}) \times I_{OS}]$ until thermal shutdown is triggered and the device turns off. After the device cools down, the internal thermal shutdown circuit turns the device back on. If the fault condition continues, the device cycles between current limit and thermal shutdown. See *Thermal Information* for more details.

The foldback current limit circuit limits the current allowed through the device to current levels lower than the minimum current limit at nominal V_{OUT} current limit (I_{LIM}) during startup. See 图 18 to 图 20 for typical foldback current limit values. If the output is loaded by a constant-current load during startup, or if the output voltage is negative when the device is enabled, then the required load current by the load may exceed the foldback current limit and the device may not rise to the full output voltage. For constant current loads, disable the output load until the TLV743P has risen to the nominal output voltage.

The TLV743P PMOS pass element has an intrinsic body diode that conducts current when the voltage at the OUT pin exceeds the voltage at the IN pin. Do not force the output voltage to exceed the input voltage because excessively high current may flow through the body diode.

7.3.4 Thermal Shutdown

Thermal shutdown protection disables the output when the junction temperature rises to approximately 160°C. Disabling the device eliminates power dissipated by the device, which allows the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, which protects the device from damage as a result of overheating.

Activating the thermal shutdown feature usually indicates excessive power dissipation as a result of the product of the (V_{IN} – V_{OUT}) voltage and the load current. For reliable operation, limit junction temperature to 125°C maximum. To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The TLV743P internal protection circuitry protects against overload conditions, but is not intended to be active in normal operation. Continuously running the TLV743P device into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage has previously exceeded the UVLO rising voltage and has not decreased below the UVLO falling threshold.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage has previously exceeded the enable rising threshold voltage and not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is less than the thermal shutdown temperature.

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this condition, the output voltage is the same the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout may result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The input voltage is less than the UVLO falling voltage, or has not yet exceeded the UVLO rising threshold.
- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

When the device is disabled, the active pulldown resistor discharges the output.

表 1 lists the conditions that result in different operating modes.

表 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT}(nom) + V_{DO}$ and $V_{IN} > UVLO_{RISE}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{LIM}$	$T_J < 160°C$
Dropout mode	$UVLO_{RISE} < V_{IN} < V_{OUT}(nom) + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{LIM}$	$T_J < 160°C$
Disabled mode (any true condition disables the device)	$V_{IN} < UVLO_{FALL}$	$V_{EN} < V_{EN(LO)}$	—	$T_J > 160°C$

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Input and Output Capacitor Selection

The TLV743P device uses an advanced internal control loop to obtain stable operation with the use of input or output capacitors. An output capacitance of 1 μF or larger generally provides good dynamic response. Use X5R- and X7R-type ceramic capacitors because these capacitors have minimal variation in value and equivalent series resistance (ESR) over temperature.

Although an input capacitor is not required for stability, increased output impedance from the input supply may compromise the performance of the TLV743P. Good analog design practice is to connect a 0.1-µF to 1-µF capacitor from IN to GND. This capacitor counteracts reactive input sources and improves transient response, input ripple, and PSRR. Use an input capacitor if the source impedance is greater than 0.5 Ω. Use a higher-value capacitor if large, fast, rise-time load transients are expected, or if the device is located several inches from the input power source.

8.1.2 Dropout Voltage

The TLV743P device uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as (V_{IN} – V_{OUT}) approaches dropout operation. See 图 7 to 图 12 for typical dropout values.

Application Information (接下页)

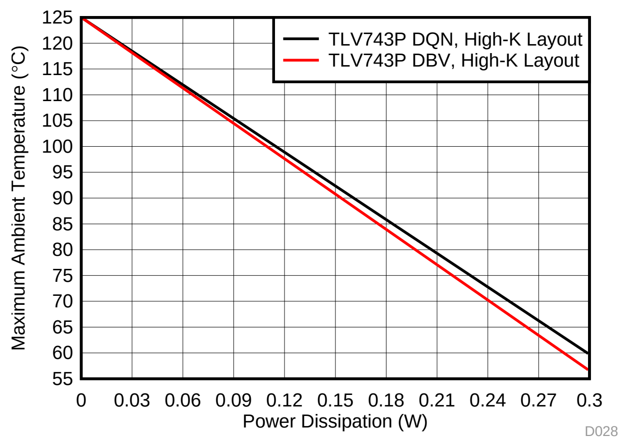
8.1.3 Power Dissipation

The ability to remove heat from the die is different for each package type and presents different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to ambient air. Performance data for JEDEC high-K boards are shown in *Thermal Information*. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves heat sink effectiveness.

Power dissipation (P_D) depends on input voltage and load conditions. P_D is equal to the product of the output current and voltage drop across the output pass element, as shown in 公式 2.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{2}$$

图 31 shows the maximum ambient temperature versus the power dissipation of the TLV743P device in the DQN and DBV packages. This figure assumes the device is soldered on JEDEC standard high-K layout with no airflow over the board. Actual board thermal impedances vary widely. If the application requires high power dissipation, it is helpful to have a thorough understanding of the board temperature and thermal impedances to make certain that the TLV743P device does not operate continuously above a junction temperature of 125°C.



TLV743P, high-K layout

图 31. Maximum Ambient Temperature vs Device Power Dissipation

8.2 Typical Application

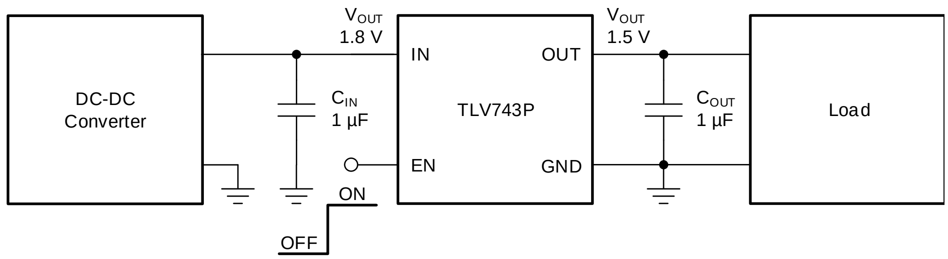


图 32. DC/DC Converter Post Regulation

8.2.1 Design Requirements

表 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	1.8 V, ±5%
Output voltage	1.5 V, ±1%
Output current	200-mA DC, 300-mA peak
Output voltage transient deviation	< 10%, 1-A/µs load step from 50 mA to 200 mA
Maximum ambient temperature	85°C

8.2.2 Detailed Design Procedure

Input and output capacitors are required to achieve the output voltage transient requirements. Capacitance values of 1 µF are selected to give the maximum output capacitance in a small, low-cost package.

图 7 shows the 1.2-V option dropout voltage. Given that dropout voltages are higher for lower output-voltage options, and given that the 1.2-V option dropout voltage is typically less than 300 mV at 125°C, then the 1.5-V option dropout voltage is typically less than 300 mV at 125°C.

See 图 31 to verify that the maximum junction temperature is not exceeded.

8.2.3 Application Curve

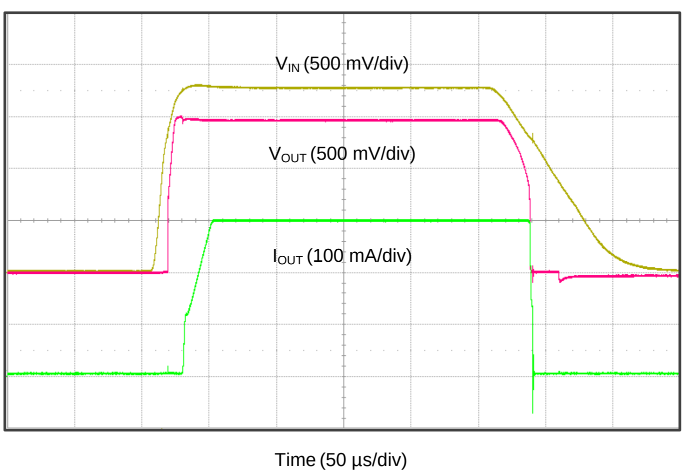


图 33. 1.8-V to 1.5-V Regulation at 300 mA

9 Power Supply Recommendations

Connect a low-output impedance power supply directly to the IN pin of the TLV743P device. Inductive impedances between the input supply and the IN pin can create significant voltage excursions at the IN pin during startup or load transient events. If inductive impedances are unavoidable, use an input capacitor.

10 Layout

10.1 Layout Guidelines

- Place input and output capacitors as close as possible to the device.
- Use copper planes for device connections to optimize thermal performance.
- Place thermal vias around the device to distribute heat.

10.2 Layout Examples

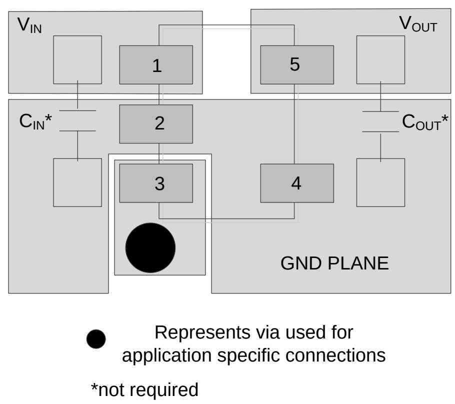
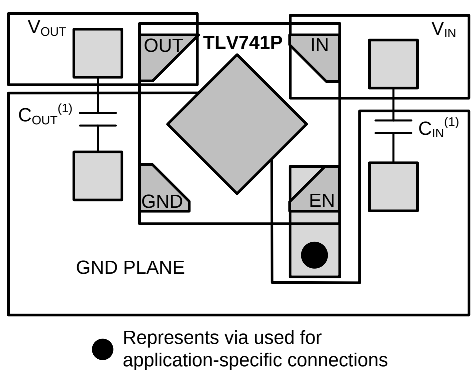


图 34. Layout Example: DBV Package



(1) Not required.

图 35. X2SON Layout Example

11 器件和文档支持

11.1 器件支持

11.1.1 开发支持

11.1.1.1 评估模块

我们为您提供了评估模块 (EVM)，可以借此来对使用 TLV743P 器件时的电路性能进行初始评估。TLV73312PEVM-643 评估模块（和相关的用户指南）可在德州仪器 (TI) 网站上的产品文件夹中获取，也可直接从 TI 网上商店购买。

11.1.2 器件命名规则

表 3. 器件命名规则 (1)(2)

产品	V_{OUT}
TLV743P**xx(x)Pyyyz(3)**	**xx(x)** 为标称输出电压。对于分辨率为 100mV 的输出电压，订货编号中使用两位数字；否则，使用三位数字（例如，28 = 2.8V；125 = 1.25V）。 **P** 表示有源输出放电功能。TLV743 系列的所有产品在器件处于禁用状态时都可以对输出进行主动放电。 **yyy** 为封装标识符。 **z** 为封装数量。R 表示卷（3000 片），T 表示带（250 片）。 **(3)** 表示其他卷带方向。3 表示引脚 1 位于第 3 象限中。请参阅*封装材料信息* 附录，获取更多信息。

(1) 要获得最新的封装和订货信息，请参阅本文档末尾的封装选项附录，或者访问器件产品文件夹（www.ti.com.cn）。
(2) 可提供 1V 至 3.3V 范围内的输出电压（以 50mV 为单位增量）。有关器件的详细信息和供货情况，请联系制造商。

11.2 文档支持

11.2.1 相关文档

《TLV73312PDQN-643 评估模块用户指南》（文献编号：SBVU024）

11.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

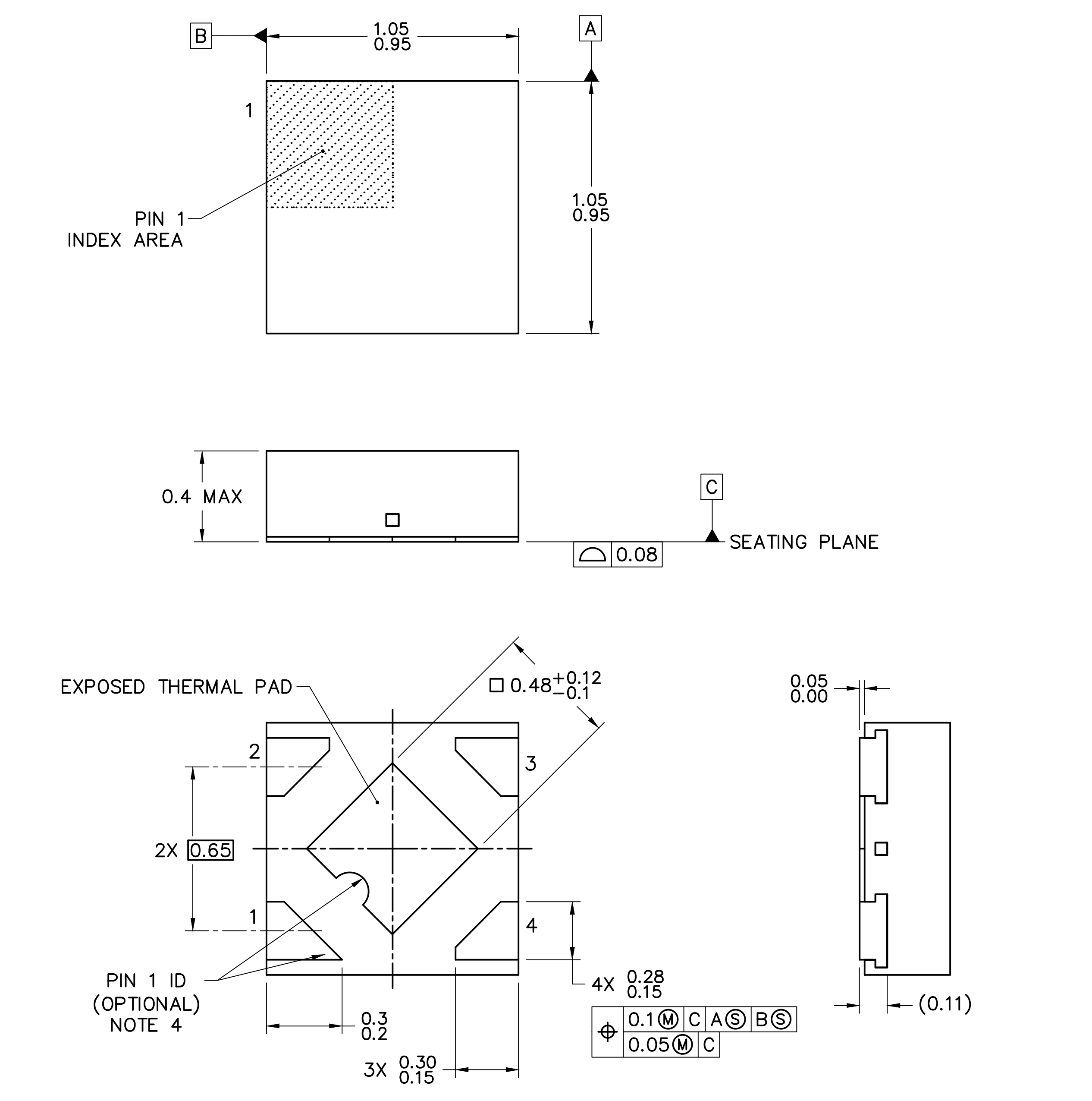
以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGE OUTLINE

DQN0004A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



4215302/D 06/2016

NOTES:

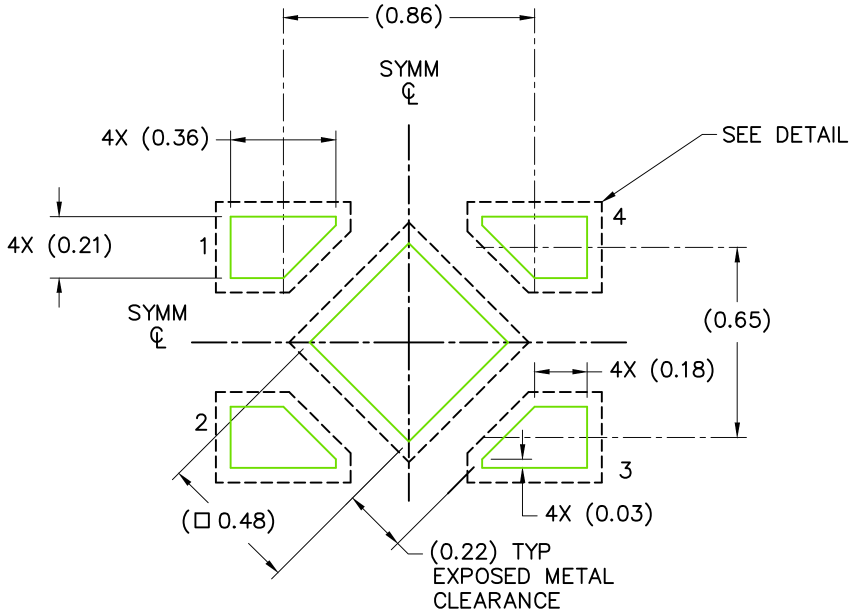
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.

EXAMPLE BOARD LAYOUT

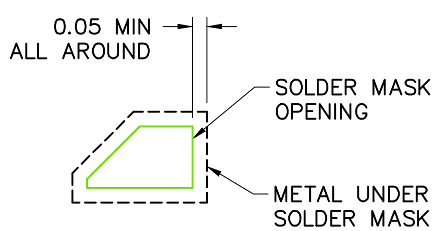
DQN0004A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE: 40X



SOLDER MASK
DEFINED

SOLDER MASK DETAIL

4215302/D 06/2016

NOTES: (continued)

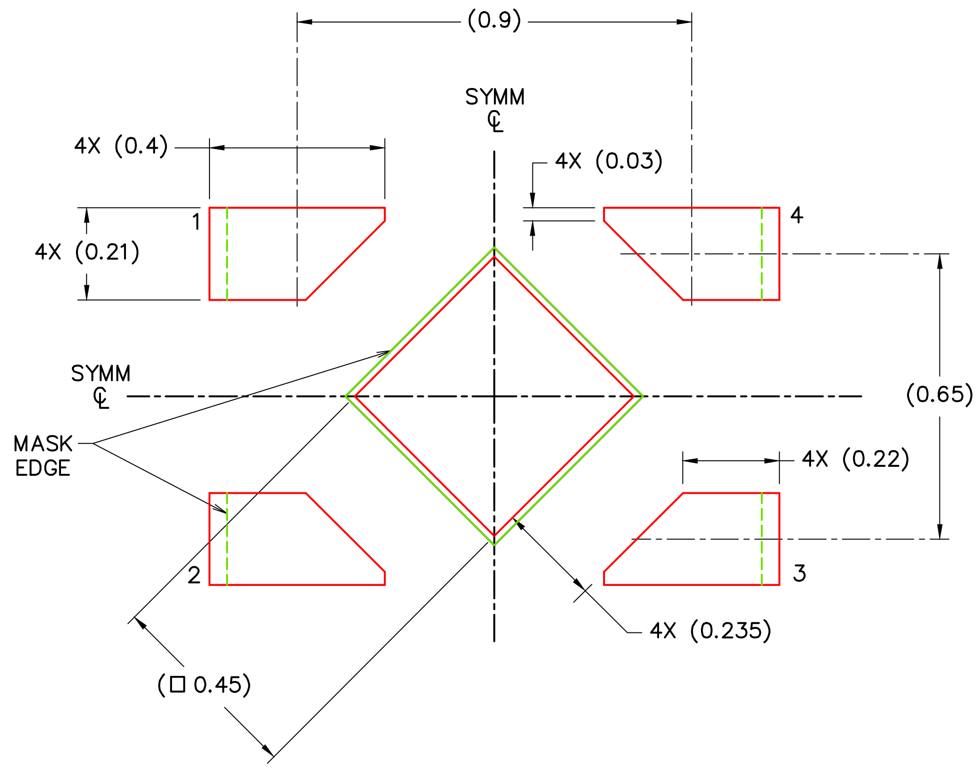
5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
6. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DQN0004A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1mm THICK STENCIL

EXPOSED PAD
88% PRINTED SOLDER COVERAGE BY AREA
SCALE: 60X

4215302/D 06/2016

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV743105PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1NGT	Samples
TLV74310PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1CCT	Samples
TLV74310PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8U	Samples
TLV74311PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1DAT	Samples
TLV74311PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8W	Samples
TLV74312PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1DBT	Samples
TLV74312PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8X	Samples
TLV74315PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1DCT	Samples
TLV74315PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8Z	Samples
TLV74318PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1D7T	Samples
TLV74318PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	9A	Samples
TLV74318PDQNR3	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	9A	Samples
TLV74325PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1DDT	Samples
TLV74325PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	9B	Samples
TLV743285PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1DET	Samples
TLV743285PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	9C	Samples
TLV74328PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1DFT	Samples
TLV74328PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	9D	Samples
TLV74328PDQNR1	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	9D	Samples
TLV74330PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1DGT	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV74330PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	9E	Samples
TLV74333PDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1CBT	Samples
TLV74333PDQNR	ACTIVE	X2SON	DQN	4	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	9F	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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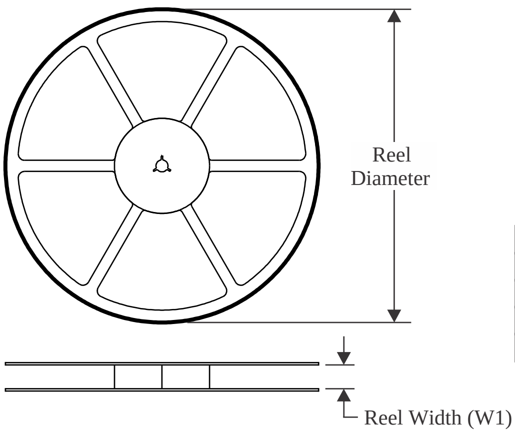
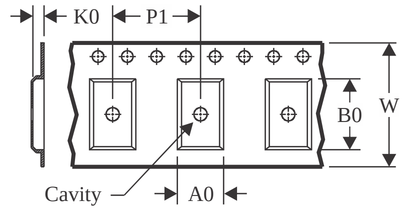
TAPE AND REEL INFORMATION

REEL DIMENSIONS

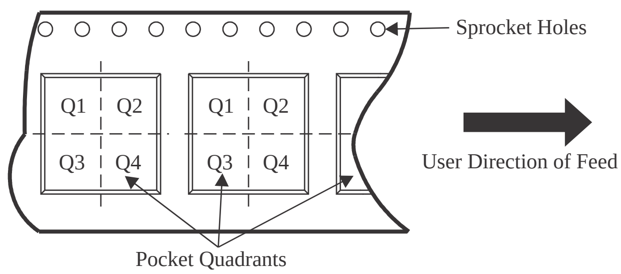


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

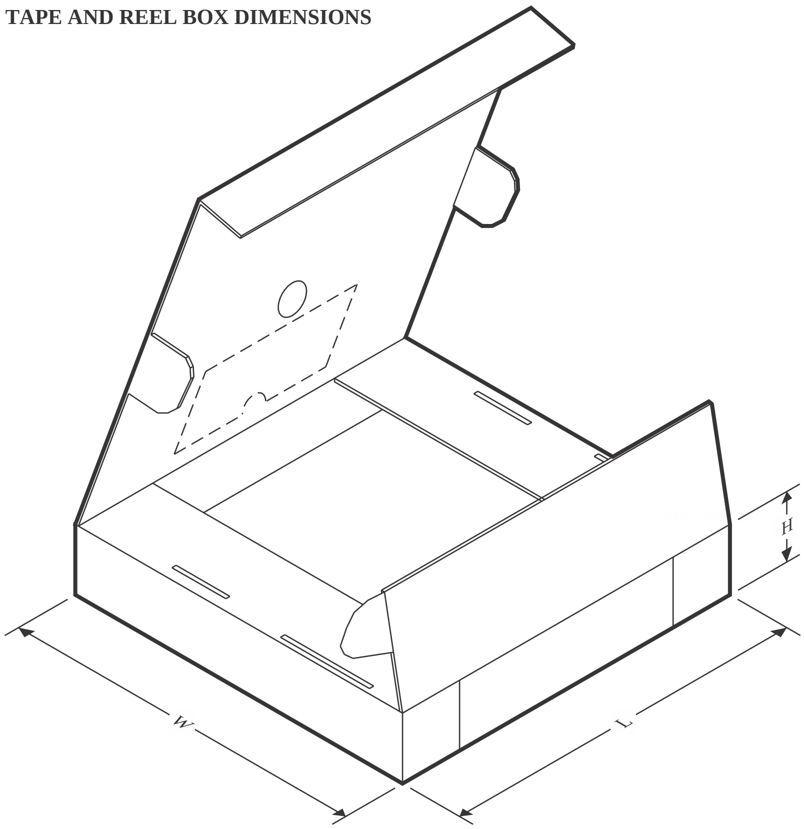


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV743105PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV74310PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV74310PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74311PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV74311PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74312PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV74312PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74315PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV74315PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74318PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV74318PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74318PDQNR3	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q3
TLV74325PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV74325PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV743285PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV743285PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV74328PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV74328PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74328PDQNR1	X2SON	DQN	4	3000	180.0	9.5	1.16	1.16	0.5	4.0	8.0	Q1
TLV74330PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV74330PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2
TLV74333PDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV74333PDQNR	X2SON	DQN	4	3000	180.0	8.4	1.16	1.16	0.5	4.0	8.0	Q2

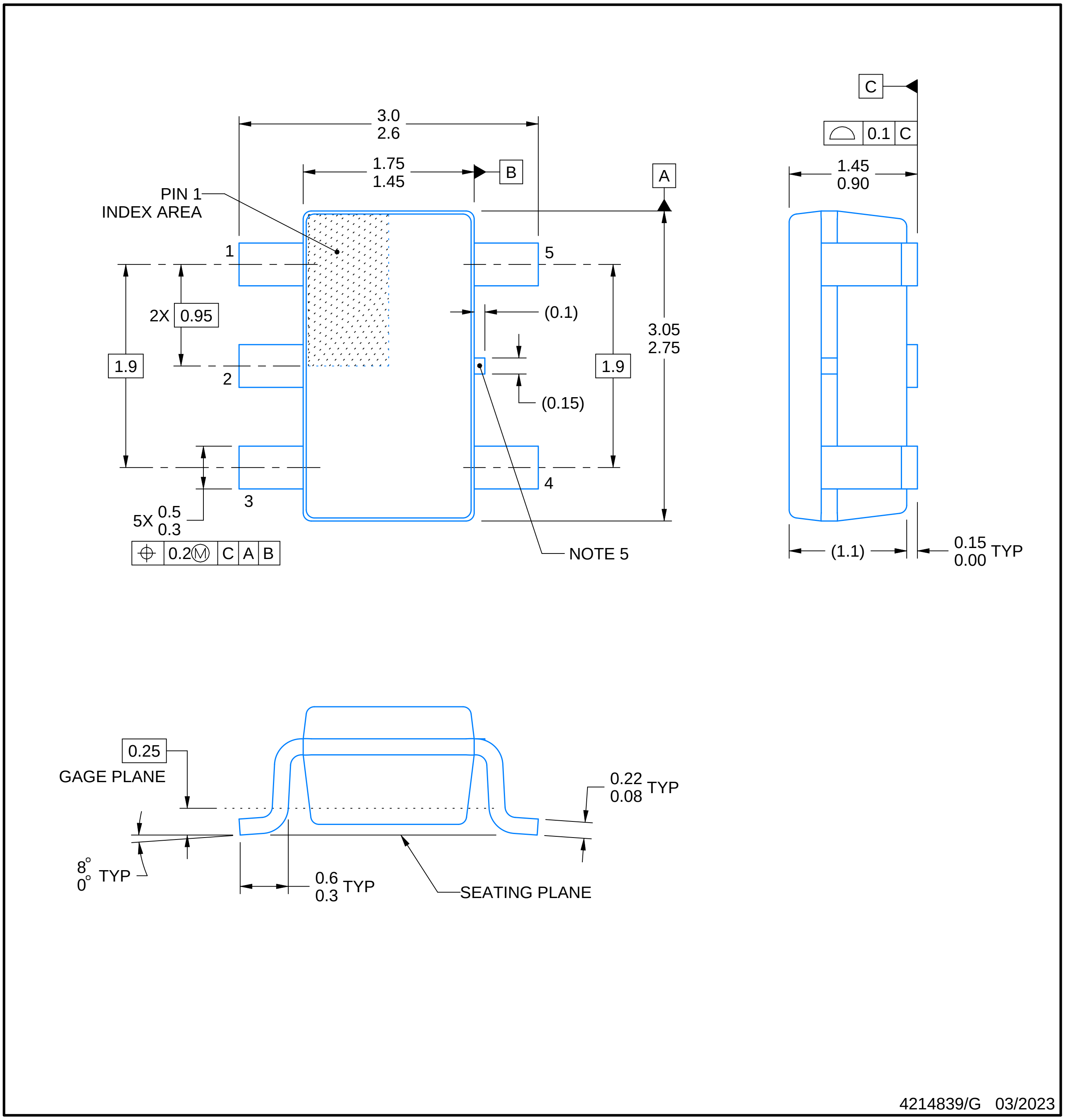
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV743105PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV74310PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV74310PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74311PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV74311PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74312PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV74312PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74315PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV74315PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74318PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV74318PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74318PDQNR3	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV74325PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV74325PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV743285PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV743285PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74328PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV74328PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0

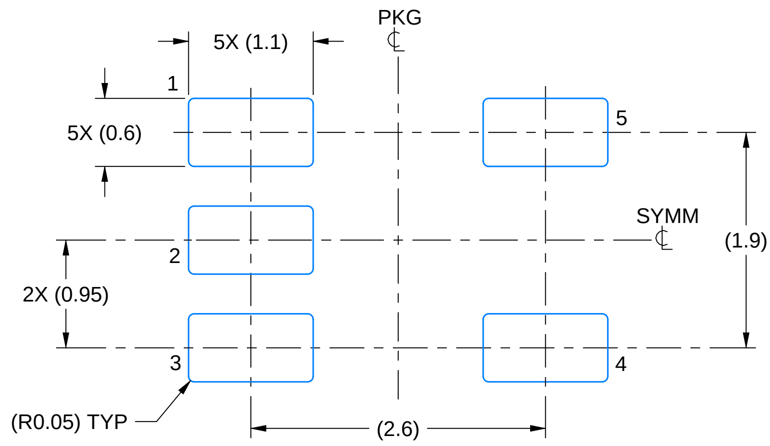
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV74328PDQNR1	X2SON	DQN	4	3000	184.0	184.0	19.0
TLV74330PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV74330PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0
TLV74333PDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV74333PDQNR	X2SON	DQN	4	3000	210.0	185.0	35.0



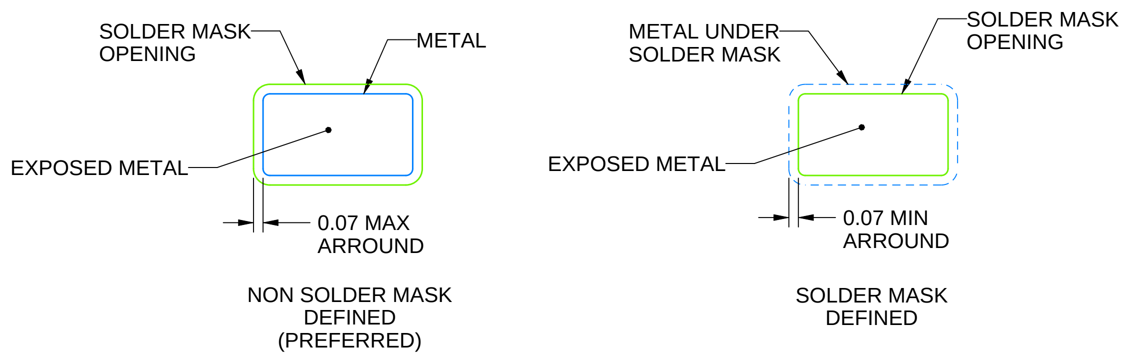
4214839/G 03/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

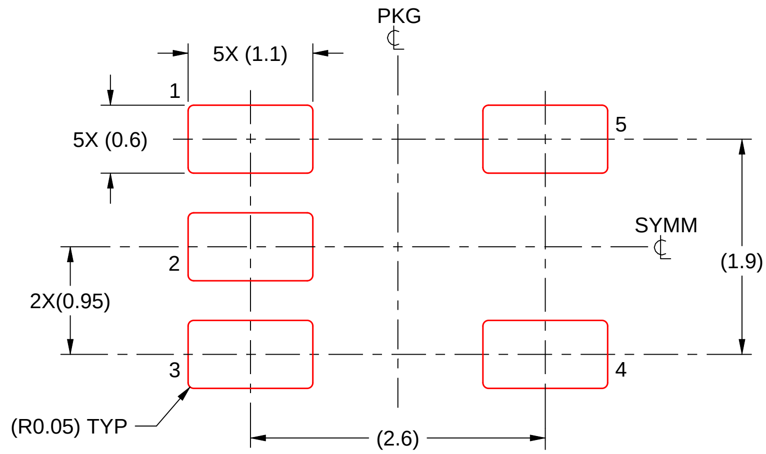


SOLDER MASK DETAILS

4214839/G 03/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/G 03/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

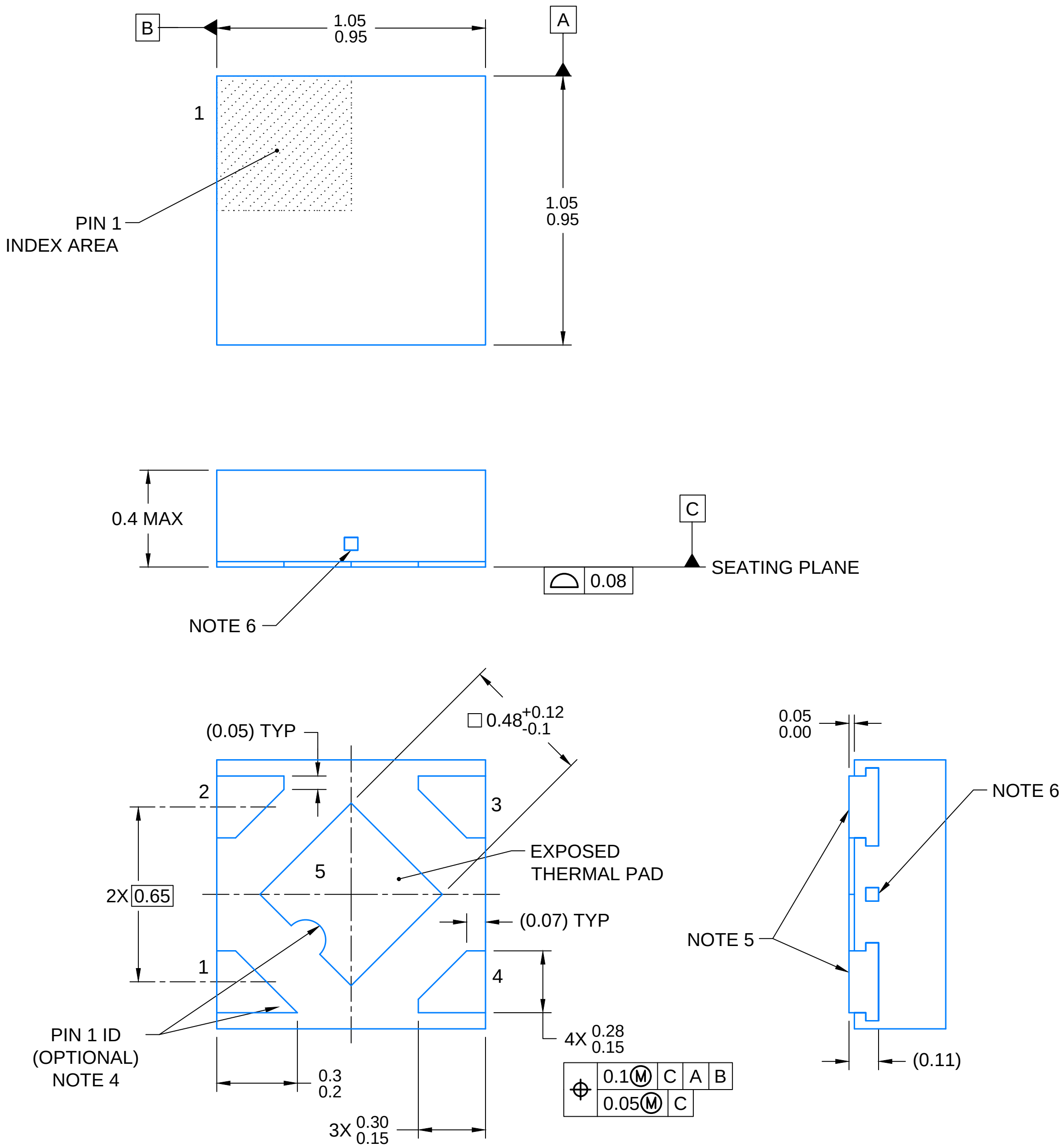
DQN 4

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

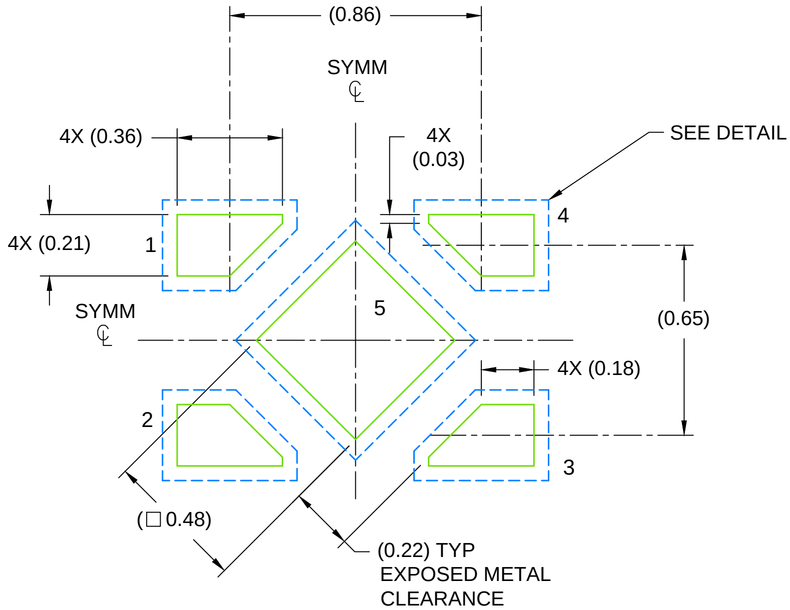
4210367/F



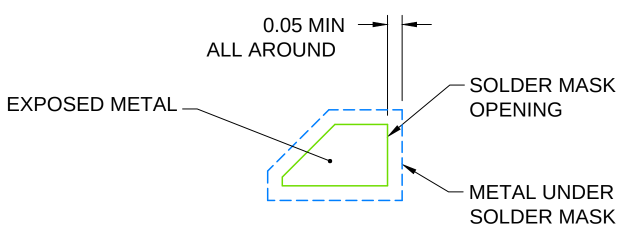
4215302/E 12/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.
4. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.
5. Shape of exposed side leads may differ.
6. Number and location of exposed tie bars may vary.



LAND PATTERN EXAMPLE
SCALE: 40X



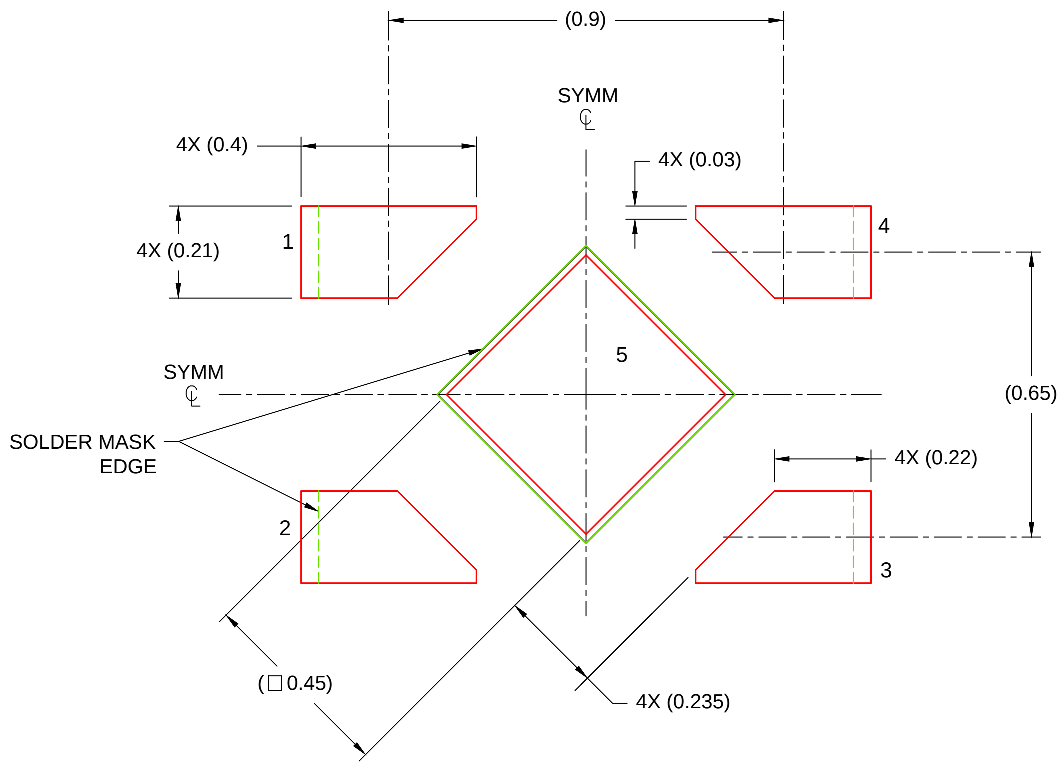
SOLDER MASK
DEFINED

SOLDER MASK DETAIL

4215302/E 12/2016

NOTES: (continued)

7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
8. If any vias are implemented, it is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1mm THICK STENCIL

EXPOSED PAD
88% PRINTED SOLDER COVERAGE BY AREA
SCALE: 60X

4215302/E 12/2016

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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