

TLV9051/TLV9052/TLV9054 5MHz 15V/ μ s 高压摆率 RRIO 运算放大器

1 特性

- 高压摆率：15V/ μ s
- 低静态电流：330 μ A
- 轨至轨输入和输出
- 低输入失调电压： ± 0.33 mV
- 单位增益带宽：5MHz
- 低宽带噪声：15 nV/ $\sqrt{\text{Hz}}$
- 低输入偏置电流：2pA
- 单位增益稳定
- 内置 RFI 和 EMI 滤波器
- 适用于低成本应用的可扩展 CMOS 运算放大器系列
- 可在电源电压低至 1.8V 的情况下运行
- 工作温度范围：-40°C 至 125°C

2 应用

- HVAC：暖通空调
- 光电二极管放大器
- 用于实现直流电机控制的电流分流监控
- 白色家电（冰箱、洗衣机等）
- 传感器信号调节
- 有源滤波器
- 低侧电流检测

3 说明

TLV9051、TLV9052 和 TLV9054 器件分别为单通道、双通道和四通道的运算放大器。这些器件旨在 1.8V 至 6.0V 的低电压下运行。它们可以在非常高的压摆率下实现轨到轨输入和输出。这些器件非常适合需要低工作电压、高压摆率和低静态电流的成本受限应用。TLV905x 系列的容性负载驱动器具有 150pF 的电容，而电阻式开环输出阻抗使其能够在更高的容性负载下更轻松地实现稳定。

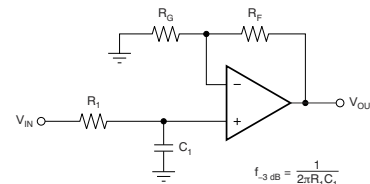
TLV905xS 器件具有关断模式，允许放大器切换至典型电流消耗低于 1 μ A 的待机模式。

TLV905x 系列易于使用，因为它具有稳定的单位增益，集成了 RFI 和 EMI 滤波器，且不会在过驱动情况下出现相位反转。

器件信息(1)

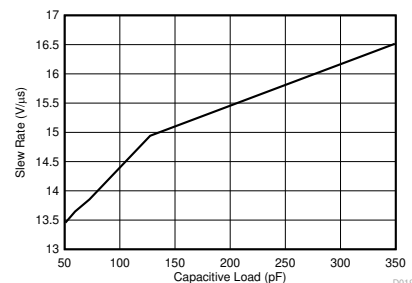
器件型号	封装	封装尺寸 (标称值)
TLV9051	SOT-23 (5)	1.60mm × 2.90mm
	SC70 (5)	1.25mm × 2.00mm
	SOT553 (5) ⁽²⁾	1.65mm × 1.20mm
	X2SON (5)	0.80mm × 0.80mm
TLV9051S	SOT-23 (6)	1.60mm × 2.90mm
TLV9052	SOIC (8)	3.91mm × 4.90mm
	TSSOP (8)	3.00mm × 4.40mm
	VSSOP (8)	3.00mm × 3.00mm
	SOT-23 (8)	1.60mm × 2.90mm
	WSON (8)	2.00mm × 2.00mm
TLV9052S	VSSOP (10)	3.00mm × 3.00mm
	X2QFN (10)	1.50mm × 2.00mm
TLV9054	SOIC (14)	8.65mm × 3.91mm
	TSSOP (14)	4.40mm × 5.00mm
	X2QFN (14)	2.00mm × 2.00mm
	WQFN (16)	3.00mm × 3.00mm
TLV9054S	WQFN (16)	3.00mm × 3.00mm

- (1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
 (2) 封装仅为预发布版。



$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right) \left(\frac{1}{1 + sR_1 C_1}\right)$$

单极低通滤波器



压摆率与负载电容间的关系



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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision H (October 2019) to Revision I (November 2022)	Page
• 将绝对最大额定值中的最大电源电压从 6V 更改为 7V.....	11
• 添加了输入偏置电流和输入失调电流的最大值.....	13
Changes from Revision G (September 2019) to Revision H (October 2019)	Page
• Added new human-body model and charged-device model ratings for TLV9051 X2SON package to the <i>ESD Ratings</i>	11
• Added <i>Packages With an Exposed Thermal Pad</i> section to <i>Feature Description</i> section.....	24
Changes from Revision F (June 2019) to Revision G (September 2019)	Page
• 删除了所有 TLV9051 封装的预发布标记.....	1
• 删除了 TLV9052 SOT-23 (8) - DDF 封装的预发布标记.....	1
• Added link to <i>Shutdown Function</i> section in all of the SHDN pin function rows.....	5
• Added <i>EMI Rejection</i> section to <i>Feature Description</i> section.....	23
• Added clarification to the <i>Shutdown Function</i> section.....	25
Changes from Revision E (May 2019) to Revision F (June 2019)	Page
• 删除了器件信息中 TLV9052S 器件的封装预发布标记.....	1
• Deleted package preview notation for TLV9052S devices under <i>Device Comparison Table</i>	4
• Deleted preview notation for TLV9052S devices in <i>Device Comparison Table</i>	4
• Deleted package preview notation for TLV9052S in <i>Pin Configuration and Functions</i> section.....	5
• Deleted package preview notation for TLV9052S under <i>Thermal Information for Dual Channel</i>	12
Changes from Revision D (April 2019) to Revision E (May 2019)	Page
• Added DDF (SOT-23) information to <i>Thermal Information for Dual Channel</i> table.....	12
Changes from Revision C (April 2019) to Revision D (April 2019)	Page
• 删除了器件信息中 TLV9054/S 器件的预发布标记.....	1

• Deleted preview notations for TLV9054 devices in <i>Device Comparison Table</i>	4
• Deleted preview notations for TLV9054S device in <i>Device Comparison Table</i>	4
• Deleted preview notations for TLV9054 packages in <i>Pin Configurations and Functions</i> section.....	5
• Deleted preview notation for TLV9054S RTE package in <i>Pin Configurations and Functions</i> section.....	5
• Deleted preview notation for TLV9054/S packages in <i>Thermal Information for Quad Channel</i>	12

Changes from Revision B (March 2019) to Revision C (April 2019) Page

• Added TLV9051 thermal information for DPW, DBV, and DCK packages.....	11
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Changes from Revision A (December 2018) to Revision B (March 2019) Page

• 向 <i>说明</i> 部分添加了关断器件说明.....	1
• 向 <i>器件信息</i> 中添加了 SOT-23 (8) 封装.....	1
• 向 <i>器件信息</i> 中添加了关断器件.....	1
• 向 TLV9054 <i>器件信息</i> 中添加了 X2QFN (RUC) 封装.....	1
• Added DDF package information to <i>Device Comparison Table</i>	4
• Added Shutdown devices (TLV9051S/TLV9052S/TLV9054S) and packages (DGS/RUG/RTE) to <i>Device Comparison Table</i>	4
• Added DDF (SOT-23) package.....	5
• Added TLV9051S pinout information to <i>Pin Configurations and Functions</i> section.....	5
• Added TLV9052S pinout information to <i>Pin Configurations and Functions</i> section.....	5
• Added TLV9054S and TLV9054 X2QFN (RUC) pinout information to <i>Pin Configurations and Functions</i> section.....	5
• Added TLV9051 and TLV9051S thermal information to <i>Thermal Information for Single Channel</i>	11
• Added TLV9052S thermal info to <i>Thermal Information for Dual Channel</i>	12
• Added DDF (SOT-23) package to <i>Thermal Information for Dual Channel</i>	12
• Added TLV9054 and TLV9054S thermal information to <i>Thermal Information for Quad Channel</i>	12
• Added Shutdown Function information in <i>Feature Description</i> section.....	25
• Added "S" suffix to <i>Related Links</i> to reflect the addition of Shutdown devices.....	31

Changes from Revision * (August 2018) to Revision A (December 2018) Page

• 将器件状态从 <i>预告信息</i> 更改为 <i>量产数据</i>	1
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5 Device Comparison Table

DEVICE	NO. OF CH.	PACKAGE LEADS												
		SC70 DCK	SOT-23 DBV	SOT-553 (1) DRL	X2SON DPW	SOIC D	WSO DSG	VSSOP DGK	TSSOP PW	SOT-23 DDF	VSSOP DGS	X2QFN RUG	X2QFN RUC	WQFN RTE
TLV9051	1	5	5	5	5	—	—	—	—	—	—	—	—	—
TLV9051S		—	6	—	—	—	—	—	—	—	—	—	—	—
TLV9052	2	—	—	—	—	8	8	8	8	8	—	—	—	—
TLV9052S		—	—	—	—	—	—	—	—	—	10	10	—	—
TLV9054	4	—	—	—	—	14	—	—	14	—	—	—	14	16
TLV9054S		—	—	—	—	—	—	—	—	—	—	—	—	16

(1) Package is for preview only.

6 Pin Configuration and Functions

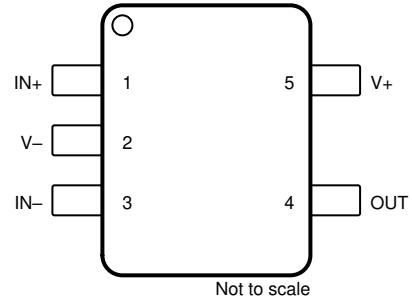
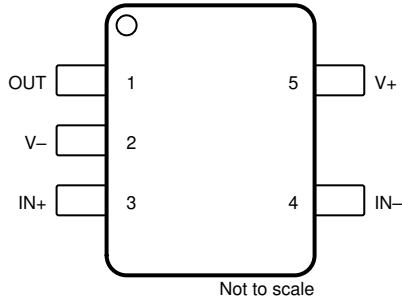


图 6-1. TLV9051 DBV, DRL Packages 5-Pin SOT-23, 图 6-2. TLV9051 DCK Package 5-Pin SC70 Top View SOT-553 Top View

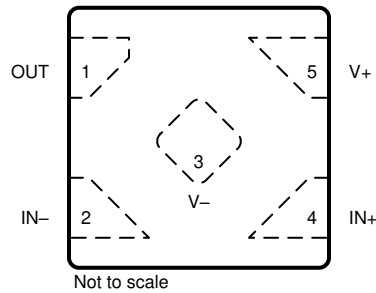


图 6-3. TLV9051 DPW Package 5-Pin X2SON Top View

表 6-1. Pin Functions: TLV9051

NAME	PIN			I/O	DESCRIPTION
	SOT-23, SOT-553	SC-70	X2SON		
IN -	4	3	2	I	Inverting input
IN+	3	1	4	I	Noninverting input
OUT	1	4	1	O	Output
V -	2	2	3	—	Negative (low) supply or ground (for single-supply operation)
V+	5	5	5	—	Positive (high) supply

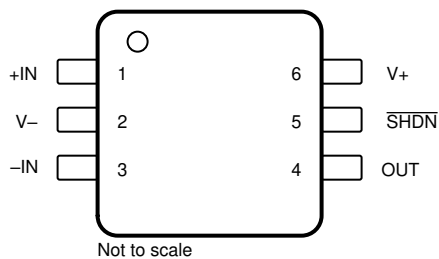


图 6-4. TLV9051S DBV Package 6-Pin SOT-23 Top View

表 6-2. Pin Functions: TLV9051S

PIN		I/O	DESCRIPTION
NAME	NO.		
- IN	4	I	Inverting input
+IN	3	I	Noninverting input
OUT	1	O	Output
SHDN	5	I	Shutdown: low = amp disabled, high = amp enabled. See § 8.3.9 for more information.
V -	2	—	Negative (lowest) supply or ground (for single-supply operation).
V+	6	—	Positive (highest) supply

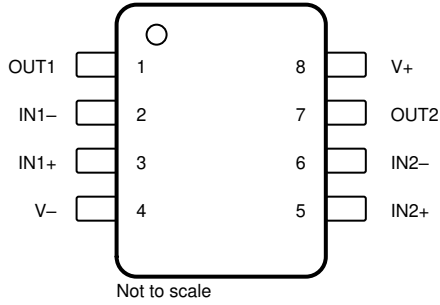
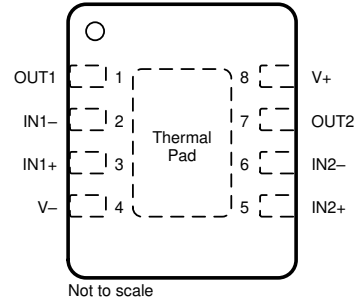


图 6-5. TLV9052 D, DGK, PW, DDF Packages 8-Pin SOIC, VSSOP, TSSOP, SOT-23 Top View

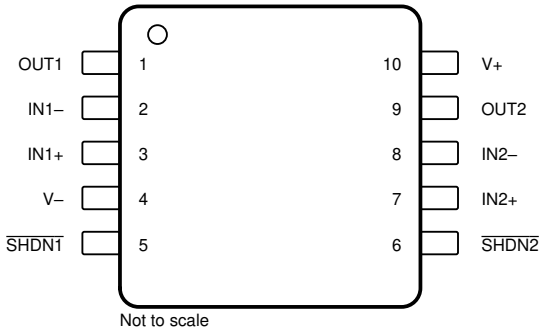


Connect exposed thermal pad to V₋. See [节 8.3.6](#) for more information.

图 6-6. TLV9052 DSG Package 8-Pin WSON With Exposed Thermal Pad Top View

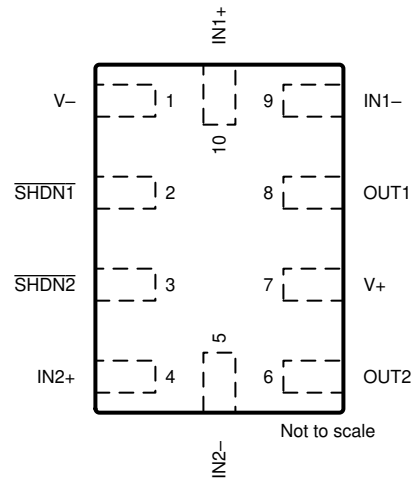
表 6-3. Pin Functions: TLV9052

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1 -	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2 -	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V -	4	—	Negative (low) supply or ground (for single-supply operation)
V+	8	—	Positive (high) supply



Not to scale

图 6-7. TLV9052S DGS Package 10-Pin VSSOP Top View



Not to scale

图 6-8. TLV9052S RUG Package 10-Pin X2QFN Top View

表 6-4. Pin Functions: TLV9052S

PIN			I/O	DESCRIPTION
NAME	VSSOP	X2QFN		
IN1 -	2	9	I	Inverting input, channel 1
IN1+	3	10	I	Noninverting input, channel 1
IN2 -	8	5	I	Inverting input, channel 2
IN2+	7	4	I	Noninverting input, channel 2
OUT1	1	8	O	Output, channel 1
OUT2	9	6	O	Output, channel 2
SHDN1	5	2	I	Shutdown: low = amp disabled, high = amp enabled, channel 1. See § 8.3.9 for more information.
SHDN2	6	3	I	Shutdown: low = amp disabled, high = amp enabled, channel 2. See § 8.3.9 for more information.
V -	4	1	—	Negative (low) supply or ground (for single-supply operation)
V+	10	7	—	Positive (high) supply

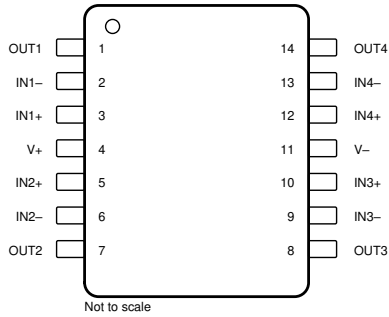


图 6-9. TLV9054 D, PW Packages 14-Pin SOIC, TSSOP Top View

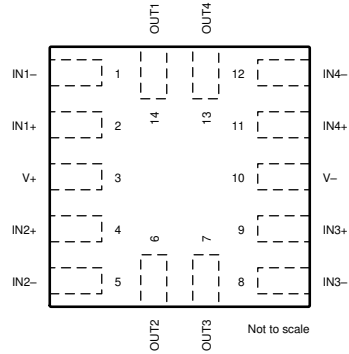
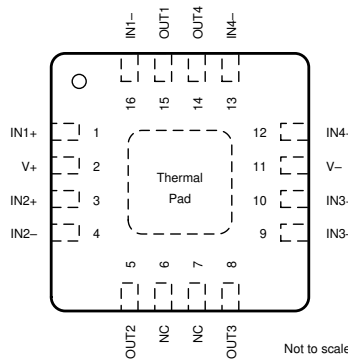


图 6-10. TLV9054 RUC Package 14-Pin X2QFN Top View

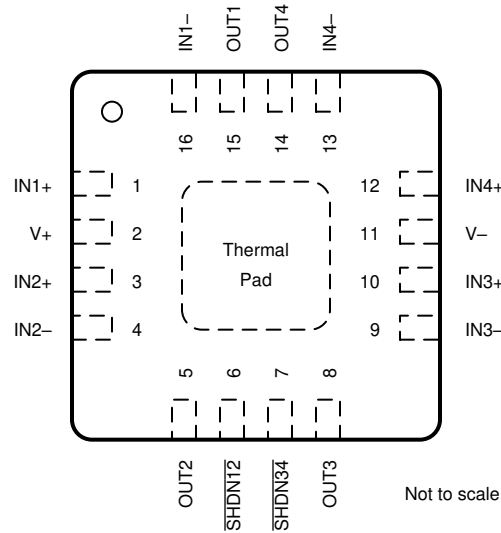


Connect exposed thermal pad to V₋. See [§ 8.3.6](#) for more information.

图 6-11. TLV9054 RTE Package 16-Pin WQFN With Exposed Thermal Pad Top View

表 6-5. Pin Functions: TLV9054

NAME	PIN			I/O	DESCRIPTION
	SOIC, TSSOP	WQFN	X2QFN		
IN1 -	2	16	1	I	Inverting input, channel 1
IN1+	3	1	2	I	Noninverting input, channel 1
IN2 -	6	4	5	I	Inverting input, channel 2
IN2+	5	3	4	I	Noninverting input, channel 2
IN3 -	9	9	8	I	Inverting input, channel 3
IN3+	10	10	9	I	Noninverting input, channel 3
IN4 -	13	13	12	I	Inverting input, channel 4
IN4+	12	12	11	I	Noninverting input, channel 4
NC	—	6, 7	—	—	No internal connection
OUT1	1	15	14	O	Output, channel 1
OUT2	7	5	6	O	Output, channel 2
OUT3	8	8	7	O	Output, channel 3
OUT4	14	14	13	O	Output, channel 4
V -	11	11	10	—	Negative (low) supply or ground (for single-supply operation)
V+	4	2	3	—	Positive (high) supply



Connect exposed thermal pad to V₋. See [§ 8.3.6](#) for more information.

图 6-12. TLV9054S RTE Package 16-Pin WQFN With Exposed Thermal Pad Top View

表 6-6. Pin Functions: TLV9054S

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1+	1	I	Noninverting input, channel 1
IN1 -	16	I	Inverting input, channel 1
IN2+	3	I	Noninverting input, channel 2
IN2 -	4	I	Inverting input, channel 2
IN3+	10	I	Noninverting input, channel 3
IN3 -	9	I	Inverting input, channel 3
IN4+	12	I	Noninverting input, channel 4
IN4 -	13	I	Inverting input, channel 4
SHDN12	6	I	Shutdown: low = amp disabled, high = amp enabled, channel 1 and 2. See § 8.3.9 for more information.
SHDN34	7	I	Shutdown: low = amp disabled, high = amp enabled, channel 3 and 4. See § 8.3.9 for more information.
OUT1	15	O	Output, channel 1
OUT2	5	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
V -	11	—	Negative (low) supply or ground (for single-supply operation)
V+	2	—	Positive (high) supply

7 Specifications

7.1 绝对最大额定值

在自然通风温度下测得 (除非另有说明) ⁽¹⁾

			最小值	最大值	单位
电源电压				7	V
信号输入引脚	电压 ⁽²⁾	共模	(V-) - 0.5	(V+) + 0.5	V
		差分		(V+) - (V-) + 0.2	
	电流 ⁽²⁾		-10	10	mA
输出短路 ⁽³⁾			连续		mA
温度	额定温度, T _A		-40	125	°C
	结温, T _J			150	
	贮存温度, T _{stg}		-65	150	

- (1) 应力超出绝对最大额定值下列出的值可能会对器件造成永久损坏。这些仅为压力额定值, 并不表示器件在这些条件下以及在建议运行条件以外的任何其他条件下能够正常运行。长时间处于绝对最大额定条件下可能会影响器件的可靠性。
- (2) 输入引脚被二极管钳制至电源轨。对于摆幅能超过电源轨 0.5V 的输入信号, 应将其电流限制在 10mA 或者更低。
- (3) 接地短路, 每个封装对应一个放大器。

7.2 ESD Ratings

			VALUE	UNIT
TLV9051 X2SON PACKAGE				
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500	
ALL OTHER PACKAGES				
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _S	Supply voltage, V _S = (V+) - (V-)	1.8	6.0	V
V _{IN}	Input pin voltage	(V-) - 0.1	(V+) + 0.1	V
	Specified temperature	-40	125	°C

7.4 Thermal Information for Single Channel

THERMAL METRIC ⁽¹⁾	TLV9051, TLV9051S					UNIT	
	DPW (X2SON)	DBV (SOT-23)		DCK (SC70)	DRL (SOT553) ⁽²⁾		
	5 PINS	5 PINS	6 PINS	5 PINS	5 PINS		
R _{θJA}	Junction-to-ambient thermal resistance	470.0	228.1	210.8	231.2	TBD	°C/W
R _{θJC(top)}	Junction-to-case(top) thermal resistance	211.9	152.1	152.1	144.4	TBD	°C/W
R _{θJB}	Junction-to-board thermal resistance	334.8	97.7	92.3	78.6	TBD	°C/W
ψ _{JT}	Junction-to-top characterization parameter	29.8	74.1	76.2	51.3	TBD	°C/W
ψ _{JB}	Junction-to-board characterization parameter	333.2	97.3	92.1	78.3	TBD	°C/W

THERMAL METRIC ⁽¹⁾		TLV9051, TLV9051S					UNIT
		DPW (X2SON)	DBV (SOT-23)		DCK (SC70)	DRL (SOT553) ⁽²⁾	
		5 PINS	5 PINS	6 PINS	5 PINS	5 PINS	
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	N/A	N/A	TBD	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

(2) This package option is for preview only.

7.5 Thermal Information for Dual Channel

THERMAL METRIC ⁽¹⁾		TLV9052, TLV9052S							UNIT
		D (SOIC)	DGK (VSSOP)	DSG (WSON)	PW (TSSOP)	DDF (SOT-23)	DGS (VSSOP)	RUG (X2QFN)	
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	155.4	208.8	102.3	205.1	184.4	170.4	197.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	95.5	93.3	120.0	93.7	112.8	84.9	93.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	98.9	130.7	68.2	135.7	99.9	113.5	123.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	41.9	26.1	15.1	25.0	18.7	16.4	3.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	98.1	128.9	68.2	134.0	99.3	112.3	120.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	43.6	N/A	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.6 Thermal Information for Quad Channel

THERMAL METRIC ⁽¹⁾		TLV9054, TLV9054S					UNIT
		D (SOIC)	PW (TSSOP)	RTE (WQFN)		RUC (X2SQFN)	
		14 PINS	14 PINS	14 PINS	16 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	115.0	147.2	65.5	65.6	209.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	71.1	67.2	70.6	70.6	68.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	71.0	91.6	40.5	40.5	153.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	29.7	16.6	5.8	5.8	3.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	70.6	90.7	40.5	40.5	152.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	N/A	N/A	24.5	24.5	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

7.7 电气特性：V_S (总电源电压) = (V+) - (V-) = 1.8V 至 5.5V

T_A = 25°C, R_L = 10kΩ (连接至 V_S/2), V_{CM} = V_S/2, V_{OUT} = V_S/2 (除非另有说明)；

参数		测试条件	最小值	典型值	最大值	单位
失调电压						
V _{OS}	输入失调电压	V _S = 5V		±0.33	±1.6	mV
		V _S = 5V, T _A = -40°C 至 +125°C			±2	
dV _{OS} /dT	漂移	V _S = 5V, T _A = -40°C 至 +125°C		±0.5		μV/°C
PSRR	电源抑制比	V _S = 1.8V - 5.5V, V _{CM} = (V-)		±13	±80	μV/V
	通道分离, 直流	在直流		115		dB
输入电压范围						
V _{CM}	共模电压	V _S = 1.8V 至 5.5V	(V-) - 0.1		(V+)+0.1	V
CMRR	共模抑制比	V _S = 5.5V, (V-) - 0.1V < V _{CM} < (V+) - 1.4V, T _A = -40°C 至 +125°C	80	96		dB
		V _S = 5.5V, V _{CM} = -0.1V 至 5.6V, T _A = -40°C 至 +125°C	62	79		
		V _S = 1.8V, (V-) - 0.1V < V _{CM} < (V+) - 1.4V, T _A = -40°C 至 +125°C		88		
		V _S = 1.8V, V _{CM} = -0.1V 至 1.9V, T _A = -40°C 至 +125°C		72		
输入偏置电流						
I _B	输入偏置电流			±2	±18 ⁽²⁾	pA
		T _A = -40°C 至 +125°C				±525 ⁽²⁾
I _{OS}	输入失调电流			±1	±15 ⁽²⁾	pA
		T _A = -40°C 至 +125°C				±440 ⁽²⁾
噪声						
E _n	输入电压噪声 (峰峰值)	V _S = 5V, f = 0.1Hz 至 10Hz		6		μV _{PP}
e _n	输入电压噪声密度	V _S = 5V, f = 10kHz		15		nV/√Hz
		V _S = 5V, f = 1kHz		20		nV/√Hz
i _n	输入电流噪声密度	f = 1kHz		18		fA/√Hz
输入电容						
C _{ID}	差分			2		pF
C _{IC}	共模			4		pF
开环增益						
A _{OL}	开环电压增益	V _S = 1.8V, (V-) + 0.04V < V _O < (V+) - 0.04V, R _L = 10kΩ		106		dB
		V _S = 5.5V, (V-) + 0.05V < V _O < (V+) - 0.05V, R _L = 10kΩ	104	128		
		V _S = 1.8V, (V-) + 0.06V < V _O < (V+) - 0.06V, R _L = 2kΩ		108		
		V _S = 5.5V, (V-) + 0.15V < V _O < (V+) - 0.15V, R _L = 2kΩ		130		
频率响应						
GBP	增益带宽积	V _S = 5.5V, G = +1		5		MHz
φ _m	相位裕度	V _S = 5.5V, G = +1		60		度
SR	压摆率	V _S = 5.5V, G = +1, C _L = 130pF		15		V/μs
t _s	趋稳时间	精度达到 0.1%, V _S = 5.5V, 2V 阶跃, G = +1, C _L = 100pF		0.75		μs
		精度达到 0.01%, V _S = 5.5V, 2V 阶跃, G = +1, C _L = 100pF		1		
t _{OR}	过载恢复时间	V _S = 5.5V, V _{IN} × 增益 > V _S		0.3		μs
THD + N	总谐波失真 + 噪声 ⁽¹⁾	V _S = 5.5V, V _{CM} = 2.5V, V _O = 1V _{RMS} , G = +1, f = 1kHz		0.0006%		
输出						

7.7 电气特性：V_S (总电源电压) = (V+) - (V-) = 1.8V 至 5.5V (continued)

 T_A = 25°C, R_L = 10kΩ (连接至 V_S/2), V_{CM} = V_S/2, V_{OUT} = V_S/2 (除非另有说明)；

参数		测试条件	最小值	典型值	最大值	单位
V _O	相对于电源轨的电压输出摆幅	V _S = 5.5V, R _L = 10kΩ,			16	mV
		V _S = 5.5V, R _L = 2kΩ,			40	
I _{SC}	短路电流	V _S = 5V		±50		mA
Z _O	开环输出阻抗	V _S = 5V, f = 5 MHz		250		Ω
电源						
I _Q	每个放大器的静态电流	V _S = 5.5V, I _O = 0mA,		330	450	μA
		V _S = 5.5V, I _O = 0mA, T _A = -40°C 至 +125°C			475	

- (1) 三阶滤波器；-3dB 时的带宽 = 80kHz。
- (2) 根据设计和特征确定；未经生产测试。

7.8 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = 5.5\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

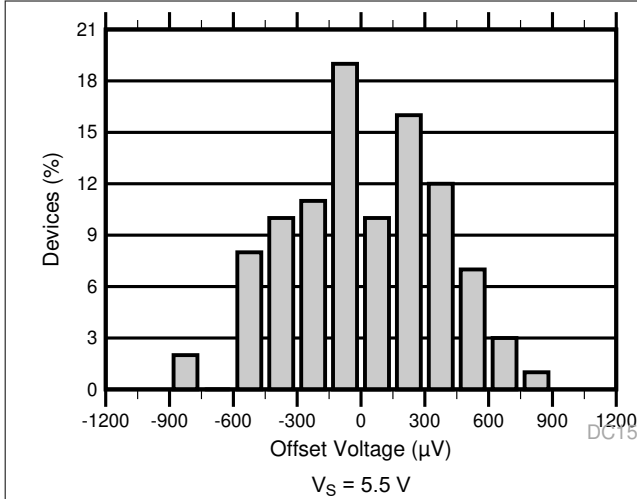


图 7-1. Offset Voltage Production Distribution

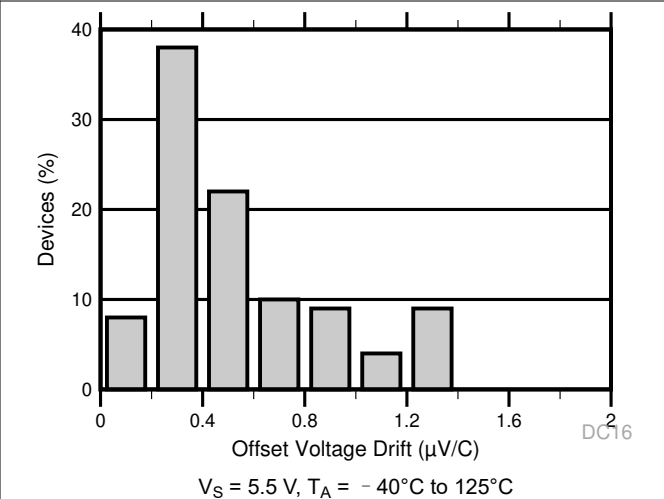


图 7-2. Offset Voltage Drift Distribution

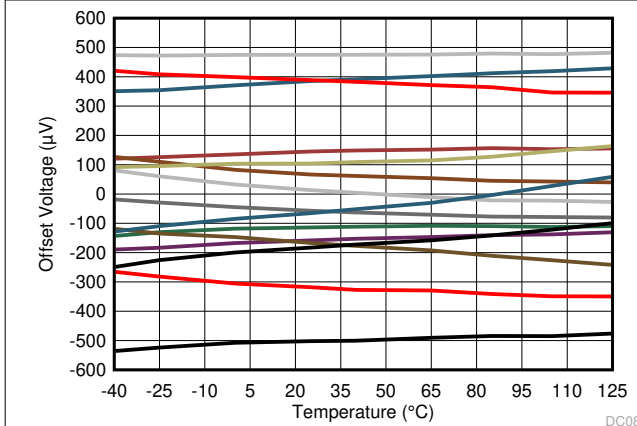


图 7-3. Offset Voltage vs Temperature

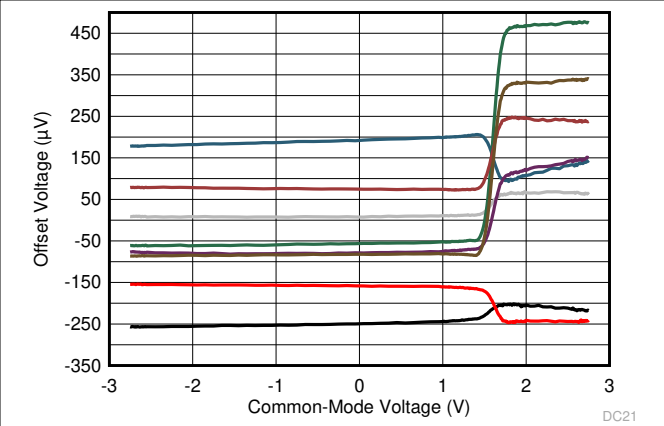


图 7-4. Offset Voltage vs Common-Mode Voltage

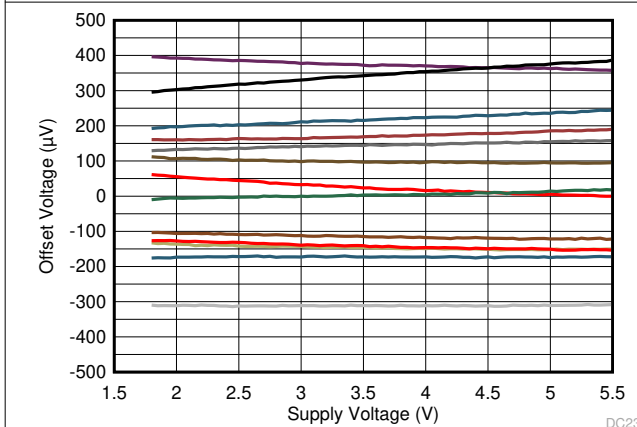


图 7-5. Offset Voltage vs Power Supply

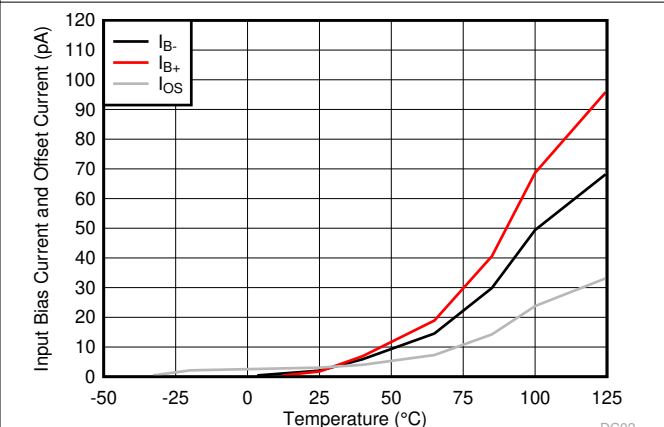


图 7-6. Input Bias Current vs Temperature

7.8 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = 5.5\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

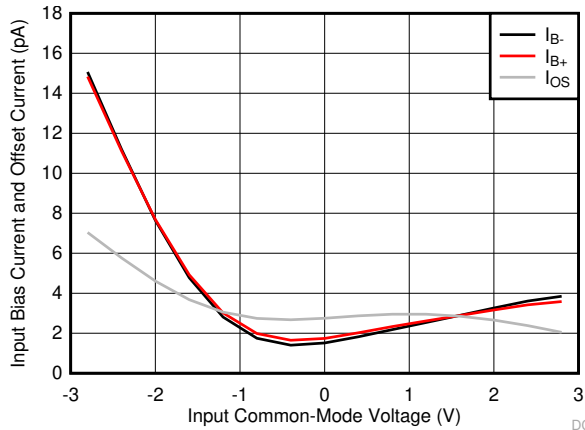


图 7-7. Input Bias Current and Offset Current vs Common-Mode Voltage

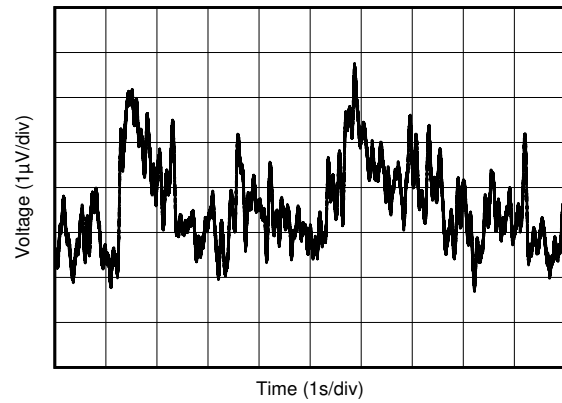


图 7-8. 0.1-Hz to 10-Hz Input Voltage Noise

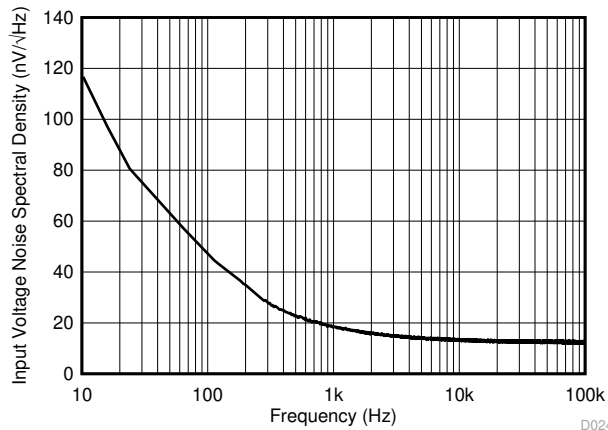


图 7-9. Input Voltage Noise Spectral Density vs Frequency

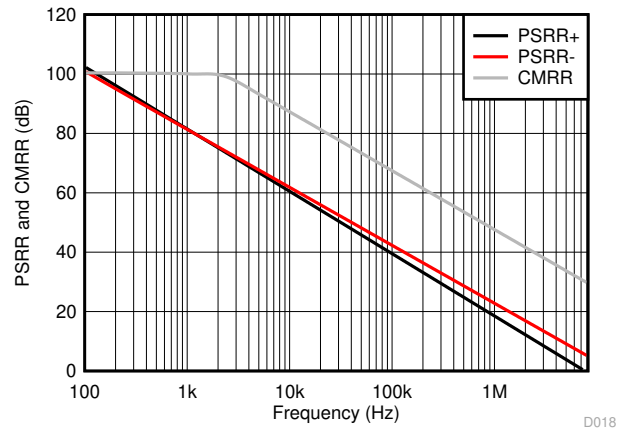


图 7-10. CMRR and PSRR vs Frequency (Referred to Input)

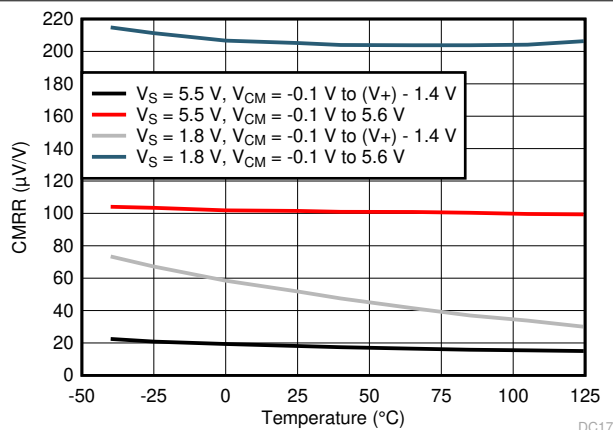


图 7-11. CMRR vs Temperature

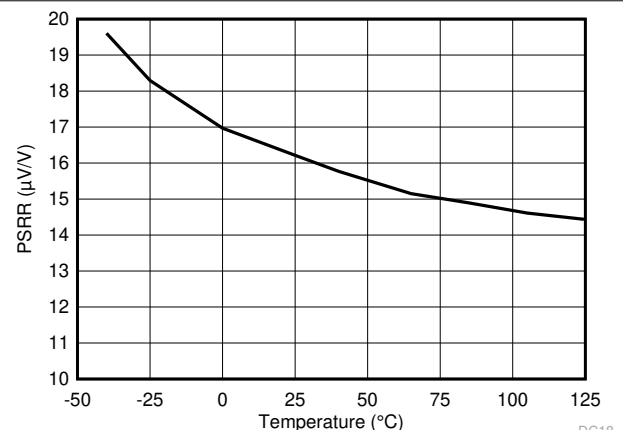


图 7-12. PSRR vs Temperature

7.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5.5\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

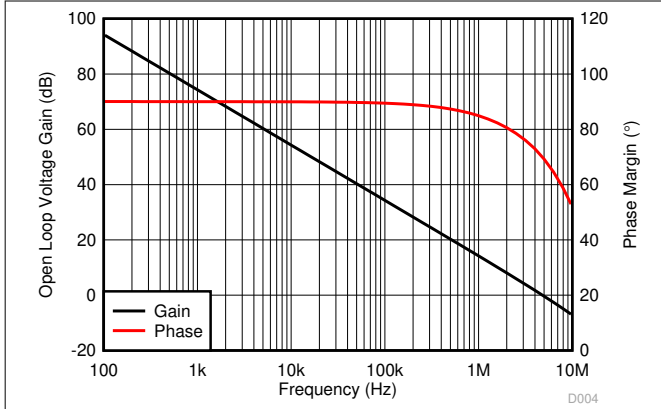


图 7-13. Open Loop Voltage Gain and Phase vs Frequency

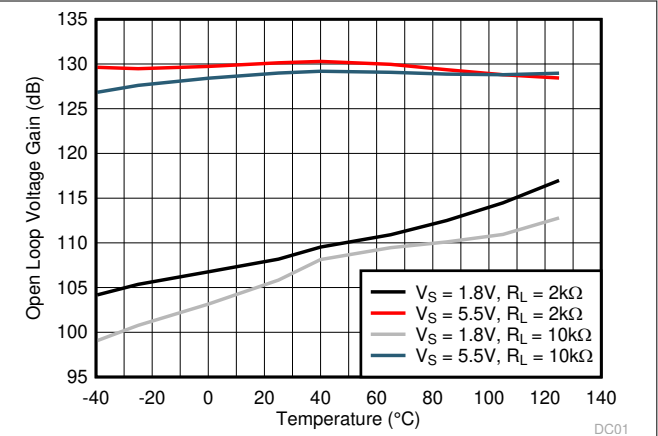


图 7-14. Open Loop Voltage Gain vs Temperature

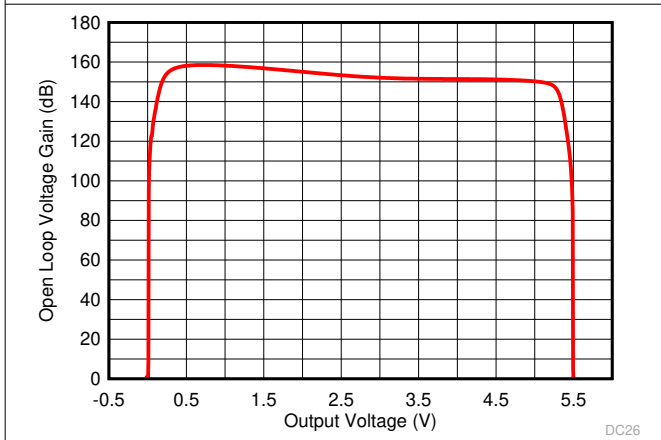


图 7-15. Open Loop Voltage Gain vs Output Voltage

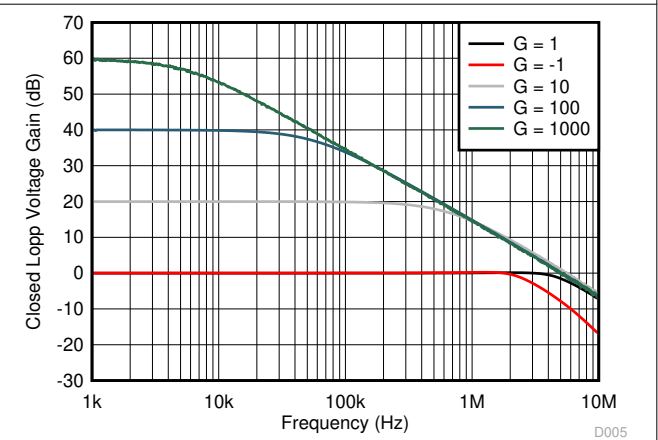


图 7-16. Closed Loop Voltage Gain vs Frequency

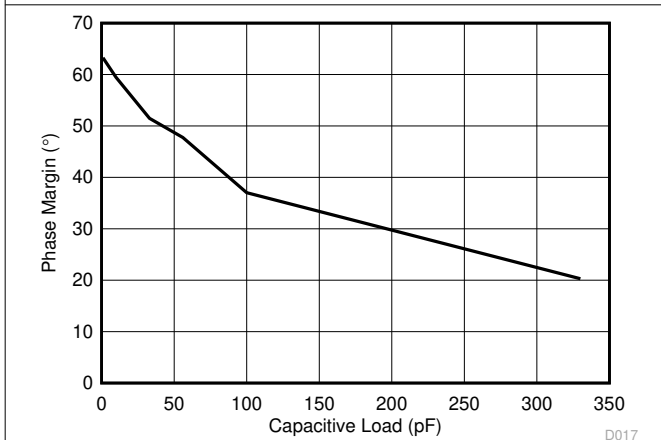


图 7-17. Phase Margin vs Capacitive Load

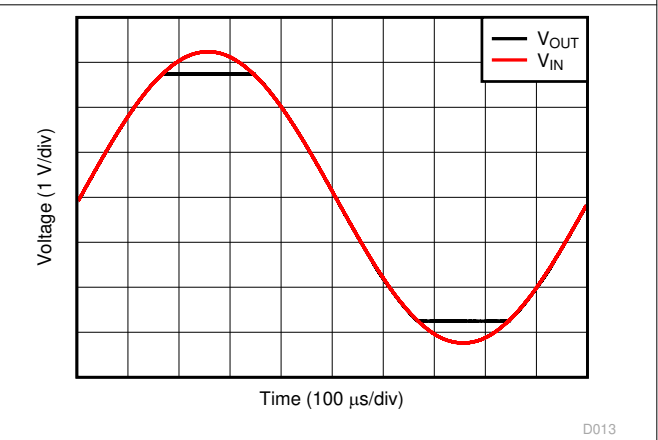


图 7-18. No Phase Reversal

7.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5.5\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

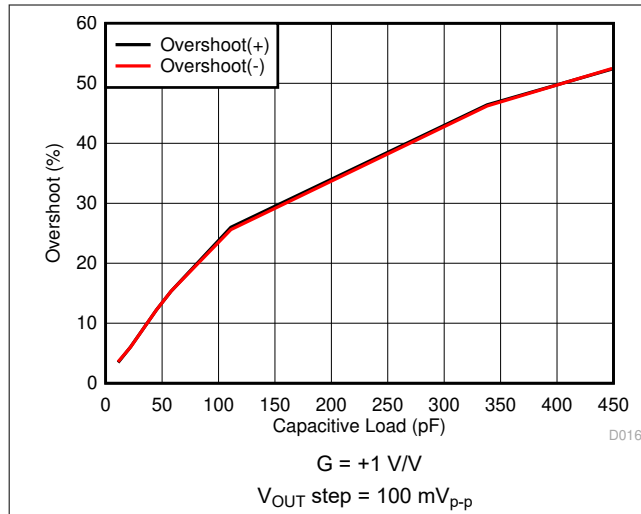


图 7-19. Small-Signal Overshoot vs Load Capacitance

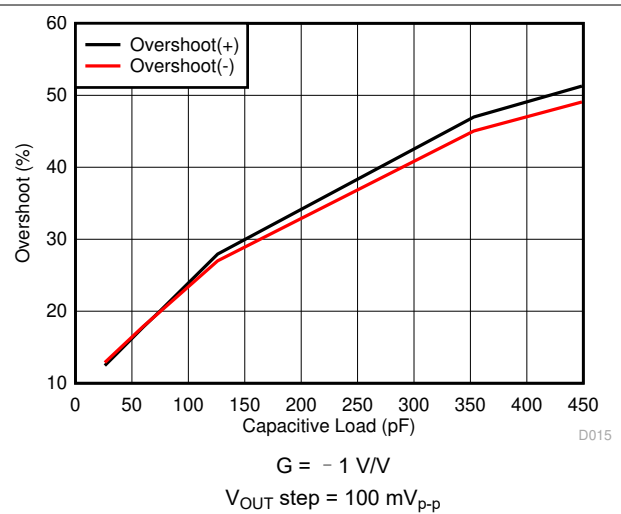


图 7-20. Small-Signal Overshoot vs Load Capacitance

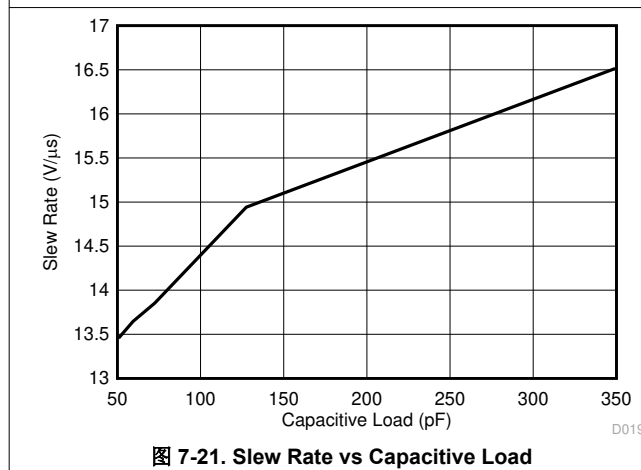


图 7-21. Slew Rate vs Capacitive Load

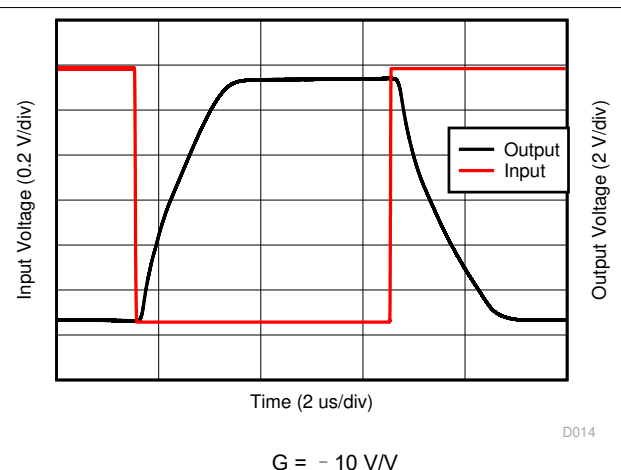


图 7-22. Overload Recovery

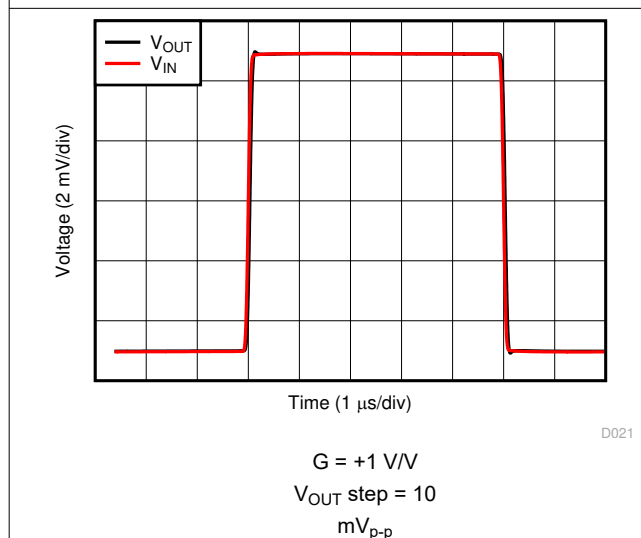


图 7-23. Small-Signal Step Response

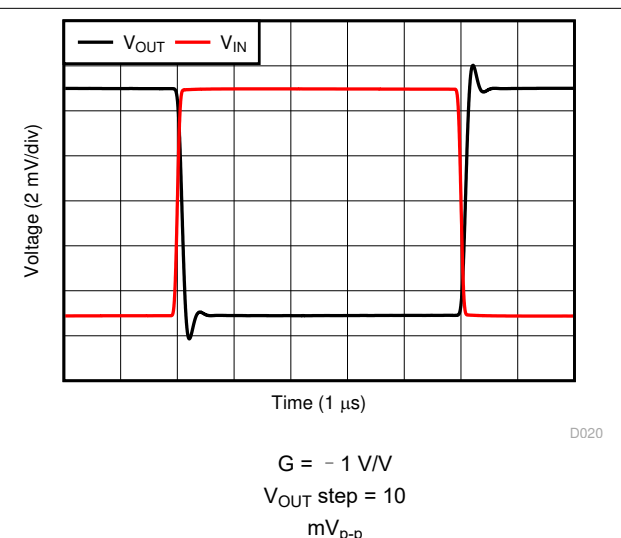
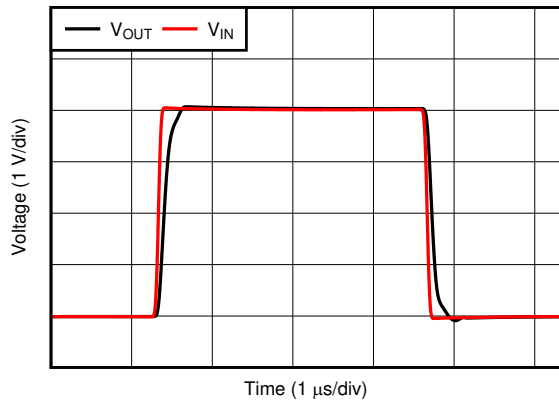


图 7-24. Small-Signal Step Response

7.8 Typical Characteristics (continued)

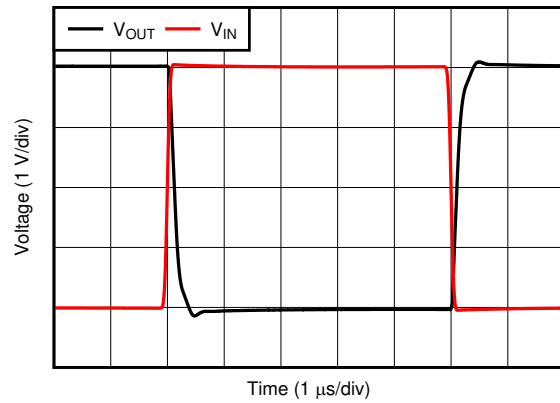
at $T_A = 25^\circ\text{C}$, $V_S = 5.5\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)



D012

$G = +1\text{ V/V}$
 $V_{OUT}\text{ step} = 4\text{ V}_{p-p}$

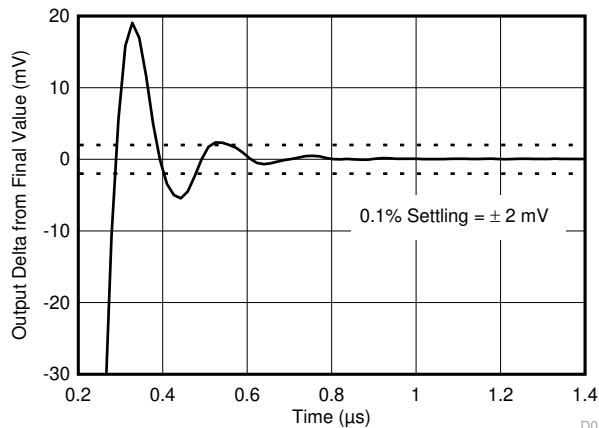
图 7-25. Large-Signal Step Response



D011

$G = -1\text{ V/V}$
 $V_{OUT}\text{ step} = 4\text{ V}_{p-p}$

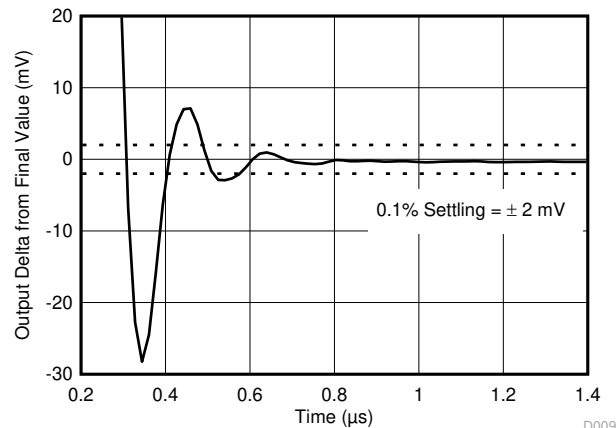
图 7-26. Large-Signal Step Response



D010

$C_L = 100\text{ pF}$ $G = +1\text{ V/V}$

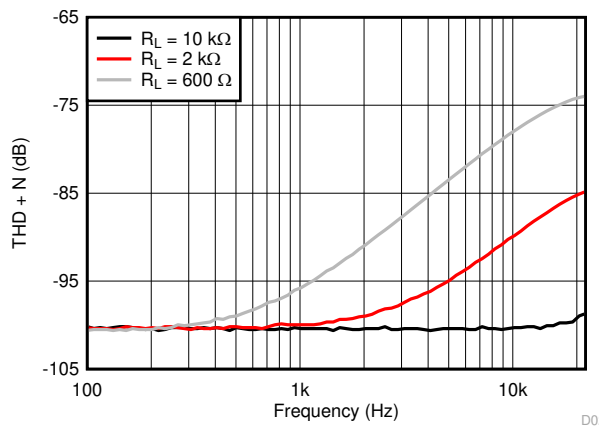
图 7-27. Positive Large-Signal Settling Time



D009

$C_L = 100\text{ pF}$ $G = +1\text{ V/V}$

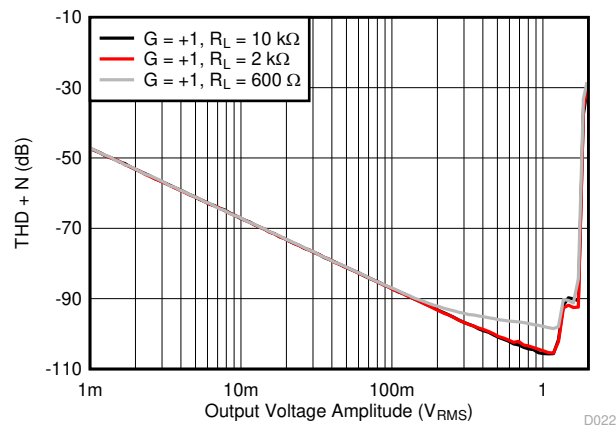
图 7-28. Negative Large-Signal Settling Time



D023

$V_{OUT} = 0.5\text{ V}_{RMS}$ $G = +1$ $V_{CM} = 2.5\text{ V}$
 $BW = 80\text{ kHz}$

图 7-29. THD + N vs Frequency



D022

$f = 1\text{ kHz}$ $G = +1$ $V_{CM} = 2.5\text{ V}$
 $BW = 80\text{ kHz}$

图 7-30. THD + N vs Amplitude

7.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5.5\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

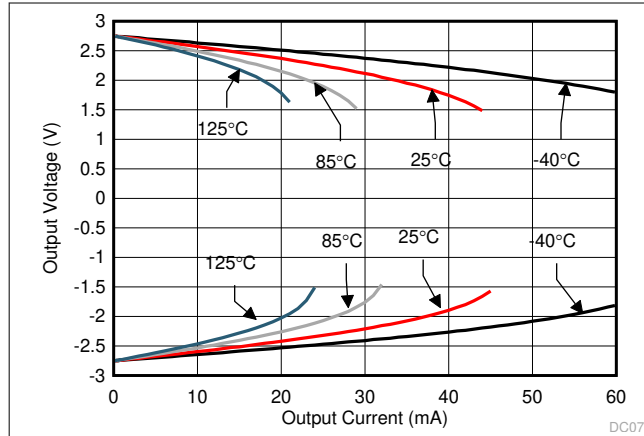


图 7-31. Output Voltage Swing vs Output Current

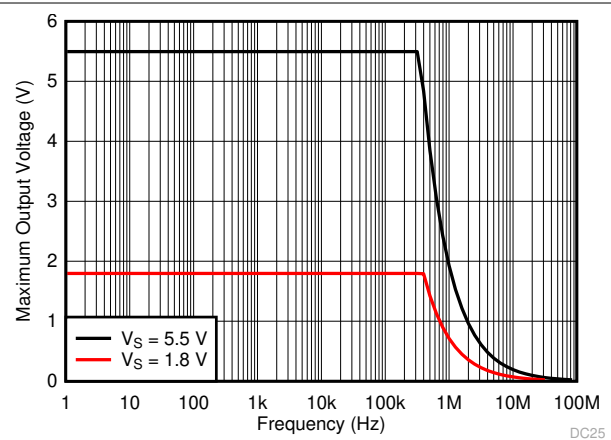


图 7-32. Maximum Output Voltage vs Frequency and Supply Voltage

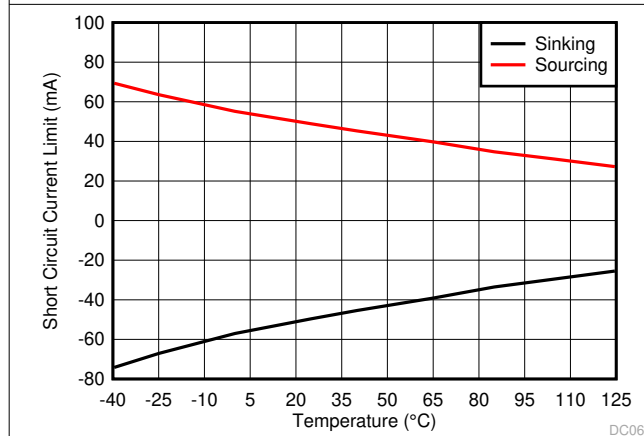


图 7-33. Short-Circuit Current vs Temperature

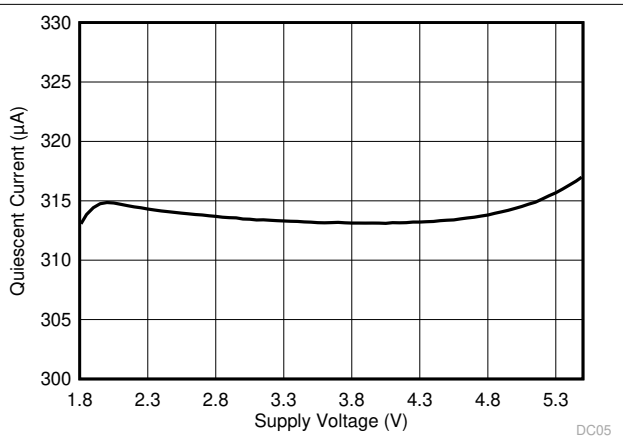


图 7-34. Quiescent Current vs Supply Voltage

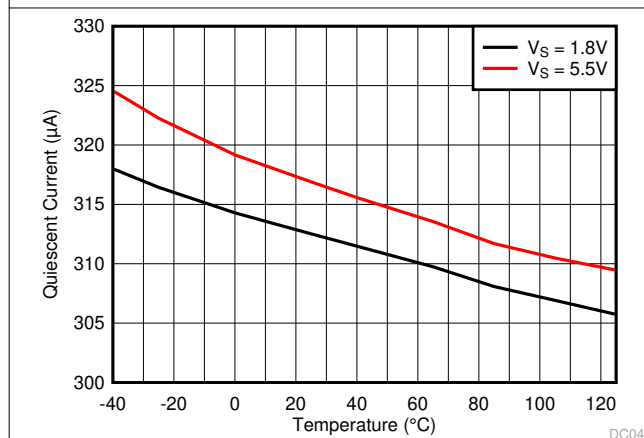


图 7-35. Quiescent Current vs Temperature

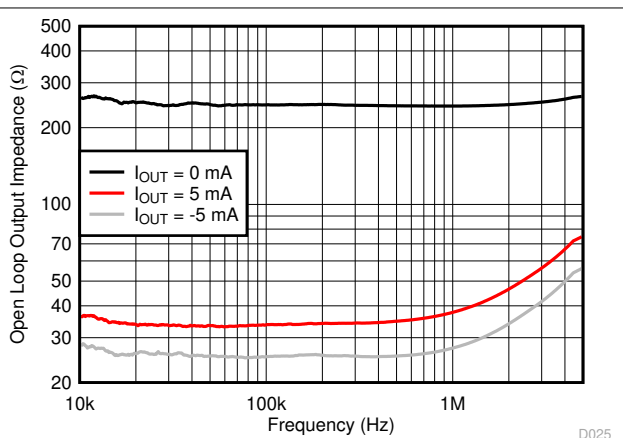
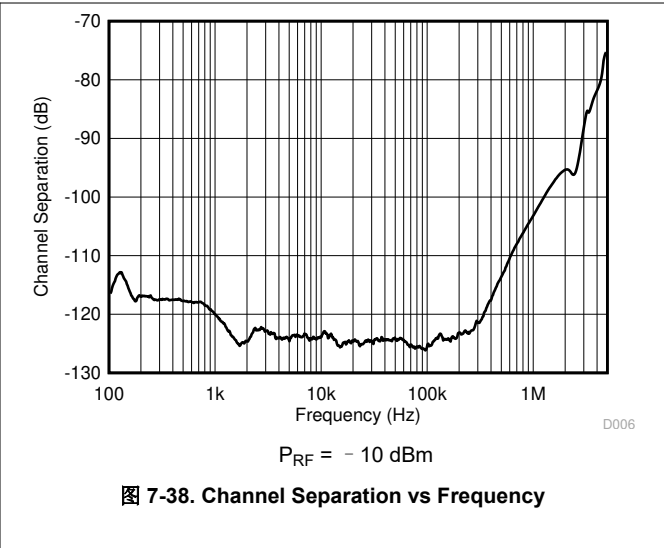
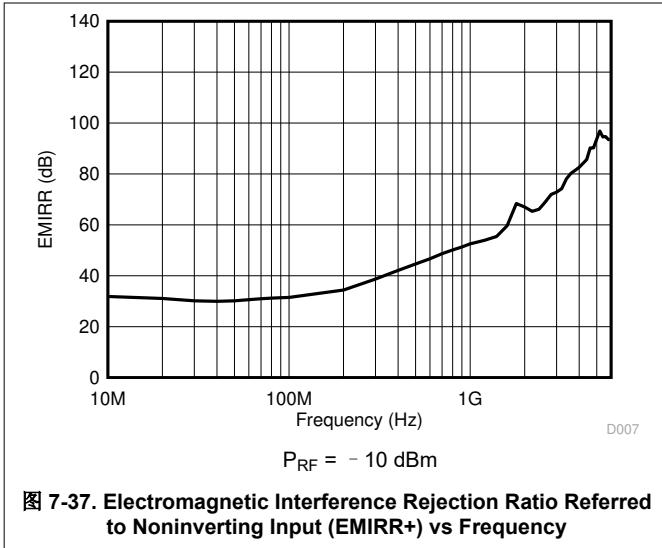


图 7-36. Open-Loop Output Impedance vs Frequency

7.8 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = 5.5\text{ V}$, $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$, $V_{CM} = V_S / 2$, and $V_{OUT} = V_S / 2$ (unless otherwise noted)

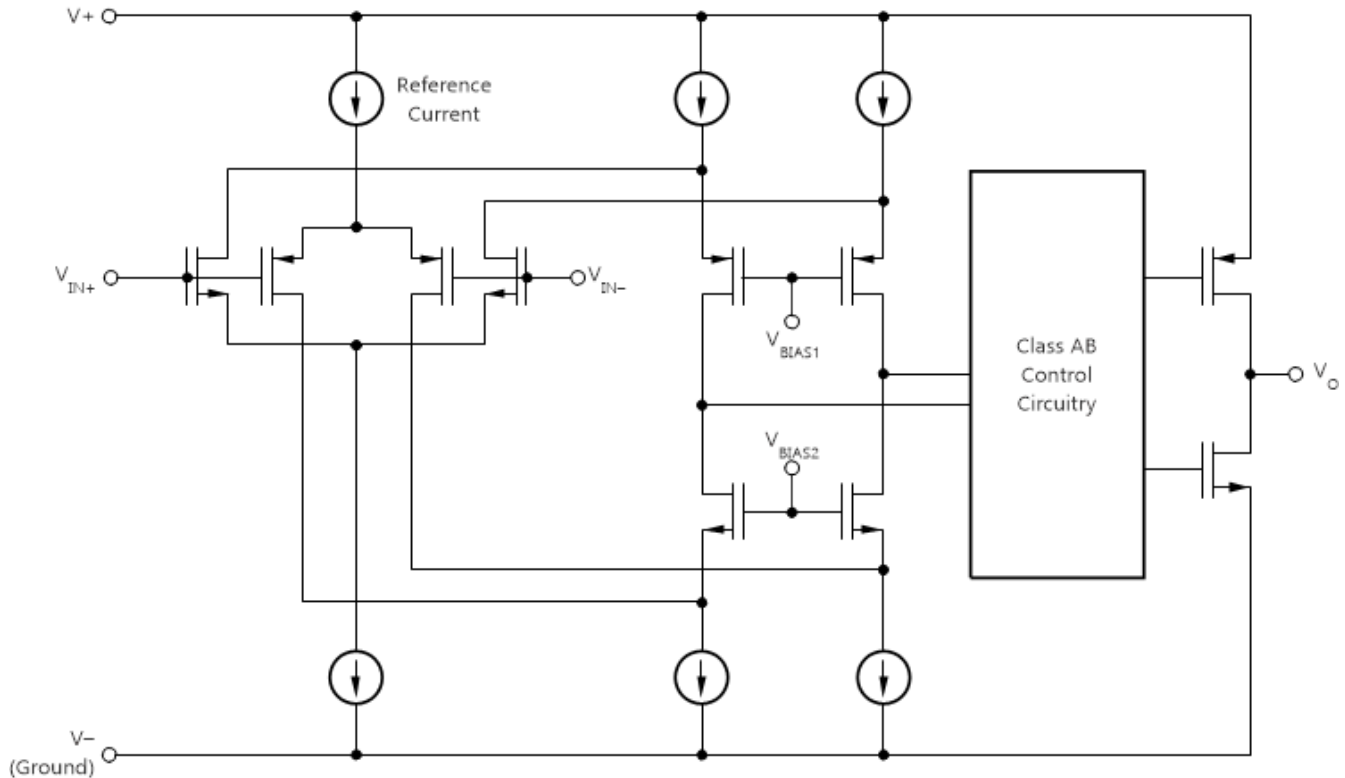


8 Detailed Description

8.1 Overview

The TLV905x devices are a 5-MHz family of low-power, rail-to-rail input and output op amps. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and are designed for a wide range of general-purpose applications. The input common-mode voltage range includes both rails and allows the TLV905x family to be used in virtually any single-supply application. The unique combination of a high slew rate and low quiescent current makes this family a potential choice for battery-powered motor-drive applications. Rail-to-rail input and output swing significantly increase dynamic range, especially in low-supply applications.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Operating Voltage

The TLV905x family of op amps is specified for operation from 1.8 V to 6.0 V. In addition, many specifications apply from -40°C to 125°C . Parameters that vary significantly with operating voltages or temperature are illustrated in the [§ 7.8](#).

8.3.2 Rail-to-Rail Input

The input common-mode voltage range of the TLV905x family extends 100 mV beyond the supply rails for the full supply voltage range of 1.8 V to 6.0 V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the [§ 8.2](#). The N-channel pair is active for input voltages close to the positive rail, typically $(V+) - 1.4\text{ V}$ to 200 mV above the positive supply, whereas the P-channel pair is active for inputs from 200 mV below the negative supply to approximately $(V+) - 1.4\text{ V}$. There is a small transition region, typically $(V+) - 1.2\text{ V}$ to $(V+) - 1\text{ V}$, in which both pairs are on. This 200-mV transition region can vary up to 200 mV with process variation. Thus, the transition region (with both stages on) can range from $(V+) - 1.4\text{ V}$ to $(V+) - 1.2\text{ V}$ on the low end, and up to $(V+) - 1\text{ V}$ to $(V+) - 0.8\text{ V}$ on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can degrade compared to device operation outside this region.

8.3.3 Rail-to-Rail Output

Designed as low-power, low-voltage operational amplifiers, the TLV905x family delivers a robust output drive capability. A class AB output stage with common-source transistors achieves full rail-to-rail output swing capability. For resistive loads of $10\text{ k}\Omega$, the output swings to within 16 mV of either supply rail, regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails.

8.3.4 EMI Rejection

The TLV905x uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the TLV905x benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. [图 8-1](#) shows the results of this testing on the TLV905x. [表 8-1](#) shows the EMIRR IN+ values for the TLV905x at particular frequencies commonly encountered in real-world applications. The [EMI Rejection Ratio of Operational Amplifiers](#) application report contains detailed information on the topic of EMIRR performance as it relates to op amps and is available for download from www.ti.com.

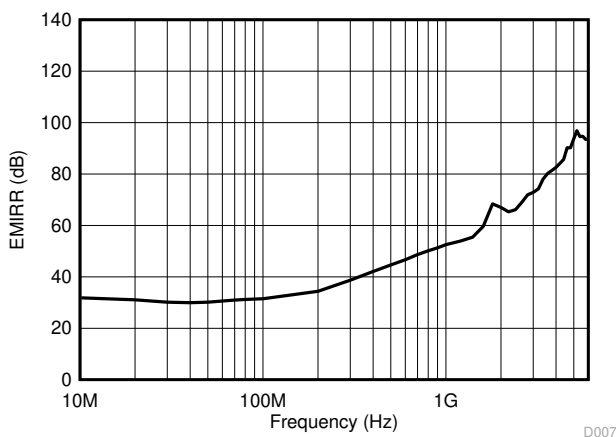


图 8-1. EMIRR Testing

表 8-1. TLV905x EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	41.8 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	53.1 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	71.8 dB
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	70.0 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	81.2 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	92.5 dB

8.3.5 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or high gain. After the device enters the saturation region, the output devices require time to return to the linear operating state. After the output devices return to their linear operating state, the device begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV905x family is approximately 300 ns.

8.3.6 Packages With an Exposed Thermal Pad

The TLV905x family is available in packages such as the WSON-8 (DSG) and WQFN-16 (RTE) which feature an exposed thermal pad. Inside the package, the die is attached to this thermal pad using an electrically conductive compound. For this reason, when using a package with an exposed thermal pad, the thermal pad must either be connected to V^- or left floating. Attaching the thermal pad to a potential other than V^- is not allowed, and the performance of the device is not verified when doing so.

8.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress. These questions tend to focus on the device inputs, but can involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. [图 8-2](#) shows the ESD circuits contained in the TLV905x devices. The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power supply lines, where they meet at an absorption device internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.

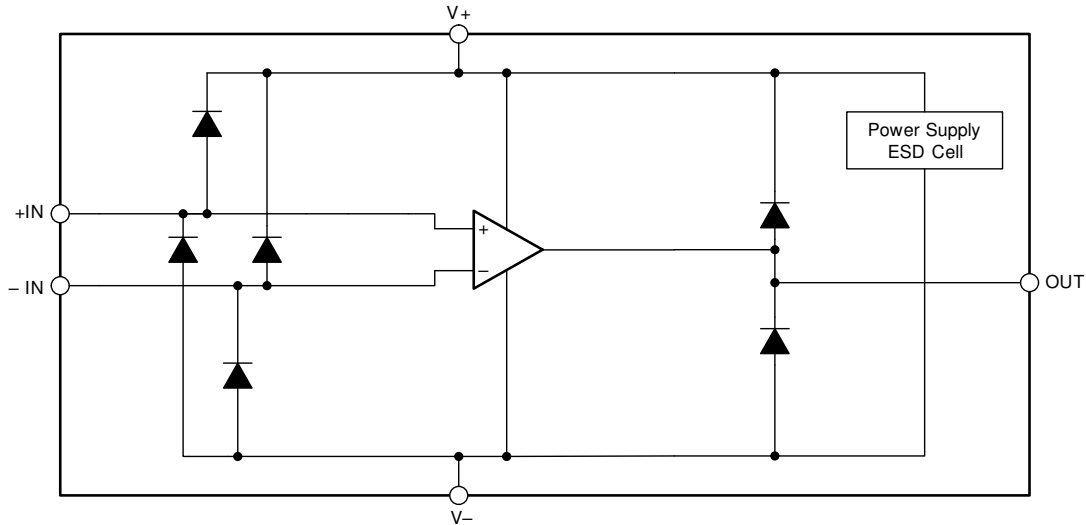


图 8-2. Equivalent Internal ESD Circuitry

8.3.8 Input Protection

The TLV905x family incorporates internal ESD protection circuits on all pins. For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA, as shown in the 7.1. 图 8-3 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

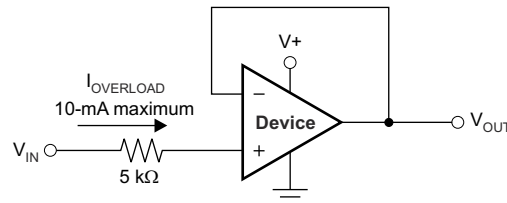


图 8-3. Input Current Protection

8.3.9 Shutdown Function

The TLV905xS devices feature $\overline{\text{SHDN}}$ pins that disable the op amp, placing the device into a low-power standby mode. In this mode, the op amp typically consumes less than 1 μA . The $\overline{\text{SHDN}}$ pins are active low, meaning that shutdown mode is enabled when the input to the $\overline{\text{SHDN}}$ pin is a valid logic low.

The $\overline{\text{SHDN}}$ pins are referenced to the negative supply voltage of the op amp. The threshold of the shutdown feature lies around 800 mV (typical) and does not change with respect to the supply voltage. Hysteresis has been included in the switching threshold to ensure smooth switching characteristics. To ensure shutdown behavior, the $\overline{\text{SHDN}}$ pins should be driven with valid logic signals. A valid logic low is defined as a voltage between V^- and $V^- + 0.4 \text{ V}$. A valid logic high is defined as a voltage between $V^- + 1.2 \text{ V}$ and V^+ . The shutdown pin circuitry includes a pull-up resistor, which will inherently pull the voltage of the pin to the positive supply rail if not driven. Thus, to enable the amplifier, the $\overline{\text{SHDN}}$ pins must either be left floating or driven to a valid logic high. To disable the amplifier, the $\overline{\text{SHDN}}$ pins must be driven to a valid logic low. While TI highly recommends that the shutdown pin be connected to a valid high or a low voltage or driven, TI has included a pull-up resistor connected to VCC. The maximum voltage allowed at the $\overline{\text{SHDN}}$ pins is $(V^+) + 0.5 \text{ V}$. Exceeding this voltage level will damage the device.

The $\overline{\text{SHDN}}$ pins are high-impedance CMOS inputs. Dual op amp versions are independently controlled and quad op amp versions are controlled in pairs with logic inputs. For battery-operated applications, this feature may be

used to greatly reduce the average current and extend battery life. The enable time is 35 μs for full shutdown of all channels; disable time is 6 μs . When disabled, the output assumes a high-impedance state. This architecture allows the TLV905xS to be operated as a gated amplifier (or to have the device output multiplexed onto a common analog output bus). Shutdown time (t_{OFF}) depends on loading conditions and increases as load resistance increases. To ensure shutdown (disable) within a specific shutdown time, the specified 10-k Ω load to midsupply ($V_{\text{S}} / 2$) is required. If using the TLV905xS without a load, the resulting turnoff time is significantly increased.

8.4 Device Functional Modes

The TLV905x family is operational when the power-supply voltage is between 1.8 V (± 0.9 V) and 6.0 V (± 3.0 V).

The TLV905xS devices feature a shutdown mode and are shutdown when a valid logic low is applied to the shutdown pin.

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The TLV905x family features 5-MHz bandwidth and very high slew rate of 15 V/ μ s with only 330 μ A of supply current per channel, providing excellent AC performance at very low-power consumption. DC applications are well served with a very low input noise voltage of 15 nV/ $\sqrt{\text{Hz}}$ at 10 kHz, low input bias current, and a typical input offset voltage of 0.33 mV.

9.2 Typical Low-Side Current Sense Application

图 9-1 shows the TLV905x configured in a low-side current sensing application.

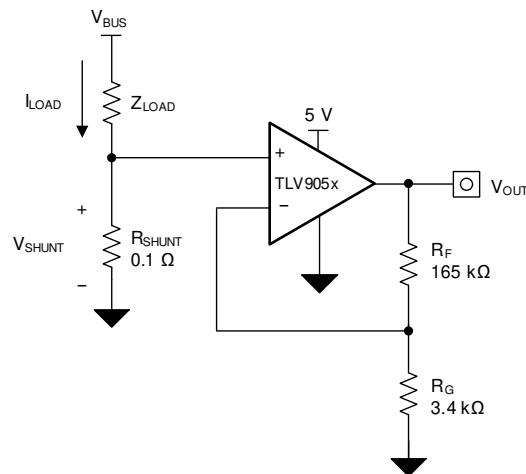


图 9-1. TLV905x in a Low-Side, Current-Sensing Application

9.2.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Output voltage: 4.95 V
- Maximum shunt voltage: 100 mV

9.2.2 Detailed Design Procedure

The transfer function of the circuit in [图 9-1](#) is given in [方程式 1](#).

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times \text{Gain} \quad (1)$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is defined using [方程式 2](#).

$$R_{SHUNT} = \frac{V_{SHUNT_MAX}}{I_{LOAD_MAX}} = \frac{100 \text{ mV}}{1 \text{ A}} = 100 \text{ m}\Omega \quad (2)$$

Using [方程式 2](#), R_{SHUNT} equals 100 m Ω . The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the TLV905x device to produce an output voltage of approximately 0 V to 4.95 V. [方程式 3](#) calculates the gain required for the TLV905x device to produce the required output voltage.

$$\text{Gain} = \frac{(V_{OUT_MAX} - V_{OUT_MIN})}{(V_{IN_MAX} - V_{IN_MIN})} \quad (3)$$

Using [方程式 3](#), the required gain equals 49.5 V/V, which is set with the R_F and R_G resistors. [方程式 4](#) sizes the R_F and R_G , resistors to set the gain of the TLV905x device to 49.5 V/V.

$$\text{Gain} = 1 + \frac{(R_F)}{(R_G)} \quad (4)$$

Selecting R_F to equal 165 k Ω and R_G to equal 3.4 k Ω provides a combination that equals approximately 49.5 V/V. [图 9-2](#) shows the measured transfer function of the circuit shown in [图 9-1](#).

9.2.3 Application Curve

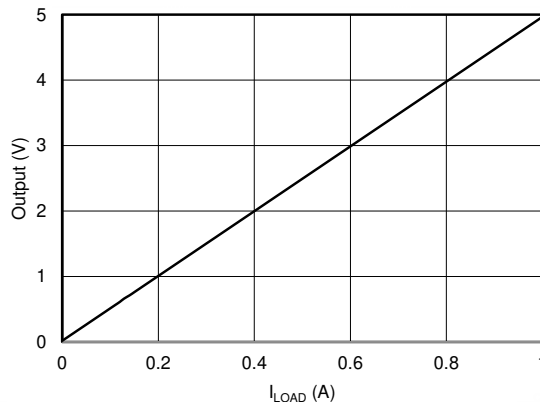


图 9-2. Low-Side, Current-Sense Transfer Function

9.3 Power Supply Recommendations

The TLV905x family is specified for operation from 1.8 V to 6.0 V (± 0.9 V to ± 3.0 V); many specifications apply from -40°C to 125°C . The [§ 7.8](#) section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

CAUTION

Supply voltages larger than 7 V can permanently damage the device; see the [§ 7.1](#) table.

Place 0.1- μF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more-detailed information on bypass capacitor placement, see the [§ 9.4.2](#) section.

9.4 Layout

9.4.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
 - Connect low-ESR, 0.1- μF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see [Circuit Board Layout Techniques](#).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in [图 9-4](#), keeping R_F and R_G close to the inverting input minimizes parasitic capacitance on the inverting input.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

9.4.2 Layout Example

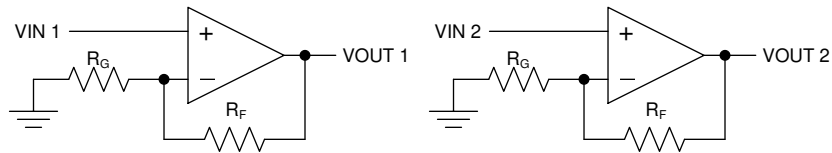


图 9-3. Schematic Representation for 图 9-4

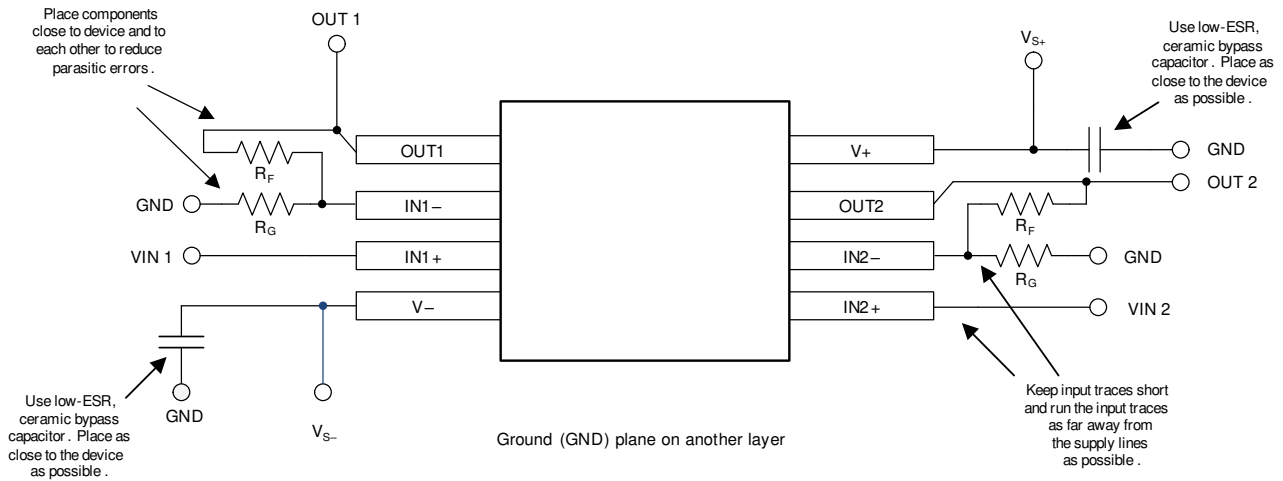


图 9-4. Layout Example

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

Texas Instruments, [TLVx313 Low-Power, Rail-to-Rail In/Out, 500- \$\mu\$ V Typical Offset, 1-MHz Operational Amplifier for Cost-Sensitive Systems](#)

Texas Instruments, [TLVx314 3-MHz, Low-Power, Internal EMI Filter, RRIO, Operational Amplifier](#)

Texas Instruments, [EMI Rejection Ratio of Operational Amplifiers](#)

Texas Instruments, [QFN/SON PCB Attachment](#)

Texas Instruments, [Quad Flatpack No-Lead Logic Packages](#)

Texas Instruments, [Circuit Board Layout Techniques](#)

Texas Instruments, [Single-Ended Input to Differential Output Conversion Circuit Reference Design](#)

10.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

表 10-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TLV9051/S	Click here	Click here	Click here	Click here	Click here
TLV9052/S	Click here	Click here	Click here	Click here	Click here
TLV9054/S	Click here	Click here	Click here	Click here	Click here

10.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

10.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.

Bluetooth® is a registered trademark of Bluetooth SIG, Inc.

所有商标均为其各自所有者的财产。

10.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 术语表

TI 术语表

本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV9051IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	T51D	Samples
TLV9051IDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	T51	Samples
TLV9051IDPWR	ACTIVE	X2SON	DPW	5	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	FH	Samples
TLV9051SIDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T51S	Samples
TLV9052IDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T052	Samples
TLV9052IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU SN NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1PWX	Samples
TLV9052IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL9052	Samples
TLV9052IDSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	9052	Samples
TLV9052IPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TL9052	Samples
TLV9052SIDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	T052	Samples
TLV9052SIRUGR	ACTIVE	X2QFN	RUG	10	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	FPF	Samples
TLV9054IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV9054D	Samples
TLV9054IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	T9054PW	Samples
TLV9054IRTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T54RT	Samples
TLV9054IRUCR	ACTIVE	QFN	RUC	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1FF	Samples
TLV9054SIRTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9054S	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9051IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9051IDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TLV9051IDPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2
TLV9051SIDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9052IDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9052IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV9052IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV9052IDSGR	WSO	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV9052IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV9052SIDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV9052SIRUGR	X2QFN	RUG	10	3000	178.0	8.4	1.75	2.25	0.56	4.0	8.0	Q1
TLV9054IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLV9054IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV9054IRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV9054IRUCR	QFN	RUC	14	3000	180.0	9.5	2.16	2.16	0.5	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9054SIRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV9051IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV9051IDCKR	SC70	DCK	5	3000	190.0	190.0	30.0
TLV9051IDPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
TLV9051SIDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TLV9052IDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV9052IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV9052IDGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
TLV9052IDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TLV9052IPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
TLV9052SIDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
TLV9052SIRUGR	X2QFN	RUG	10	3000	205.0	200.0	33.0
TLV9054IDR	SOIC	D	14	2500	356.0	356.0	35.0
TLV9054IPWR	TSSOP	PW	14	2000	366.0	364.0	50.0
TLV9054IRTER	WQFN	RTE	16	3000	367.0	367.0	35.0
TLV9054IRUCR	QFN	RUC	14	3000	205.0	200.0	30.0
TLV9054SIRTER	WQFN	RTE	16	3000	367.0	367.0	35.0

DGS0010A



PACKAGE OUTLINE

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.

EXAMPLE BOARD LAYOUT

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGS0010A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DPW 5

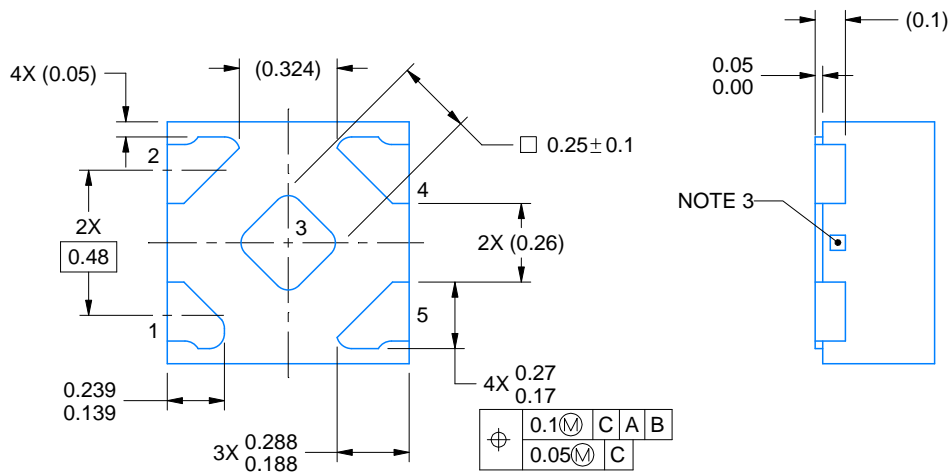
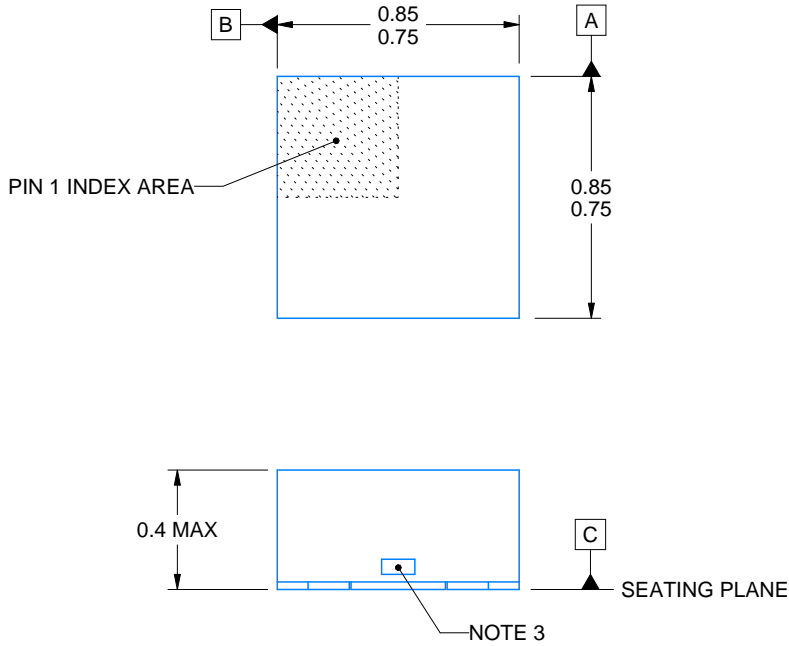
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4211218-3/D



4223102/D 03/2022

NOTES:

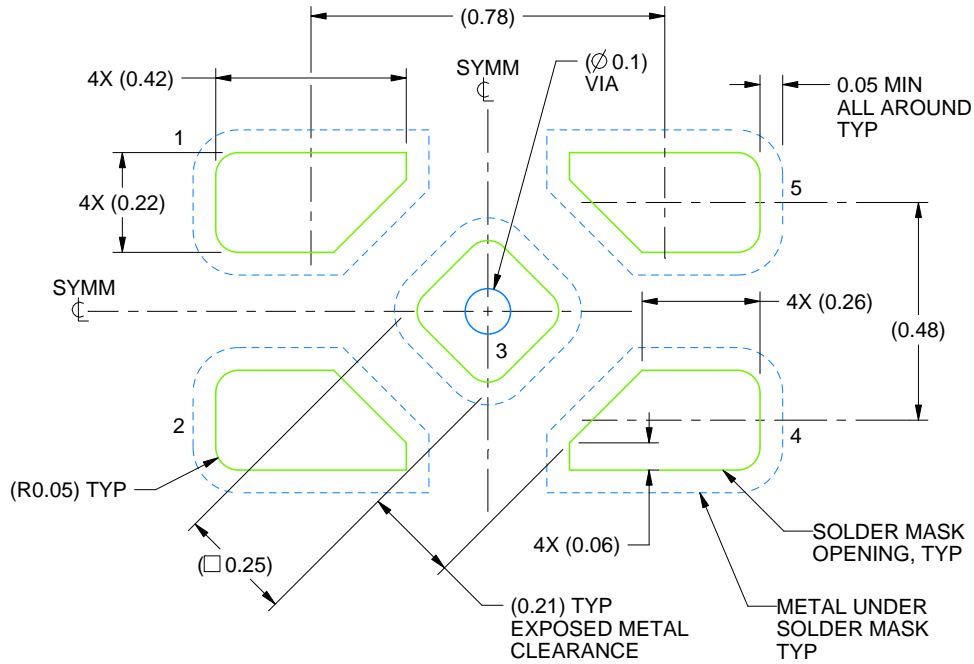
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

EXAMPLE BOARD LAYOUT

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/D 03/2022

NOTES: (continued)

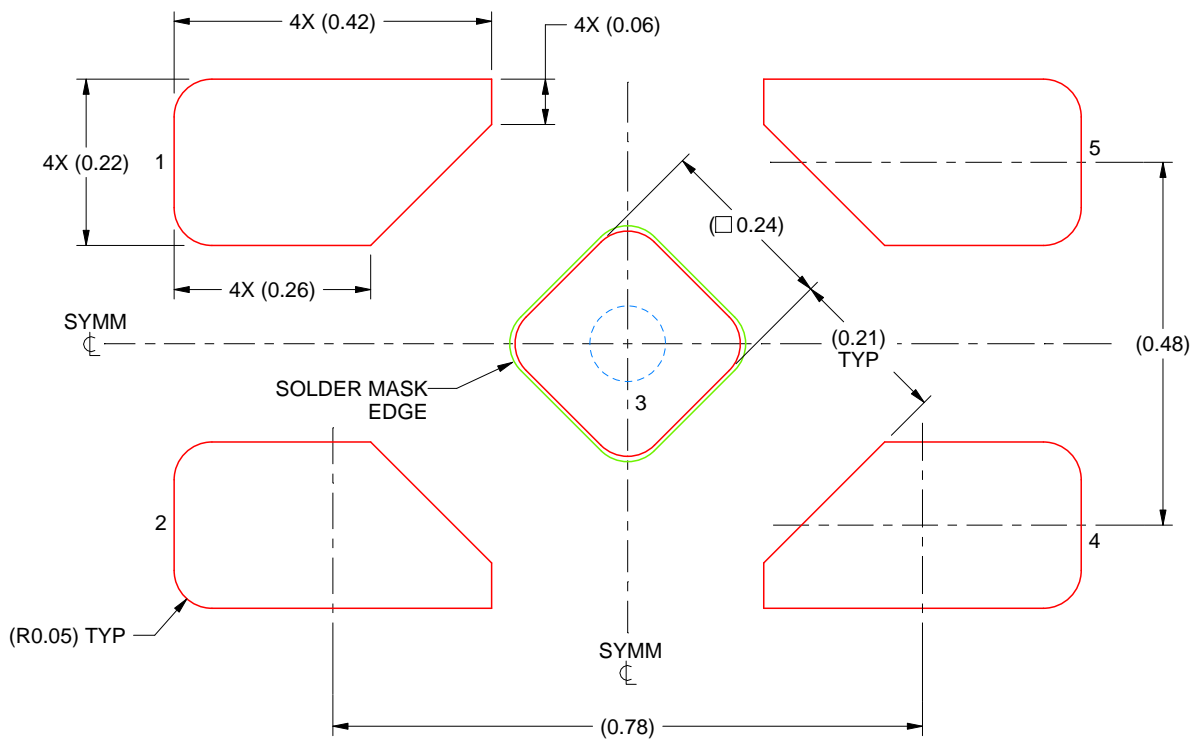
4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

4223102/D 03/2022

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

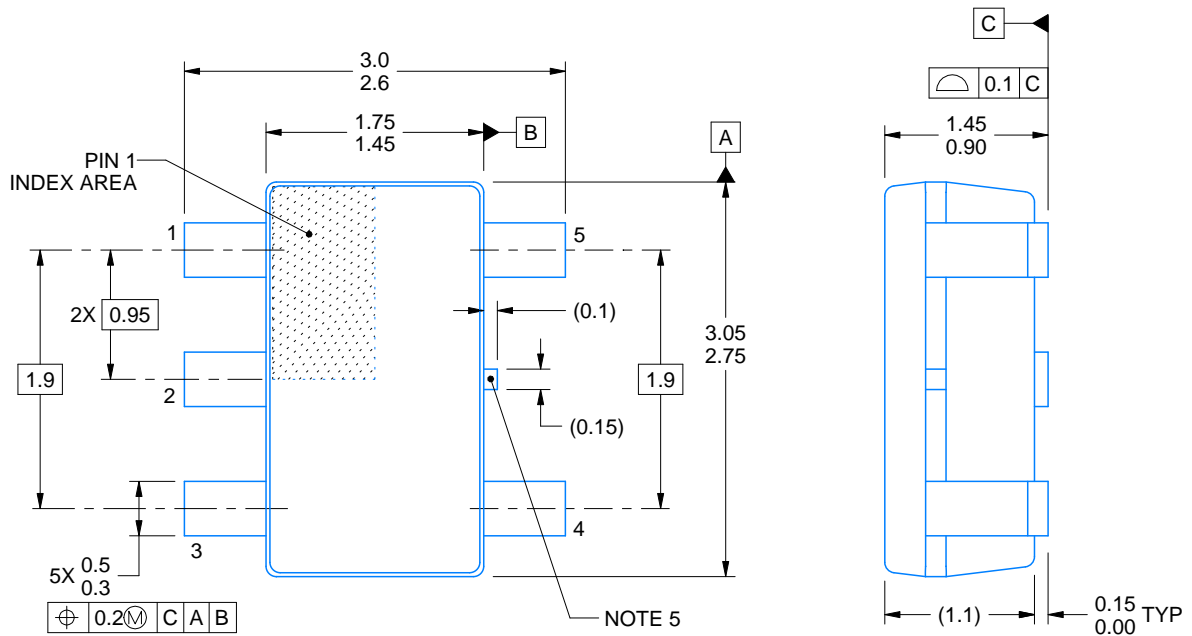
DBV0005A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/G 03/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/G 03/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/G 03/2023

NOTES: (continued)



8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

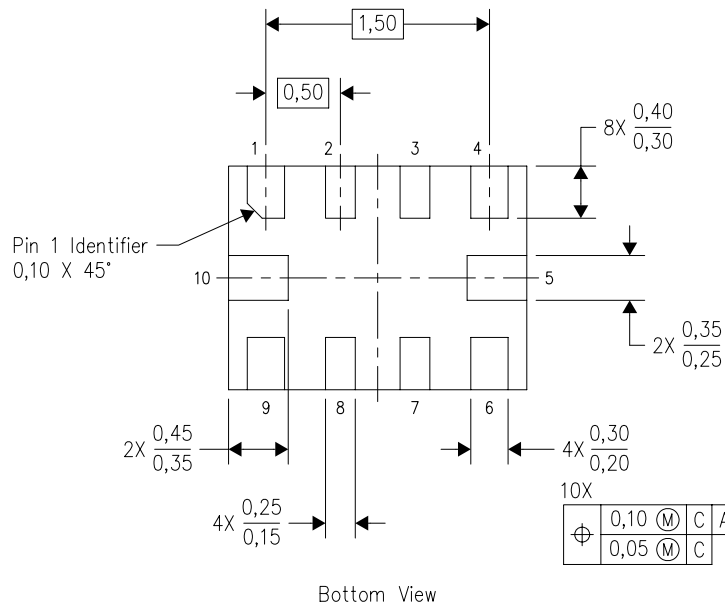
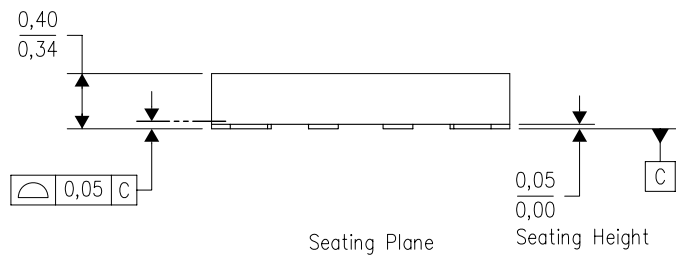
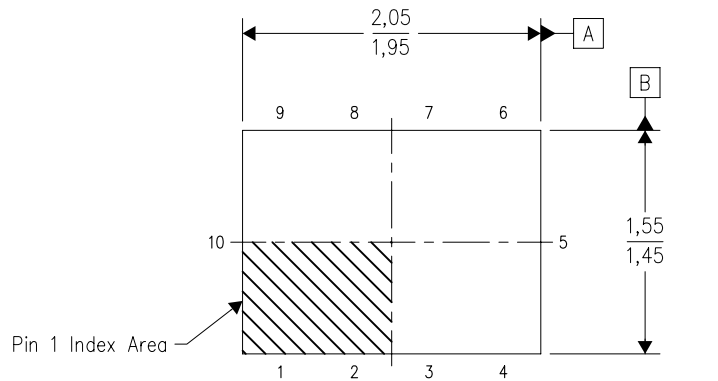


4211284-2/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RUG (R-PQFP-N10)

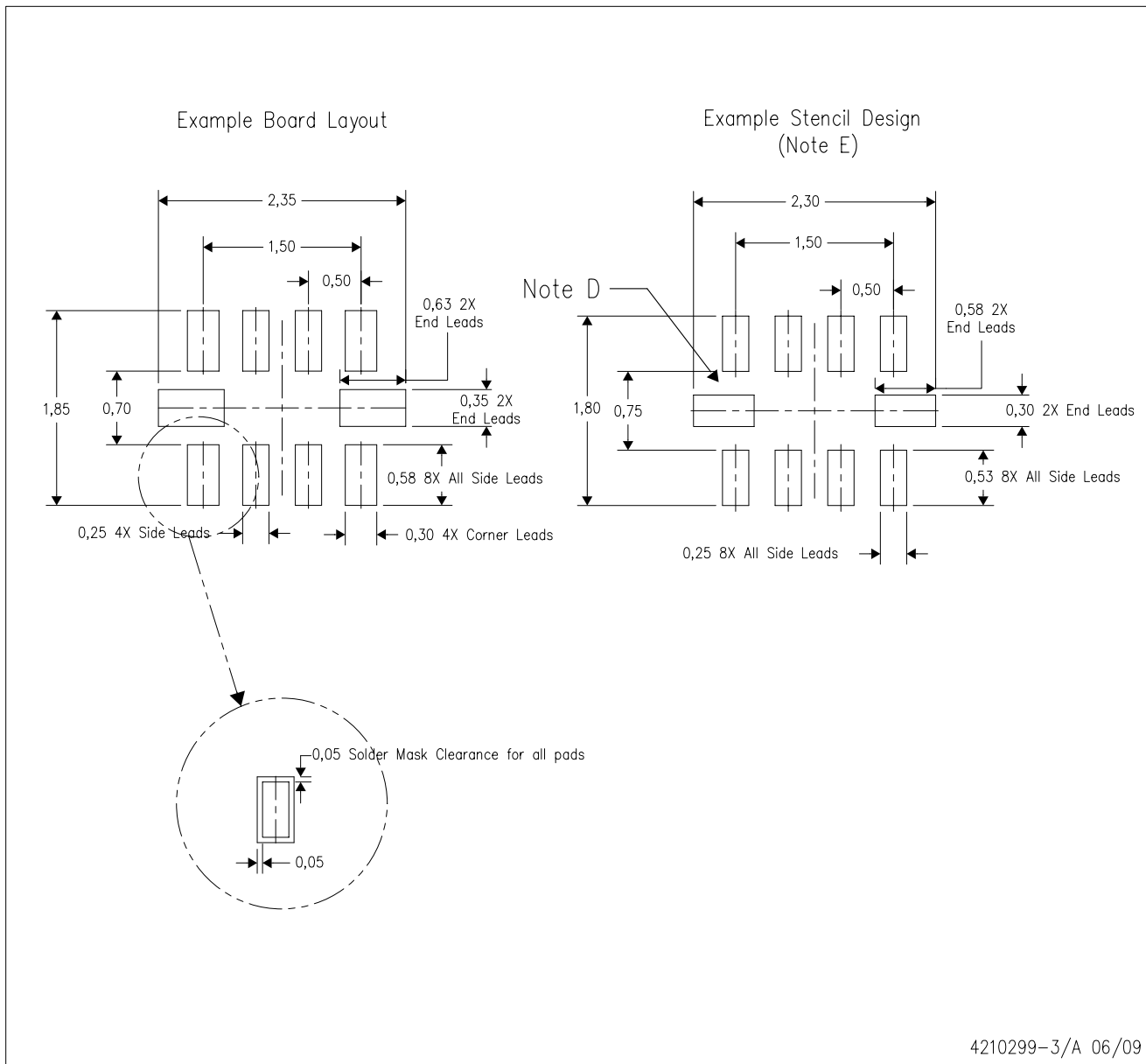
PLASTIC QUAD FLATPACK



4208528-3/B 04/2008

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. QFN (Quad Flatpack No-Lead) package configuration.
 - D. This package complies to JEDEC MO-288 variation X2EFD.

RUG (R-PQFP-N10)



4210299-3/A 06/09

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
 - E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
 - F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - G. Side aperture dimensions over-print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed $.006$ [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

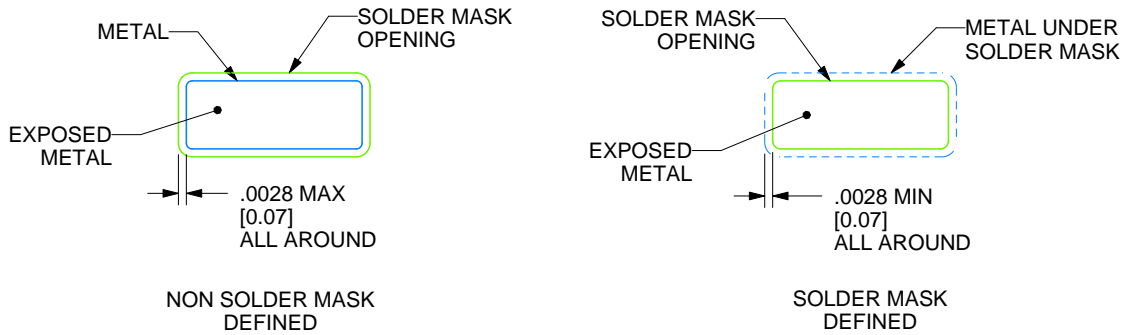
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

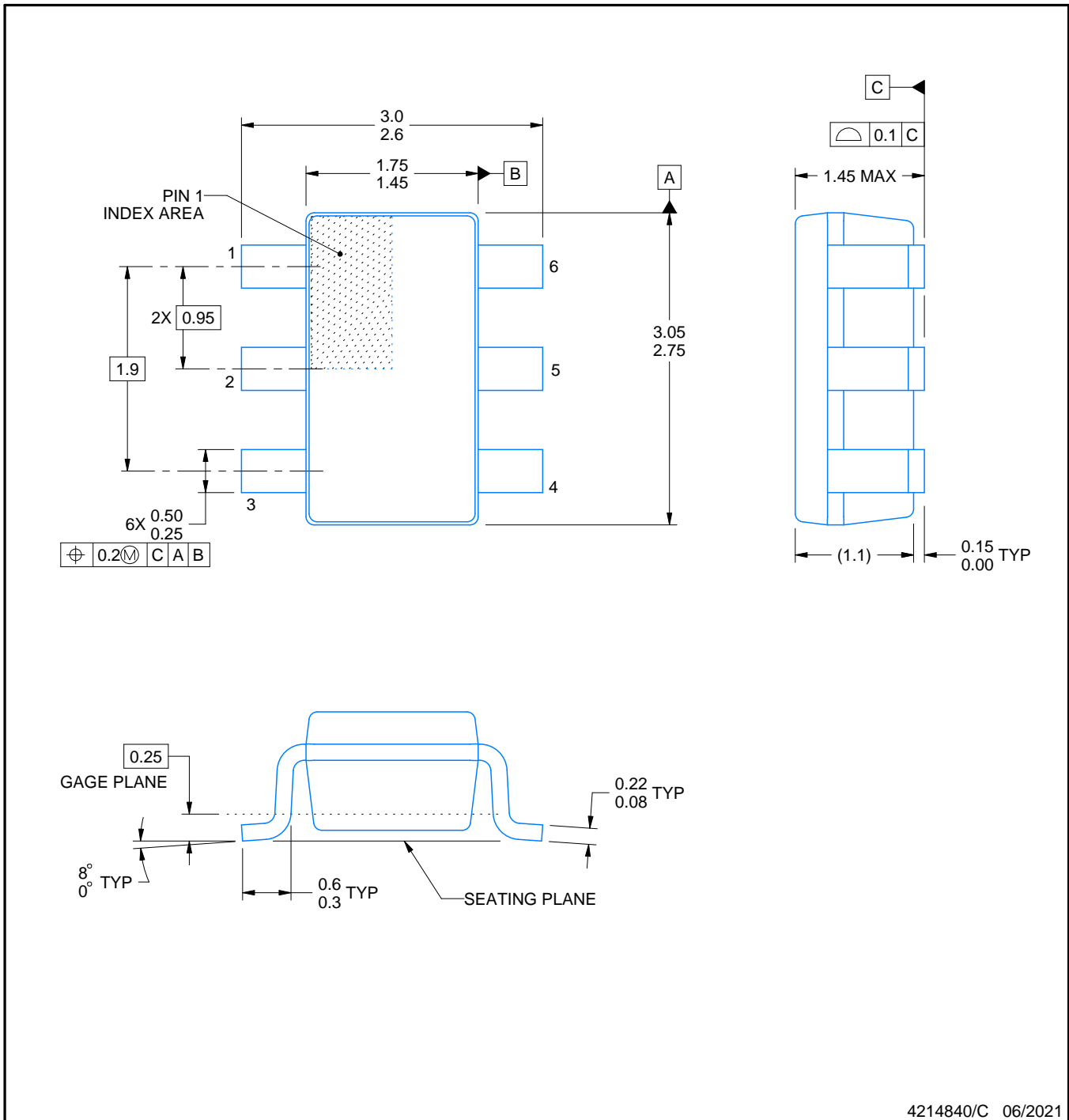
DBV0006A



PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214840/C 06/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Reference JEDEC MO-178.

EXAMPLE BOARD LAYOUT

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214840/C 06/2021

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

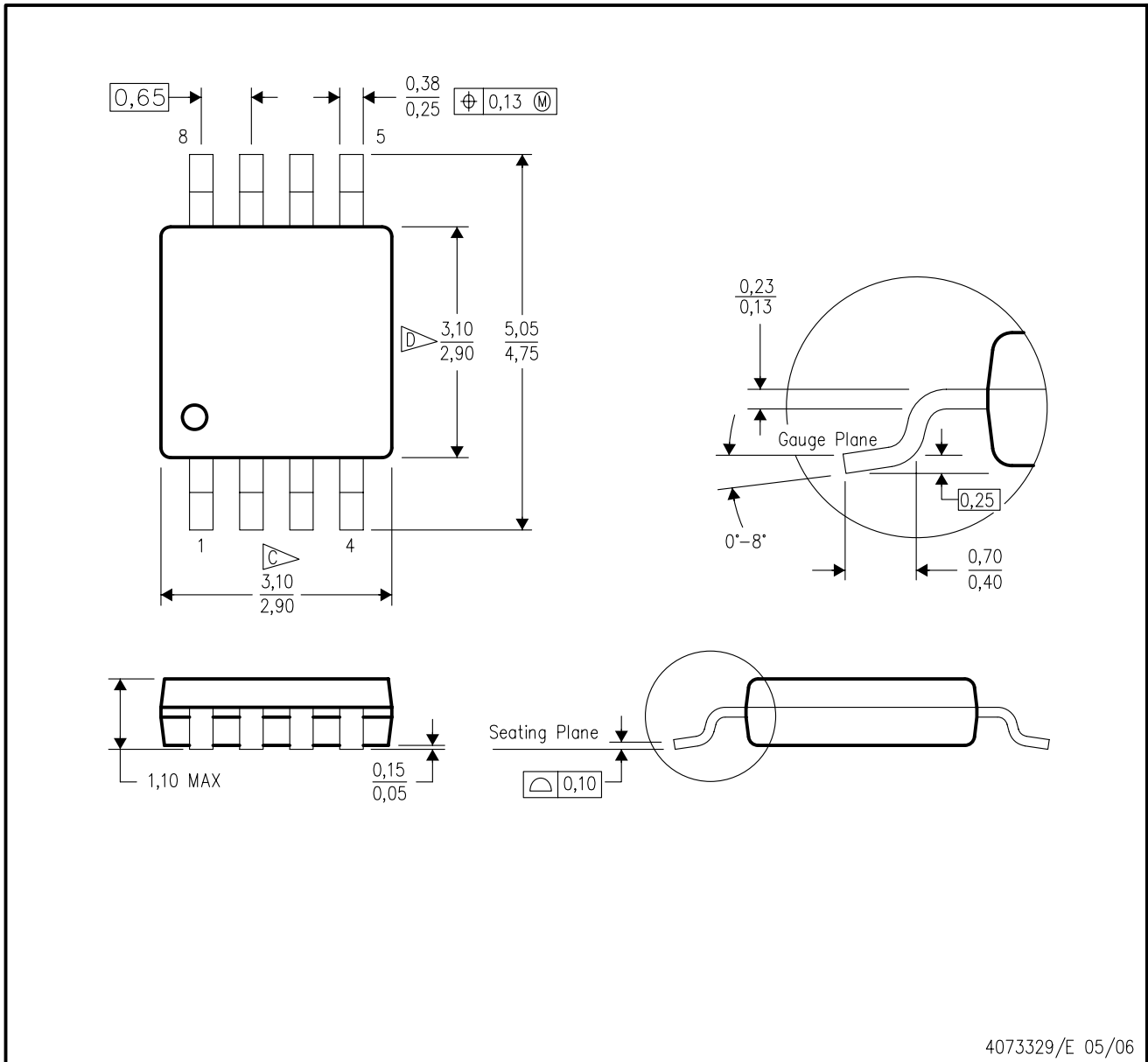
4214840/C 06/2021

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
 - E. Falls within JEDEC MO-187 variation AA, except interlead flash.



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224783/A

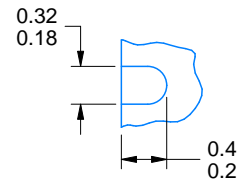
DSG0008A



PACKAGE OUTLINE

WSON - 0.8 mm max height

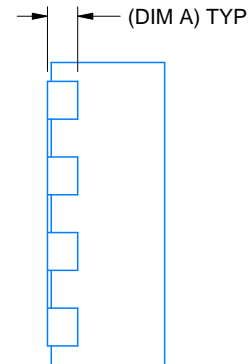
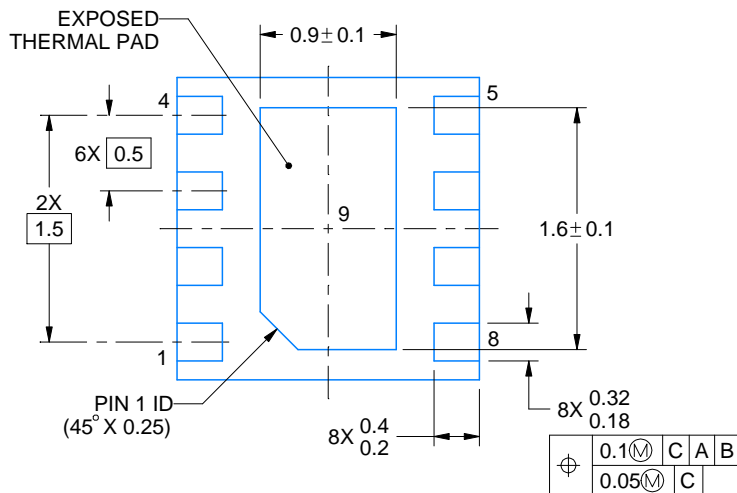
PLASTIC SMALL OUTLINE - NO LEAD



ALTERNATIVE TERMINAL SHAPE TYPICAL



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2



4218900/E 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DSG0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

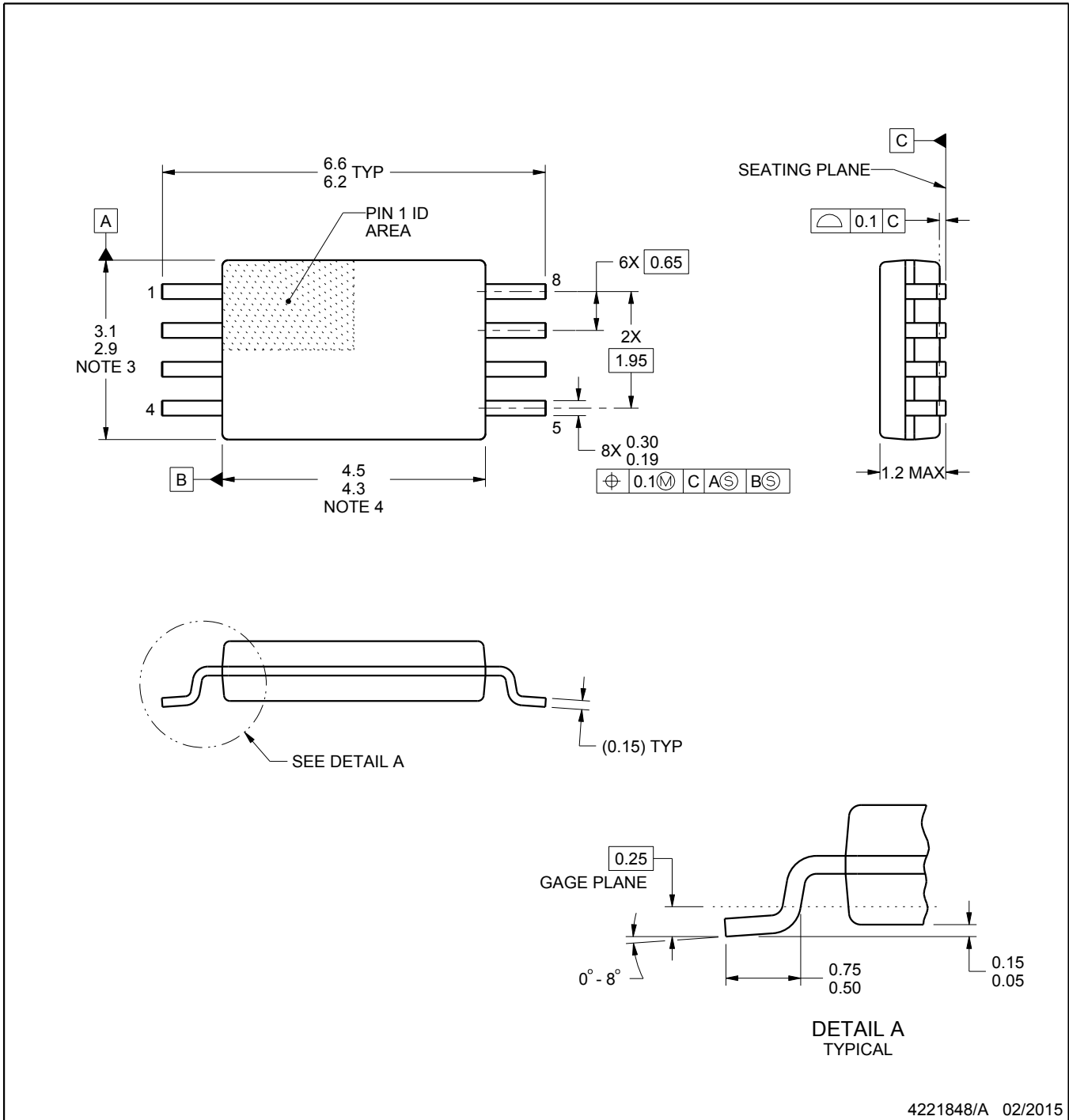
PW0008A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

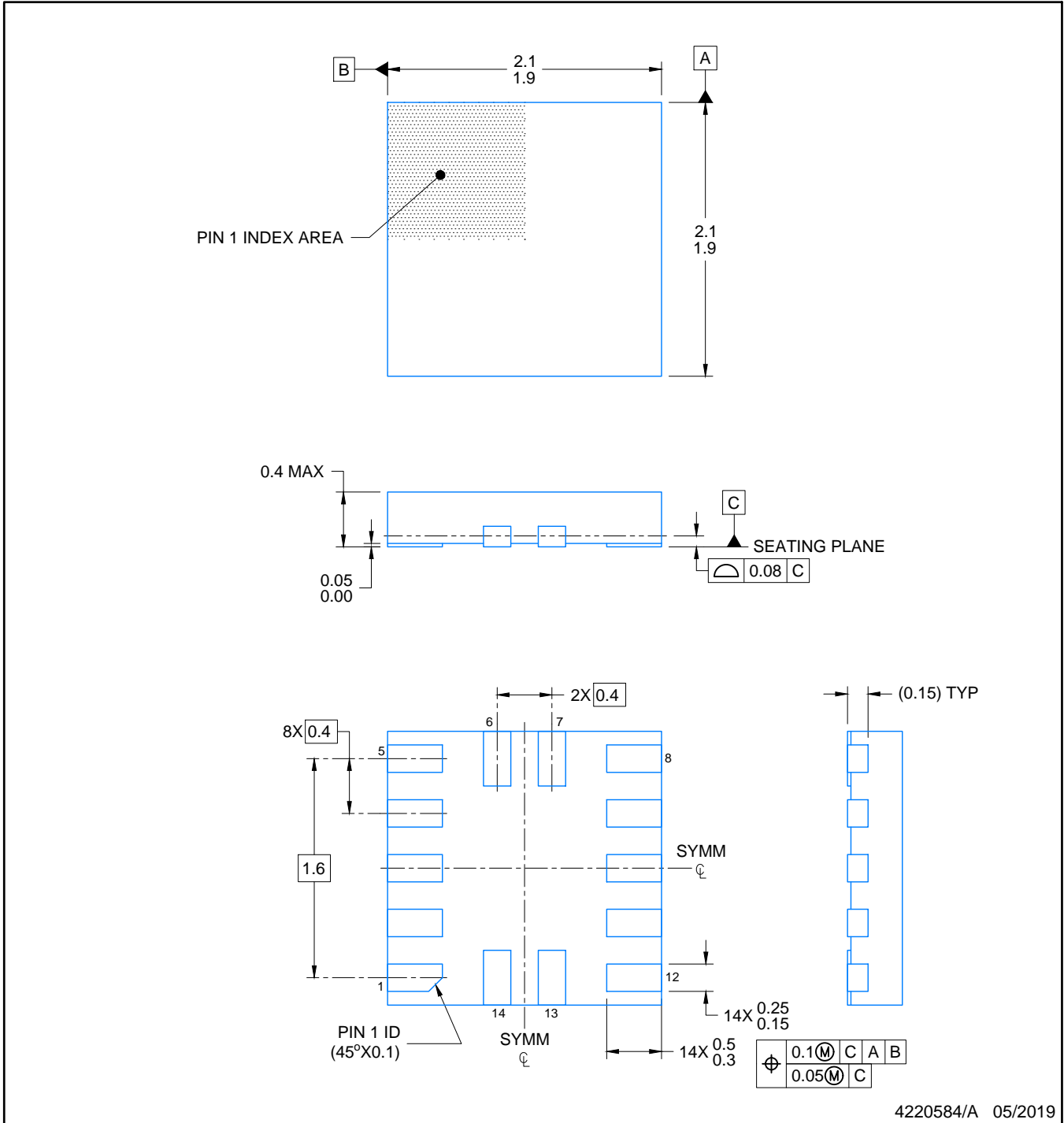


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

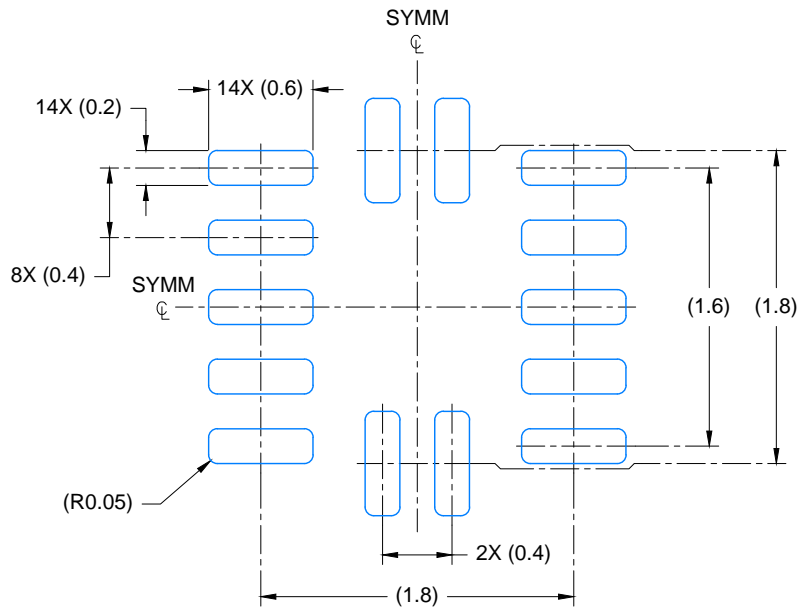
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



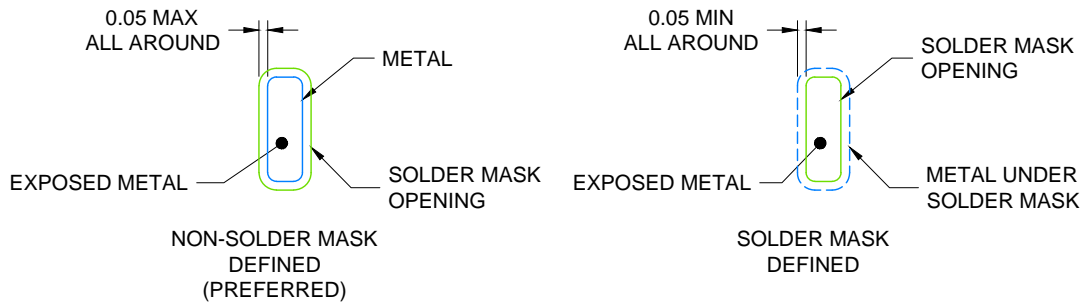
4220584/A 05/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 23X



SOLDER MASK DETAILS

4220584/A 05/2019

NOTES: (continued)

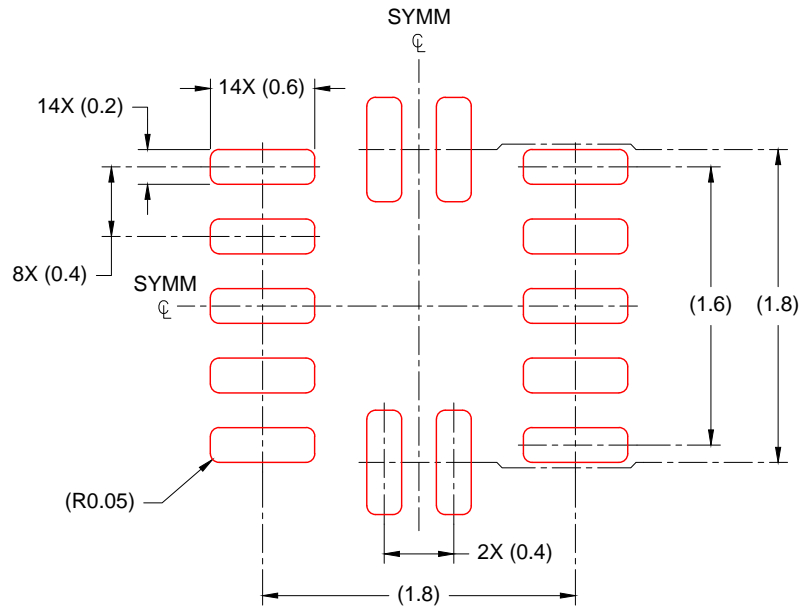
- For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

RUC0014A

X2QFN - 0.4 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.100mm THICK STENCIL
SCALE: 23X

4220584/A 05/2019

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

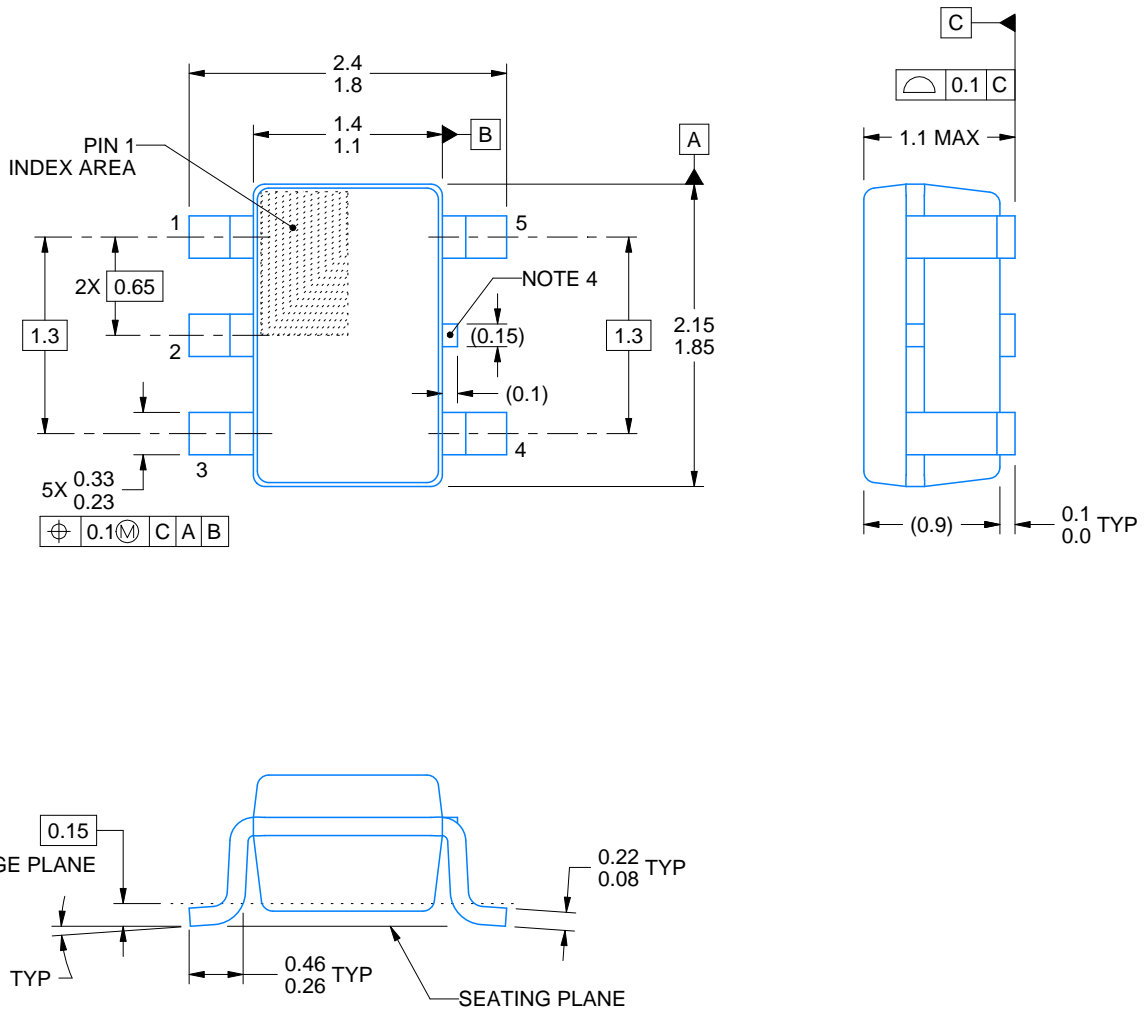
DCK0005A



PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/C 03/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.

EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/C 03/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

DDF0008A



PACKAGE OUTLINE

SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

DDF0008A

SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
SCALE:15X



NON SOLDER MASK
DEFINED



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/C 10/2022

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/C 10/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

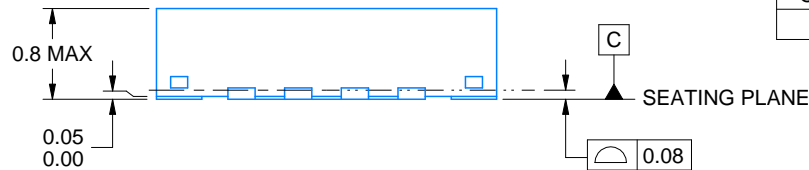
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225944/A



SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2



4219117/B 04/2022

NOTES:

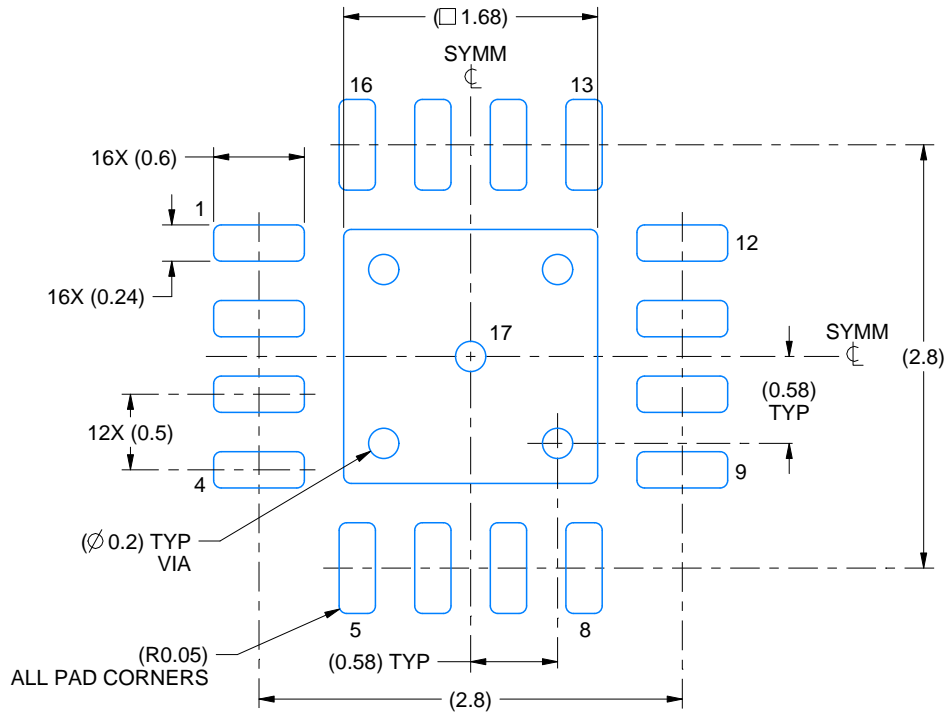
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

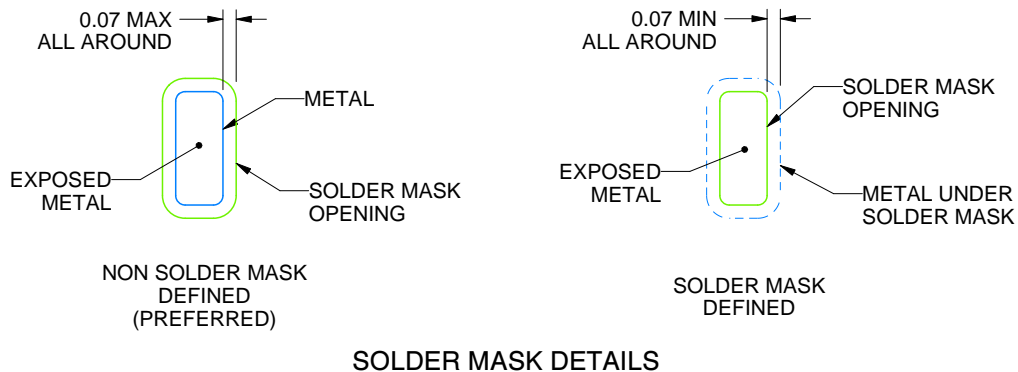
RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4219117/B 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/B 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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