

## 具有看门狗功能的 TPL5010 纳瓦级功耗系统计时器

### 1 特性

- 电源电压范围为 1.8V 至 5.5V
- 电压为 2.5V 时，电流消耗为 35nA（典型值）
- 可选计时间隔：100ms 至 7200s
- 计时器精度：1%（典型值）
- 可通过电阻选择时间间隔
- 看门狗功能
- 手动复位

### 2 应用

- 电池供电系统
- 物联网 (IoT)
- 出入探测
- 篡改检测
- 家庭自动化传感器
- 温度调节装置
- 消费类电子产品
- 远程传感器
- 白色家电

### 3 说明

TPL5010 纳瓦级计时器是一款超低功耗计时器，其看门狗功能专为占空比、电池供电型应用（比如物联网中的应用）中的系统唤醒功能而设计。其中许多应用需要使用  $\mu\text{C}$ ，因此，通常希望将  $\mu\text{C}$  维持在低功耗模式以更大限度节省电流，而仅在某些时间间隔内唤醒以收集数据或为中断提供服务。虽然  $\mu\text{C}$  的内部计时器可用于系统唤醒，但它可能单独消耗数微安的总系统电流。

TPL5010 仅消耗 35nA，可替代集成式  $\mu\text{C}$  计时器的功能。这样就可将  $\mu\text{C}$  置于低得多的功耗模式，将内部计时器关闭，并在被 TPL5010 中断时仅返回到激活模式。TPL5010 通过提供近两个数量级的功率节省，可以大幅减小能量采集或无线传感器应用中所使用的电池尺寸。TPL5010 提供 100ms 至 7200s 的可选时间间隔，适用于中断驱动型应用。出于安全考虑，某些标准（如 EN50271）要求实现看门狗功能。TPL5010 不仅实现了看门狗功能，而且几乎没有增加功耗。

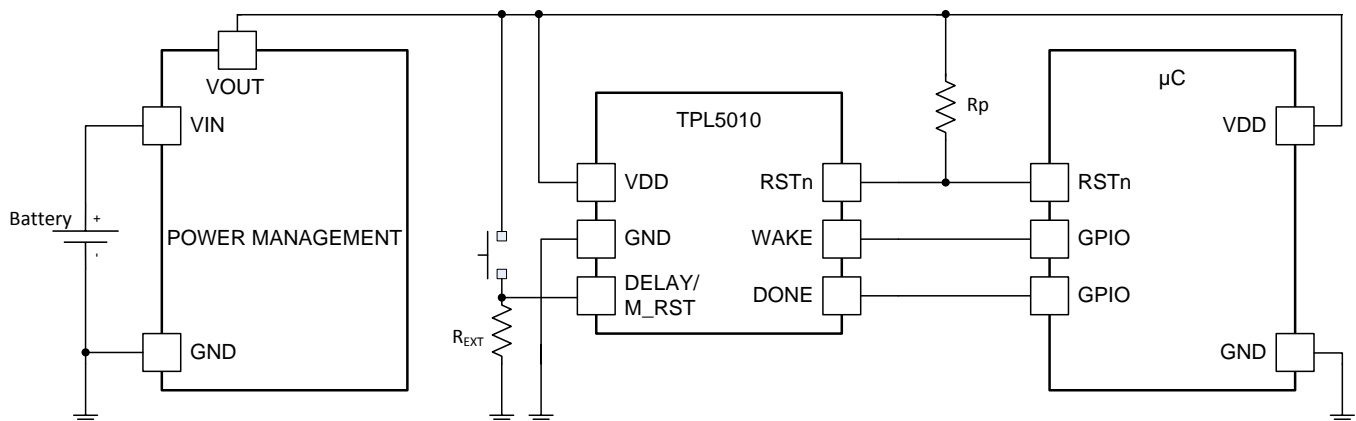
TPL5010 采用 6 引脚小外形尺寸晶体管 (SOT23) 封装。

#### 器件信息(1)

器件编号	封装	封装尺寸（标称值）
TPL5010	SOT23 (6)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

简化应用电路原理图



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## 4 修订历史记录

### Changes from Original (January 2015) to Revision A

**Page**

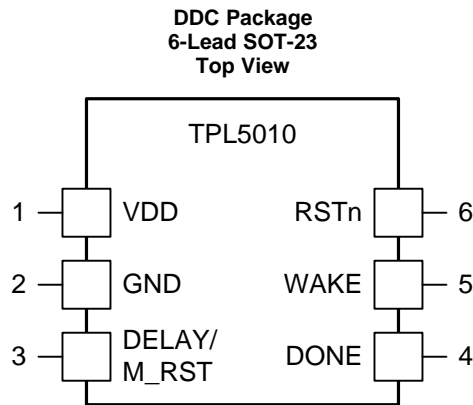
•	添加了 TPL5x1x 系列纳瓦级计时器表 .....	<b>3</b>
•	Changed $T_{ADC}$ and $R_D$ equations in the <i>Quantization Error</i> section .....	<b>14</b>
•	添加了接收文档更新通知部分 .....	<b>19</b>

## 5 器件比较表

**TPL5x1x 系列纳瓦级计时器**

器件编号	特殊 特性	输出	评分
TPL5010	低功耗计时器、看门狗功能	高电平有效	目录
TPL5010Q	低功耗计时器、看门狗功能	高电平有效	汽车
TPL5111	低功耗计时器、电源门控 MOS 驱动器	高电平有效	目录
TPL5110	低功耗计时器、电源门控 MOS 驱动器	低电平有效	目录

## 6 Pin Configuration and Functions



### Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION	APPLICATION INFORMATION
NO.	NAME			
1	VDD	P	Supply voltage	
2	GND	G	Ground	
3	DELAY/ M_RST	I	Time Interval set and Manual Reset	Resistance between this pin and GND is used to select the time interval. The reset switch is also connected to this pin.
4	DONE	I	Logic Input for watchdog functionality	Digital signal driven by the $\mu$ C to indicate successful processing of the WAKE signal.
5	WAKE	O	Timer output signal generated every $t_{IP}$ period.	Digital pulsed signal to wake up the $\mu$ C at the end of the programmed time interval.
6	RSTn	O	Reset Output (open drain output)	Digital signal to RESET the $\mu$ C, pullup resistance is required

(1) G= Ground, P= Power, O= Output, I= Input.

## 7 Specifications

### 7.1 Absolute Maximum Ratings<sup>(1)</sup>

	MIN	MAX	UNIT
Supply Voltage (VDD-GND)	-0.3	6	V
Input Voltage at any pin <sup>(2)</sup>	-0.3	VDD + 0.3	V
Input Current on any pin	-5	+5	mA
Junction Temperature, T <sub>J</sub> <sup>(3)</sup>		150	°C
Storage Temperature, T <sub>stg</sub>	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The voltage between any two pins should not exceed 6V.
- (3) The maximum power dissipation is a function of T<sub>J</sub>(MAX), θ<sub>JA</sub>, and the ambient temperature, T<sub>A</sub>. The maximum allowable power dissipation at any ambient temperature is P<sub>D</sub>MAX = (T<sub>J</sub>(MAX) - T<sub>A</sub>) / θ<sub>JA</sub>. All numbers apply for packages soldered directly onto a printed-circuit board (PCB).

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human Body Model, per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±1000	V
	Charged-device model (CDM), per JEDEC specification JESD22-101 <sup>(2)</sup>	±250	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Ratings

	MIN	MAX	UNIT
Supply Voltage (VDD-GND)	1.8	5.5	V
Temperature	-40	105	°C

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPL5010	UNIT
		DDC (SOT-23)	
		6 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	163	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	26	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	57	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	7.5	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	57	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report (SPRA953).

## 7.5 Electrical Characteristics<sup>(1)</sup>

Specifications are for  $T_A = 25^\circ\text{C}$ ,  $V_{DD-GND} = 2.5\text{ V}$ , unless otherwise stated.

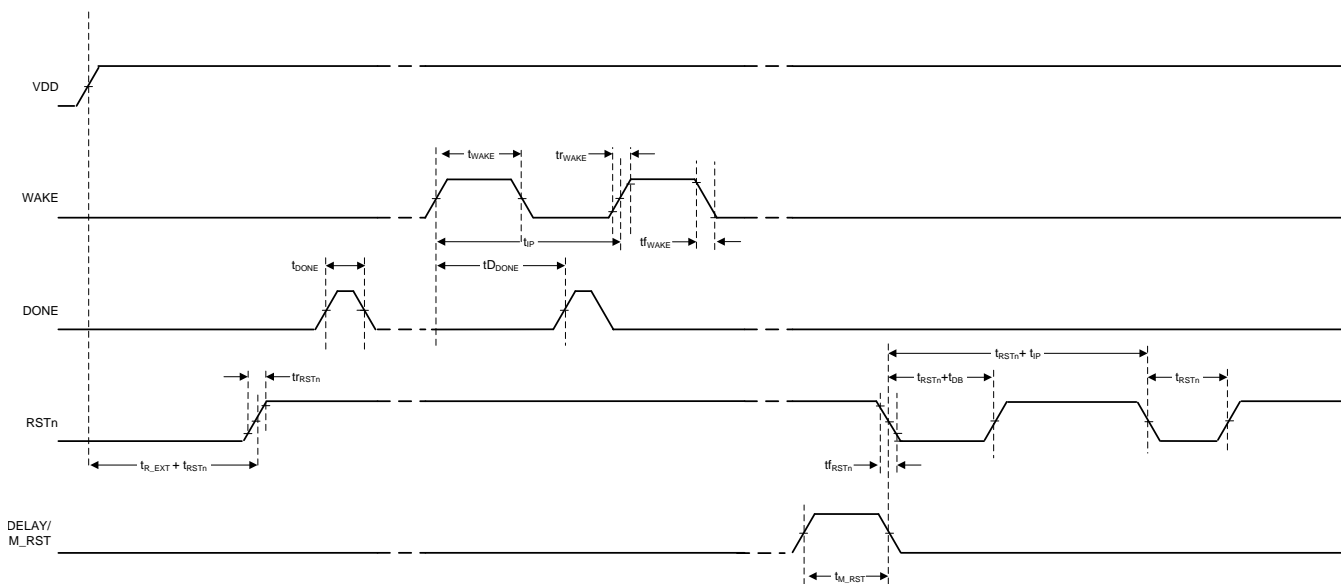
PARAMETER		TEST CONDITIONS		MIN <sup>(2)</sup>	TYP <sup>(3)</sup>	MAX <sup>(2)</sup>	UNIT
<b>POWER SUPPLY</b>							
IDD	Supply current <sup>(4)</sup>	Operation mode			35	50	nA
		Digital conversion of external resistance (Rext)			200	400	$\mu\text{A}$
<b>TIMER</b>							
t <sub>IP</sub>	Time Interval Period	1650 selectable Time Intervals	Minimum time interval		100		ms
			Maximum time interval		7200		s
	Time Interval Setting Accuracy <sup>(5)</sup>		Excluding the precision of Rext		±0.6%		
	Timer Interval Setting Accuracy over supply voltage		1.8 V ≤ VDD ≤ 5.5 V		±25		ppm/V
t <sub>OSC</sub>	Oscillator Accuracy			-0.5%		0.5%	
	Oscillator Accuracy over temperature <sup>(6)</sup>		-40°C ≤ T <sub>A</sub> ≤ 105°C		±100		±400 ppm/°C
	Oscillator Accuracy over supply voltage		1.8 V ≤ VDD ≤ 5.5 V		±0.4		%/V
	Oscillator Accuracy over life time <sup>(7)</sup>				0.24%		
t <sub>DONE</sub>	DONE Pulse width <sup>(6)</sup>			100			ns
t <sub>RSTn</sub>	RSTn Pulse width			320			ms
t <sub>WAKE</sub>	WAKE Pulse width			20			ms
t <sub>Rext</sub>	Time to convert Rext			100	120		ms
<b>DIGITAL LOGIC LEVELS</b>							
VIH	Logic High Threshold DONE pin			0.7 × VDD			V
VIL	Logic Low Threshold DONE pin					0.3 × VDD	V
VOH	Logic output High Level WAKE pin	I <sub>out</sub> = 100 $\mu\text{A}$		VDD - 0.3			V
		I <sub>out</sub> = 1 mA		VDD - 0.7			V
VOL	Logic output Low Level WAKE pin	I <sub>out</sub> = -100 $\mu\text{A}$				0.3	V
		I <sub>out</sub> = -1 mA				0.7	V
VOL <sub>RSTn</sub>	RSTn Logic output Low Level		I <sub>OL</sub> = -1 mA			0.3	V
IOH <sub>RSTn</sub>	RSTn High Level output current		VOH <sub>RSTn</sub> = VDD		1		nA
VIH <sub>M_RST</sub>	Logic High Threshold DELAY/M_RST pin			1.5			V

- (1) *Electrical Characteristics* values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that  $T_J = T_A$ . No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where  $T_J > T_A$ . *Absolute Maximum Ratings* indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
- (2) Limits are specified by testing, design, or statistical analysis at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
- (3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
- (4) The supply current excludes load and pullup resistor current. Input pins are at GND or VDD.
- (5) The accuracy for time interval settings below 1 second is ±100 ms.
- (6) This parameter is specified by design and/or characterization and is not tested in production.
- (7) Operational life time test procedure equivalent to 10 years.

## 7.6 Timing Requirements

			MIN <sup>(1)</sup>	NOM <sup>(2)</sup>	MAX <sup>(1)</sup>	UNIT
$t_{rRSTn}$	Rise Time RSTn <sup>(3)</sup>	Capacitive load 50 pF, Rpullup 100 kΩ		11		μs
$t_{fRSTn}$	Fall Time RSTn <sup>(3)</sup>	Capacitive load 50 pF, Rpullup 100 kΩ		50		ns
$t_{rWAKE}$	Rise Time WAKE <sup>(3)</sup>	Capacitive load 50 pF		50		ns
$t_{fWAKE}$	Fall Time WAKE <sup>(3)</sup>	Capacitive load 50 pF		50		ns
$t_{D_{DONE}}$	DONE to RSTn or WAKE to DONE delay	Minimum delay <sup>(4)</sup>		100		ns
		Maximum delay <sup>(4)</sup>		$t_{ip}$ - 20ms		ms
$t_{M\_RST}$	Valid Manual Reset	Observation time 30 ms	20			ms
$t_{DB}$	De-bounce Manual Reset			20		ms

- (1) Limits are specified by testing, design, or statistical analysis at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
- (2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
- (3) This parameter is specified by design and/or characterization and is not tested in production.
- (4) In case of RSTn from its falling edge, or in case of WAKE from its rising edge.



**Figure 1. TPL5010 Timing**

### 7.7 Typical Characteristics

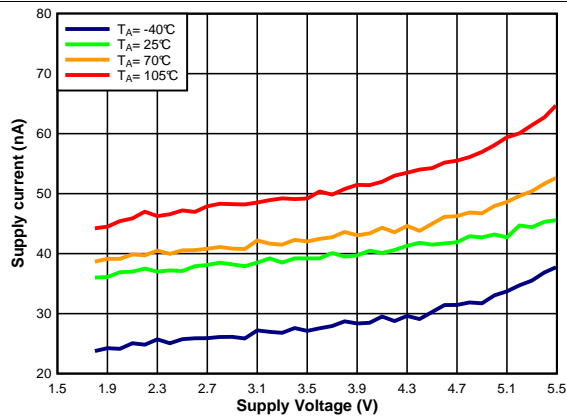


Figure 2.  $I_{DD}$  vs.  $V_{DD}$

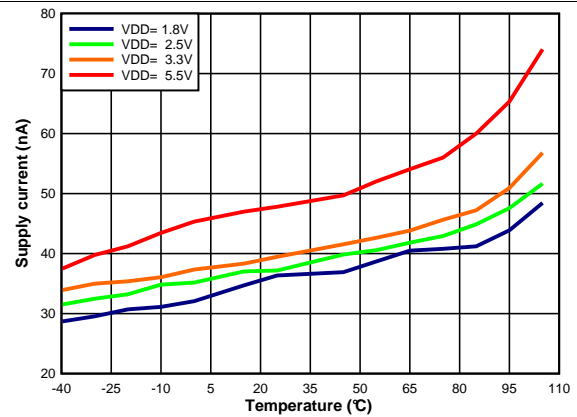


Figure 3.  $I_{DD}$  vs. Temperature

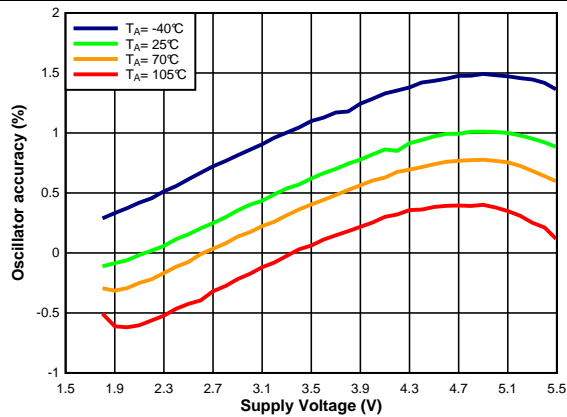


Figure 4. Oscillator Accuracy vs.  $V_{DD}$

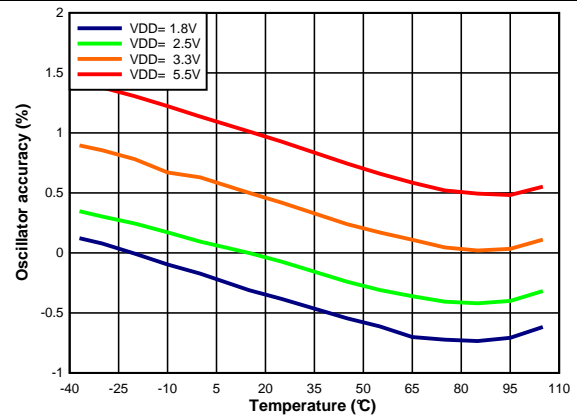


Figure 5. Oscillator Accuracy vs. Temperature

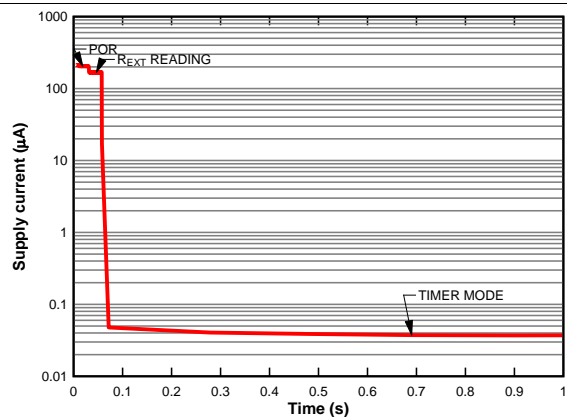
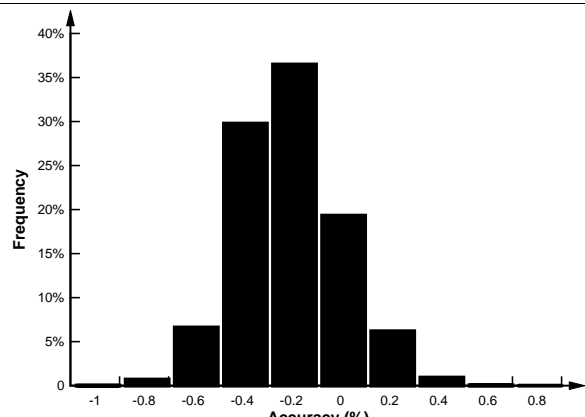


Figure 6.  $I_{DD}$  vs. Time



number of observations >20000  
 $1s < t_{IP} \leq 7200s$

Figure 7. Time Interval Setting Accuracy

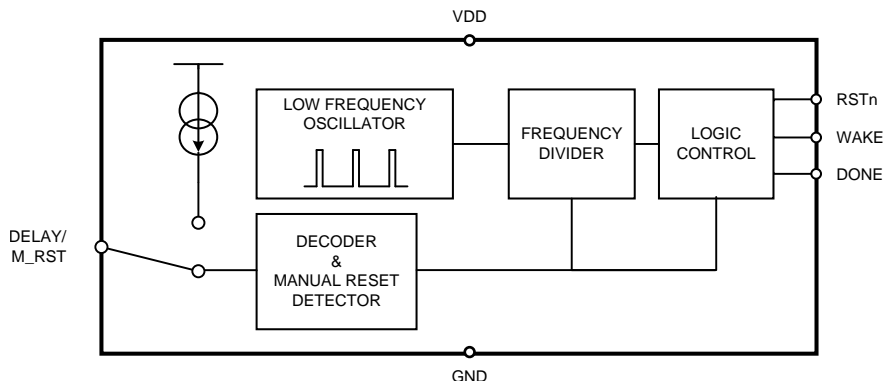


## 8 Detailed Description

### 8.1 Overview

The TPL5010 is a system wake-up timer with a watchdog feature designed for low-power applications. The TPL5010 can be used in interrupt-driven applications and provides selectable timing from 100 ms to 7200 s.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

The DONE, WAKE and RSTn signals are used to implement the watchdog function. The TPL5010 is programmed to issue a periodic WAKE pulse to a  $\mu\text{C}$  which is in sleep or standby mode. After receiving the WAKE pulse, the  $\mu\text{C}$  must issue a DONE signal to the TPL5010 at least 20 ms before the rising edge of the next WAKE pulse. If the DONE signal is not asserted, the TPL5010 asserts the RSTn signal to reset the  $\mu\text{C}$ . A manual reset function is realized by momentarily pulling the DELAY/M\_RST pin to VDD.

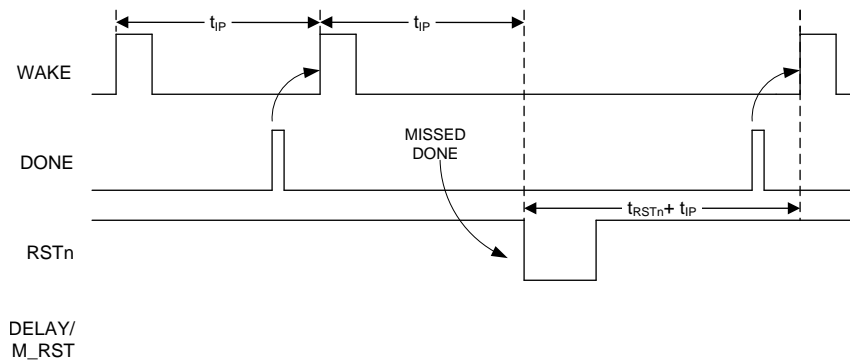


Figure 8. Watchdog

#### 8.3.1 WAKE

The WAKE pulse is sent out from the TPL5010 when the programmed time interval starts (except at the beginning of the first cycle or if in the previous interval the DONE has not been received).

This signal is normally low.

#### 8.3.2 DONE

The DONE pin is driven by a  $\mu\text{C}$  to signal successful processing of the WAKE signal. The TPL5010 recognizes a valid DONE signal as a low to high transition. If two or more DONE signals are received within the time interval, only the first DONE signal is processed.

The DONE signal resets the counter of the watchdog only. If the DONE signal is received when the WAKE is still high, the WAKE will go low as soon as the DONE is recognized.

## Feature Description (continued)

### 8.3.3 RSTn

To implement the reset interface between the TPL5010 and the  $\mu\text{C}$  a pullup resistance is required. 100 k $\Omega$  is recommended to minimize current.

During the POR and the reading of the REXT, the RSTn signal is LOW.

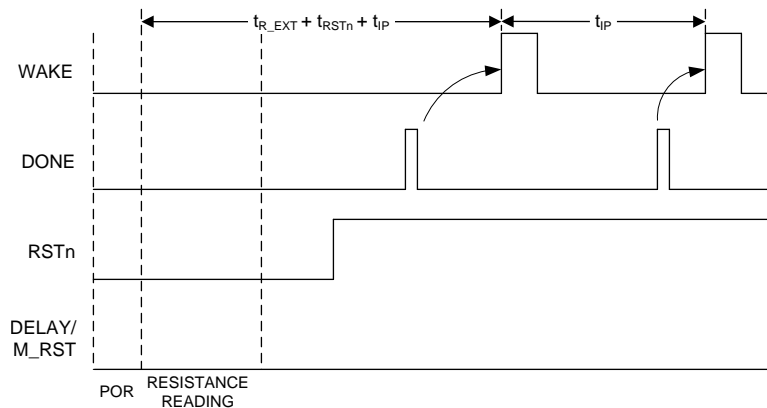
RSTn is asserted (LOW) for either one of the following conditions:

1. If the DELAY/M\_RST pin is high for at least two consecutive cycles of the internal oscillator (approximately 20 ms).
2. At the beginning of a new time interval if DONE is not received at least 20 ms before the next WAKE rising edge (see [Figure 8](#)).

## 8.4 Device Functional Modes

### 8.4.1 Start-Up

During start-up after POR, the TPL5010 executes a one-time measurement of the resistance attached to the DELAY/M\_RST pin to determine the desired time interval for WAKE. This measurement interval is  $t_{R\_EXT}$ . During this measurement, a constant current is temporarily flowing into  $R_{EXT}$ .



**Figure 9. Start-Up**

### 8.4.2 Normal Operating Mode

During normal operating mode, the TPL5010 asserts periodic WAKE pulses in response to valid DONE pulses from the  $\mu\text{C}$ . If either a manual reset is applied (logic HIGH on DELAY/M\_RST pin), or the  $\mu\text{C}$  does not issue a DONE pulse within the required time, the TPL5010 asserts the RSTn signal to the  $\mu\text{C}$  and restarts its internal counters. See [Figure 8](#) and [Figure 10](#).

## 8.5 Programming

### 8.5.1 Configuring the WAKE Interval With the DELAY/M\_RST Pin

The time interval between two adjacent WAKE pulses (rising edges) is selectable through an external resistance ( $R_{EXT}$ ) between the DELAY/M\_RST pin and ground. The value of the resistance  $R_{EXT}$  is converted one time after POR. The allowable range of  $R_{EXT}$  is 500  $\Omega$  to 170 k $\Omega$ . At least a 1% precision resistance is recommended. See section [Timer Interval Selection Using External Resistance](#) on how to set the WAKE pulse interval using  $R_{EXT}$ .

The time between two adjacent RESET signals (falling edges), or between a RESET (falling edge) and a WAKE (rising edge), is given by the sum of the programmed time interval and the  $t_{RSTn}$  (reset pulse width).

## Programming (continued)

### 8.5.2 Manual Reset

If VDD is connected to the DELAY/M\_RST pin, the TPL5010 recognizes this as a manual reset condition. In this case, the time interval is not set. If the manual reset is asserted during the POR or during the reading procedure, the reading procedure is aborted and is restarted as soon as the manual reset switch is released. A pulse on the DELAY/M\_RST pin is recognized as a valid manual reset only if it lasts at least 20 ms (observation time is 30 ms).

A valid manual reset resets all the counters inside the TPL5010. The counters restart only when the high digital voltage at DELAY/M\_RST is removed and the next  $t_{RSTn}$  is elapsed.

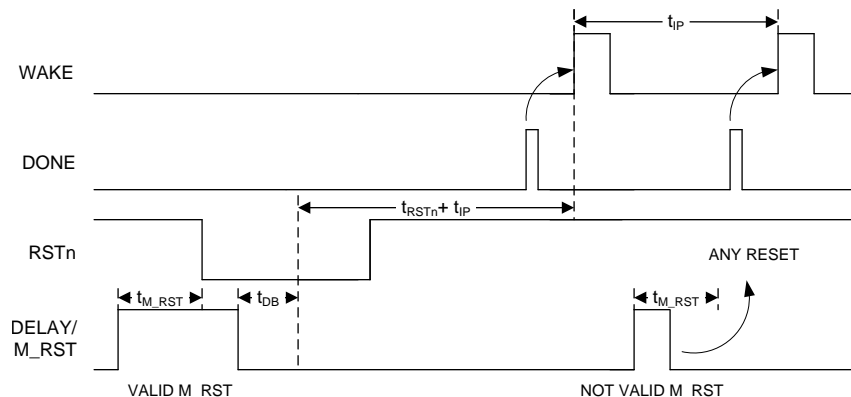


Figure 10. Manual Reset

#### 8.5.2.1 DELAY/M\_RST

A resistance in the range between 500  $\Omega$  and 170 k $\Omega$  needs to be connected to select a valid time interval. At the POR and during the reading of the resistance the DELAY/M\_RST is connected to an analog signal chain though a mux. After the reading of the resistance the analog circuit is switched off and the DELAY/RST is connected to a digital circuit.

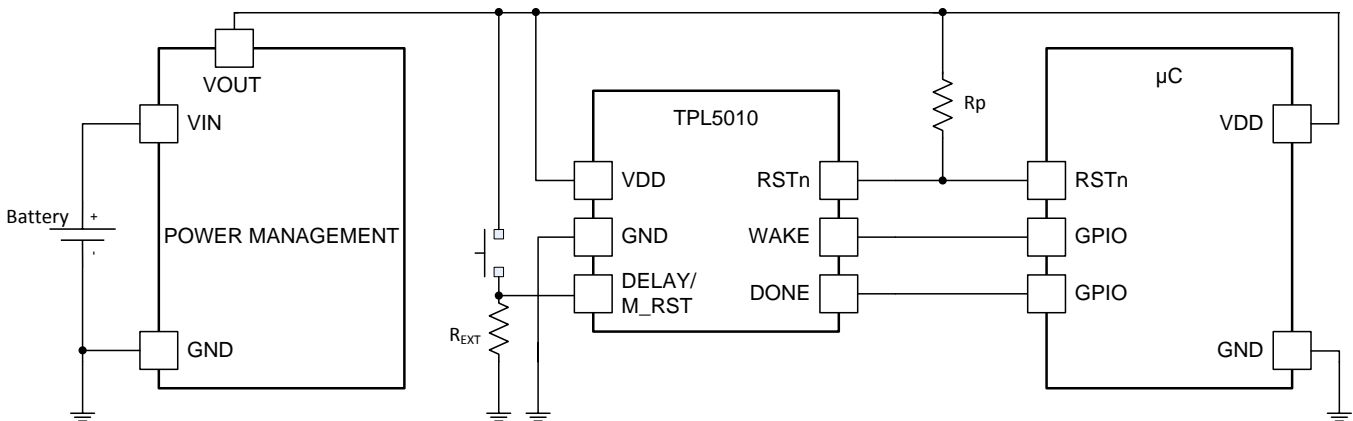
The manual reset detection is supported with a de-bounce feature which makes the TPL5010 insensitive to the glitches on the DELAY/M\_RST pin. When a valid manual reset signal is asserted on the DELAY/M\_RST pin, the RSTn signal is asserted LOW after a delay of  $t_{M\_RST}$ . It remains LOW after a valid manual reset is asserted +  $t_{DB}$  +  $t_{RSTn}$ . Due to the asynchronous nature of the manual reset signal and its arbitrary duration, the LOW status of the RSTn signal maybe affected by an uncertainty of about  $\pm 5$  ms.

A valid manual reset puts all the digital output signals at their default values:

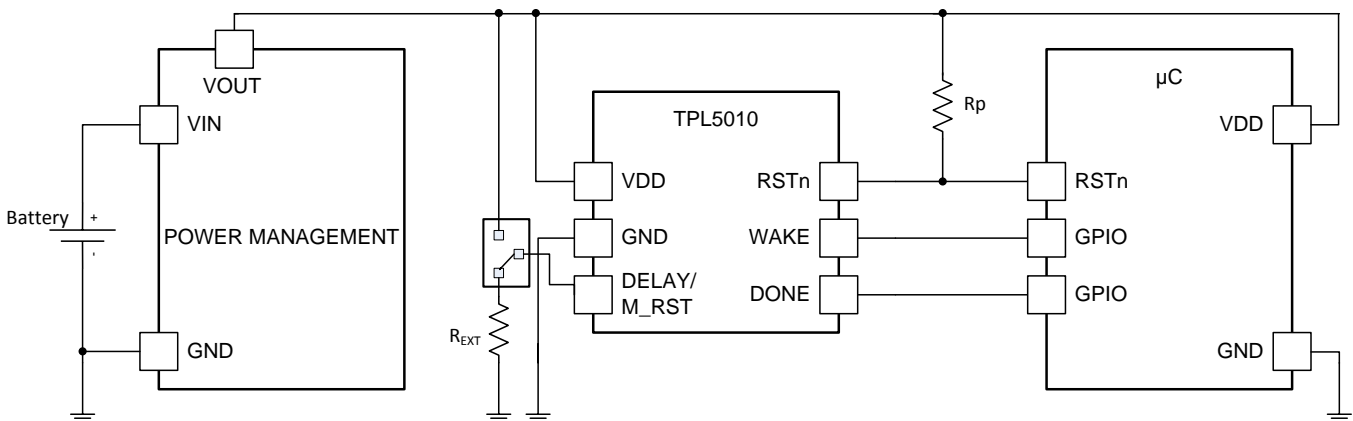
- WAKE = LOW
- RSTn = asserted LOW

#### 8.5.2.2 Circuitry

The manual reset may be implemented using a switch (momentary mechanical action). The TPL5010 offers two possible approaches according to the power consumption constraints of the application.

**Programming (continued)**

**Figure 11. Manual Reset With SPST Switch**

For use cases that do not require the lowest power consumption, using a single-pole single-throw switch may offer a lower-cost solution. The DELAY/M\_RST pin may be directly connected to VDD with  $R_{EXT}$  in the circuit. The current drawn from the supply voltage during the reset is given by  $VDD/R_{EXT}$ .


**Figure 12. Manual Reset With SPDT Switch**

The reset function may also be asserted by switching DELAY/M\_RST from  $R_{EXT}$  to VDD using a single-pole double-throw switch, which will provide a lower power solution for the manual reset, because no current flows.

**8.5.3 Timer Interval Selection Using External Resistance**

To set the time interval, the external resistance  $R_{EXT}$  is selected according to [Equation 1](#):

$$R_{EXT} = 100 \left( \frac{-b + \sqrt{b^2 - 4a(c - 100T)}}{2a} \right)$$

where

- T is the desired time interval in seconds.
- $R_{EXT}$  is the resistance value to use in  $\Omega$ .
- a, b, and c are coefficients depending on the range of the time interval.

(1)

**Programming (continued)**
**Table 1. Coefficients for Equation 1**

SET	Time interval Range (s)	a	b	c
1	1 < T ≤ 5	0.2253	-20.7654	570.5679
2	5 < T ≤ 10	-0.1284	46.9861	-2651.8889
3	10 < T ≤ 100	0.1972	-19.3450	692.1201
4	100 < T ≤ 1000	0.2617	-56.2407	5957.7934
5	T > 1000	0.3177	-136.2571	34522.4680

**EXAMPLE**

Required time interval: 8 s

The coefficient set to be selected is the number 2. The formula becomes Equation 2.

$$R_{EXT} = 100 \left( \frac{46.9861 - \sqrt{46.9861^2 + 4 * 0.1284 (-2561.8889 - 100 * 8)}}{2 * 0.1284} \right) \quad (2)$$

The resistance value is 10.18 kΩ.

Table 2 and Table 3 contain example values of t<sub>IP</sub> and their corresponding value of R<sub>EXT</sub>.

**Table 2. First 9 Time Intervals**

t <sub>IP</sub> (ms)	Resistance (Ω)	Closest Real Value (Ω)	Parallel of Two 1% Tolerance Resistors, (kΩ)
100	500	500	1.0 // 1.0
200	1000	1000	-
300	1500	1500	2.43 // 3.92
400	2000	2000	-
500	2500	2500	4.42 // 5.76
600	3000	3000	5.36 // 6.81
700	3500	3500	4.75 // 13.5
800	4000	4000	6.19 // 11.3
900	4500	4501	6.19 // 16.5

**Table 3. Most Common Time Intervals Between 1s to 2h**

t <sub>IP</sub>	Calculated Resistance (kΩ)	Closest Real Value (kΩ)	Parallel of Two 1% Tolerance Resistors, (kΩ)
1s	5.20	5.202	7.15 // 19.1
2s	6.79	6.788	12.4 // 15.0
3s	7.64	7.628	12.7 // 19.1
4s	8.30	8.306	14.7 // 19.1
5s	8.85	8.852	16.5 // 19.1
6s	9.27	9.223	18.2 // 18.7
7s	9.71	9.673	19.1 // 19.6
8s	10.18	10.180	11.5 // 8.87
9s	10.68	10.68	17.8 // 26.7
10s	11.20	11.199	15.0 // 44.2
20s	14.41	14.405	16.9 // 97.6
30s	16.78	16.778	32.4 // 34.8
40s	18.75	18.748	22.6 // 110.0
50s	20.047	20.047	28.7 // 66.5

**Table 3. Most Common Time Intervals Between 1s to 2h (continued)**

$t_P$	Calculated Resistance (k $\Omega$ )	Closest Real Value (k $\Omega$ )	Parallel of Two 1% Tolerance Resistors, (k $\Omega$ )
1min	22.02	22.021	40.2 // 48.7
2min	29.35	29.349	35.7 // 165.0
3min	34.73	34.729	63.4 // 76.8
4min	39.11	39.097	63.4 // 102.0
5min	42.90	42.887	54.9 // 196.0
6min	46.29	46.301	75.0 // 121.0
7min	49.38	49.392	97.6 // 100.0
8min	52.24	52.224	88.7 // 127.0
9min	54.92	54.902	86.6 // 150.0
10min	57.44	57.437	107.0 // 124.0
20min	77.57	77.579	140.0 // 174.0
30min	92.43	92.233	182.0 // 187.0
40min	104.67	104.625	130.0 // 536.00
50min	115.33	115.331	150.0 // 499.00
1h	124.91	124.856	221.0 // 287.00
1h30min	149.39	149.398	165.0 // 1580.0
2h	170.00	170.00	340.0 // 340.0

#### 8.5.4 Quantization Error

The TPL5010 can generate 1650 discrete timer intervals in the range of 100 ms to 7200 s. The first 9 intervals are multiples of 100 ms. The remaining 1641 intervals cover the range between 1 s to 7200 s. Because they are discrete intervals, there is a quantization error associated with each value.

The quantization error can be evaluated according to [Equation 3](#):

$$Err = 100 \frac{(T_{DESIRED} - T_{ADC})}{T_{DESIRED}}$$

where

- $T_{ADC} = \text{INT} \left[ \frac{1}{100} (aR_D^2 + bR_D + c) \right]$
- $R_D = \frac{R_{EXT}}{100}$

(3)

$R_{EXT}$  is the resistance calculated with [Equation 1](#) and a, b, c are the coefficients of the equation listed in [Table 1](#).

#### 8.5.5 Error Due to Real External Resistance

$R_{EXT}$  is a theoretical value and may not be available in standard commercial resistor values. It is possible to closely approach the theoretical  $R_{EXT}$  using two or more standard values in parallel. However, standard values are characterized by a certain tolerance. This tolerance will affect the accuracy of the time interval.

The accuracy can be evaluated using the following procedure:

1. Evaluate the min and max values of  $R_{EXT}$  ( $R_{EXT\_MIN}$ ,  $R_{EXT\_MAX}$  with [Equation 1](#) using the selected commercial resistance values and their tolerances.
2. Evaluate the time intervals ( $T_{ADC\_MIN}[R_{EXT\_MIN}]$ ,  $T_{ADC\_MAX}[R_{EXT\_MAX}]$ ) with the  $T_{ADC}$  equation mentioned in [Equation 3](#).
3. Find the errors using [Equation 3](#) with  $T_{ADC\_MIN}$ ,  $T_{ADC\_MAX}$ .

The results of the formula indicate the accuracy of the time interval.

The example below illustrates the procedure.

- Desired time interval,  $T_{\text{desired}} = 600 \text{ s}$ ,
- Required  $R_{\text{EXT}}$  from [Equation 1](#),  $R_{\text{EXT}} = 57.44 \text{ k}\Omega$ .

From [Table 3](#)  $R_{\text{EXT}}$  can be built with a parallel combination of two commercial values with 1% tolerance:  $R_1 = 107 \text{ k}\Omega$ ,  $R_2 = 124 \text{ k}\Omega$ . The uncertainty of the equivalent parallel resistance can be found using [Equation 4](#):

$$uR_{//} = R_{//} \sqrt{\left(\frac{u_{R1}}{R1}\right)^2 + \left(\frac{u_{R2}}{R2}\right)^2}$$

where

- $u_{Rn}$  ( $n=1,2$ ) represent the uncertainty of a resistance (see [Equation 5](#)) (4)

$$u_{Rn} = Rn \frac{\textit{Tolerance}}{\sqrt{3}} \tag{5}$$

The uncertainty of the parallel resistance is 0.82%, which means the value of  $R_{\text{EXT}}$  may range between  $R_{\text{EXT\_MIN}} = 56.96 \text{ k}\Omega$  and  $R_{\text{EXT\_MAX}} = 57.90 \text{ k}\Omega$ .

Using these value of  $R_{\text{EXT}}$ , the digitized timer intervals calculated by  $T_{\text{ADC}}$  equation mentioned in [Equation 3](#) are respectively  $T_{\text{ADC\_MIN}} = 586.85 \text{ s}$  and  $T_{\text{ADC\_MAX}} = 611.3 \text{ s}$ , giving an error range of  $-1.88\% / +2.19\%$ . The asymmetry of the error range is due to the quadratic transfer function of the resistance digitizer.

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

In battery-powered applications, one design constraint is the need for low current consumption. The TPL5010 is designed for applications where there is a need to monitor environmental conditions at a fixed time interval. Often in these applications a watchdog or other internal timer in a  $\mu\text{C}$  is used to implement a wake-up function. Using the TPL5010 to implement the watchdog function will consume only tens of nA, significantly improving the power consumption of the system.

### 9.2 Typical Application

The TPL5010 can be used in conjunction with environment sensors to build a low-power environment data-logger, such as an air quality data-logger. In this application, due to the monitored phenomena, the  $\mu\text{C}$  and the front end of the sensor spend most of the time in the idle state, waiting for the next logging interval, usually a few hundred of milliseconds. Figure 13 shows a data logging application based on a  $\mu\text{C}$  and a front end for a gas sensor based on the LMP91000.

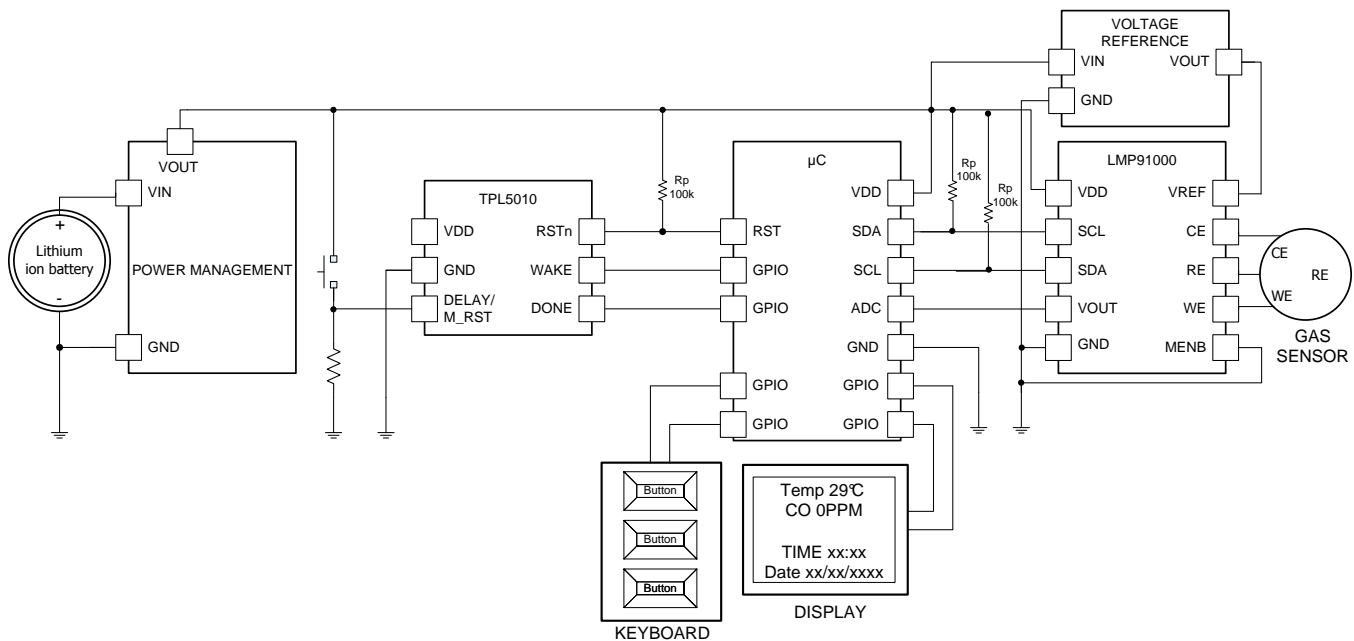


Figure 13. Data-Logger

#### 9.2.1 Design Requirements

The design is driven by the low-current consumption constraint. The data are usually acquired on a rate that ranges between 1 s and 10 s. The highest necessity is the maximization of the battery life. The TPL5010 helps achieve that goal because it allows putting the  $\mu\text{C}$  in its lowest power mode. The TPL5010 will take care of the watchdog and the timing.



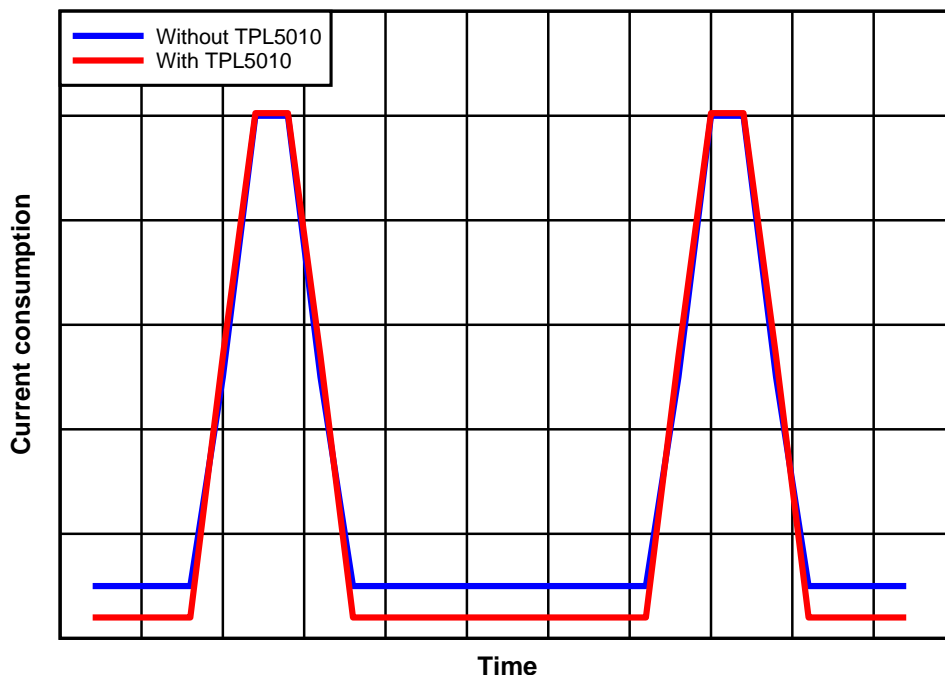
**Typical Application (continued)**

**9.2.2 Detailed Design Procedure**

When the main constraint is the battery life, the selection of a low power voltage reference, the  $\mu\text{C}$ , and the display is mandatory. The first step in the design is the calculation of the power consumption of the devices in their different mode of operations. For instance, the LMP91000 burns most of the power when in gas measurement mode, then, according to the connected gas sensor, it has two idle states (standby and deep sleep). The same is true for the  $\mu\text{C}$ , such as one of the MSP430 family, which can be placed in one of its lower power modes, such as LMP3.5 or LMP4.5. In this case, the TPL5010 can be used to implement the watchdog and wake-up timing functions.

After the power budget calculation, it is possible to select the appropriate time interval which satisfies the application constraints and maximize the life of the battery.

**9.2.3 Application Curve**



**Figure 14. Effect of TPL5010 on Current Consumption**

## 10 Power Supply Recommendations

The TPL5010 requires a voltage supply within 1.8 V and 5.5 V. A multilayer ceramic bypass X7R capacitor of 0.1  $\mu$ F between VDD and GND pin is recommended.

## 11 Layout

### 11.1 Layout Guidelines

The DELAY/M\_RST pin is sensitive to parasitic capacitance. TI suggests that the traces connecting the resistance on this pin to GROUND be kept as short as possible to minimize parasitic capacitance. This capacitance can affect the initial set up of the time interval. Signal integrity on the WAKE and RSTn pins is also improved by keeping the trace length between the TPL5010 and the  $\mu$ C short to reduce the parasitic capacitance.

### 11.2 Layout Example

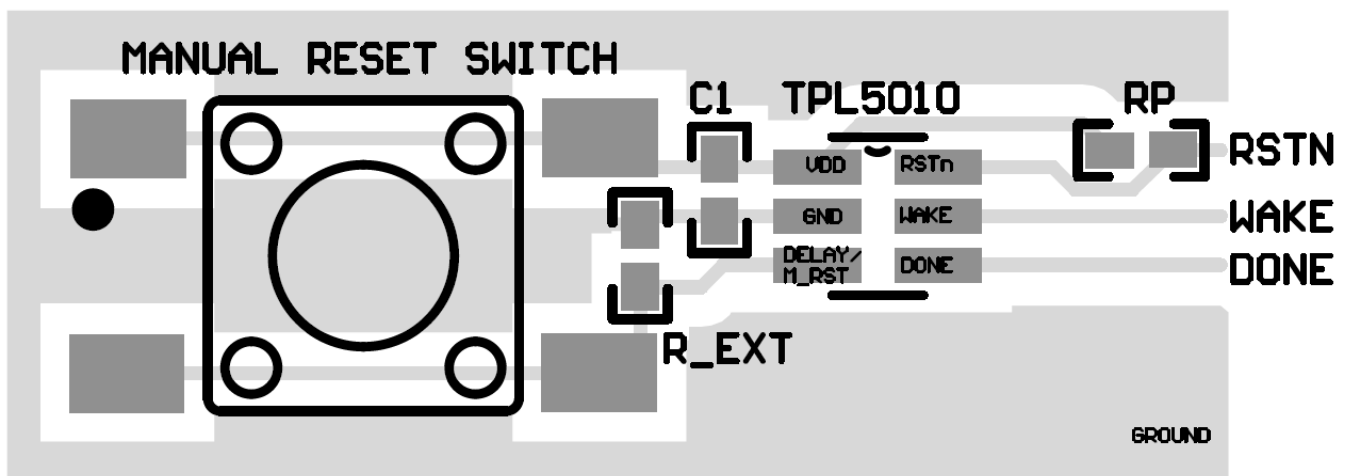


Figure 15. Layout

## 12 器件和文档支持

### 12.1 接收文档更新通知

要接收文档更新通知，请导航至 [TI.com.cn](http://TI.com.cn) 上的器件产品文件夹。单击右上角的 [通知我](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 12.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [《使用条款》](#)。

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**设计支持** [TI 参考设计支持](#) 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

### 12.3 商标

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### 12.4 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 12.5 术语表

[SLYZ022](#) — *TI* 术语表。

这份术语表列出并解释术语、缩写和定义。

## 13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此产品说明书的浏览器版本，请查阅左侧的导航栏。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPL5010DDCR	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ZAKX	<a href="#">Samples</a>
TPL5010DDCT	ACTIVE	SOT-23-THIN	DDC	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	ZAKX	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

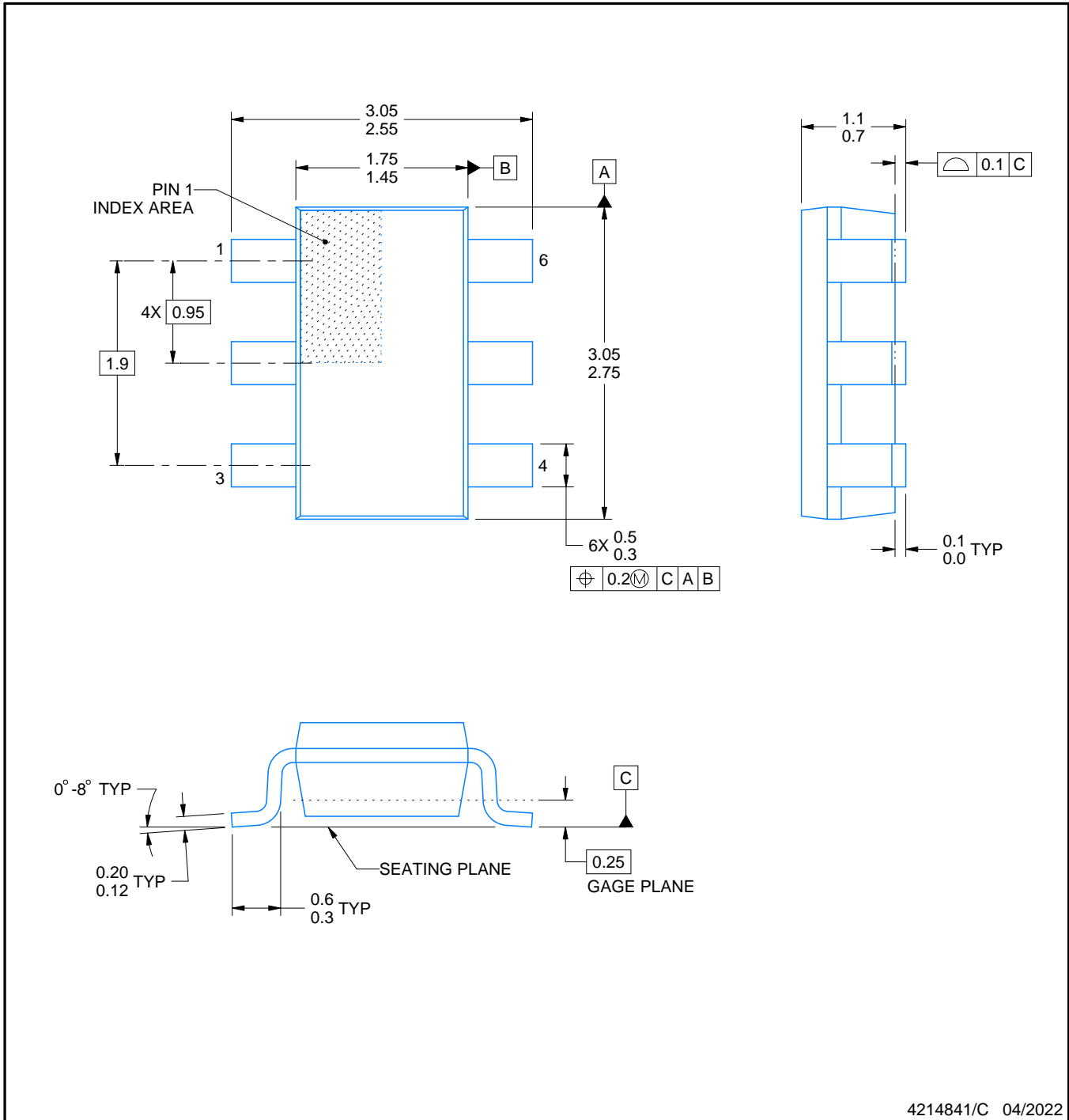

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPL5010DDCR	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPL5010DDCT	SOT-23-THIN	DDC	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPL5010DDCT	SOT-23-THIN	DDC	6	250	180.0	8.4	3.1	3.05	1.1	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPL5010DDCR	SOT-23-THIN	DDC	6	3000	208.0	191.0	35.0
TPL5010DDCT	SOT-23-THIN	DDC	6	250	208.0	191.0	35.0
TPL5010DDCT	SOT-23-THIN	DDC	6	250	183.0	183.0	20.0

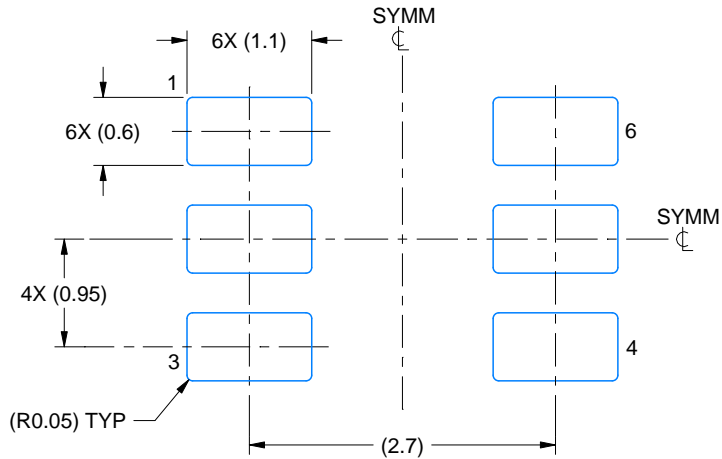


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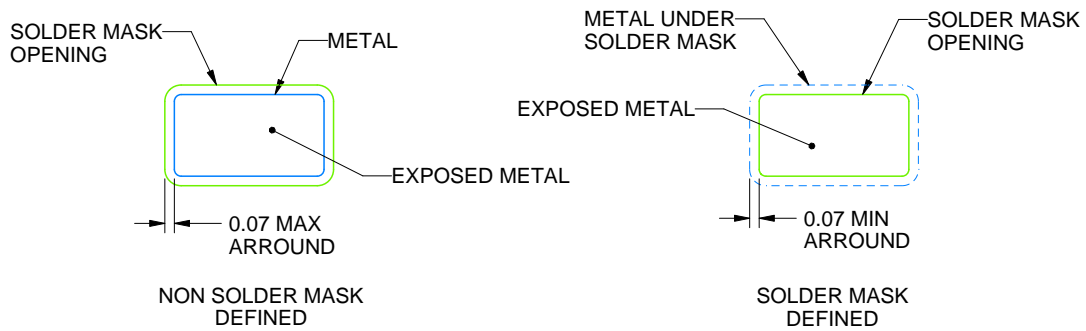
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.





LAND PATTERN EXAMPLE  
EXPLODED METAL SHOWN  
SCALE:15X



SOLDEMASK DETAILS

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NOTES: (continued)

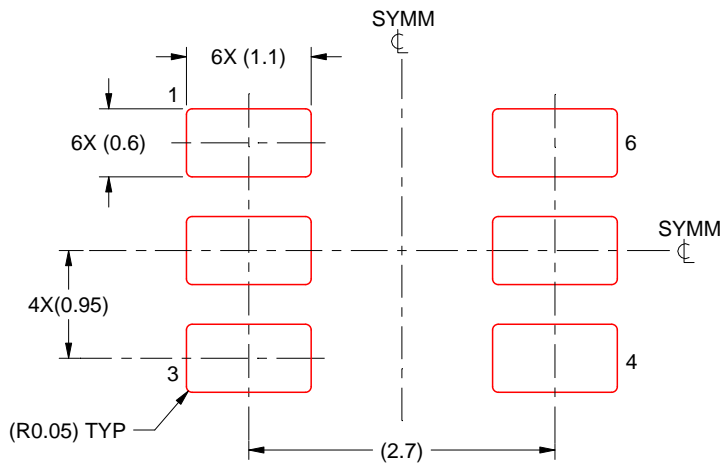
- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:15X

4214841/C 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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