TPL7407L 40V 7 通道低侧驱动器

查询样片: TPL7407L

特性

- **600mA** 额定漏极电流（每通道）
- **7** 通道达灵顿 **(Darlington)** 阵列（例如 **ULN2003A**）的 **CMOS** 引脚到引脚改进
- 功耗（极低 V_{OL}）
  - 电流为 **100mA** 时，V_{OL} 低于达灵顿 **(Darlington)** 阵列的四分之一
- 每通道小于 **10nA** 的极低输出泄露
- 扩展环境温度范围：
  T_A **= -40°C** 至 **125°C**
- 高压输出 **40V**
- 与 **1.8V** 至 **5.0V** 微控制器和逻辑接口兼容
- 用于感应反冲保护的内部自振荡二极管
- 输入下拉电阻器可实现三态输入驱动器
- 用来消除嘈杂环境中寄生运行的输入电阻电容 **(RC)** 缓冲器
- 电感负载驱动器应用
- 静电放电 **(ESD)** 保护性能超过 **JESD 22** 规范要求
  - **2kV** 人体模型 **(HBM)**，**500V** 充电器件模型 **(CDM)**
- 采用 **16** 引脚小外形尺寸集成电路 **(SOIC)** 和薄型小外形尺寸 **(TSSOP)** 封装

应用范围

- 电感负载
  - 继电器
  - 单极步进 **&** 有刷直流电机
  - 螺线管 **&** 阀门
- 发光二极管 **(LED)**
- 逻辑电平位移
- 栅极 **&** 绝缘栅双极型晶体管 **(IGBT)** 驱动

说明

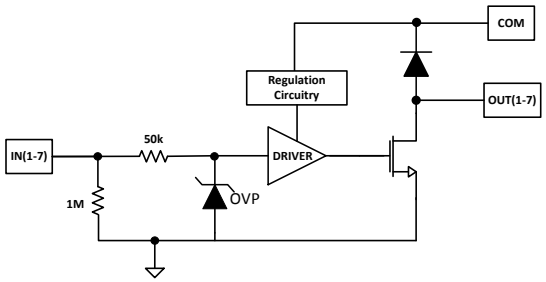
TPL7407L 是一款高压、高电流 NMOS 晶体管阵列。这个器件包含 7 个特有高压输出的 NMOS 晶体管，这些晶体管具有针对开关电感负载的共阴极钳位二极管。一个单个 NMOS 通道的最大漏极电流额定值为 600mA。 增加的全新稳压和驱动电路在整个通用输入输出 (GPIO) 范围内 (1.8V-5.0V) 提供最大驱动强度。可将这些晶体管并联以实现更高的电流能力。

TPL7407L 的主要优势是其经提升的效率以及低于双极达灵顿 (Darlington) 器件的泄露值。 借助于较低的 V_{OL}，功率耗散比传统中继驱动器少一半，每通道的电流少于 250mA。

器件信息

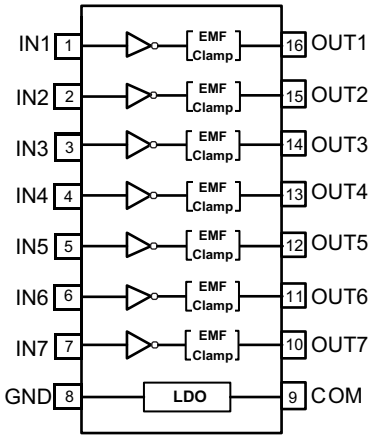
订货编号	封装（引脚）	封装尺寸
TPL7407L	SOIC (16)	9.9mm x 3.91mm
TPL7407L	TSSOP (16)	5.0mm x 4.4mm

简化电路原理图



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TERMINAL CONFIGURATION AND FUNCTIONS



Terminal Functions

TERMINAL		DESCRIPTION
NAME	NUMBER	
IN(X)	1, 2, 3, 4, 5, 6, 7	GPIO inputs that will drive the outputs "low" (or sinnk current) when driven "high"
OUT(X)	16, 15, 14, 13, 12, 11, 10	Driver output that sinks currents after input is driven "high"
COM	9	Supply PIn that should be tied to 8.5V or higher for proper operation
GND	8	Ground pin

Specifications

Absolute Maximum Ratings(1)

at 25°C free-air temperature (unless otherwise noted)

		MIN	MAX	UNIT
V_{OUT}	Pins OUT1-OUT7 to GND voltage	-0.3	42	V
V_{OK}	Ouput Clamp diode reverse voltage(2)	-0.3	42	V
V_{COM}	COM pin voltage(2)	-0.3	42	V
V_{IN}	Pins IN1-IN7 to GND voltage (2)	-0.3	30	V
I_{DS}	Continuous drain current per channel(3) (4)		600	mA
I_{OK}	Output clamp current		500	mA
I_{GND}	Total continuous GND-terminal current		–2	A
T_A	Operating free-air temperature range	–40	125	°C
T_J	Operating virtual junction temperature	-40	150	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the GND/substrate terminal, unless otherwise noted.
(3) Maximum power dissipation is a function of $T_J(max)$, θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

Thermal Information

THERMAL METRIC[1]		TPL7407L		UNIT
		SOIC (D)	TSSOP (PW)	
		16 PINS	16 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	91.9	115.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	50.1	49.5	°C/W
θ_{JB}	Junction-to-board thermal resistance	49.4	60.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.6	8.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	49.1	60.2	°C/W
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

Recommended Operating Conditions

Over operating temperature range

		MIN	NOM	MAX	UNIT
V_{OUT}	OUT1- OUT7 pin voltage for recommended operation	0		40	V
V_{COM}	COM pin voltage range for full output drive	8.5		40	V
V_{IL}	IN1- IN7 input low voltage ("Off" high impedance output)			0.9	V
V_{IH}	IN1- IN7 input high voltage ("Full Drive" low impedance output)	1.5			V
T_J	Operating virtual junction temperature	-40		125	°C
I_{DS}	Continuous drain current	0		500	mA

Electrical Characteristics

T_J= –40°C to 125°C; Typical Values at T_A=T_J= 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OL} (V_{DS})	OUT1- OUT7 low-level output voltage	V_{IN} ≥ 1.5V	I_D = 100 mA		200	320	mV
			I_D = 200 mA		420	650	
$I_{OUT(OFF)}$ (I_{DS_OFF})	OUT1- OUT7 OFF-state leakage current	V_{OUT} = 24V,	V_{IN} ≤ 1.0V		10	500	nA
V_F	Clamp forward voltage	I_F = 200 mA				1.4	V
$I_{IN(off)}$	IN1- IN7 Off-state input current	V_{INX}= 0V	V_{OUT}=40V			500	nA
$I_{IN(ON)}$	IN1- IN7 ON state input current	V_{INX}=1.5V-5.0V				10	µA
I_{COM}	Static current flowing through COM pin	V_{COM}=8.5V-40V			15	25	µA

Switching Characteristics

Typical Values at T_A=T_J= 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_{INX} ≥1.65V, Vpullup=24V, Rpull-up = 48Ω		350		ns
t_{PHL}	Propagation delay time, high- to low-level output	V_{INX} ≥1.65V, Vpullup=24V, Rpull-up = 48Ω		350		ns
C_i	Input capacitance	V_I = 0, f = 100KHz		5		pF

Typical Characteristics

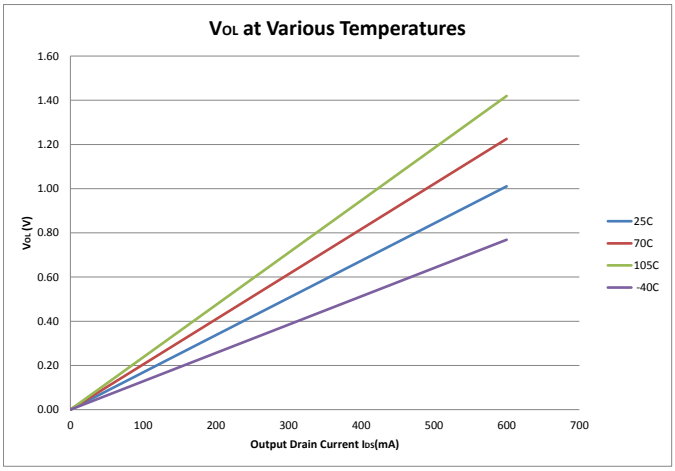


Figure 1. V_{OL} (V_{DS})

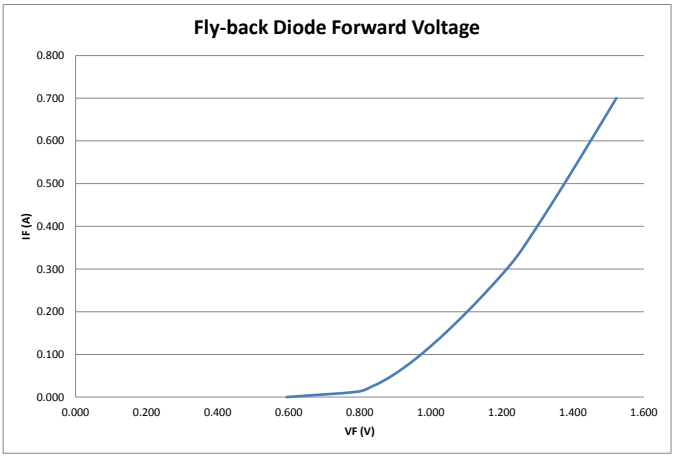


Figure 2. Flyback Diode Forward Voltage

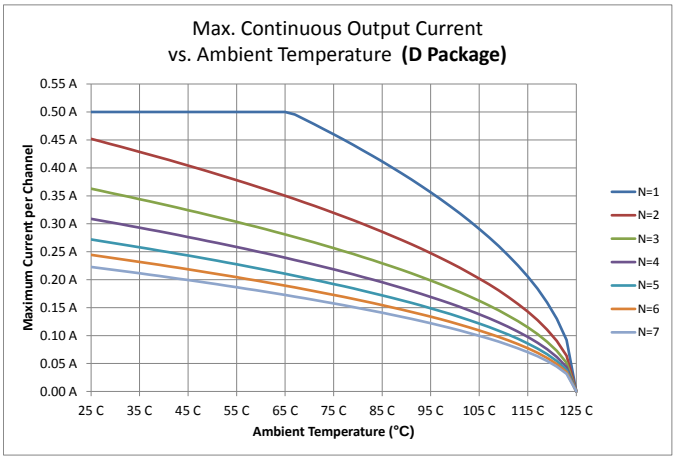


Figure 3. Maximum Output Current vs. Temperature (SOIC)

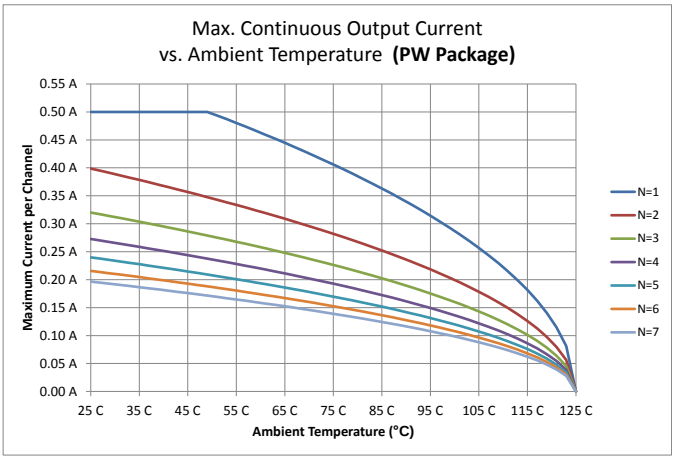


Figure 4. Maximum Output Current vs. Temperature (TSSOP)

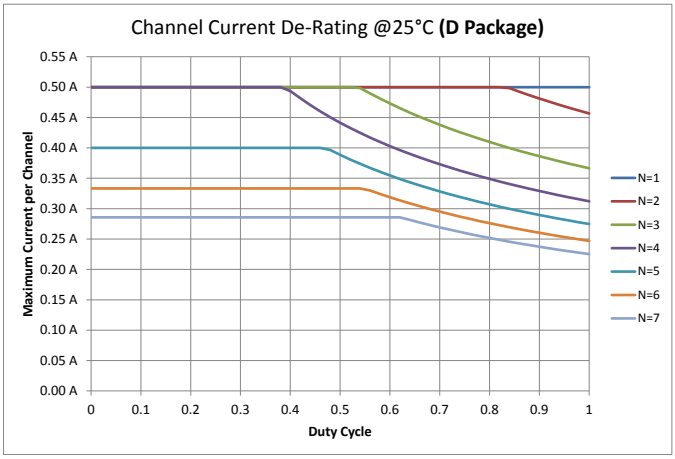


Figure 5. D Package Maximum Collector Current Vs. Duty Cycle at 25°C

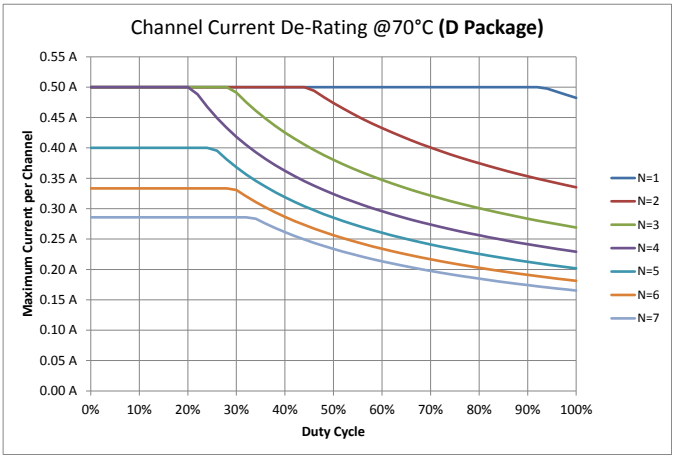


Figure 6. D Package Maximum Collector Current Vs. Duty Cycle at 70°C

Typical Characteristics (continued)

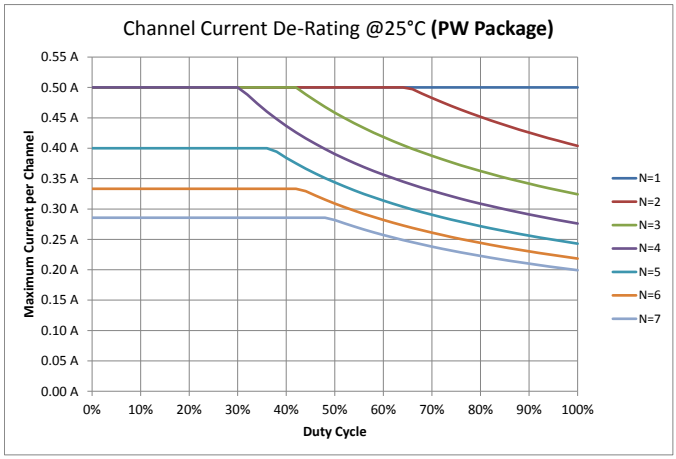


Figure 7. PW Package Maximum Collector Current Vs. Duty Cycle at 25°C

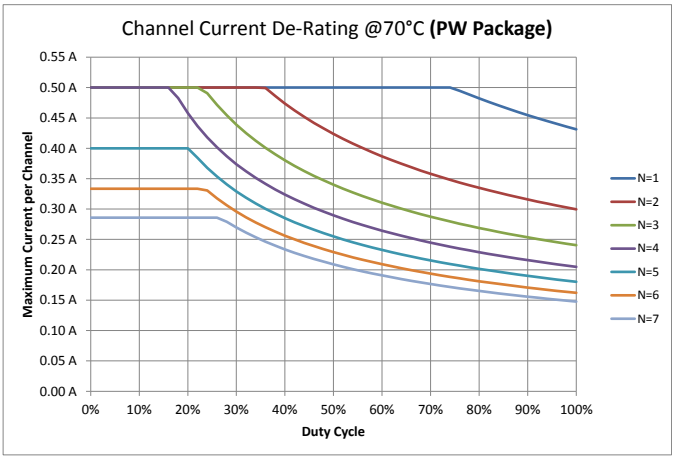


Figure 8. PW Package Maximum Collector Current Vs. Duty Cycle at 70°C

APPLICATION AND IMPLEMENTATION

TTL and other Logic Inputs

TPL7407L input interface is specified for standard 1.8V and 5V CMOS logic interface and can tolerate up to 30V. At any input voltage the output drivers will be driven at it's maximum when Vcom is greater than or equal to 8.5V.

Input RC Snubber

TPL7407L features an input RC snubber that helps prevent spurious switching in noisy environment. Connect an external 1kΩ to 5kΩ resistor in series with the input to further enhance TPL7407L's noise tolerance.

High-impedance Input Drivers

TPL7407L features a 1MΩ input pull-down resistor. The presence of this resistor allows the input drivers to be tri-stated. When a high-impedance driver is connected to a channel input the TPL7407L detects the channel input as a low level input and remains in the OFF position. The input RC snubber helps improve noise tolerance when input drivers are in the high-impedance state.

On-chip Power Dissipation

Use the below equation to calculate TPL7407L on-chip power dissipation P_D:

$$P_D = \sum_{i=1}^{N} V_{OLi} \times I_{Li} \quad (1)$$

Where:

N is the number of channels active together.

V_{OLi} is the OUT_i pin voltage for the load current I_{Li}.

Thermal Reliability

It is recommended to limit TPL7407L IC's die junction temperature to less than 125°C. The IC junction temperature is directly proportional to the on-chip power dissipation. Use the following equation to calculate the maximum allowable on-chip power dissipation for a target IC junction temperature:

$$PD_{(MAX)} = \left(T_{J(MAX)} - T_A\right) \Big/ \theta_{JA} \quad (2)$$

Where:

$T_{J(MAX)}$ is the target maximum junction temperature.

T_A is the operating ambient temperature.

θ_{JA} is the package junction to ambient thermal resistance.

Improving Package Thermal Performance

θ_{JA} value depends on the PC board layout. An external heat sink and/or a cooling mechanism, like a cold air fan, can help reduce θ_{JA} and thus improve device thermal capabilities. Refer to TI's design support web page at www.ti.com/thermal for a general guidance on improving device thermal performance.

Application Examples

Unipolar Stepper Motor Driver

Figure 9 shows an implementation of TPL7407L for driving a uniploar stepper motor. The unconnected input channels can be used for other functions. When an input pin is left open the internal 1MΩ pull down resistor pulls the respective input pin to GND potential. For higher noise immunity use an external short across an unconnected input and GND pins. The COM pin must be tied to the supply of whichever inductive load is being driven for the driver to be protected by the free-wheeling diode.

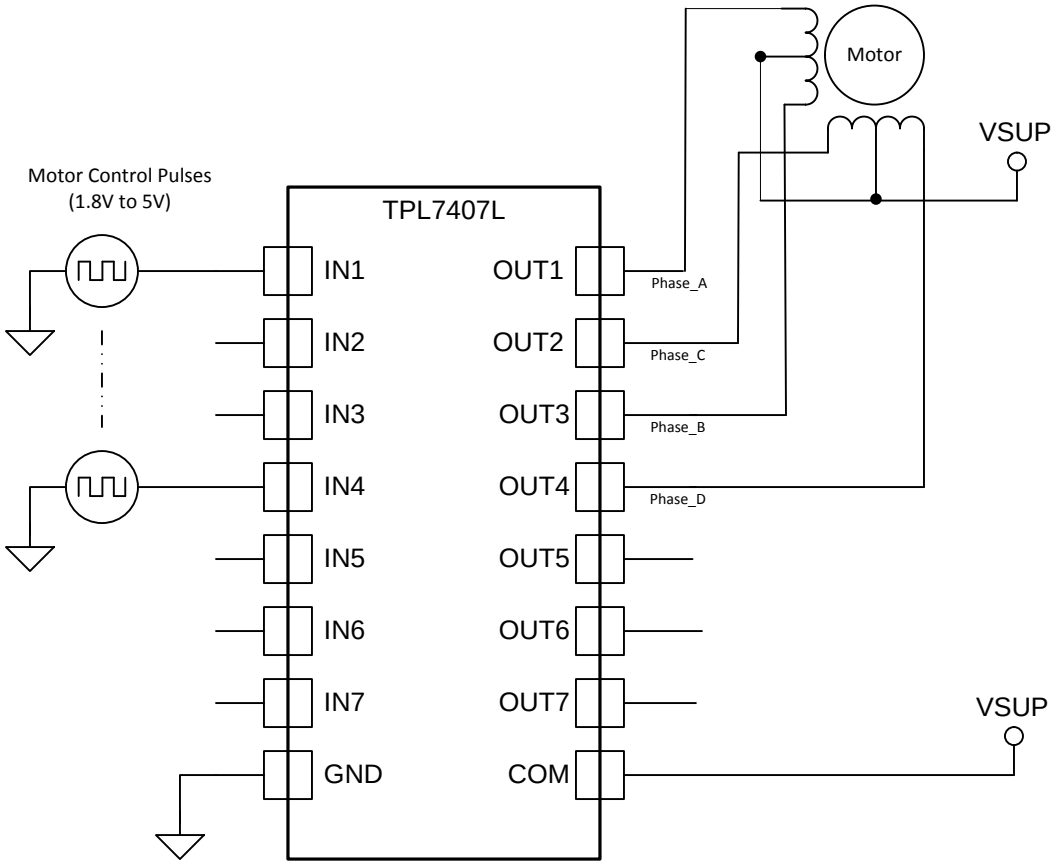


Figure 9. TPL7407L as a Stepper Motor Driver

Multi-Purpose Sink Driver

When configured as per Figure 10 TPL7407L can be used as a multi-purpose driver. The output channels can be tied together to sink more current. TPL7407L can easily drive motors, relays & LEDs with little power dissipation. COM must be tied to highest load voltage, which may or may not be same as inductive load supply.

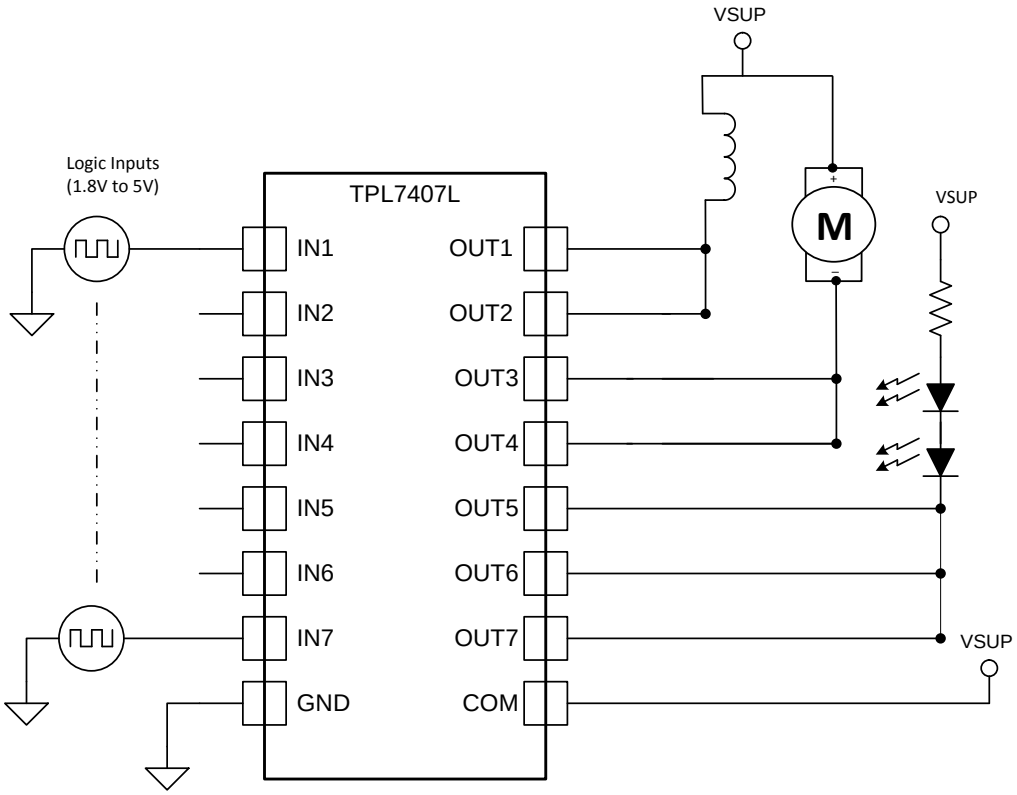


Figure 10. TPL7407L Multi-Purpose Sink Driver Application

24V Relay Driver

To drive lower resistance relays, like <48Ω , connect two or more adjacent channels in parallel as shown in Figure 11. Connecting several channels in parallel lowers the channel output resistance and increases the drive current. TPL7407L can be used for driving 12V, 24V & 36V relays with similar a implementation.

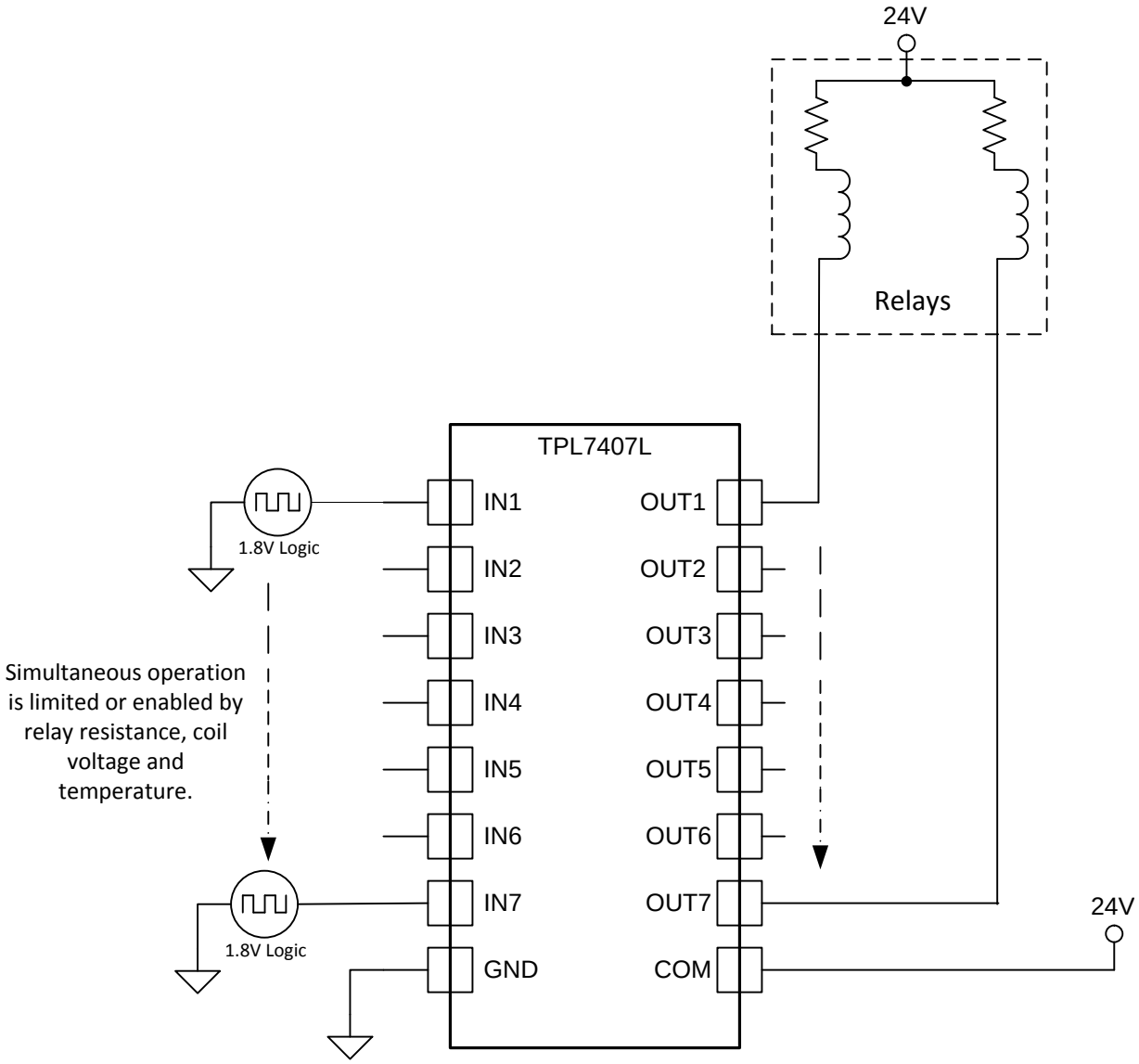


Figure 11. TPL7407L Driving 24V Relays

REVISION HISTORY

Changes from Original (January 2014) to Revision A	Page
• 初次发布完整版本。	1

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPL7407LDR	ACTIVE	SOIC	D	16	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	TPL7407L	Samples
TPL7407LPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	TPL7407L	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

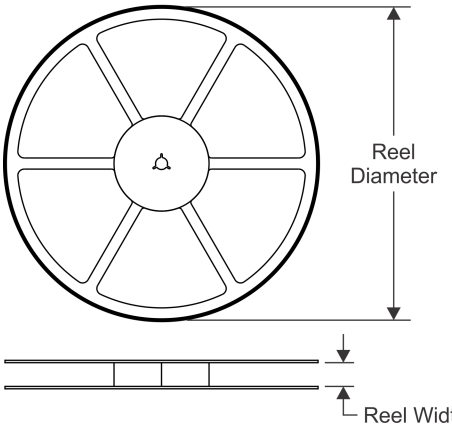
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

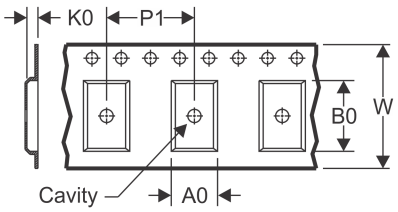
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

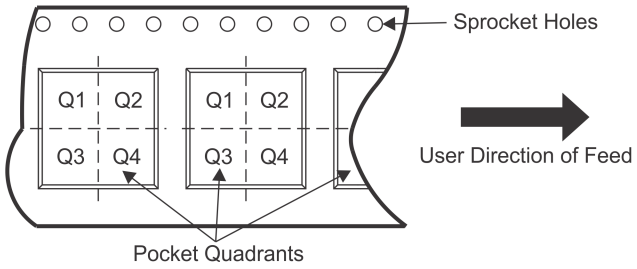


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

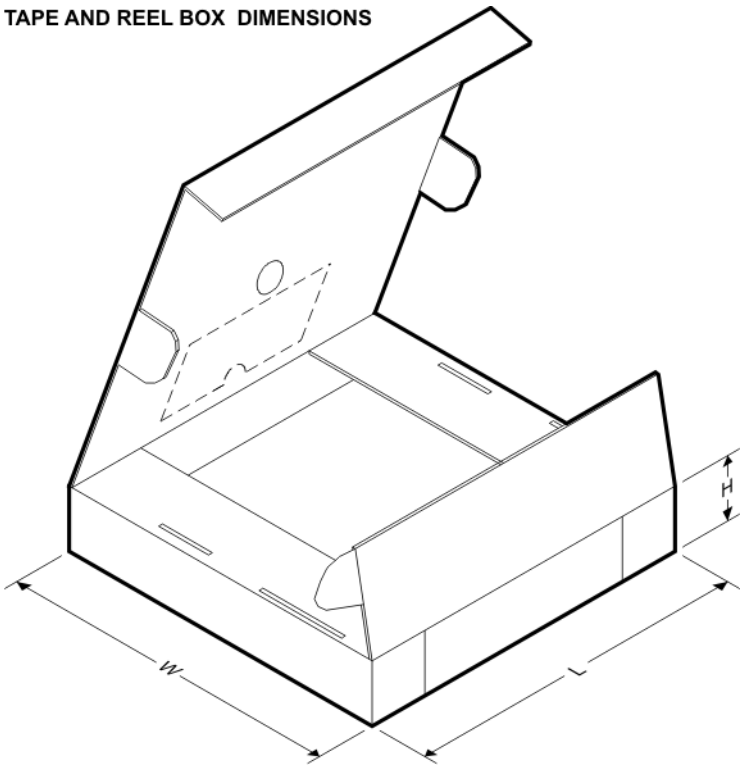
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPL7407LDR	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
TPL7407LPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

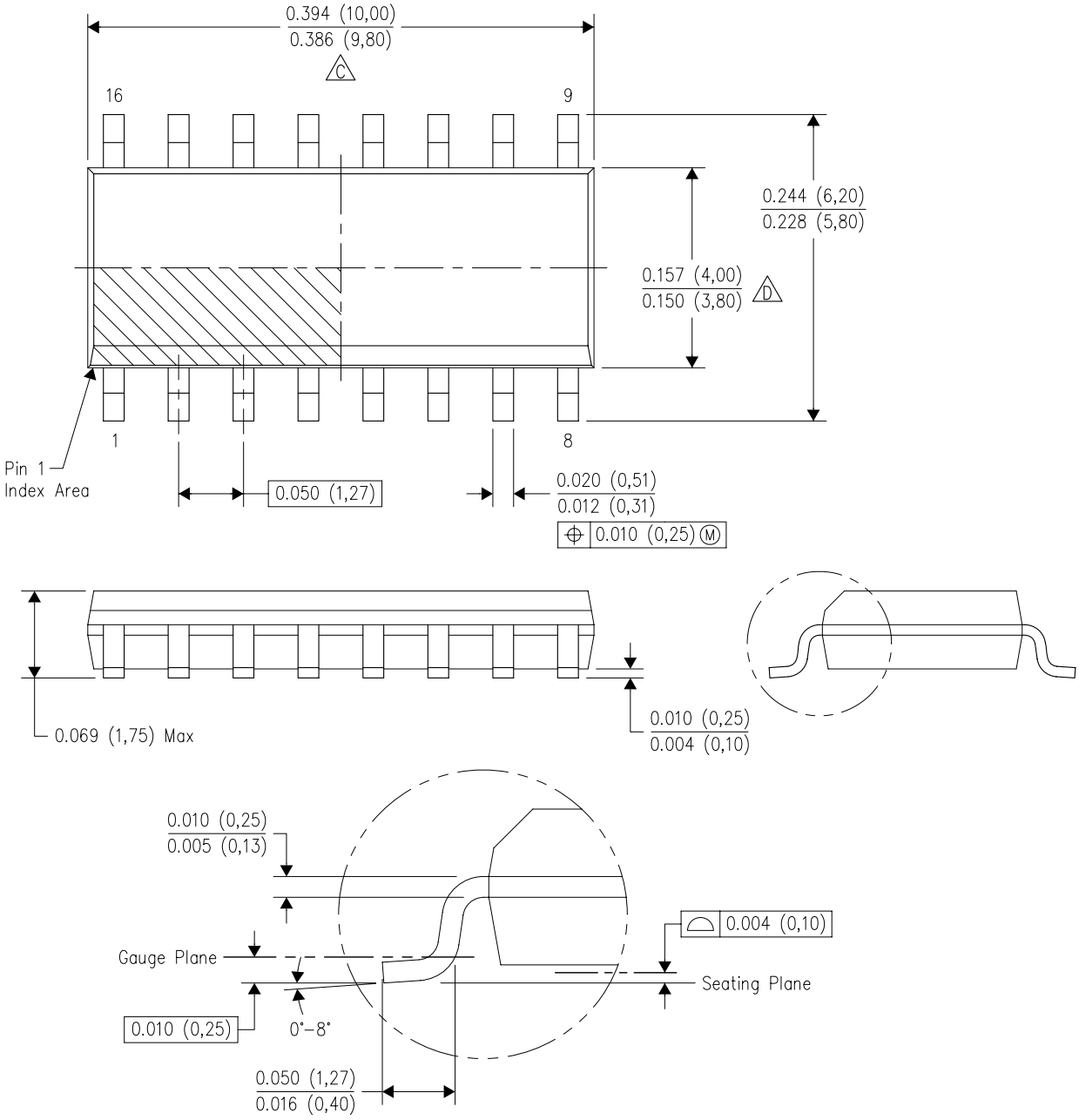
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

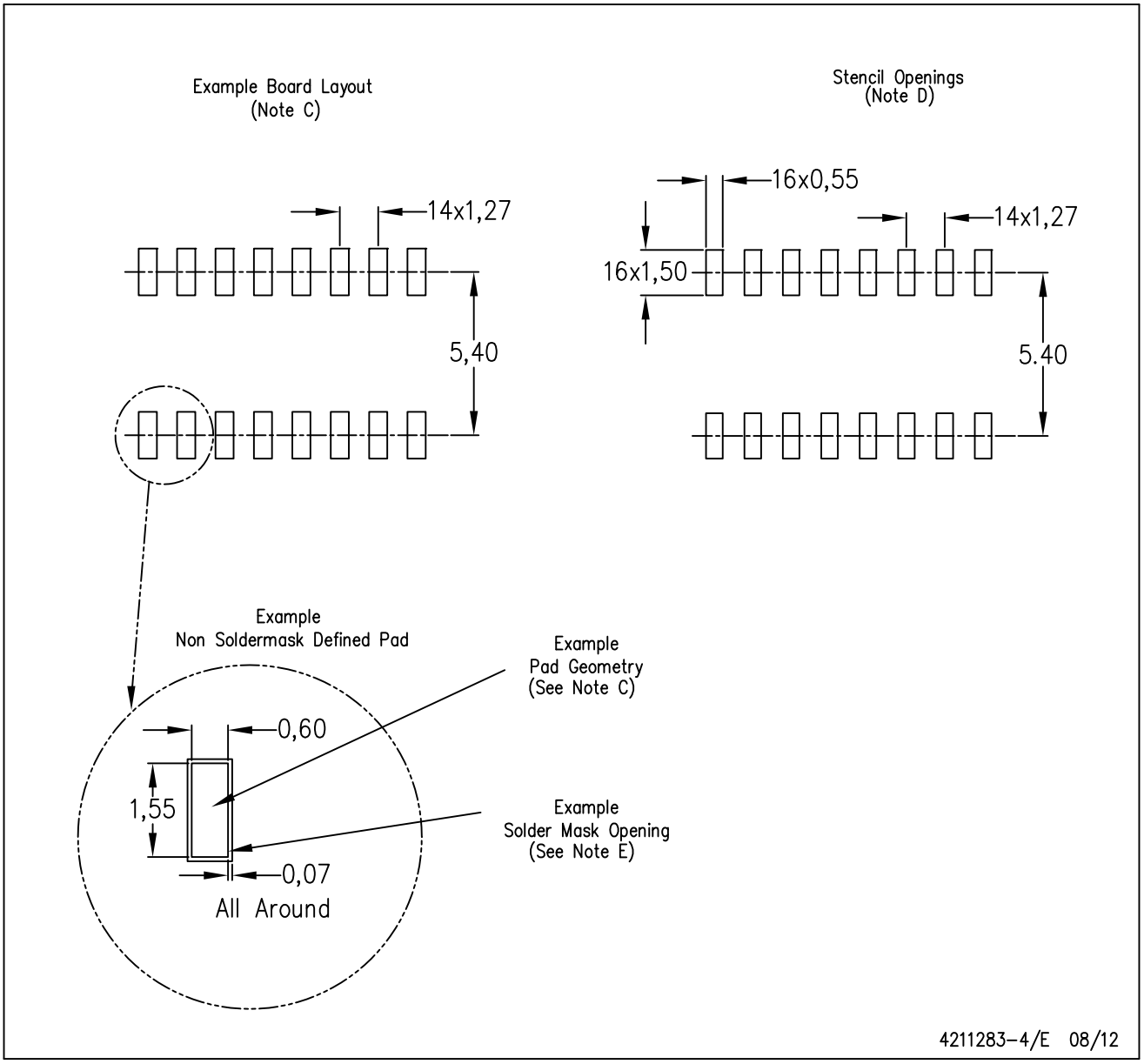
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPL7407LDR	SOIC	D	16	2500	364.0	364.0	27.0
TPL7407LPWR	TSSOP	PW	16	2000	364.0	364.0	27.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



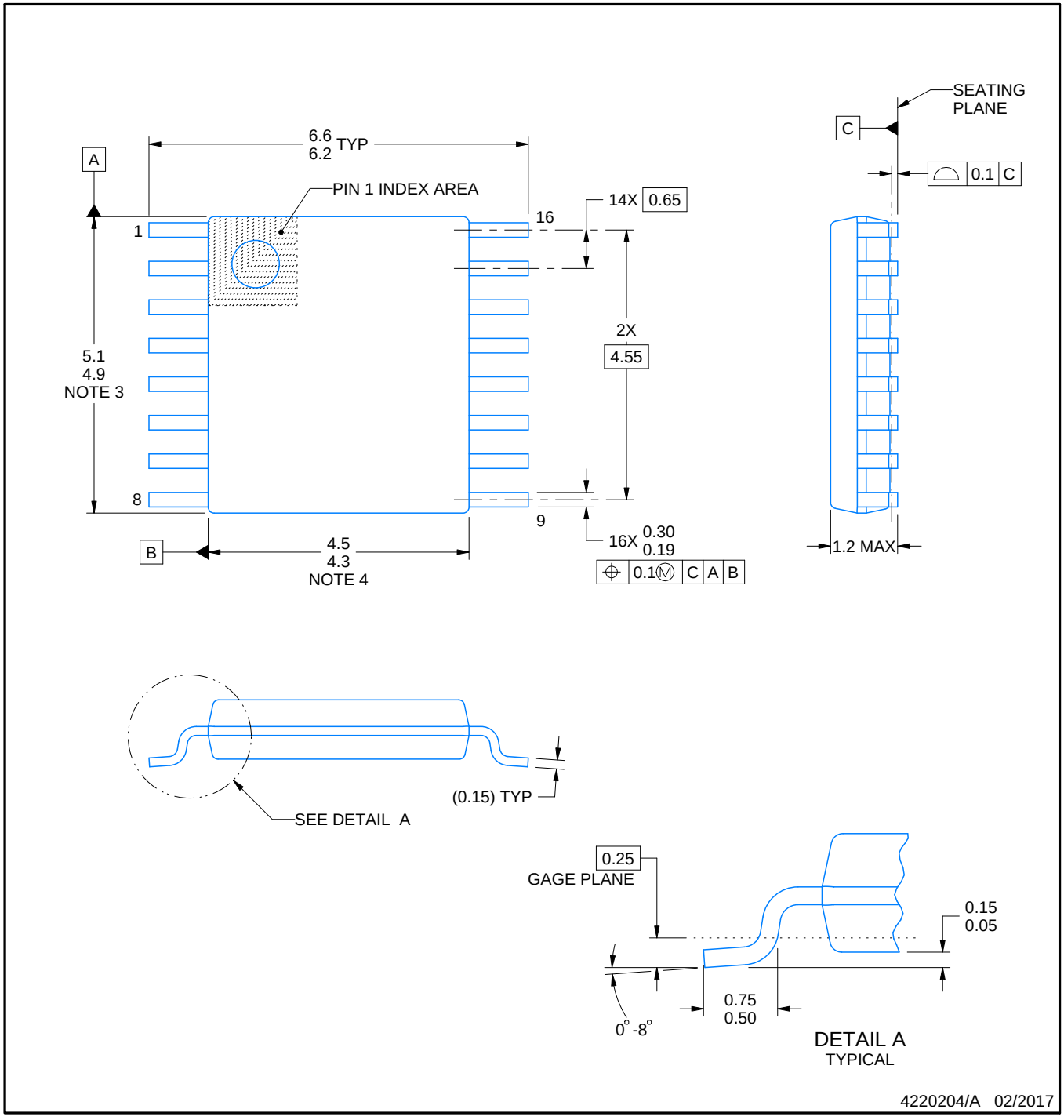
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0016A

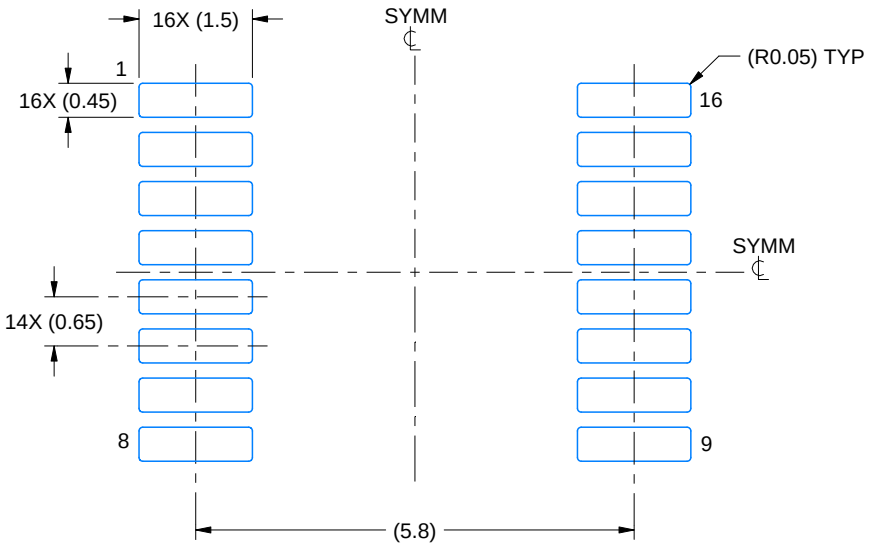
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

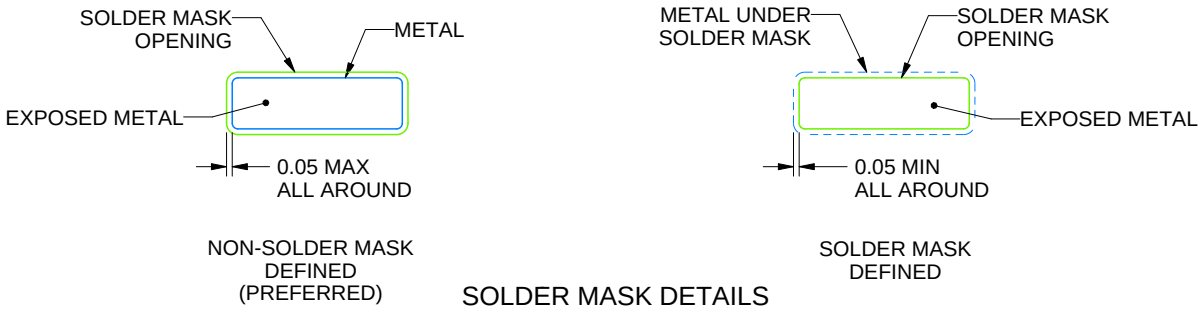


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

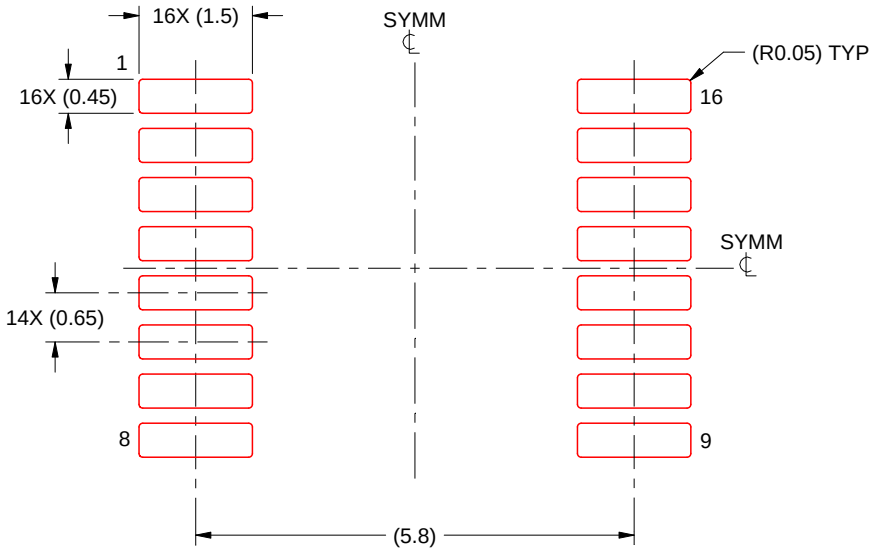


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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