TPS22925 3.6V、3A、导通电阻为 9mΩ 的负载开关

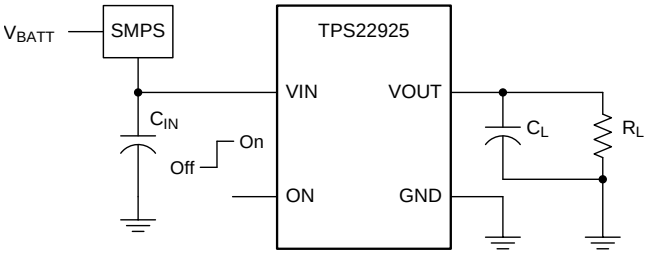
1 特性

- 输入电压范围：0.65V 至 3.6V
- 导通电阻
  - V_{IN} = 3.6V 时，R_{ON} = 9.2mΩ
  - V_{IN} = 1.8V 时，R_{ON} = 9.2mΩ
  - V_{IN} = 1V 时，R_{ON} = 10.2mΩ
  - V_{IN} = 0.65V 时，R_{ON} = 13.1mΩ
- 3A 最大连续开关电流
- 静态电流 $I_{Q,VIN}$ = 29μA（V_{IN} = 3.6V 时）
- 低控制输入阈值，支持使用 1.2V、1.8V、2.5V 或 3.3V 逻辑器件
- 受控转换率
  - t_R = 97μs（V_{IN} = 3.6V 时）(TPS22925Bx)
  - t_R = 810μs（V_{IN} = 3.6V 时）(TPS22925Cx)
- 阻断反向电流（禁用时）
- 快速输出放电 (QOD)（仅限 TPS22925B 和 TPS22925C）
- 晶圆级芯片规模封装：
  - 0.9mm x 1.4mm、间距为 0.5mm、高度为 0.5mm
- 静电放电 (ESD) 性能经测试符合 JESD 22 规范
  - 1kV 人体放电模式 (HBM) 和 500V 组件充电模式(CDM)

2 应用

- 计算
- 固态硬盘 (SSD)
- 平板电脑
- 可穿戴产品
- 电子销售点 (EPOS)

简化应用



3 说明

TPS22925 产品系列包括 4 款器件：TPS22925B、TPS22925BN、TPS22925C 和 TPS22925CN。每款器件都是一个转换率受控的 9mΩ 单通道负载开关。

该系列器件包含一个可在 0.65V 至 3.6V 输入电压范围内运行的 N 沟道 MOSFET，最高可支持 3A 持续电流。这种持续电流性能使得该系列器件适用于多种设计与终端设备。TPS22925 系列的每一款器件在禁用时都提供反向电流阻断功能，从而保护电源并且实现电源多路复用功能。

器件的可控上升时间可大幅降低大容量负载电容所产生的浪涌电流，从而降低或消除电源压降。当工作输入电压为 3.6V 时，TPS22925Bx 器件的上升时间为 97μs，而 TPS22925Cx 器件的上升时间为 810μs。

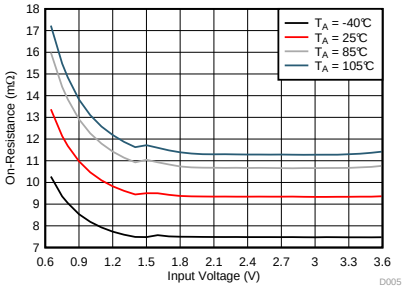
TPS22925 系列器件提供一个可选的 150Ω 集成下拉电阻，方便在开关断开时实现快速输出放电 (QOD)，这有助于缩减总体解决方案尺寸。TPS22925 系列的每一款器件都采用 0.9mm × 1.4mm、间距 0.5mm、高度为 0.4mm 的 6 引脚晶圆级芯片规模封装 (WCSP)，有助于实现尺寸更小、集成度更高的设计。WCSP 封装与 9mΩ 导通电阻使得该系列器件适用于空间受限型电池供电类 应用。器件在自然通风环境下的额定工作温度范围为 –40°C 至 105°C。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS22925B	DSBGA (6)	0.90mm x 1.40mm
TPS22925BN		
TPS22925C		
TPS22925CN		

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

导通电阻与输入电压间的关系



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4 修订历史记录

Changes from Revision B (January 2016) to Revision C **Page**

- 已更改*Device Comparison Table* ... 1

Changes from Revision A (December 2015) to Revision B **Page**

- Deleted the STATUS column from the *Device Comparison Table* ... 3

Changes from Original (November 2015) to Revision A **Page**

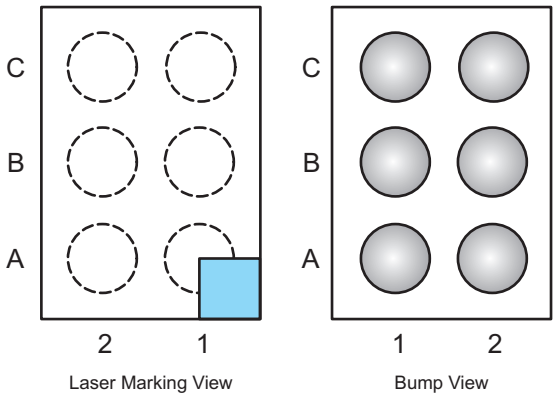
- 已将文档状态由“*产品预览*”更新为“*量产数据*” ... 1

5 Device Comparison Table

DEVICE	QOD	R_{ON} (mΩ) at V_{IN} = 3.6 V	t_R (µs) at V_{IN} = 3.6 V	MAXIMUM OUTPUT CURRENT I_{MAX} (A)	ENABLE (ON PIN)
TPS22925B	Yes	9.2	97	3	Active High
TPS22925BN	No				
TPS22925C	Yes		810		
TPS22925CN	No				

6 Pin Configuration and Functions

YPH Package
6–Pin DSBGA
Top View



Pin Assignments

C	GND	ON
B	VOUT	VIN
A	VOUT	VIN
	1	**2**

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	C1	GND	Ground
ON	C2	I	Switch control input. Active high. Do not leave floating.
VIN	A2	I	Switch input; bypass this input with a ceramic capacitor to ground. See *Application Information* section for more detail.
	B2		
VOUT	A1	O	Switch output
	B1		

7 Specifications

7.1 Absolute Maximum Ratings

over operating free–air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN, ON	–0.3	4	V
Output voltage	VOUT	–0.3	4	V
Maximum continuous switch current at T_A = 60°C	I_{MAX}		3	A
Maximum pulsed switch current, 100–µs pulse, 2% duty cycle	I_{PLS}		4	A
Junction temperature, T_J			125	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human–body model (HBM), per ANSI/ESDA/JEDEC JS–001(1)	±1000	V
		Charged–device model (CDM), per JEDEC specification JESD22–C101(2)	±500	

(1) JEDEC document JEP155 states that 500–V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500–V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250–V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250–V CDM is possible with the necessary precautions.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage	0.65	3.6	V
V_{OUT}	Output voltage	0	3.6	V
V_{IH}	High–level input voltage, ON	0.9	3.6	V
V_{IL}	Low–level input voltage, ON	0	0.45	V
C_{IN}	Input capacitance	1		µF
T_A	Operating free–air temperature	–40	105	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS22925xx YPH (DSBGA) 6 PINS	UNIT
$R_{\theta JA}$	Junction–to–ambient thermal resistance	110.9	°C/W
$R_{\theta JC(top)}$	Junction–to–case (top) thermal resistance	1.2	°C/W
$R_{\theta JB}$	Junction–to–board thermal resistance	30.4	°C/W
ψ_{JT}	Junction–to–top characterization parameter	0.8	°C/W
ψ_{JB}	Junction–to–board characterization parameter	30.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

over operating free–air temperature range (unless otherwise noted). Typical values are for T_A = 25°C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
$I_{Q,VIN}$	Quiescent current	V_{ON} = 3.6 V, I_{OUT} = 0 A	V_{IN} = 3.6 V	–40°C to 85°C		29	71	µA
				–40°C to 105°C			84	
			V_{IN} = 2.5 V	–40°C to 85°C		28	67	
				–40°C to 105°C			79	
			V_{IN} = 1.8 V	–40°C to 85°C		26	65	
				–40°C to 105°C			76	
			V_{IN} = 1.2 V	–40°C to 85°C		20	55	
				–40°C to 105°C			66	
			V_{IN} = 1.0 V	–40°C to 85°C		16	50	
				–40°C to 105°C			60	
			V_{IN} = 0.65 V	–40°C to 85°C		10	39	
				–40°C to 105°C			49	
$I_{SD,VIN}$	VIN shutdown current	V_{ON} = 0 V, V_{OUT} = 0 V	V_{IN} = 3.6 V	–40°C to 85°C		0.5	5	µA
				–40°C to 105°C			9	
			V_{IN} = 2.5 V	–40°C to 85°C		0.5	4	
				–40°C to 105°C			6	
			V_{IN} = 1.8 V	–40°C to 85°C		0.5	4	
				–40°C to 105°C			6	
			V_{IN} = 1.2 V	–40°C to 85°C		0.5	3	
				–40°C to 105°C			5	
			V_{IN} = 1.0 V	–40°C to 85°C		0.5	3	
				–40°C to 105°C			5	
			V_{IN} = 0.65 V	–40°C to 85°C		0.5	3	
				–40°C to 105°C			5	
I_{ON}	ON pin input leakage current	0.9 V ≤ V_{ON} ≤ 3.6 V		–40°C to 105°C			0.1	µA
$I_{RC,VIN}$	Reverse current when disabled	V_{IN} = V_{ON} = 0 V, V_{OUT} = 3.6 V		–40°C to 85°C		–0.2	–2.5	µA
				–40°C to 105°C			–6	
R_{ON}	On-resistance	I_{OUT} = –200 mA	V_{IN} = 3.6 V	25°C		9.2	13	mΩ
				–40°C to 85°C			15	
				–40°C to 105°C			16	
			V_{IN} = 2.5 V	25°C		9.2	13	
				–40°C to 85°C			15	
				–40°C to 105°C			16	
			V_{IN} = 1.8 V	25°C		9.2	13	
				–40°C to 85°C			15	
				–40°C to 105°C			16	
			V_{IN} = 1.2 V	25°C		9.5	14	
				–40°C to 85°C			16	
				–40°C to 105°C			17	
			V_{IN} = 1.0 V	25°C		10.2	15	
				–40°C to 85°C			17	
				–40°C to 105°C			18	
			V_{IN} = 0.65 V	25°C		13.1	20	
				–40°C to 85°C			23	
				–40°C to 105°C			25	

Electrical Characteristics (continued)

over operating free–air temperature range (unless otherwise noted). Typical values are for T_A = 25°C.

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
V_{HYS}	ON pin hysteresis	V_{IN} = 3.6 V	25°C		86		mV
		V_{IN} = 2.5 V			83		
		V_{IN} = 1.8 V			82		
		V_{IN} = 1.2 V			80		
		V_{IN} = 1.0 V			79		
		V_{IN} = 0.65 V			79		
R_{PD} (1)	Output pull-down resistance	V_{IN} = V_{OUT} = 3.6 V, V_{ON} = 0 V	–40°C to 85°C		150	205	Ω
			–40°C to 105°C			215	

(1) Applies to TPS22925B and TPS22925C only.

7.6 Switching Characteristics(1)

over operating free-air temperature range (unless otherwise noted) V_{ON} = 3.6 V, R_L = 10 Ω, C_{IN} = 1 µF, C_L = 0.1 µF, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP (TPS22925Bx)	TYP (TPS22925Cx)	UNIT
t_{ON}	Turn-on time	V_{IN} = 3.6 V	110	900	µs
		V_{IN} = 1.8 V	94	730	
		V_{IN} = 0.65 V	86	620	
t_{OFF}	Turn-off time	V_{IN} = 3.6 V	3	3	µs
		V_{IN} = 1.8 V	2.7	2.7	
		V_{IN} = 0.65 V	10.9	10.9	
t_R	Output voltage rise time	V_{IN} = 3.6 V	97	810	µs
		V_{IN} = 1.8 V	61	520	
		V_{IN} = 0.65 V	36	300	
t_F	Output voltage fall time	V_{IN} = 3.6 V	2.2	2.2	µs
		V_{IN} = 1.8 V	2.1	2.1	
		V_{IN} = 0.65 V	3.6	3.6	
t_D	Delay time	V_{IN} = 3.6 V	64	500	µs
		V_{IN} = 1.8 V	66	490	
		V_{IN} = 0.65 V	68	470	

(1) Turn-off time and fall time are dependent on the time constant at the load. For TPS22925BN and TPS22925CN, there is no QOD. The time constant is $R_L \times C_L$. For TPS22925B and TPS22925C, internal pull-down resistor R_{PD} is enabled when the switch is disabled. The time constant is $(R_{PD} \parallel R_L) \times C_L$.

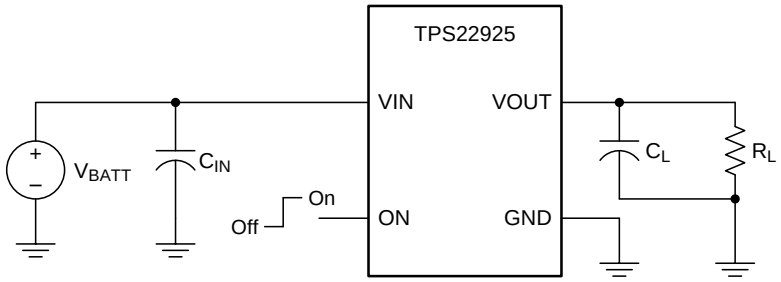
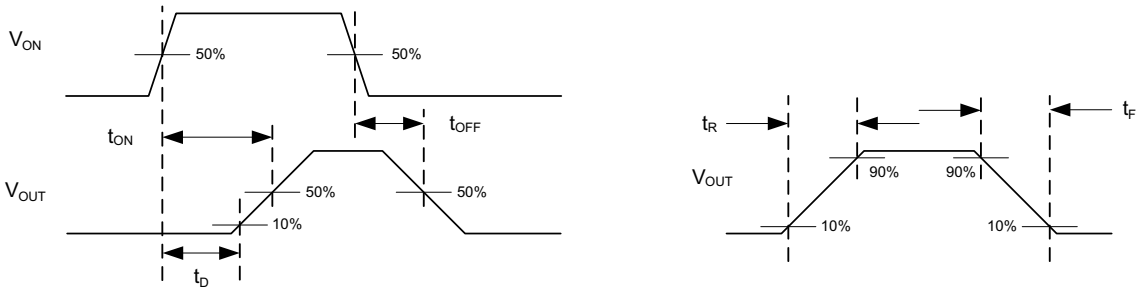


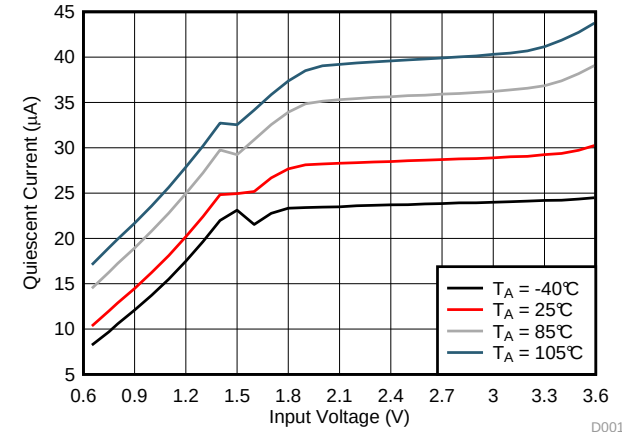
Figure 1. Timing Test Circuit



Rise times and fall times of the control signal is 100 ns.

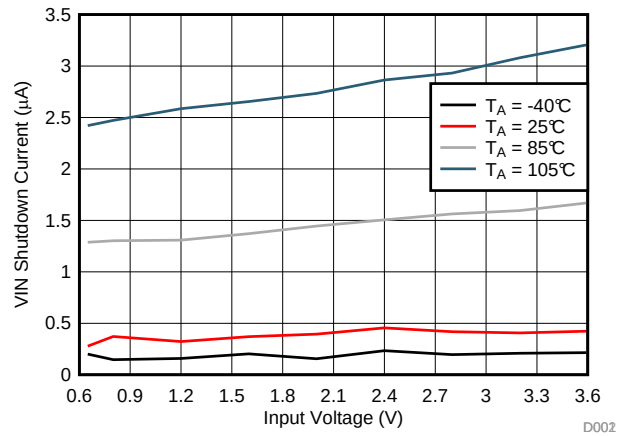
Figure 2. Timing Waveforms

7.7 Typical Characteristics



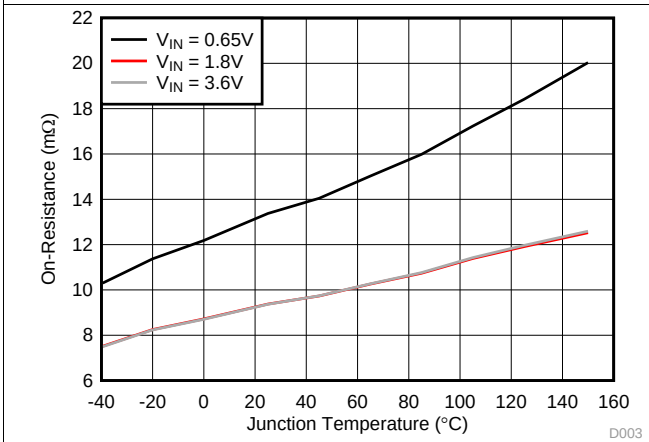
V_{ON} = 3.6 V I_{OUT} = 0 A

Figure 3. Quiescent Current vs Input Voltage



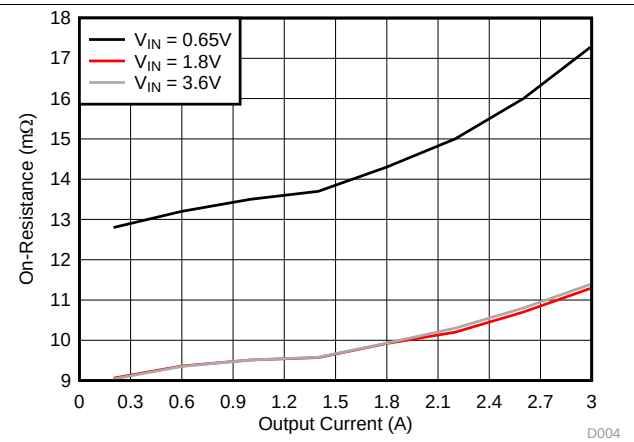
V_{ON} = 0 V V_{OUT} = 0 V

Figure 4. Input Shutdown Current vs Input Voltage



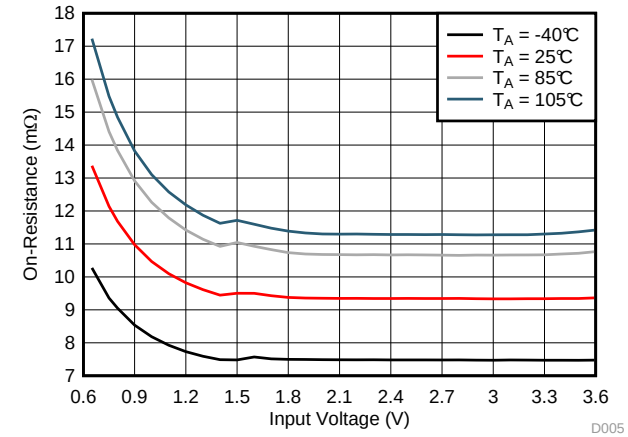
V_{ON} = 3.6 V I_{OUT} = –200 mA

Figure 5. On-Resistance vs Temperature



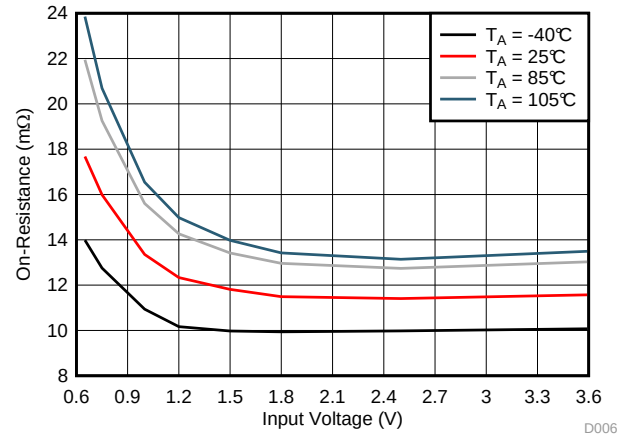
V_{ON} = 3.6 V T_A = 25°C

Figure 6. On-Resistance vs Output Current



V_{ON} = 3.6 V I_{OUT} = –200 mA

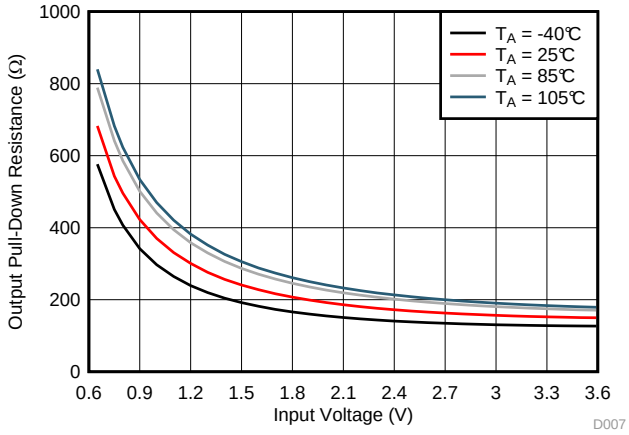
Figure 7. On-Resistance vs Input Voltage



V_{ON} = 3.6 V I_{OUT} = –3 A

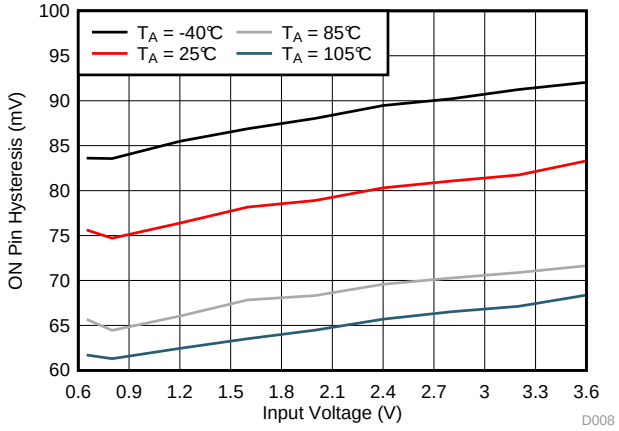
Figure 8. On-Resistance vs Input Voltage

Typical Characteristics (continued)



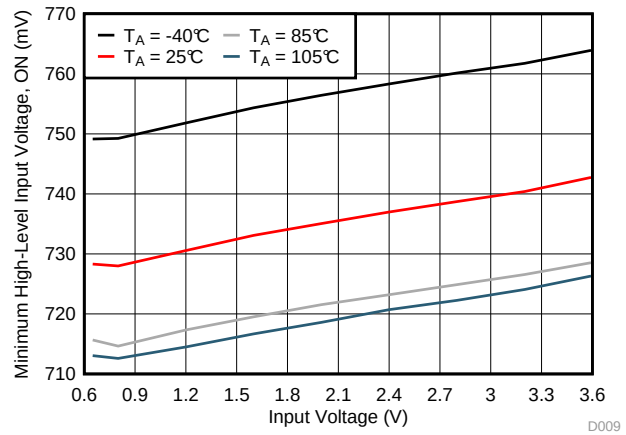
V_{ON} = 0 V V_{OUT} = V_{IN}

Figure 9. Output Pull-Down Resistance vs Input Voltage



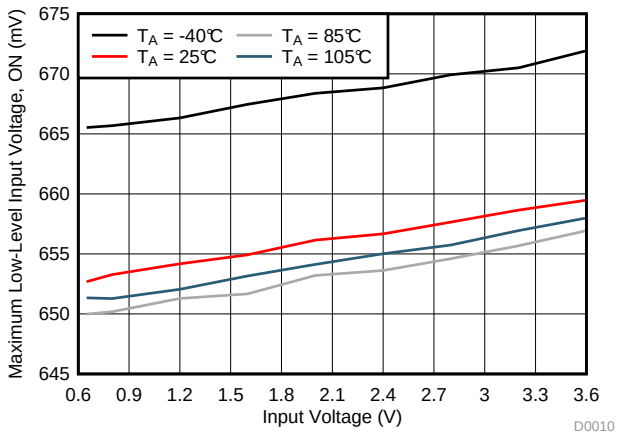
I_{OUT} = 0 A

Figure 10. Hysteresis vs Input Voltage



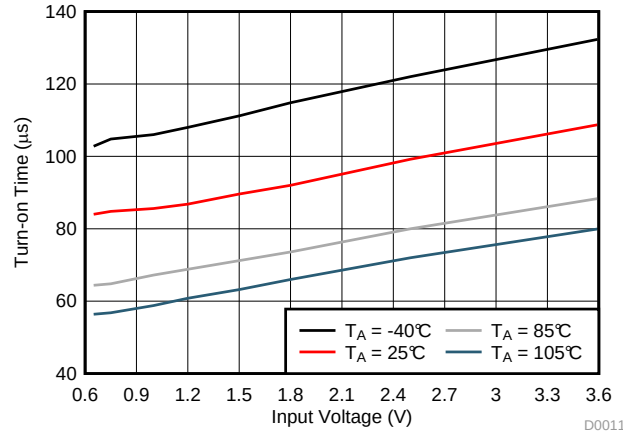
I_{OUT} = 0 A

Figure 11. High-Level Input Voltage vs Input Voltage



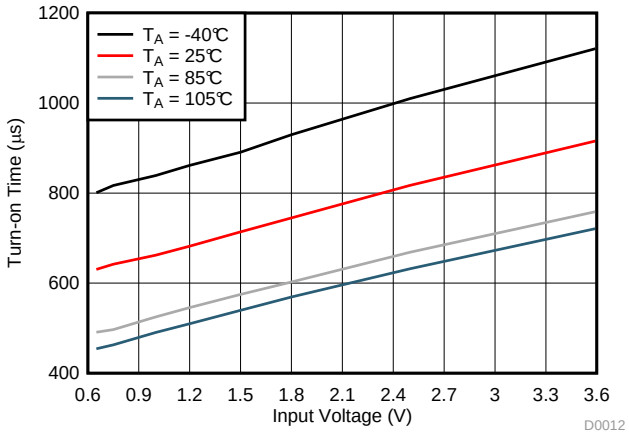
I_{OUT} = 0 A

Figure 12. Low-Level Input Voltage vs Input Voltage



V_{ON} rising from 0 V to 3.6 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

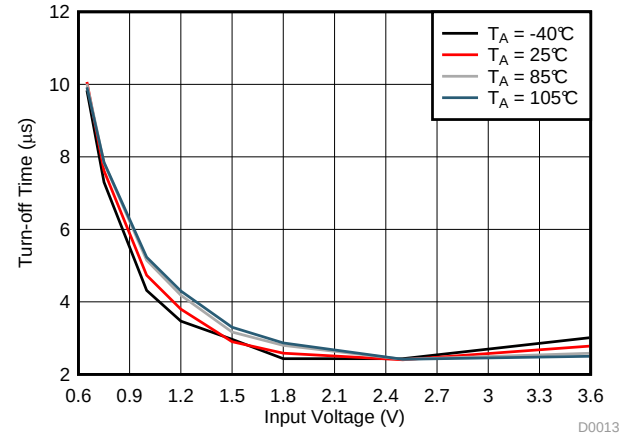
Figure 13. Turn-on Time vs Input Voltage (TPS22925Bx)



V_{ON} rising from 0 V to 3.6 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

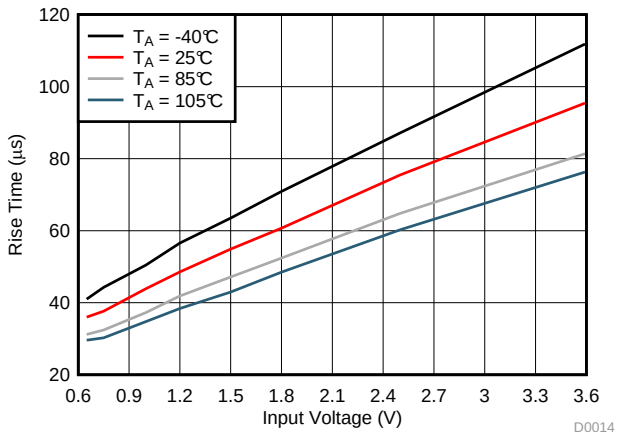
Figure 14. Turn-On Time vs Input Voltage (TPS22925Cx)

Typical Characteristics (continued)



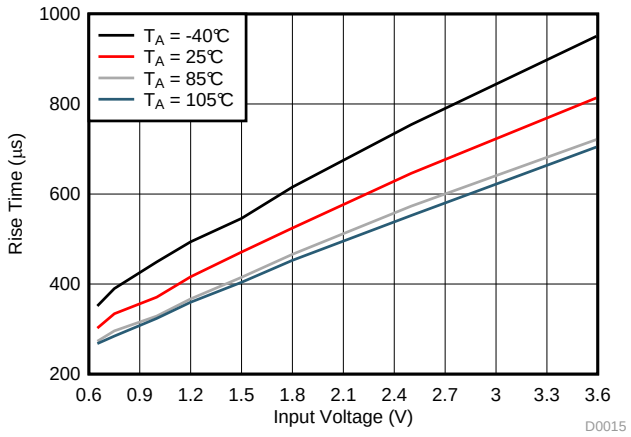
V_{ON} falling from 3.6 V to 0 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 15. Turn-Off Time vs Input Voltage



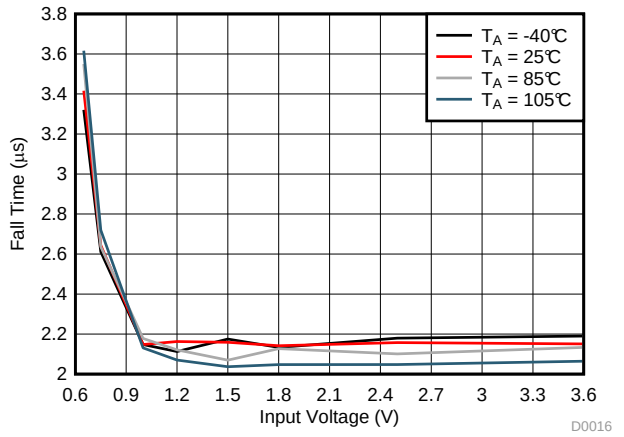
V_{ON} rising from 0 V to 3.6 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 16. Rise Time vs Input Voltage (TPS22925Bx)



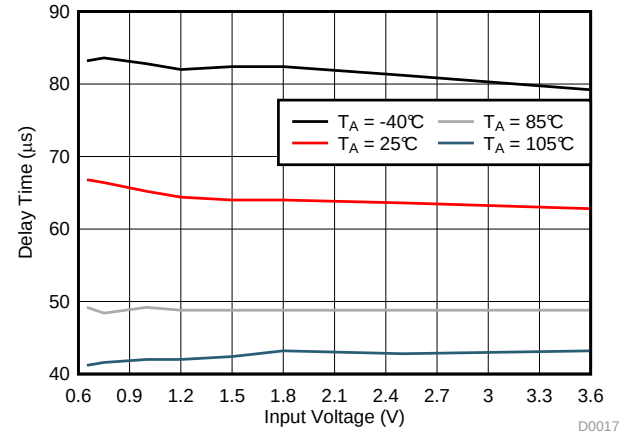
V_{ON} rising from 0 V to 3.6 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 17. Rise Time vs Input Voltage (TPS22925Cx)



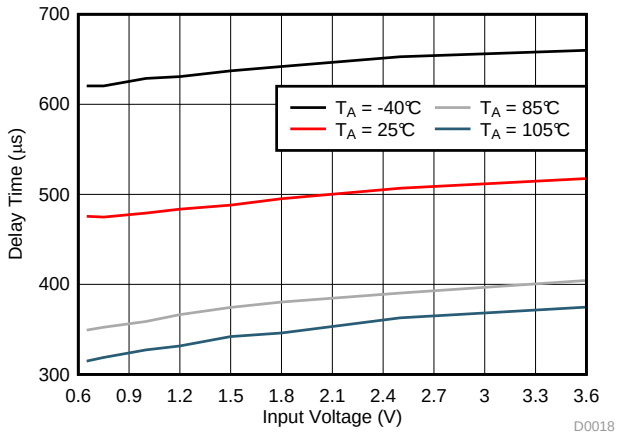
V_{ON} falling from 3.6 V to 0 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 18. Fall Time vs Input Voltage



V_{ON} rising from 0 V to 3.6 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 19. Delay Time vs Input Voltage (TPS22925Bx)

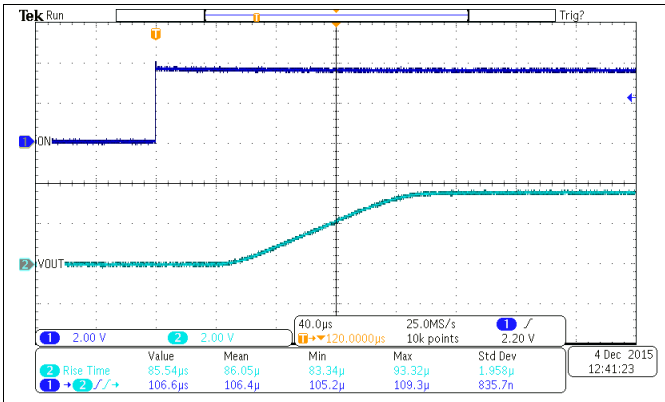


V_{ON} rising from 0 V to 3.6 V C_{IN} = 1 µF
C_L = 0.1 µF R_L = 10 Ω

Figure 20. Delay Time vs Input Voltage (TPS22925Cx)

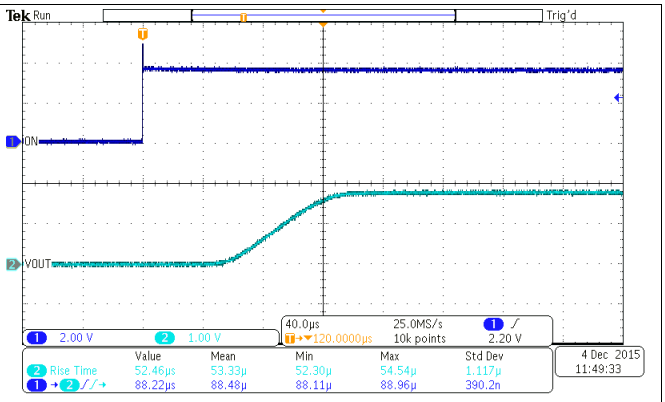
7.8 Typical Characteristics

C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω, T_A = 25°C



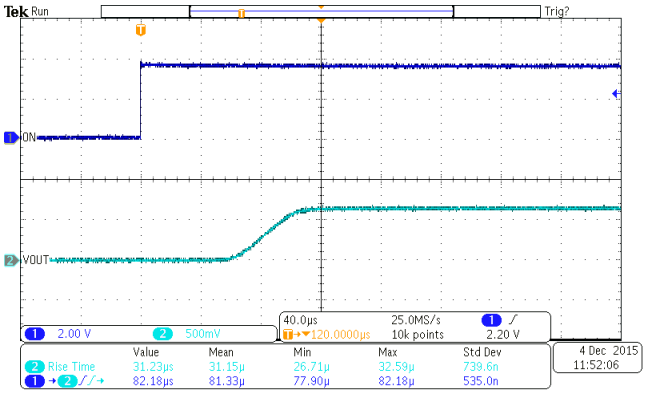
V_{IN} = 3.6 V

Figure 21. Turn-On Response (TPS22925Bx)



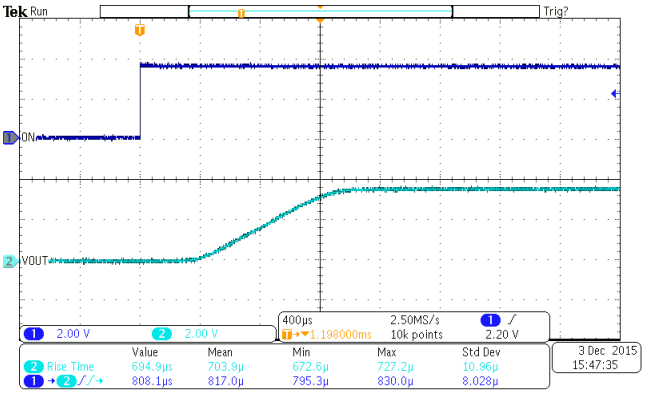
V_{IN} = 1.8 V

Figure 22. Turn-On Response (TPS22925Bx)



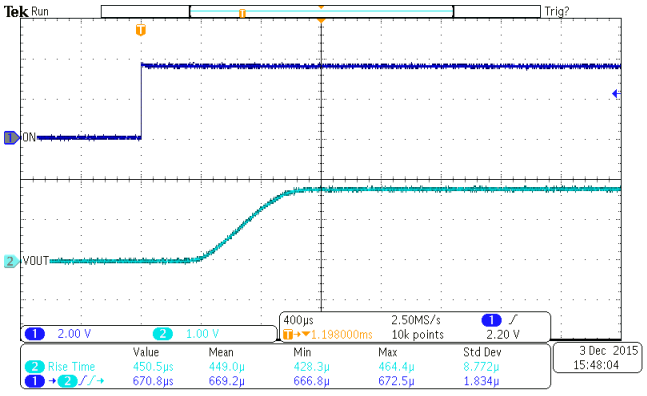
V_{IN} = 0.65 V

Figure 23. Turn-On Response (TPS22925Bx)



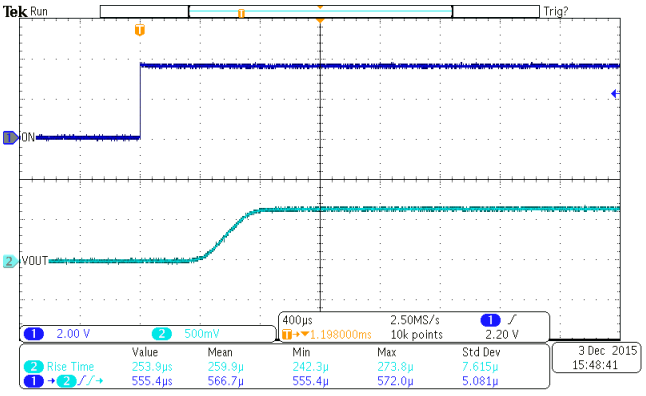
V_{IN} = 3.6 V

Figure 24. Turn-On Response (TPS22925Cx)



V_{IN} = 1.8 V

Figure 25. Turn-On Response (TPS22925Cx)

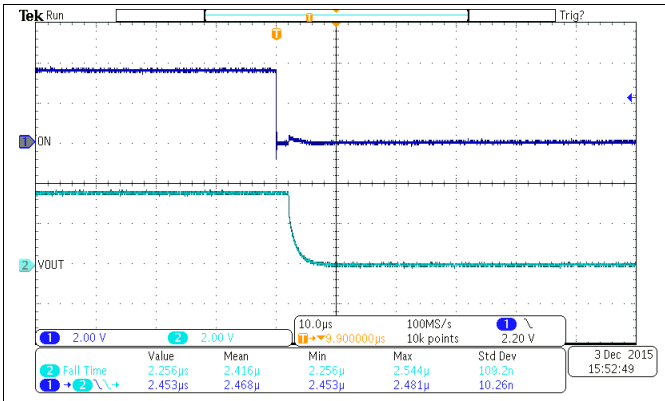


V_{IN} = 0.65 V

Figure 26. Turn-On Response (TPS22925Cx)

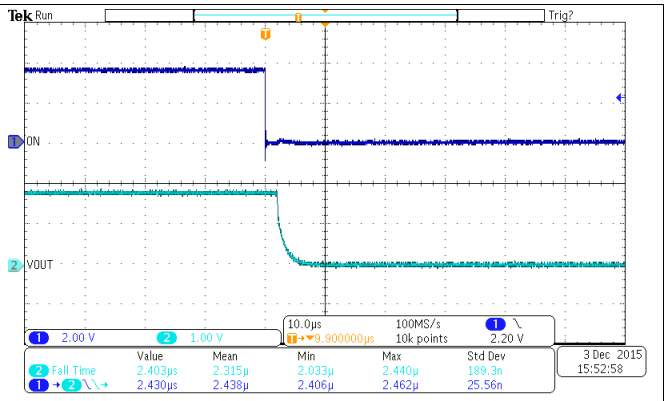
Typical Characteristics (continued)

C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω, T_A = 25°C



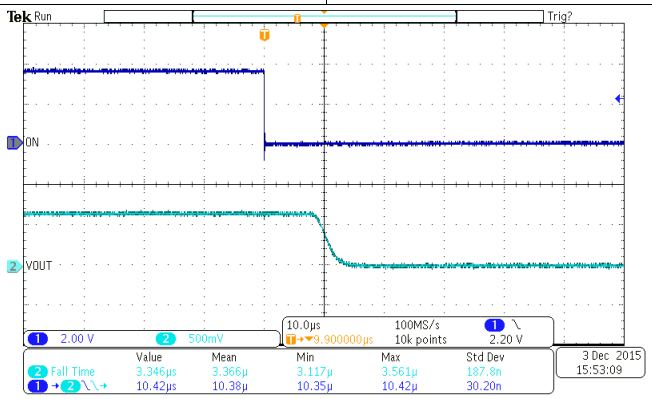
V_{IN} = 3.6 V

Figure 27. Turn-Off Response (TPS22925xx)



V_{IN} =1.8 V

Figure 28. Turn-Off Response (TPS22925xx)



V_{IN} = 0.65 V

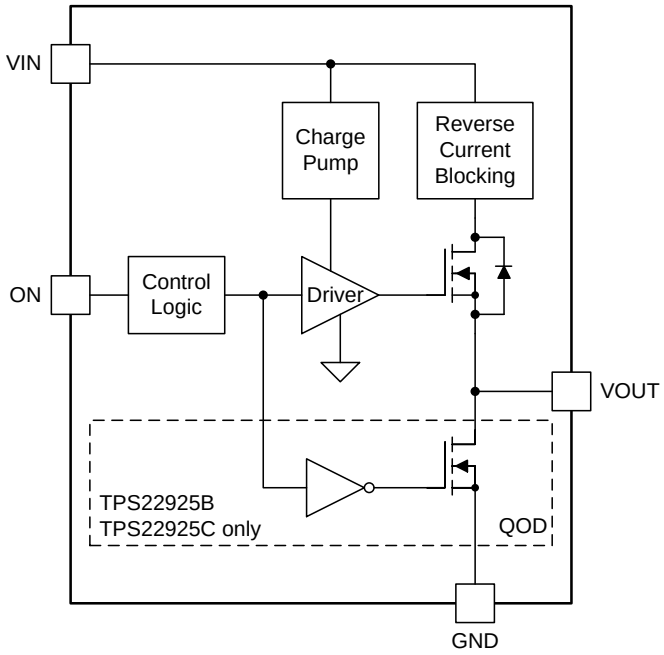
Figure 29. Turn-Off Response (TPS22925xx)

8 Detailed Description

8.1 Overview

The TPS22925 is a single channel, 3-A load switch in a WCSP-6 package. This device implements an N-channel MOSFET with a controlled rise time for applications that need to limit inrush current. The device is also designed to have low leakage current during off state. This prevents downstream circuits from pulling high standby current from the supply. The TPS22925 provides reverse current blocking when the power switch is disabled. Integrated control logic, driver, and output discharge FET eliminates the need for additional external components, which reduces solution size and bill of material (BOM) count.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 ON and OFF Control

The ON pin controls the state of the switch. Asserting the ON pin high enables the switch. The ON pin is compatible with GPIOs of 1.5 V and above.

8.3.2 Quick Output Discharge (QOD) (TPS22925B and TPS22925C only)

When the switch is disabled, a discharge path is enabled between the output and ground with a typical resistance of 150 Ω. The resistance pulls down the output and prevents it from floating when the device is disabled.

Feature Description (continued)

8.3.3 Reverse Current Blocking

The reverse current blocking feature prevents current flow from the VOUT pin to the VIN pin when the TPS22925 devices are disabled. This feature is particularly useful when the output of the device needs to be driven by another voltage source after TPS22925 is disabled (for example in a power multiplexer application). In order for this feature to work, the TPS22925 must be disabled and either of the following conditions must be met:

- $V_{IN} \geq 0.65$ V or
- $V_{OUT} \geq 0.65$ V

Figure 30 describes the ideal behavior of reverse current blocking circuit in TPS22925 devices where

- I_{VIN} is the current through the VIN pin
- V_{SRC} is the input voltage applied to the device
- V_{FORCE} is the external voltage source forced at the VOUT pin
- I_{OUT} is the output load current

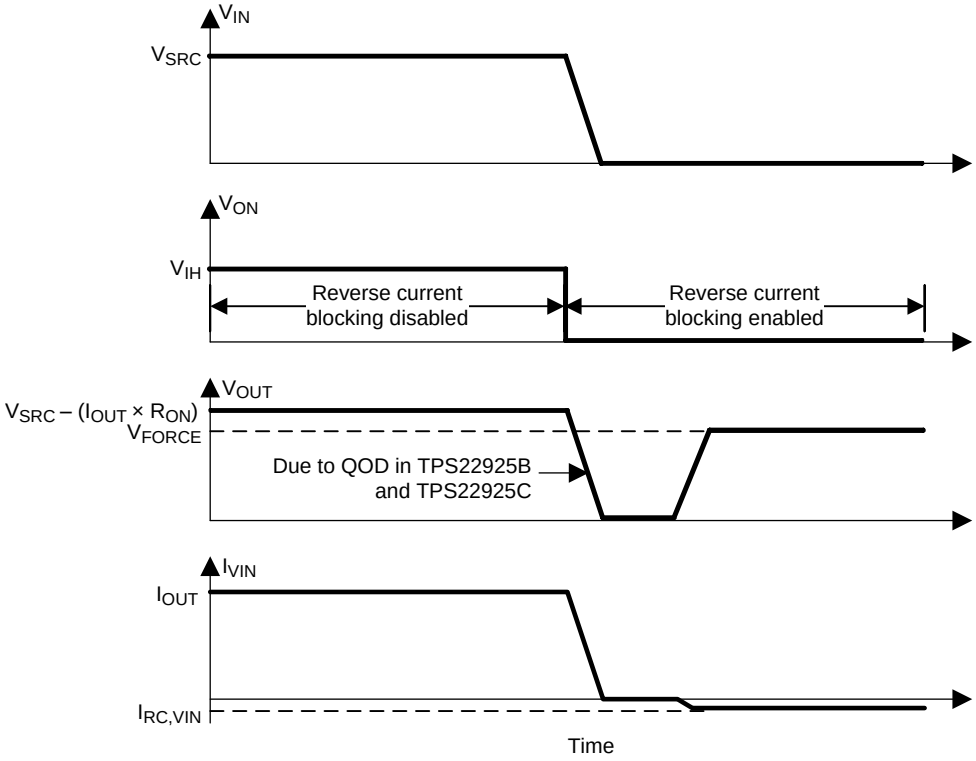


Figure 30. Reverse Current Blocking

After the device is disabled via the ON pin and VOUT is forced to an external voltage (V_{FORCE}), less than 6 µA of current flows from the VOUT pin to the VIN pin. This limitation prevents any extra current loading on the voltage source supplying the V_{FORCE} voltage.

8.4 Device Functional Modes

Table 1 shows the function table for the TPS22925xx devices.

Table 1. Function Table

ON	VIN to VOUT	OUTPUT DISCHARGE(1)
L	OFF	ENABLED
H	ON	DISABLED

(1) This feature is in the TPS22925B and TPS22925C only (not in the TPS22925BN and TPS22925CN).

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS22925 device is a 9-mΩ, single-channel load switch with a controlled slew rate. This design example describes a device containing an N–channel MOSFET that operates at an input voltage range of 3.6 V and supports a maximum continuous current of 3 A. The devices provides reverse current blocking when disabled allowing for power supply protection and power multiplexing capabilities.

9.1.1 VIN to VOUT Voltage Drop

The VIN pin to VOUT pin voltage drop in the device is determined by the R_{ON} of the device and the load current. The on-resistance of the device depends upon the VIN condition of the device. Refer to the on-resistance specification in the *Electrical Characteristics* table. After the on-resistance of the device is determined based upon the input voltage conditions, use Equation 1 to calculate the VIN-to-VOUT voltage drop.

$$\Delta V = I_L \times R_{ON} \quad (1)$$

where

- ΔV is the voltage drop from the VIN pin to the VOUT pin
- I_L is the load current
- R_{ON} is the on-resistance of the device for a specific input voltage
- Choose an appropriate I_L so that the maximum current (I_{MAX}) specification of the device is not violated

9.1.2 Input Capacitor (C_{IN})

To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor, place a capacitor between VIN and GND close to the pins. A 1-µF ceramic capacitor, C_{IN}, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop.

9.1.3 Load Capacitor (C_L)

A C_{IN} to C_L ratio of 10-to-1 is recommended for minimizing the input voltage dip caused by inrush currents during startup.

Application Information (continued)

9.1.4 Standby Power Reduction

Any end equipment that is being powered from the battery has a need to reduce current consumption in order to maintain the battery charge for a longer time. TPS22925 devices help to accomplish this reduction by turning off the supply to the modules that are in standby state and hence significantly reducing the leakage current overhead of the standby modules.

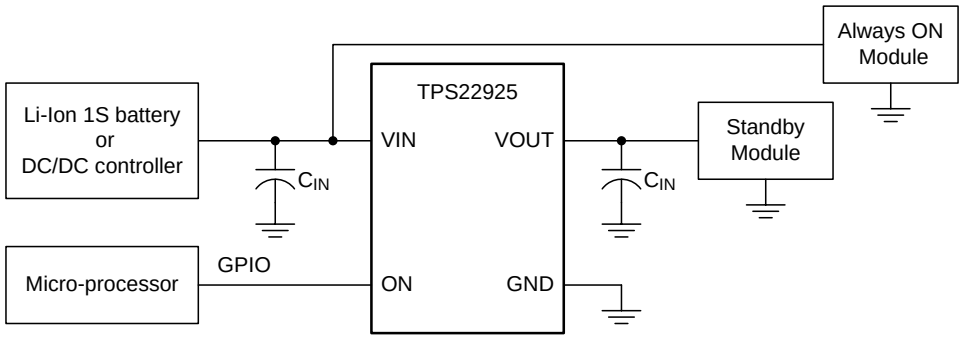


Figure 31. Standby Power Reduction

9.1.5 Power Multiplexing

Figure 32 shows a power multiplexing application using two TPS22925xN devices. Use the non-QOD version in order to maintain the output voltage. Configure the GPIO control from the microprocessor unit as break-before-make (BBM).

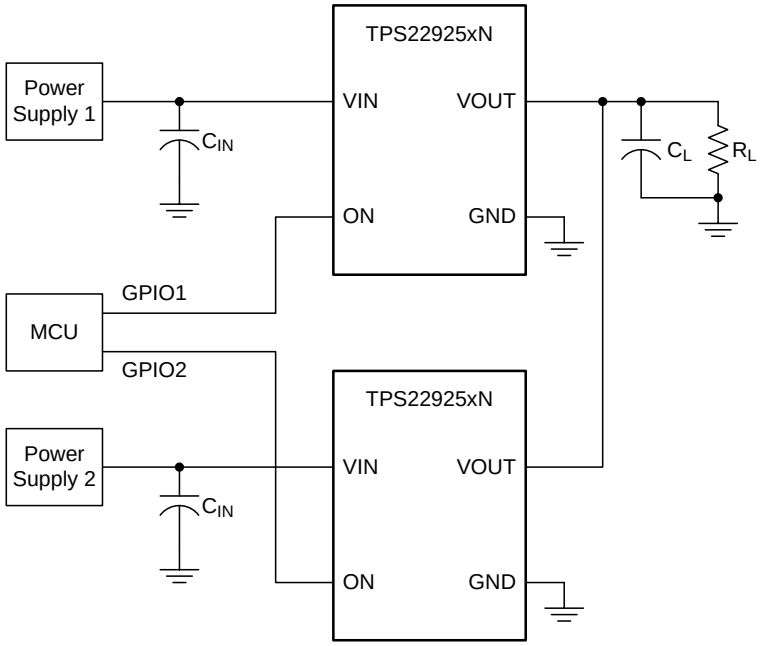


Figure 32. Power Multiplexing with Two TPS22925xN Devices

Application Information (continued)

9.1.6 Thermal Considerations

Restrict the maximum junction temperature lower than 125°C. Use Equation 2 to calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output load current and ambient temperature.

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{R_{\theta JA}} \quad (2)$$

where

- $P_{D(max)}$ is the maximum allowable power dissipation
- $T_{J(max)}$ is the maximum allowable junction temperature
- T_A is the ambient temperature of the device
- $R_{\theta JA}$ is the junction-to-air thermal impedance

NOTE

The $R_{\theta JA}$ parameter is highly dependent upon board layout. (See the *Thermal Information* table)

9.2 Typical Application

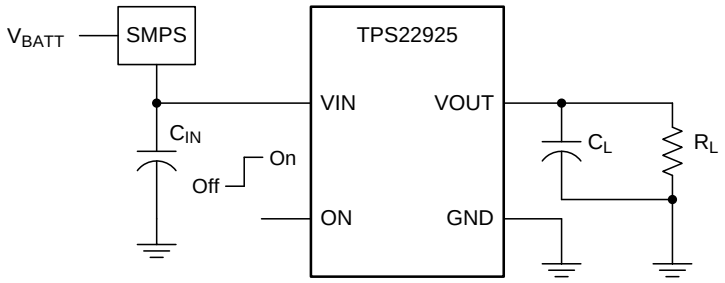


Figure 33. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the following as the input parameters.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	3.6 V
C_L	1 µF
Maximum Acceptable Inrush Current	40 mA

9.2.2 Detailed Design Procedure

9.2.2.1 Managing Inrush Current

When the switch is enabled, the V_{IN} capacitors must be charged up from 0 V to V_{IN}. This charge arrives in the form of inrush current. Calculate the inrush current using Equation 3.

$$I_{INRUSH} = C_L \times \frac{dv}{dt} \quad (3)$$

where

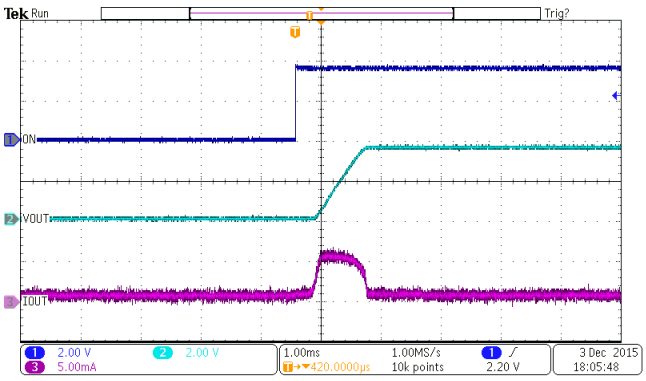
- I_{INRUSH} is the inrush current
- C_L is the load capacitance
- dv/dt is the output slew rate

TPS22925Bx and TPS22925Cx have different controlled rise time. TPS22925Bx has shorter rise time than TPS22925Cx. In the application where fast rise time is required and higher inrush current can be tolerated, consider using the TPS22925Bx. For an application that requires a longer rise time and lower inrush current, consider using the TPS22925Cx. Calculate the maximum acceptable slew rate using the design requirements and Equation 4.

$$\frac{dv}{dt} = \frac{I_{INRUSH}}{C_L} = \frac{40\ mA}{1.0\ \mu F} = 40\ V/ms \tag{4}$$

The TPS22925Bx has a typical rise time of 97 µs at 3.6 V. This results in a slew rate of 29.7 V/ms which meets the above design requirements. The TPS22925Cx has a typical rise time of 810 µs at 3.6 V. This results in a slew rate of 3.6 V/ms which also meets the above design requirements. Base on inrush current requirement, either devices can be used.

9.2.3 Application Curve



C_L = 1 µF

Figure 34. Inrush Current (TPS22925C)

10 Power Supply Recommendations

This family of devices is designed to operate with a VIN range of 0.65 V to 3.6 V. This supply must be well regulated and placed as close to the device terminal as possible with the recommended 1 µF bypass capacitor. If the supply is located more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum, or ceramic capacitor of 10 µF may be sufficient.

11 Layout

11.1 Layout Guidelines

For best performance, all traces should be as short as possible. To be most effective, the input and load capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects.

11.2 Layout Example

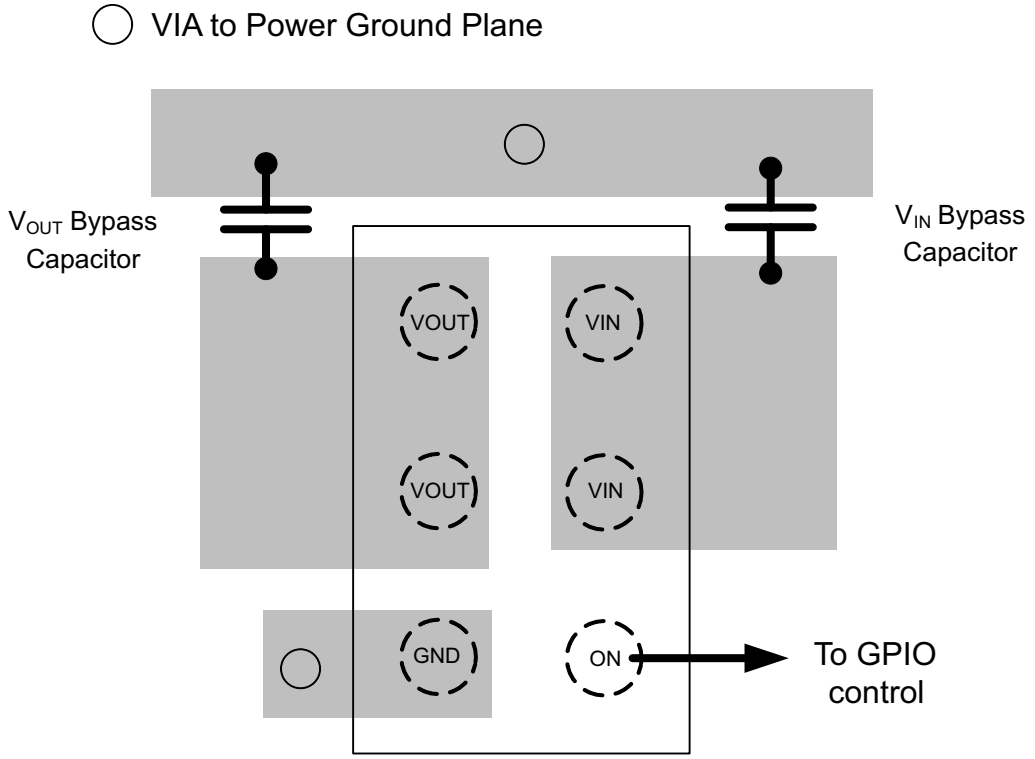


Figure 35. TPS22925xx Layout Example

12 器件和文档支持

12.1 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 商标

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这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。要获得这份数据表的浏览器版本，请查阅左侧导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22925BNYPHR	ACTIVE	DSBGA	YPH	6	3000	RoHS & Green	SAC396 | SNAGCU	Level-1-260C-UNLIM	-40 to 105	12D9	Samples
TPS22925BNYPHT	ACTIVE	DSBGA	YPH	6	250	RoHS & Green	SAC396 | SNAGCU	Level-1-260C-UNLIM	-40 to 105	12D9	Samples
TPS22925BYPHR	ACTIVE	DSBGA	YPH	6	3000	RoHS & Green	SAC396 | SNAGCU	Level-1-260C-UNLIM	-40 to 105	12A8	Samples
TPS22925BYPHT	ACTIVE	DSBGA	YPH	6	250	RoHS & Green	SAC396 | SNAGCU	Level-1-260C-UNLIM	-40 to 105	12A8	Samples
TPS22925CNYPHR	ACTIVE	DSBGA	YPH	6	3000	RoHS & Green	SAC396 | SNAGCU	Level-1-260C-UNLIM	-40 to 105	12C9	Samples
TPS22925CNYPHT	ACTIVE	DSBGA	YPH	6	250	RoHS & Green	SAC396 | SNAGCU	Level-1-260C-UNLIM	-40 to 105	12C9	Samples
TPS22925CYPHR	ACTIVE	DSBGA	YPH	6	3000	RoHS & Green	SAC396 | SNAGCU	Level-1-260C-UNLIM	-40 to 105	12B9	Samples
TPS22925CYPHT	ACTIVE	DSBGA	YPH	6	250	RoHS & Green	SAC396 | SNAGCU	Level-1-260C-UNLIM	-40 to 105	12B9	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

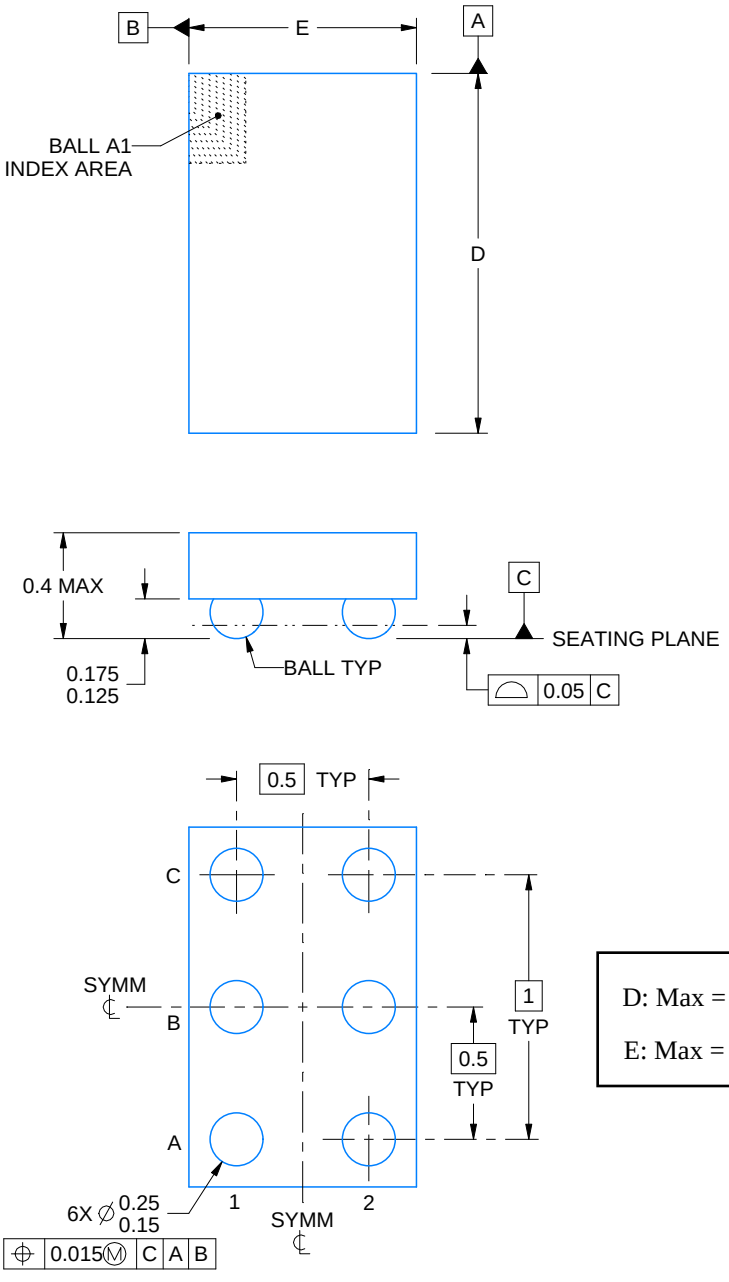
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

YPH0006

DSBGA - 0.4 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.393 mm, Min =1.332 mm

E: Max = 0.892 mm, Min =0.832 mm

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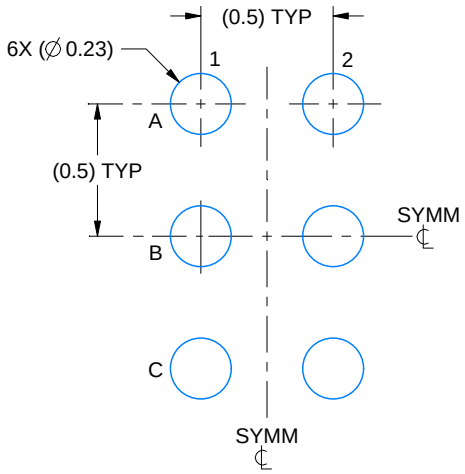
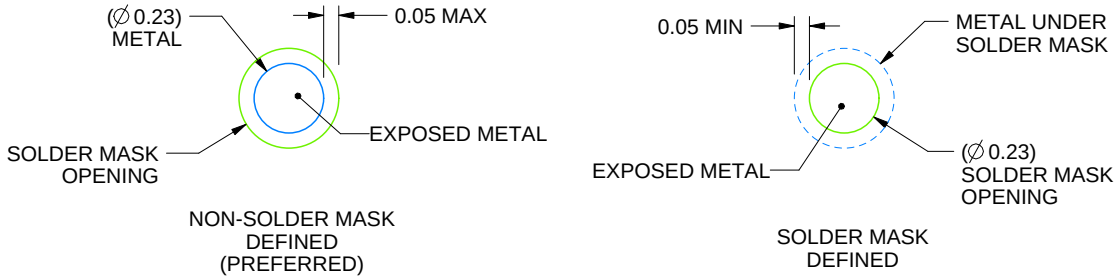
NanoFree Is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:35X



SOLDER MASK DETAILS
NOT TO SCALE

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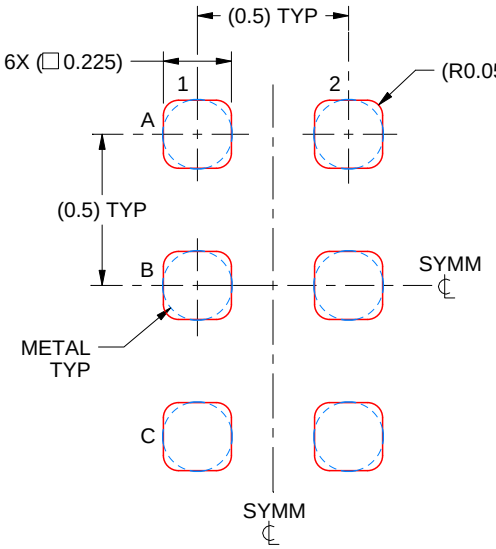
NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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