Ultra-Small, Low-Input-Voltage, Low r_{ON} Load Switch With Hysteresis Control Input

1 Features

- Integrated Single Channel Load Switch
- Input Voltage: 1.5 V to 3.6 V
- ON-Resistance
  - $r_{DS(ON)}$ = 63 mΩ at V_{IN} = 3.6 V
  - $r_{DS(ON)}$ = 69 mΩ at V_{IN} = 2.5 V
  - $r_{DS(ON)}$ = 78 mΩ at V_{IN} = 1.8 V
  - $r_{DS(ON)}$ = 87 mΩ at V_{IN} = 1.5 V
- 1-A Maximum Continuous Switch Current
- Integrated Hysteresis Enable Input (ON Pin) Allows Easy Power-Rail Sequencing
- Controlled Slew Rate Option: 26 µs at 3.6 V
- Quick Output Discharge Transistor
- Ultra-Small CSP-4 Package
- ESD Performance Tested Per JESD 22
  - 3000-V Human-Body Model (A114-B, Class II)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Battery-Powered Equipment
- Portable Industrial Equipment
- Portable Medical Equipment
- Portable Media Players
- Point-of-Sales Terminals
- GPS Devices
- Digital Cameras
- Portable Instrumentation
- Smart Phones

3 Description

The TPS22934 is a small, low ON-resistance (r_{ON}) load switch with controlled turnon. The devices contain a P-channel MOSFETs that can operate over an input voltage range of 1.5 V to 3.6 V.

The switch is controlled by an ON/OFF input (ON), which has built-in hysteresis ($V_{TH+(typ)}$ = 2.35 V) allowing an easy use of TPS22934 in power-rail sequencing applications.

In the TPS22934 a 35-Ω on-chip load resistor is added for output quick discharge when switch is turned off.

In the TPS22934, the rise time of the device is internally controlled to avoid inrush current. The TPS22934 features a typical rise time of 26 µs with a 3.6-V input.

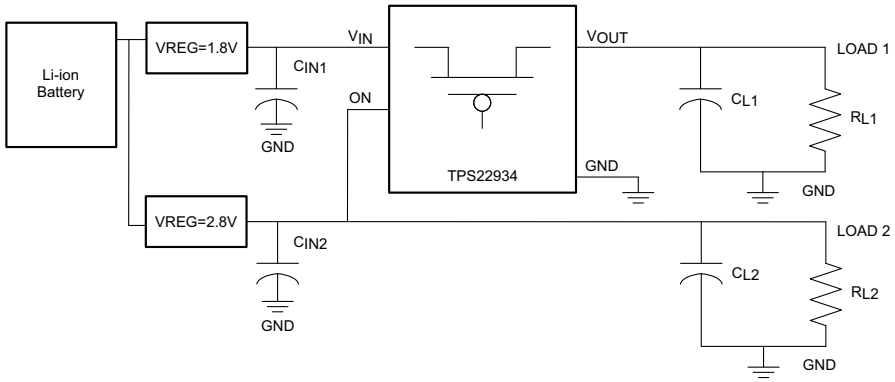
The the TPS22934 is available in an ultra-small space-saving 4-pin CSP package and is characterized for operation over the free-air temperature range of –40ºC to 85ºC.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS22934	DSBGA (4)	0.90 mm × 0.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application
1.8-V Power-Rail Sequencing



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (June 2013) to Revision B — **Page**

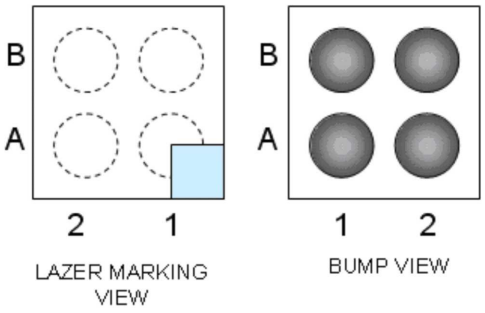
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Moved Operating free-air temperature row from Absolute Maximum Ratings to *Recommended Operating Conditions* ... 4
- Deleted *Dissipation Ratings* table and replaced it with *Thermal Information* table ... 4

Changes from Original (August 2010) to Revision A — **Page**

- Updated package reference from YZP to YZV throughout document ... 1

5 Pin Configuration and Functions

YZV Package
4-Pin DSBGA
Lazer Marking View and Bump View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
A1	VOUT	O	Switch output
A2	VIN	I	Switch input, bypass this input with a ceramic capacitor to ground
B1	GND	—	Ground
B2	ON	I	Switch control input, active high. Do not leave floating

Table 1. Terminals Assignments (YZV Package)

B	ON	GND
A	VIN	VOUT
	2	**1**

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	4	V
V_{OUT}	Output voltage		V_{IN} + 0.3	V
V_{ON}	Control input voltage	–0.3	4	V
I_{MAX}	Maximum continuous switch current, T_A = –40°C to 85°C		1	A
I_{PLS}	Maximum pulsed switch current, 100-µs pulse, 2% duty cycle, T_A = –40°C to 85°C		1.4	A
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±3000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	1.5		3.6	V
V_{ON}	Control input voltage	0		3.6	
V_{OUT}	Output voltage			V_{IN}	V
C_{IN}	Input capacitance	1 (1)			µF
T_A	Operating free-air temperature	–40		85	°C

(1) See the *Input Capacitor* section in *Application Information*.

6.4 Thermal Information

THERMAL METRIC (1)		TPS22934 YZV (DSBGA) 4 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	189.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	36.8	
ψ_{JT}	Junction-to-top characterization parameter	11.3	
ψ_{JB}	Junction-to-board characterization parameter	36.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Unless otherwise noted, the specification in the following table applies over the operating ambient temperature –40°C ≤ T_A ≤ 85°C (full). Typical values are for T_A = 25°C. V_{IN} = 1.5 V to 3.6 V.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP(1)	MAX	UNIT
I_{IN}	Quiescent current	I_{OUT} = 0, V_{IN} = V_{ON} = 3.6 V		Full		3.5	20	µA
$I_{IN(OFF)}$	OFF-state supply current	V_{ON} = GND, V_{OUT} = 0		Full		2.5	5	µA
r_{ON}	ON-state resistance	I_{OUT} = -200 mA	V_{IN} = 3.6 V	25°C		63	77	mΩ
				Full			80	
			V_{IN} = 2.5 V	25°C		69	85	
				Full			89	
			V_{IN} = 1.8 V	25°C		78	96	
				Full			100	
			V_{IN} = 1.5 V	25°C		87	107	
				Full			115	
r_{PD}	Output pulldown resistance	V_{IN} = 3.3 V, V_{ON} < V_{TH-}, I_{OUT} = 30 mA		25°C		35	65	Ω
I_{ON}	ON input bias current	V_{ON} = 1.5 V to 3.6 V or GND		Full		0.7	1.5	µA
UVLO	Undervoltage lockout	V_{IN} increasing	V_{ON} = 3.6 V, I_{OUT} = -100 mA	Full	0.8	1.05	1.4	V
		V_{IN} decreasing		Full	0.7	0.95	1.3	
V_{TH+}	Positive going ON voltage threshold	V_{IN} = 1.5 V to 3.6 V		Full	2.1	2.35	2.7	V
V_{TH-}	Negative going ON voltage threshold	V_{IN} = 1.5 V to 3.6 V		Full	1.3	1.45	1.6	V
ΔV_{TH}	Hysteresis (V_{TH+} – V_{TH-})	V_{IN} = 1.5 V to 3.6 V		Full	0.7	0.9	1.1	V

(1) Typical values are at V_{IN} = 3.3 V and T_A = 25°C.

6.6 Switching Characteristics: V_{IN} = 3.6 V

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Turnon time	R_L = 500 Ω, C_L = 0.1 µF		33		µs
t_{OFF}	Turnoff time	R_L = 500 Ω, C_L = 0.1 µF		17		µs
t_r	V_{OUT} rise time	R_L = 500 Ω, C_L = 0.1 µF		26		µs
t_f	V_{OUT} fall time	R_L = 500 Ω, C_L = 0.1 µF		7.5		µs

6.7 Switching Characteristics: V_{IN} = 2.5 V

T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Turnon time	R_L = 500 Ω, C_L = 0.1 µF		42		µs
t_{OFF}	Turnoff time	R_L = 500 Ω, C_L = 0.1 µF		17		µs
t_r	V_{OUT} rise time	R_L = 500 Ω, C_L = 0.1 µF		31		µs
t_f	V_{OUT} fall time	R_L = 500 Ω, C_L = 0.1 µF		8		µs

6.8 Switching Characteristics: V_{IN} = 1.8 V

T_A = 25°C (unless otherwise noted)

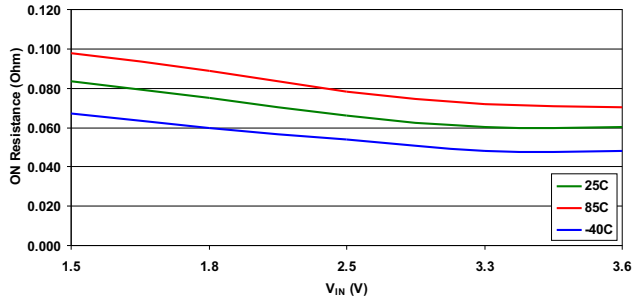
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Turnon time	R_L = 500 Ω, C_L = 0.1 µF		54		µs
t_{OFF}	Turnoff time	R_L = 500 Ω, C_L = 0.1 µF		15		µs
t_r	V_{OUT} rise time	R_L = 500 Ω, C_L = 0.1 µF		37		µs
t_f	V_{OUT} fall time	R_L = 500 Ω, C_L = 0.1 µF		10		µs

6.9 Switching Characteristics: V_{IN} = 1.5 V

T_A = 25°C (unless otherwise noted)

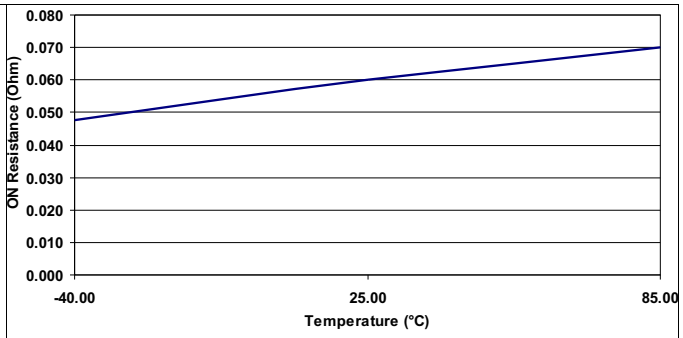
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{ON}	Turnon time	R_L = 500 Ω, C_L = 0.1 µF		64		µs
t_{OFF}	Turnoff time	R_L = 500 Ω, C_L = 0.1 µF		14		µs
t_r	V_{OUT} rise time	R_L = 500 Ω, C_L = 0.1 µF		42		µs
t_f	V_{OUT} fall time	R_L = 500 Ω, C_L = 0.1 µF		12		µs

6.10 Typical Characteristics



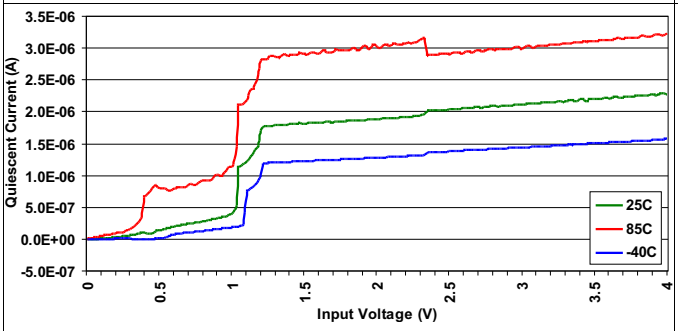
I_{OUT} = –200 mA

Figure 1. ON-Resistance vs Input Voltage



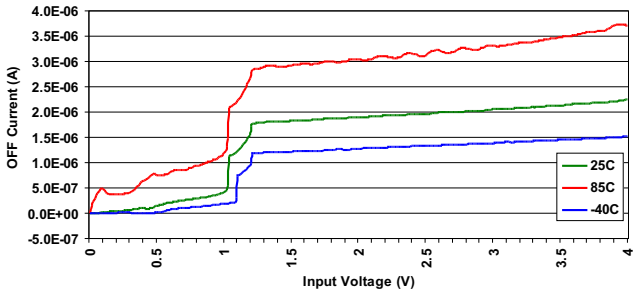
V_{IN} = 3.6 V I_{OUT} = –200 mA

Figure 2. ON-Resistance vs Temperature



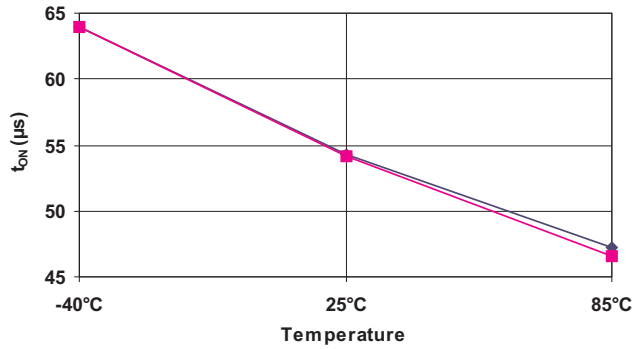
V_{ON} = V_{IN} = 3.6 V I_{OUT} = 0

Figure 3. I_{IN} (Quiescent Current) vs Input Voltage



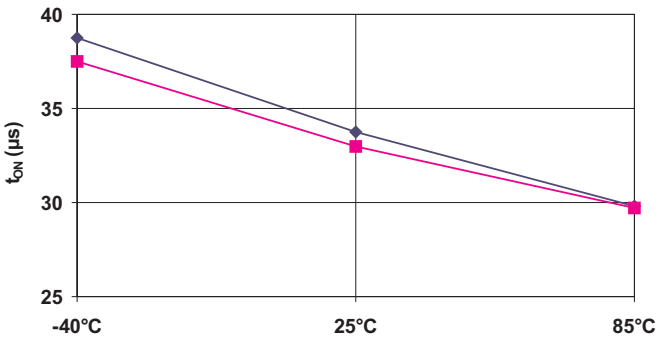
V_{ON} = 0 V

Figure 4. OFF Current (I_{INOFF}) vs Input Voltage



C_L = 0.1 µF R_L = 500 Ω

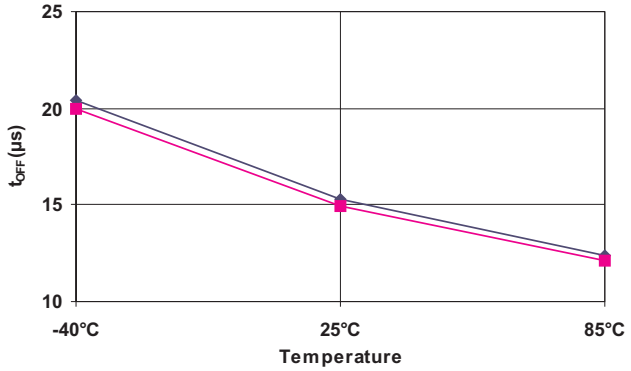
Figure 5. t_{ON} vs Temperature (V_{IN} = 1.8 V)



C_L = 0.1 µF R_L = 500 Ω

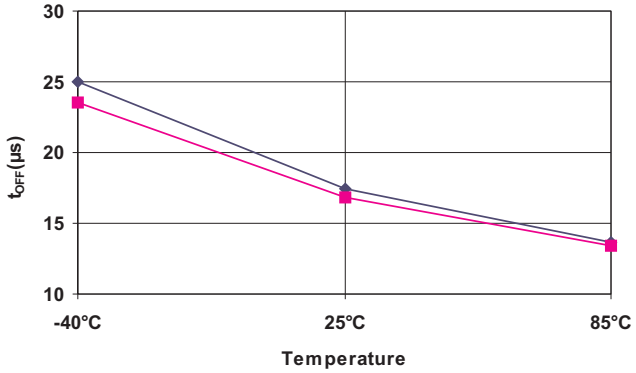
Figure 6. t_{ON} vs Temperature (V_{IN} = 3.6 V)

Typical Characteristics (continued)



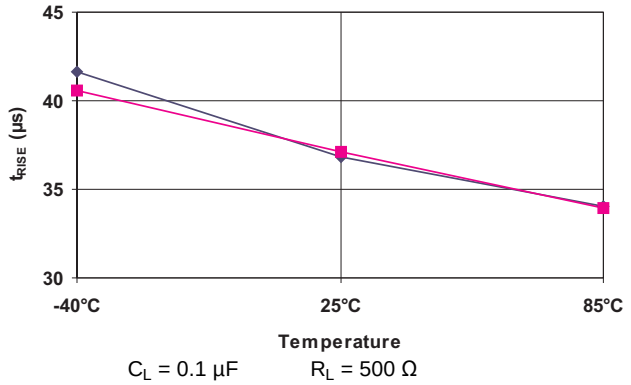
C_L = 0.1 µF R_L = 500 Ω

Figure 7. t_{OFF} vs Temperature (V_{IN} = 1.8 V)



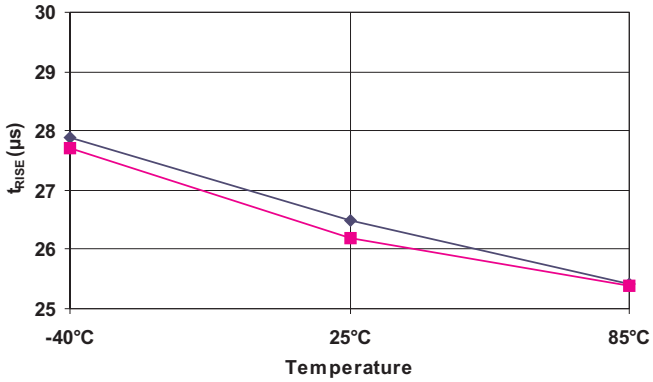
C_L = 0.1 µF R_L = 500 Ω

Figure 8. t_{OFF} vs Temperature (V_{IN} = 3.6 V)



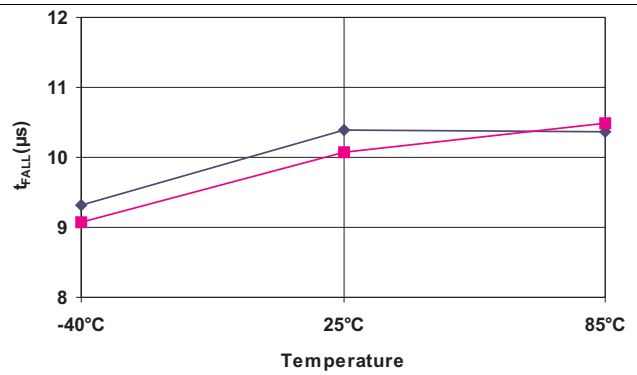
C_L = 0.1 µF R_L = 500 Ω

Figure 9. t_{RISE} vs Temperature (V_{IN} = 1.8 V)



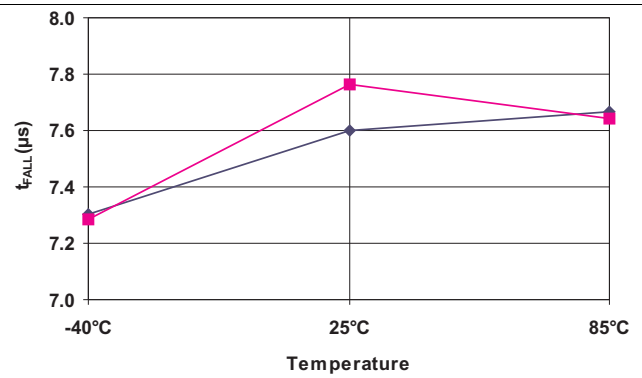
C_L = 0.1 µF R_L = 500 Ω

Figure 10. t_{RISE} vs Temperature (V_{IN} = 3.6 V)



C_L = 0.1 µF R_L = 500 Ω

Figure 11. t_{FALL} vs Temperature (V_{IN} = 1.8 V)



C_L = 0.1 µF R_L = 500 Ω

Figure 12. T_{FALL} vs Temperature (V_{IN} = 3.6 V)

Typical Characteristics (continued)

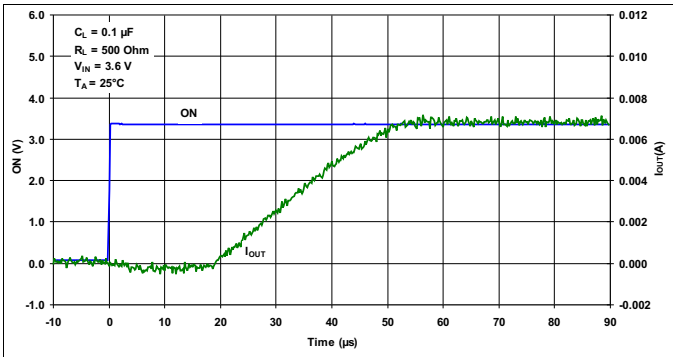


Figure 13. t_{ON} Response

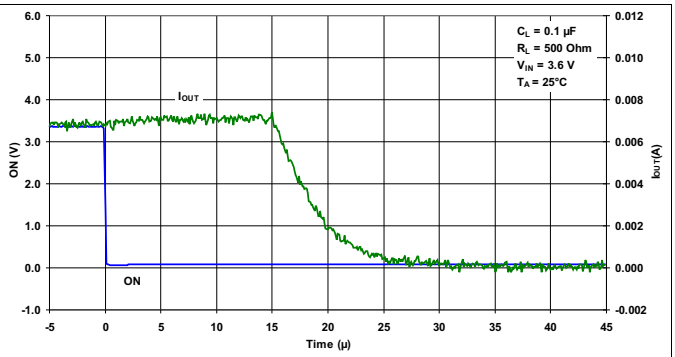


Figure 14. t_{OFF} Response

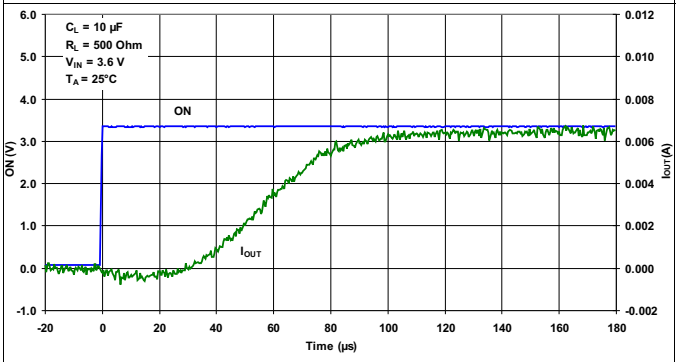


Figure 15. t_{ON} Response

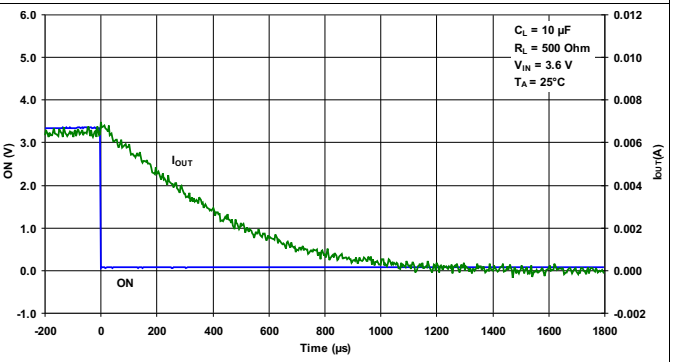


Figure 16. t_{OFF} Response

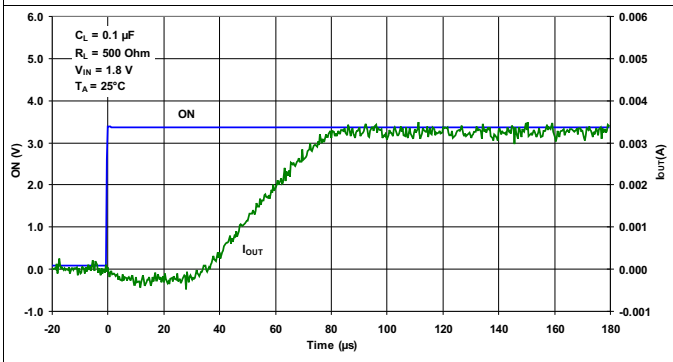


Figure 17. t_{ON} Response

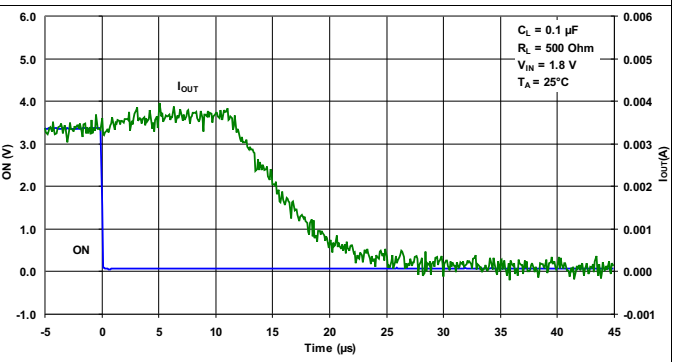


Figure 18. t_{OFF} Response

Typical Characteristics (continued)

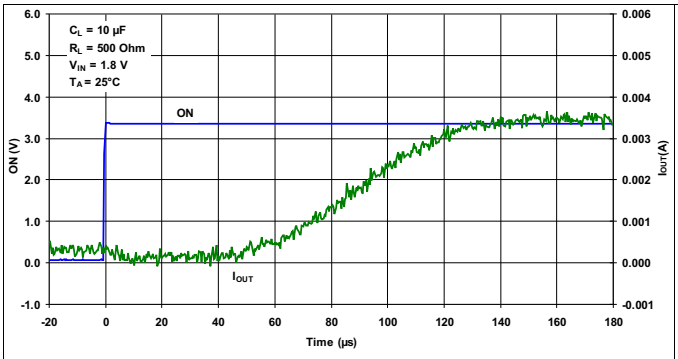


Figure 19. t_{ON} Response

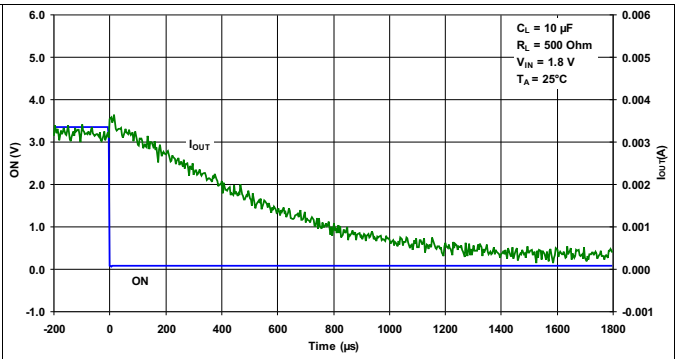


Figure 20. t_{OFF} Response

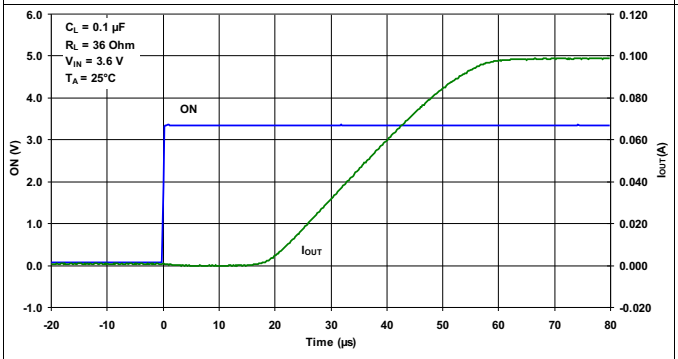


Figure 21. t_{ON} Response

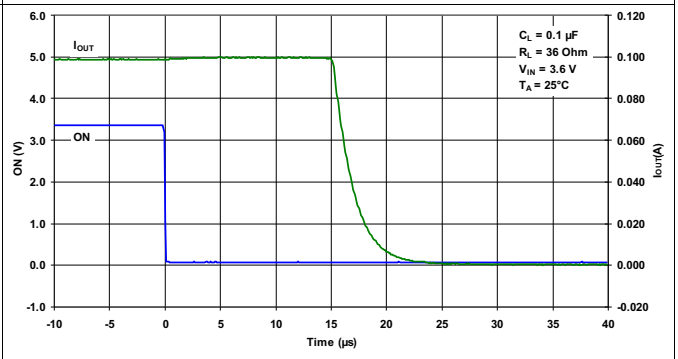


Figure 22. t_{OFF} Response

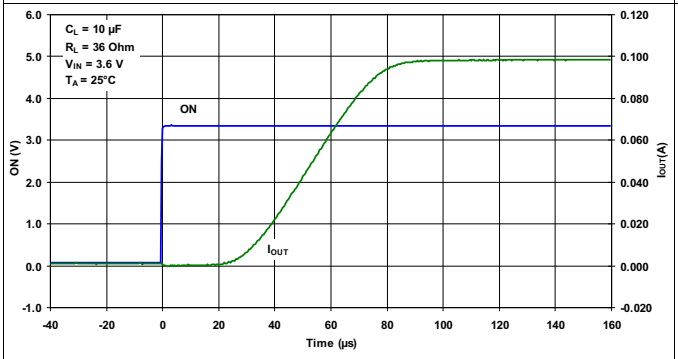


Figure 23. t_{ON} Response

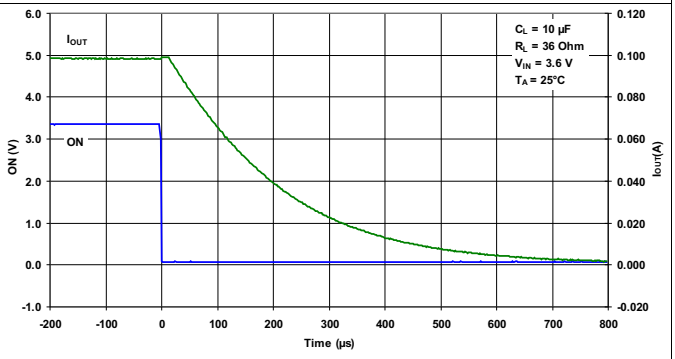


Figure 24. t_{OFF} Response

Typical Characteristics (continued)

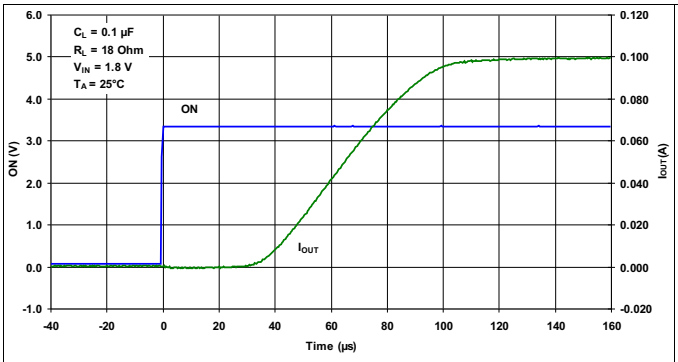


Figure 25. t_{ON} Response

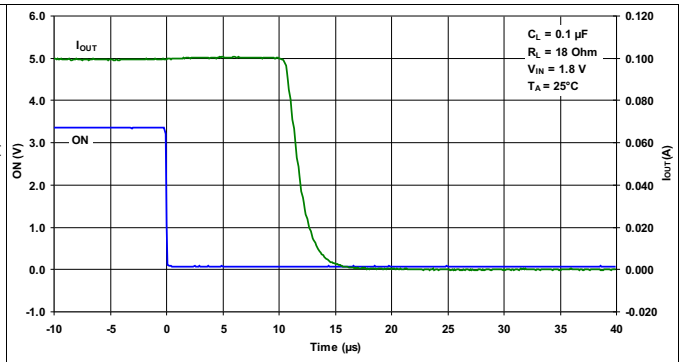


Figure 26. t_{OFF} Response

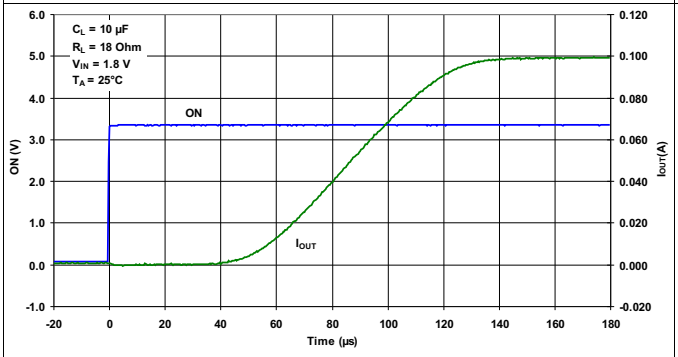


Figure 27. t_{ON} Response

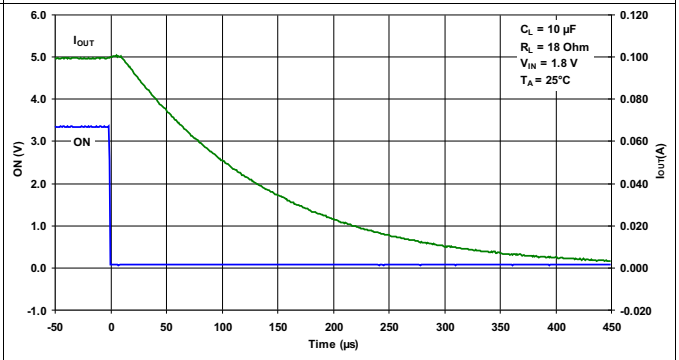
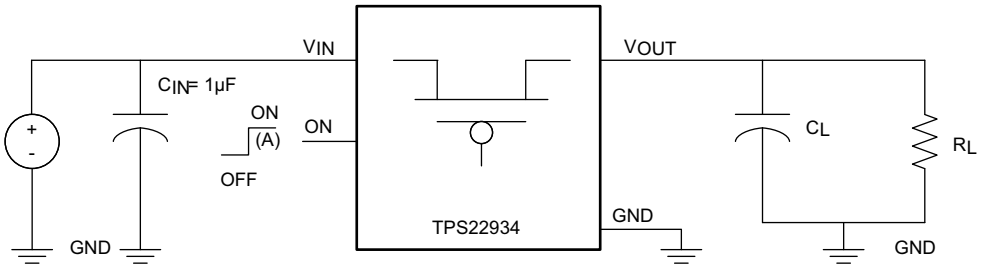
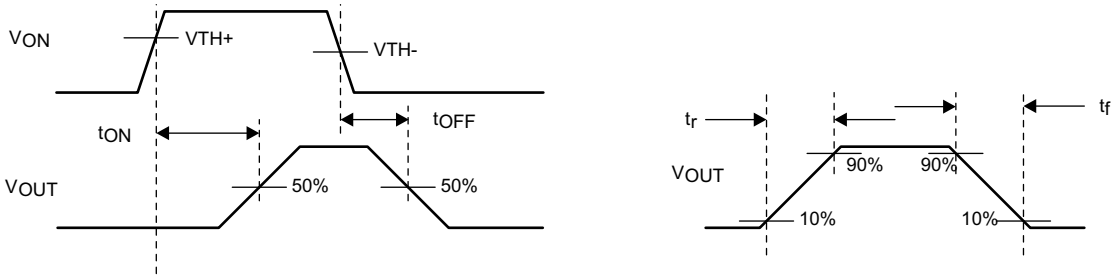


Figure 28. t_{OFF} Response

7 Parameter Measurement Information



Timing test circuit



Timing waveforms

A. Rise and fall times of the control signal is 100 ns.

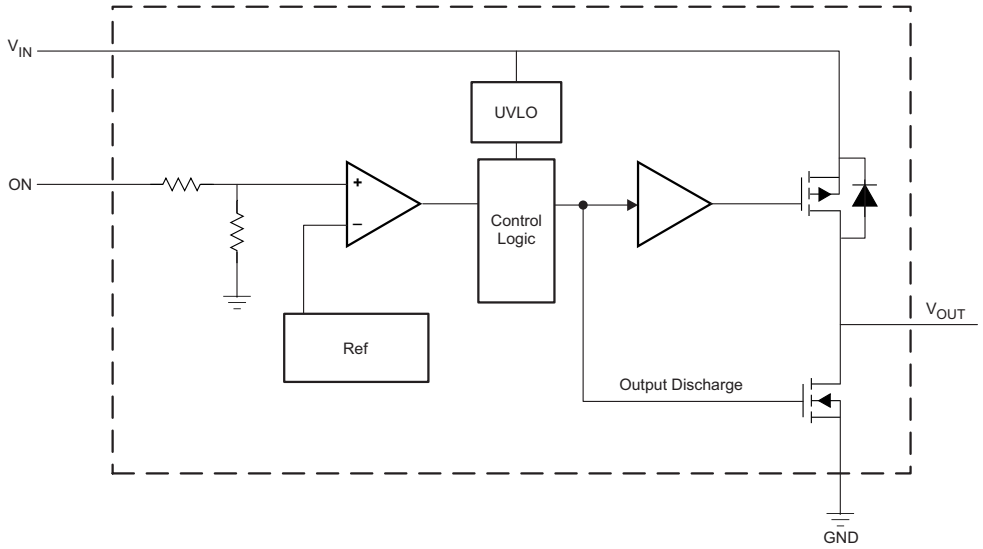
Figure 29. Test Circuit and t_{ON}/t_{OFF} Waveforms

8 Detailed Description

8.1 Overview

The TPS22934 is a single-channel, 1-A load switch in a small, space-saving DSBGA-4 package. These devices implement a P-channel MOSFET to provide a low ON-resistance for a low voltage drop across the device. A controlled rise time is used in applications to limit the inrush current. The switch is controlled by an ON/OFF input (ON), which has built-in hysteresis (VTH+(typ) = 2.35 V) allowing an easy use of TPS22934 in power-rail sequencing applications.

8.2 Functional Block Diagram



8.3 Feature Description

Table 2. Feature List

	r_{ON} (TYP) AT 3.6 V	SLEW RATE (TYP) AT 3.6 V	QUICK OUTPUT DISCHARGE	MAXIMUM OUTPUT CURRENT	ENABLE
TPS22934	63 mΩ	26 µs	Yes	1 A	Hysteresis Input $V_{TH+(typ)}$ = 2.35 V

8.3.1 ON and OFF Control

The ON pin controls the state of the switch. The TPS22934 has built-in hysteresis on its control inputs. The load switch is active when the ON voltage is greater than the positive going voltage threshold (V_{TH+}). If the ON voltage is lower than the negative going voltage threshold (V_{TH-}), then the pass FET is deactivated and the active pulldown from VOUT to GND is activated.

This scenario is ideal for power-rail sequencing applications as shown in Figure 30 where the 2.8-V supply must be valid before the 1.8-V supply turnon.

8.3.2 Undervoltage Lockout

The undervoltage lockout turns off the switch if the input voltage drops below the undervoltage lockout threshold. With the ON pin active, the input voltage rising above the undervoltage lockout threshold causes a controlled turnon of the switch, which limits current overshoots.

8.3.3 Quick Output Discharge

The TPS22934 includes the Quick Output Discharge (QOD) feature. When the switch is disabled, a discharge resistance with a typical value of 35 Ω is connected between the output and ground. This resistance pulls down the output and prevents it from floating when the device is disabled.

8.4 Device Functional Modes

Table 3. Function Table

ON (Control Signal)	VIN to VOUT	VOUT to GND
VON < V_{TH-}	OFF	ON
VON > V_{TH+}	ON	OFF

9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS22934 device is a single channel, 1-A load switch supporting VIN in the range of 1.5 to 3.6 V. The ON pin controls the state of the switch. ON pin voltage can be between 0 and 3.6 V. The device has built-in hysteresis on its control input. The load switch is active when ON voltage is greater than the positive going voltage threshold (VTH+). If the ON voltage is lower than the negative going voltage threshold (VTH-), then the pass FET is deactivated and the active pulldown from VOUT to GND is activated.

9.1.1 VIN to VOUT Voltage Drop

The VIN to VOUT voltage drop in the device is determined by the R_{ON} of the device and the load current. The R_{ON} of the device depends upon the VIN condition of the device. Refer to the R_{ON} specification of the device in the Electrical Characteristics table of this data sheet. Once the R_{ON} of the device is determined based upon the VIN conditions, use Equation 1 to calculate the VIN to VOUT voltage drop:

$$\Delta V = I_{LOAD} \times R_{ON} \quad (1)$$

where

- ΔV = Voltage drop from VIN to VOUT
- I_{LOAD} = Load current
- R_{ON} = On-resistance of the device for a specific V_{IN}
- An appropriate I_{LOAD} must be chosen such that the I_{MAX} specification of the device is not violated.

9.1.2 Input Capacitor

To limit the voltage drop on the input supply caused by transient inrush currents, when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between VIN and GND. A 1-µF ceramic capacitor, C_{IN}, placed close to the pins is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop.

9.1.3 Output Capacitor

TI recommends a C_{IN} to C_L ratio of 10 to 1 for minimizing V_{IN} dip caused by inrush currents during start-up.

9.2 Typical Application

Figure 30 demonstrates how the TPS22934 can be used for power-rail sequencing.

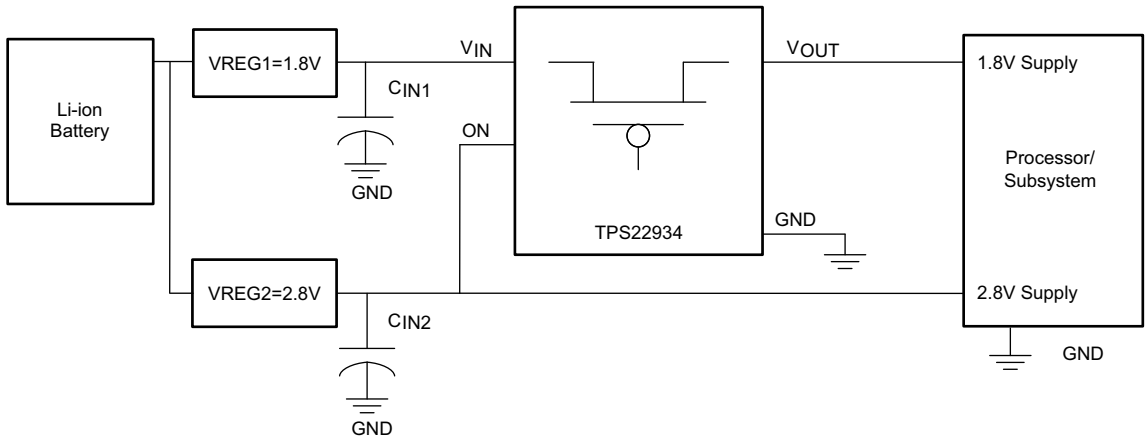


Figure 30. 1.8-V and 2.8-V Power-Rail Sequencing

9.2.1 Design Requirements

Table 4. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VREG1	1.8 V
VREG2	2.8 V

9.2.2 Detailed Design Procedure

9.2.2.1 Input Capacitor

To limit the voltage drop on the input supply caused by transient in-rush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor must be placed between VIN and GND. A 1-µF ceramic capacitor, C_{IN}, placed close to the pins is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop. A C_{IN} to C_L ratio of 10 to 1 is recommended.

9.2.2.2 Output Capacitor

Due to the integral body diode in the PMOS switch, TI highly recommends a C_{IN} greater than C_L. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN}.

9.2.3 Application Curve

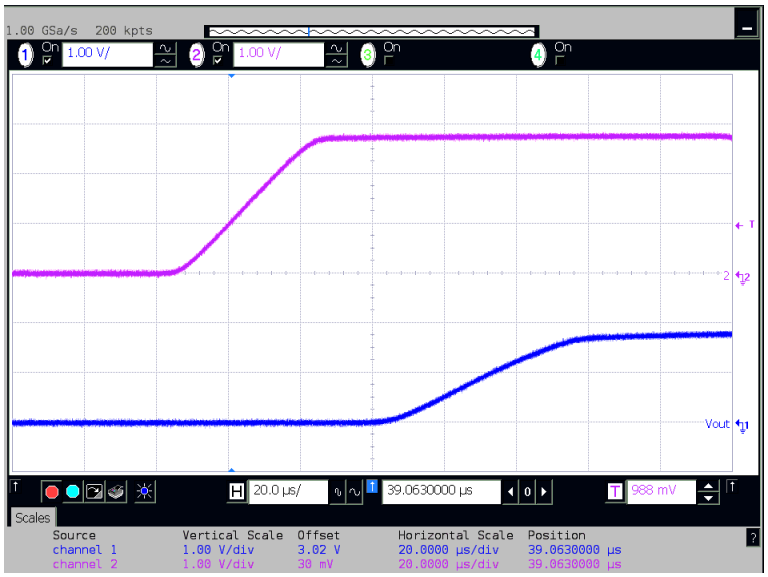


Figure 31. Power-Rail Sequencing of 2.8-V and 1.8-V Rail

10 Power Supply Recommendations

The device is designed to operate with a VIN range of 1.5 V to 3.6 V.

11 Layout

11.1 Layout Guidelines

For best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance.

11.2 Layout Example

Figure 32 shows an example for these devices. Notice the connection to system ground between the V_{OUT} Bypass Capacitor ground and the GND pin of the load switch, this creates a ground barrier which helps to reduce the ground noise seen by the device.

Layout Example (continued)

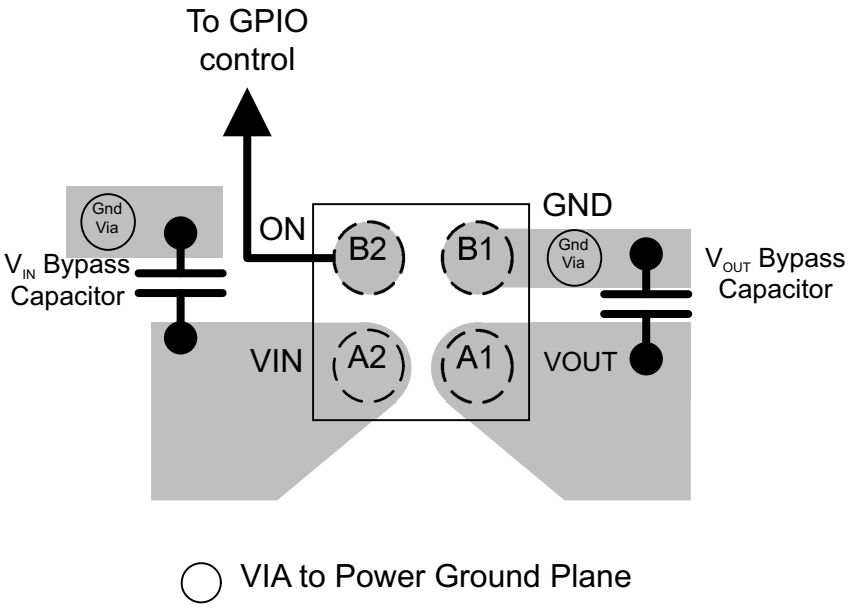


Figure 32. Recommended Layout Example

11.3 Thermal Considerations

The maximum IC junction temperature should be restricted to 125°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$ for a given output current and ambient temperature, use the following equation as a guideline:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} \quad (2)$$

where

- $P_{D(max)}$ = maximum allowable power dissipation
- $T_{J(max)}$ = maximum allowable junction temperature
- T_A = ambient temperature of the device
- θ_{JA} = junction to air thermal impedance. See the *Thermal Information* section. This parameter is highly dependent upon board layout.

12 Device and Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22934YZVR	ACTIVE	DSBGA	YZV	4	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	62 N	Samples
TPS22934YZVT	ACTIVE	DSBGA	YZV	4	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	62 N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

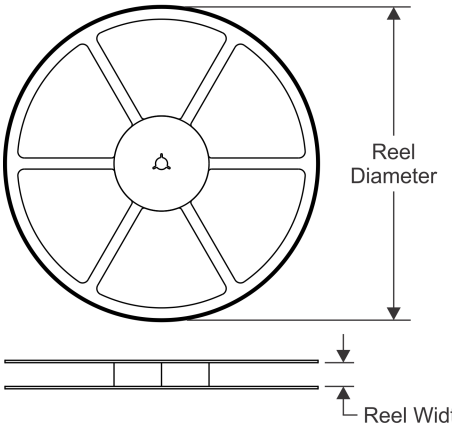
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

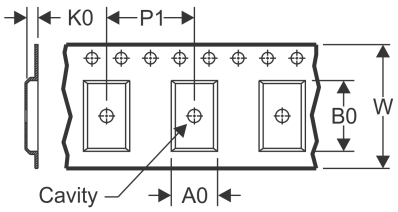
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

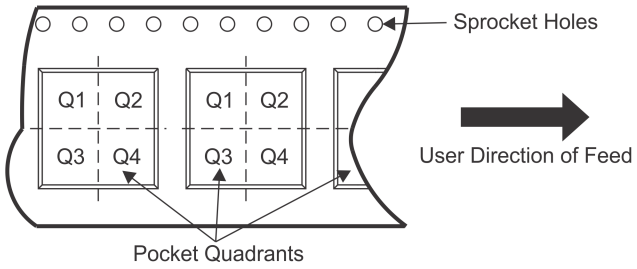


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

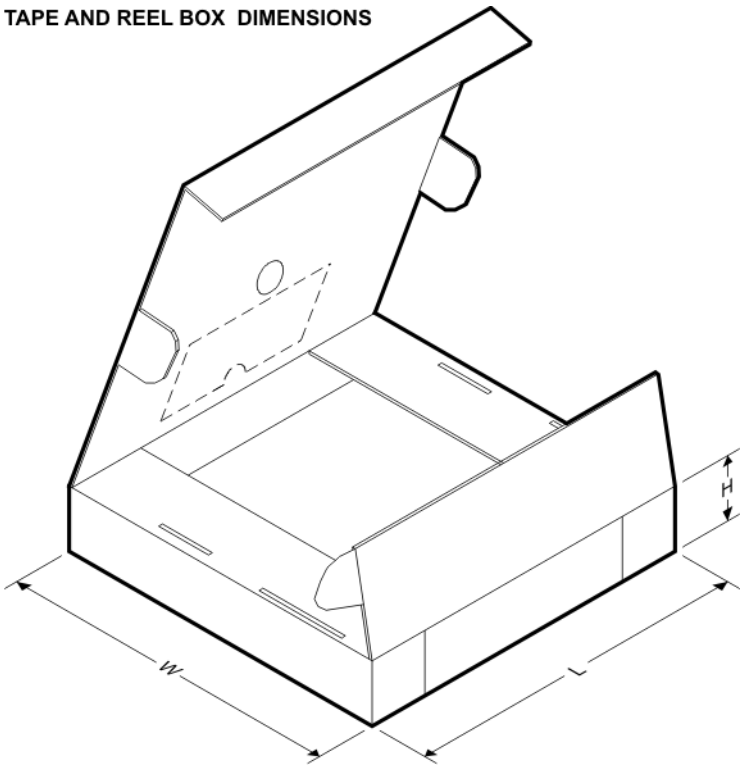
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22934YZVR	DSBGA	YZV	4	3000	178.0	9.2	1.0	1.0	0.63	4.0	8.0	Q1
TPS22934YZVT	DSBGA	YZV	4	250	178.0	9.2	1.0	1.0	0.63	4.0	8.0	Q1

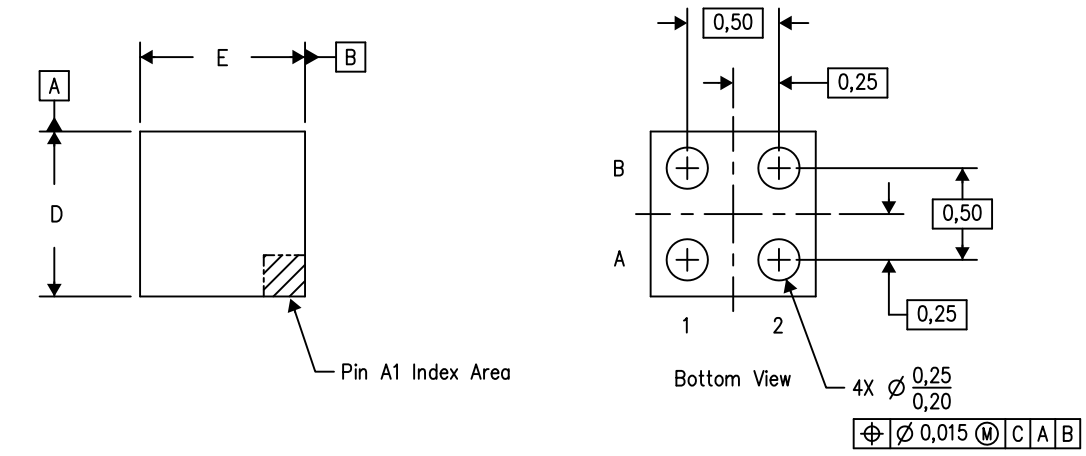
TAPE AND REEL BOX DIMENSIONS

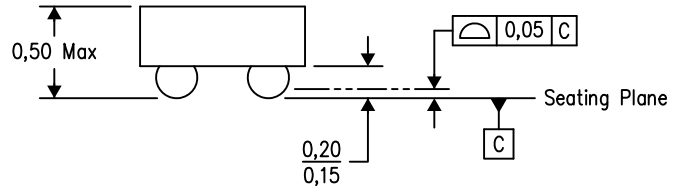


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22934YZVR	DSBGA	YZV	4	3000	220.0	220.0	35.0
TPS22934YZVT	DSBGA	YZV	4	250	220.0	220.0	35.0

YZV (S–XBGA–N4) DIE–SIZE BALL GRID ARRAY





D: Max = 0.918 mm, Min =0.858 mm

E: Max = 0.918 mm, Min =0.858 mm

4206083/C 07/13

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

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