# 具有 Eco-Mode™ 的 7 V 至 18 V 输入、4.5 A 同步降压 SWIFT™ 转换器

查询样品: TPS54429E

## 特性

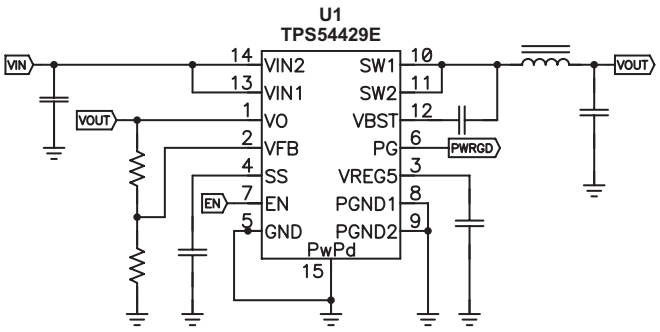
- **D-CAP2™** 模式支持快速瞬态响应
- 低输出纹波，支持陶瓷输出电容器
- 宽泛的$_{输入}$电压：**7 V** 至 **18 V**
- 输出电压范围： **0.76 V** 至 **5.5 V**
- 高效率集成型 **FET**
  针对更低占空比应用进行了优化
  ，支持 **63 mΩ**（高侧）与 **55 mΩ** （低侧）
- 关断时的高效率， 流耗不足 **10 µA**
- 初始带隙参考的高精度
- 可调软启动
- 预偏置软启动
- **700 kHz** 开关频率 **($f_{SW}$)**
- 逐周期限流
- 电源良好输出
- 在轻负载条件下执行自动跳跃 **(Auto-Skip) Eco-mode™** 模式以实现高效率

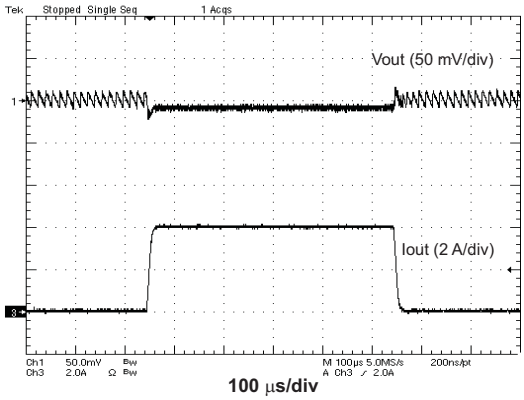
## 应用

- 用于低电压系统的广泛应用
  - 数字电视电源
  - 高清蓝 蓝光光盘™ 播放器
  - 网络家庭终端设备
  - 数字机顶盒**(STB)**

## 说明

TPS54429E 是一款自适应接通时间 D-CAP2™ 模式同步降压转换器。 TPS54429E 可帮助系统设计人员通过一个低成本、低组件数的低待机电流解决方案来完成各种终端设备的电源总线调节器集。 TPS54429E 的主控制环路采用 D-CAP2™ 模式控制，无需外部补偿组件便可实现极快的瞬态响应。 自适应接通时间控制可在更高负载状态下的 PWM 模式与轻负载下的 Eco-mode™ 工作之间实现无缝转换。 Eco-mode™ 使 TPS54429E 能够在较轻负载状况下保持高效率。 此外，TPS54429E 的专有电流还可使该器件能够适应 POSCAP与 SP-CAP 等低等效串联电阻 (ESR) 输出电容器以及超低 ESR陶瓷电容器。 该器件宽泛的工作输入电压介于 7 V 至 18 V 之间。 可在 0.76 V 至 5.5V 的范围内对输出电压进行编程。 此外，该器件还支持可调软启动时间与功率良好功能。 TPS54429E 采用 14 引脚 HTSSOP 封装与 16引脚 QFN 封装，支持从 –20°C 到 85°C 的宽泛工作温度。

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION(1)

| $T_A$ | PACKAGE(2) (3) | ORDERABLE PART NUMBER | PIN | TRANSPORT MEDIA |
|---|---|---|---|---|
| –20°C to 85°C | PowerPAD™ (HTSSOP) – PWP | TPS54429EPWP | 14 | Tube |
| | | TPS54429EPWPR | | Tape and Reel |
| | Plastic Quad Flat Pack (QFN) | TPS54429ERSAT | 16 | Tape and Reel |
| | | TPS54429ERSAR | | Tape and Reel |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) All package options have Cu NIPDAU lead/ball finish.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

| | | | VALUE | | UNIT |
|---|---|---|---|---|---|
| | | | MIN | MAX | |
| $V_I$ | Input voltage range | $V_{IN1}$, $V_{IN2}$, EN | –0.3 | 20 | V |
| | | $V_{BST}$ | –0.3 | 26 | |
| | | $V_{BST}$ (10 ns transient) | –0.3 | 28 | |
| | | $V_{FB}$, $V_O$, SS, PG | –0.3 | 6.5 | |
| | | SW1, SW2 | –2 | 20 | |
| | | SW1, SW2 (10 ns transient) | –3 | 22 | |
| $V_O$ | Output voltage range | $V_{REG5}$ | –0.3 | 6.5 | |
| | | $P_{GND1}$, $P_{GND2}$ | –0.3 | 0.3 | |
| $V_{diff}$ | Voltage from GND to POWERPAD | | –0.2 | 0.2 | |
| ESD rating | Electrostatic discharge | Human Body Model (HBM) | | 2 | kV |
| | | Charged Device Model (CDM) | | 500 | V |
| $T_J$ | Operating junction temperature | | –20 | 150 | °C |
| $T_{stg}$ | Storage temperature | | –55 | 150 | |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## THERMAL INFORMATION

| THERMAL METRIC(1) | | TPS54426 | | UNITS |
|---|---|---|---|---|
| | | PWP (14) PINS | RSA (16) PINS | |
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 55.6 | 37.3 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance | 51.3 | 42.5 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 36.4 | 14.9 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 1.8 | 0.8 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 20.6 | 14.8 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance | 4.3 | 4.9 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.


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## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{IN}$ | Supply input voltage range | | 7 | 18 | V |
| $V_I$ | Input voltage range | VBST | –0.3 | 24 | V |
| | | VBST (10 ns transient) | –0.3 | 27 | |
| | | SS, PG | –0.1 | 5.7 | |
| | | EN | –0.1 | 18 | |
| | | VO, VFB | –0.1 | 5.5 | |
| | | SW1, SW2 | –1.8 | 18 | |
| | | SW1, SW2 (10 ns transient) | –3 | 21 | |
| | | PGND1, PGND2 | –0.1 | 0.1 | |
| $V_O$ | Output voltage range | VREG5 | –0.1 | 5.7 | V |
| $I_O$ | Output Current range | $I_{VREG5}$ | 0 | 10 | mA |
| $T_A$ | Operating free-air temperature | | –20 | 85 | °C |
| $T_J$ | Operating junction temperature | | –20 | 150 | °C |

## ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, $V_{IN}$ = 12V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | |
| $I_{VIN}$ | Operating - non-switching supply current | $V_{IN}$ current, $T_A$ = 25°C, EN = 5 V, $V_{FB}$ = 0.8 V | | 850 | 1300 | µA |
| $I_{VINSDN}$ | Shutdown supply current | $V_{IN}$ current, $T_A$ = 25°C, EN = 0 V | | 1.8 | 10 | µA |
| **LOGIC THRESHOLD** | | | | | | |
| $V_{ENH}$ | EN high-level input voltage | EN | 2 | | | V |
| $V_{ENL}$ | EN low-level input voltage | EN | | | 0.48 | V |
| **$V_{FB}$ VOLTAGE AND DISCHARGE RESISTANCE** | | | | | | |
| $V_{FBTH}$ | $V_{FB}$ threshold voltage | VFB voltage light load mode, $T_A$ = 25°C, $V_O$ = 1.05 V, $I_O$ = 10mA | | 771 | | mV |
| | | $T_A$ = 25°C, $V_O$ = 1.05 V, continuous mode | 757 | 765 | 773 | |
| | | $T_A$ = 0°C to 85°C, $V_O$ = 1.05 V, continuous mode(1) | 753 | | 777 | |
| | | $T_A$ = –20°C to 85°C, $V_O$ = 1.05 V, continuous mode(1) | 751 | | 779 | |
| $I_{VFB}$ | $V_{FB}$ input current | $V_{FB}$ = 0.8 V, $T_A$ = 25°C | | 0 | ±0.1 | µA |
| $R_{Dischg}$ | $V_O$ discharge resistance | EN = 0 V, $V_O$ = 0.5 V, $T_A$ = 25°C | | 50 | 100 | Ω |
| **$V_{REG5}$ OUTPUT** | | | | | | |
| $V_{VREG5}$ | $V_{REG5}$ output voltage | $T_A$ = 25°C, 7 V < $V_{IN}$ < 18 V, 0 < $I_{VREG5}$ < 5 mA | 5.3 | 5.5 | 5.7 | V |
| $V_{LN5}$ | Line regulation | 7 V < $V_{IN}$ < 18 V, $I_{VREG5}$ = 5 mA | | | 20 | mV |
| $V_{LD5}$ | Load regulation | 0 mA < $I_{VREG5}$ < 5 mA | | | 100 | mV |
| $I_{VREG5}$ | Output current | $V_{IN}$ = 7 V, $V_{REG5}$ = 4 V, $T_A$ = 25°C | | 70 | | mA |
| **MOSFET** | | | | | | |
| $R_{dsonh}$ | High side switch resistance | 25°C, $V_{BST}$ - SW1,2 = 5.5 V | | 63 | | mΩ |
| $R_{dsonl}$ | Low side switch resistance | 25°C | | 55 | | mΩ |

(1) Not production tested.

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## ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, $V_{IN}$ = 12V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **CURRENT LIMIT** | | | | | | |
| $I_{ocl}$ | Current limit | $L_{OUT}$ = 1.5 µH(2), $T_A$ = -20 ºC to 85 ºC | 5.2 | 5.9 | 8.0 | A |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{SDN}$ | Thermal shutdown threshold | Shutdown temperature (2) | | 165 | | °C |
| | | Hysteresis (2) | | 30 | | |
| **ON-TIME TIMER CONTROL** | | | | | | |
| $T_{ON}$ | On time | $V_{IN}$ = 12 V, $V_O$ = 1.05 V | | 145 | | ns |
| $T_{OFF(MIN)}$ | Minimum off time | $T_A$ = 25°C, $V_{FB}$ = 0.7 V | | 260 | 310 | ns |
| **SOFT START** | | | | | | |
| $I_{SSC}$ | SS charge current | $V_{SS}$ = 0 V | 1.4 | 2.0 | 2.6 | µA |
| $I_{SSD}$ | SS discharge current | $V_{SS}$ = 0.5 V | 0.1 | 0.2 | | mA |
| **POWER GOOD** | | | | | | |
| $V_{THPG}$ | PG threshold | $V_{FB}$ rising (good) | 85 | 90 | 95 | % |
| | | $V_{FB}$ falling (fault) | | 85 | | % |
| $I_{PG}$ | PG sink current | PG = 0.5 V | 2.5 | 5 | | mA |
| **OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION** | | | | | | |
| $V_{OVP}$ | Output OVP trip threshold | OVP detect | 115 | 120 | 125 | % |
| $T_{OVPDEL}$ | Output OVP prop delay | | | 10 | | µs |
| $V_{UVP}$ | Output UVP trip threshold | UVP detect | 60 | 65 | 70 | % |
| | | Hysteresis | | 10 | | % |
| $T_{UVPDEL}$ | Output UVP delay | | | 0.25 | | ms |
| $T_{UVPEN}$ | Output UVP enable delay | Relative to soft-start time | | x 1.7 | | |
| **UVLO** | | | | | | |
| $V_{UVLO}$ | UVLO threshold | Wake up $V_{REG5}$ voltage | 3.5 | 3.8 | 4.1 | V |
| | | Hysteresis $V_{REG5}$ voltage | 0.23 | 0.35 | 0.47 | |

(2) Not production tested.


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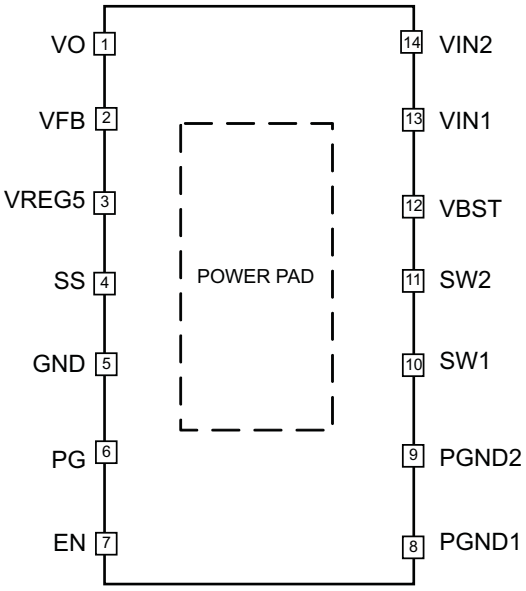
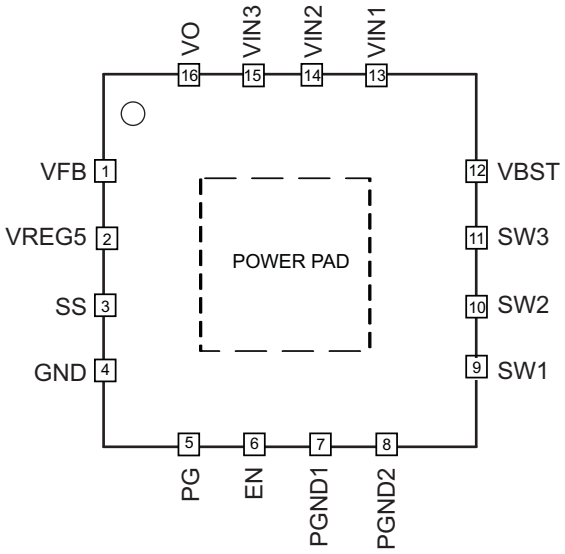
## DEVICE INFORMATION

**PWP PACKAGE**
**(TOP VIEW)**




**RSA PACKAGE**
**(TOP VIEW)**




### PIN FUNCTIONS

| PIN | | | DESCRIPTION |
|---|---|---|---|
| NAME | NUMBER | | |
| | PWP 14 | RSA 16 | |
| VO | 1 | 16 | Connect to output of converter. This terminal is used for On-Time Adjustment. |
| VFB | 2 | 1 | Converter feedback input. Connect to output voltage with feedback resistor divider. |
| VREG5 | 3 | 2 | 5.5 V power supply output. A capacitor (typical 1 µF) should be connected to GND. VREG5 is not active when EN is low. |
| SS | 4 | 3 | Soft-start control. A external capacitor should be connected to GND. |
| GND | 5 | 4 | Signal ground pin. |
| PG | 6 | 5 | Open drain power good output. |
| EN | 7 | 6 | Enable control input. EN is active high and must be pulled up to enable the device. |
| PGND1, PGND2 | 8, 9 | 7, 8 | Ground returns for low-side MOSFET. Also serve as inputs of current comparators. Connect PGND and GND strongly together near the IC. |
| SW1, SW2 | 10, 11 | 9, 10, 11 | Switch node connection between high-side NFET and low-side NFET. Also serve as inputs to current comparators. |
| VBST | 12 | 12 | Supply input for high-side NFET gate driver (boost terminal). Connect capacitor from this pin to respective SW1, SW2 terminals. An internal PN diode is connected between VREG5 to VBST pin. |
| VIN1, VIN2 | 13, 14 | 13, 14, 15 | Power input and connected to high side NFET drain. Supply input for 5-V internal linear regulator for the control circuitry. |
| PowerPAD™ or Thermal Pad | Back side | Back side | Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Should be connected to PGND. |

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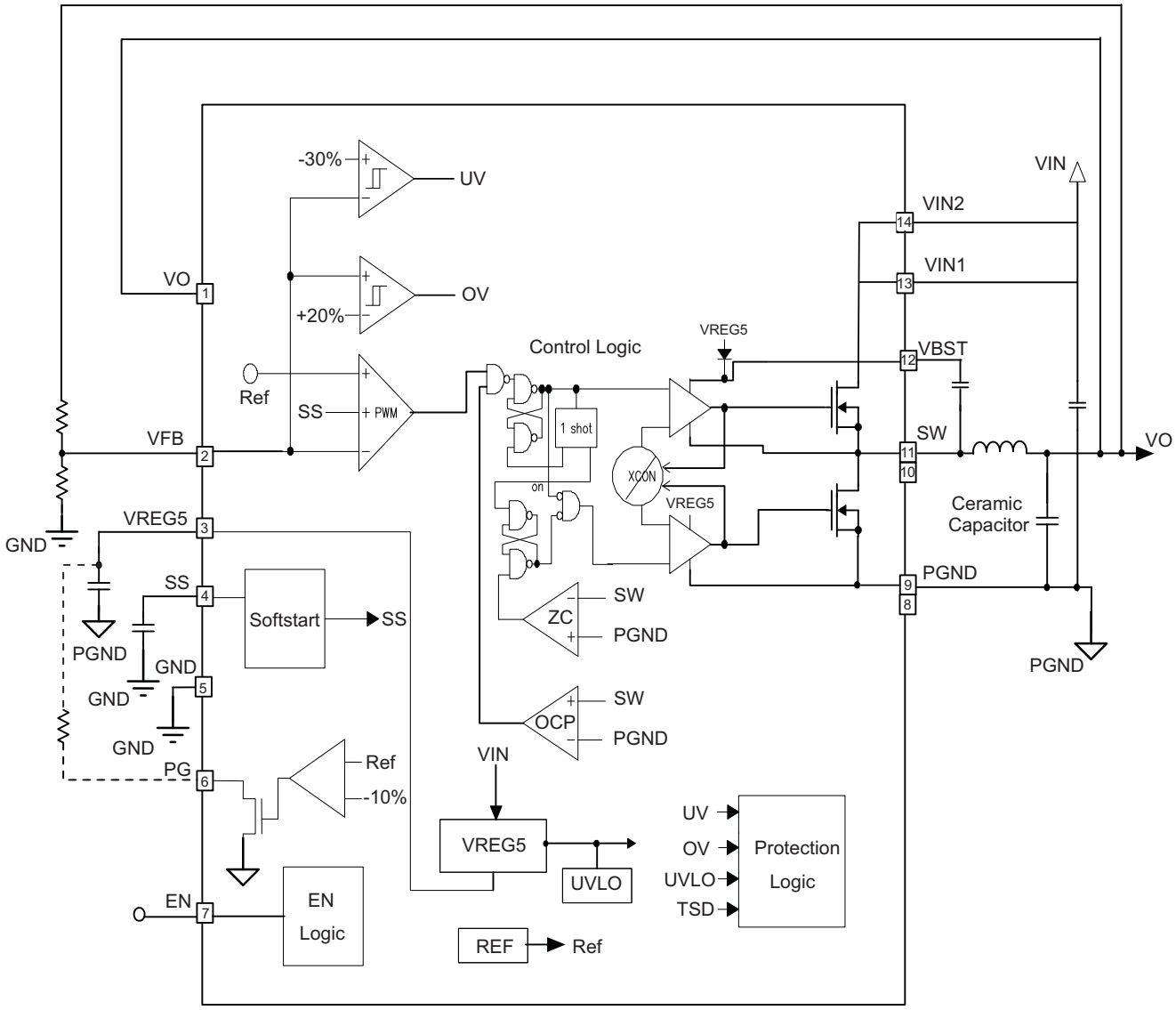
## FUNCTIONAL BLOCK DIAGRAM




A. The block diagram shown is for the PWP 14 pin package. The QFN 16 pin package block diagram is identical except for the pin out.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## OVERVIEW

The TPS54429E is a 4.5-A synchronous step-down (buck) converter with two integrated N-channel MOSFETs and auto-skip Eco-mode™ to improve light lode efficiency. It operates using D-CAP2™ mode control. The fast transient response of D-CAP2™ control reduces the output capacitance required to meet a specific level of performance. Proprietary internal circuitry allows the use of low ESR output capacitors including ceramic and special polymer types.

## DETAILED DESCRIPTION

### PWM Operation

The main control loop of the TPS54429E is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ mode control. D-CAP2™ mode control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. The MOSFET is turned off after the internal one-shot timer expires. The one-shot timer is set by the converter input voltage, VIN, and the output voltage, VO, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2™ mode control.

### PWM Frequency and Adaptive On-Time Control

TPS54429E uses an adaptive on-time control scheme and does not have a dedicated on board oscillator. The TPS54429E runs with a pseudo-constant frequency of 700 kHz by using the input voltage and output voltage to set the on-time one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage. The actual frequency may vary from 700 kHz depending on the off time, which is ended when the fed back portion of the output voltage falls to the VFB threshold voltage.

### Auto-Skip Eco-Mode™ Control

The TPS54429E is designed with Auto-Skip Eco-mode™ to increase light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when its zero inductor current is detected. As the load current further decreases the converter run into discontinuous conduction mode. The on-time is kept almost the same as is was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. The transition point to the light load operation $I_{OUT(LL)}$ current can be calculated in Equation 1.

$$I_{OUT(LL)} = \frac{1}{2 \cdot L \cdot fsw} \cdot \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{V_{IN}} \quad (1)$$

### Soft Start and Pre-Biased Soft Start

The soft start function is adjustable. When the EN pin becomes high, 2 µA current begins charging the capacitor which is connected from the SS pin to GND. Smooth control of the output voltage is maintained during start up. The equation for the slow start time is shown in Equation 2. VFB voltage is 0.765 V and SS pin source current is 2 µA.

$$Tss(ms) = \frac{C6(nF) \bullet Vref}{Iss(\mu A)} = \frac{C6(nF) \bullet 0.765}{2} \quad (2)$$

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The TPS54429E contains a unique circuit to prevent current from being pulled from the output during startup if the output is pre-biased. When the soft-start commands a voltage higher than the pre-bias level (internal soft start becomes greater than feedback voltage $V_{FB}$), the controller slowly activates synchronous rectification by starting the first low side FET gate driver pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-bias output, and ensure that the out voltage (VO) starts and ramps up smoothly into regulation and the control loop is given time to transition from pre-biased start-up to normal mode operation.

### Power Good

The TPS54429E has power-good open drain output. The power good function is activated after soft start has finished. The power good function becomes active after 1.7 times soft-start time. When the output voltage is within -10% of the target value, internal comparators detect power good state and the power good signal becomes high. If the PG output is pulled up to VREG5, the resister value, which is connected between PG and VREG5, must be in the range of 20k ohm to 150k ohm. If the feedback voltage goes under 15% of the target value, the power good signal becomes low after a 5 µs internal delay.

### VREG5

VREG5 is an internally generated voltage source used by the TPS54429E. It is derived directly from the input voltage and is nominally regulated to 5.5 V when the input voltage is above 5.6 V. The output of the VREG5 regulator is the input to the internal UVLO function. VREG5 must be above the UVLO wake up threshold voltage (3.8 V typical) for the TPS54429E to function. Connect a 1.0 µF capacitor between pin 3 of the TPS54429E and power ground for proper regulation of the VREG5 output. The VREG5 output voltage is available for external use and can typically source up to 70 mA. The VREG5 output is disabled when the TPS54429E EN pin is open or pulled low.

### Output Discharge Control

TPS54429E discharges the output when EN is low, or the controller is turned off by the protection functions (OVP, UVP, UVLO and thermal shutdown). The output is discharged by an internal 50-Ω MOSFET which is connected from VO to PGND. The internal low-side MOSFET is not turned on during the output discharge operation to avoid the possibility of causing negative voltage at the output.

### Current Protection

The output overcurrent protection (OCP) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored by measuring the low-side FET switch voltage between the SW pin and GND. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on-time of the high-side FET switch, the switch current increases at a linear rate determined by $V_{IN}$, $V_{OUT}$, the on-time, and the output inductor value. During the on-time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current $I_{OUT}$. If the measured voltage is above the voltage proportional to the current limit, the device constantly monitors the low-side FET switch voltage, which is proportional to the switch current, during the low-side on-time. The converter maintains the low-side switch on until the measured voltage is below the voltage corresponding to the current limit at which time the switching cycle is terminated and a new switching cycle begins. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of overcurrent protection. The load current one half of the peak-to-peak inductor current higher than the overcurrent threshold. Also when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This may cause the output under-voltage protection circuit to be activated. When the overcurrent condition is removed, the output voltage will return to the regulated value. This protection is non-latching.


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### Over/Under Voltage Protection

The TPS54429E detects over and undervoltage conditions by monitoring the feedback voltage (VFB). This function is enabled after approximately 1.7 times the soft-start time. When the feedback voltage becomes higher than 120% of the target voltage, the OVP comparator output goes high and the circuit latches the high-side MOSFET driver turns off and the low-side MOSFET turns on. When the feedback voltage becomes lower than 65% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins. After 250 µs, the device latches off both internal top and bottom MOSFET.

### UVLO Protection

Undervoltage lock out protection (UVLO) monitors the voltage of the $V_{REG5}$ pin. When the $V_{REG5}$ voltage is lower than UVLO threshold voltage, the TPS54429E is shut off. This is protection is non-latching.

### Thermal Shutdown

Thermal protection is self-activating. If the junction temperature exceeds the threshold value (typically 165°C), the TPS54429E shuts off. This protection is non-latching.

## TYPICAL CHARACTERISTICS

**Vin CURRENT vs JUNCTION TEMPERATURE**

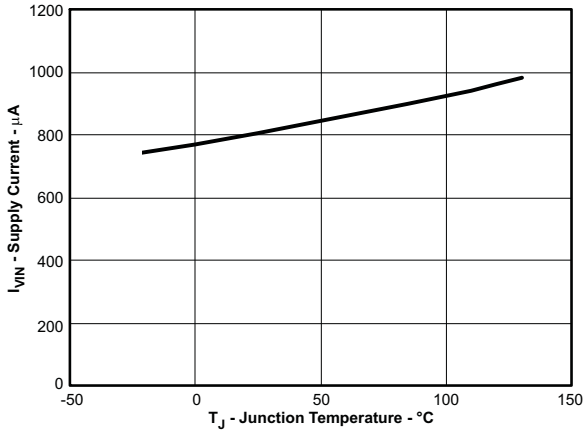


**Figure 1.**

**Vin SHUTDOWN CURRENT vs JUNCTION TEMPERATURE**

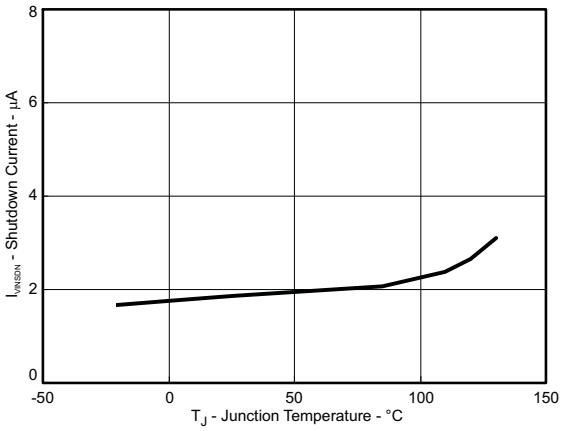


**Figure 2.**

## TYPICAL CHARACTERISTICS (continued)

**EN CURRENT vs EN VOLTAGE**

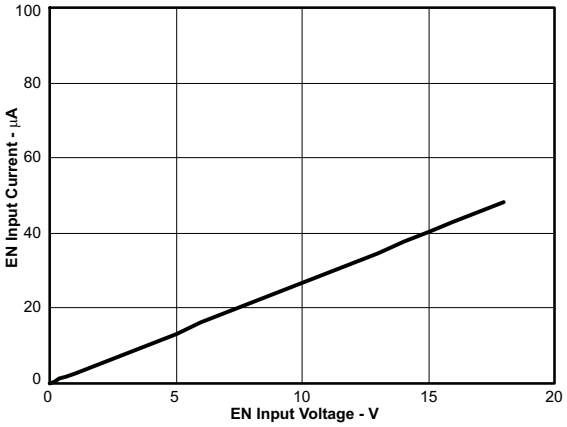


**Figure 3.**

**1.05V OUTPUT VOLTAGE vs OUTPUT CURRENT**

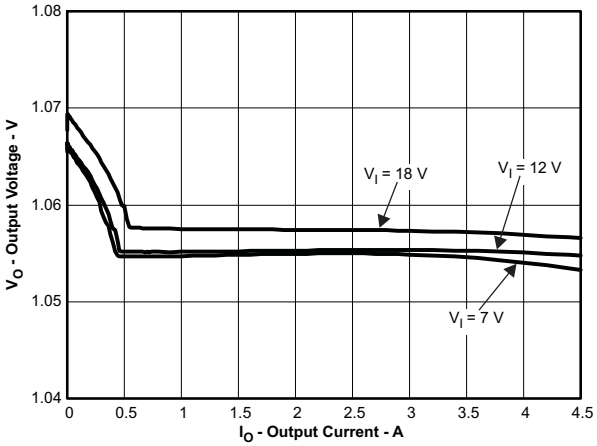


**Figure 4.**

**1.05V OUTPUT VOLTAGE vs INPUT VOLTAGE**

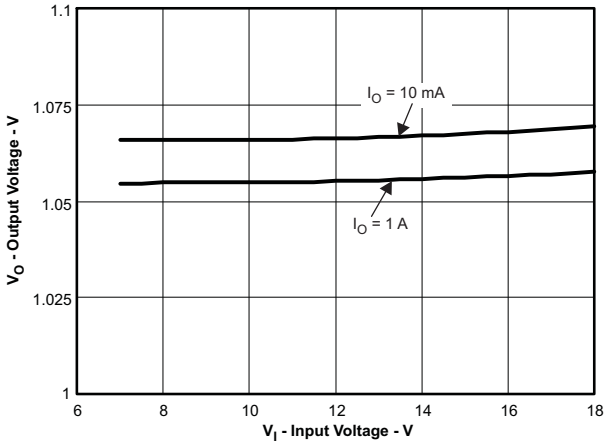


**Figure 5.**

**1.05V 50mA to 4A LOAD TRANSIENT RESPONSE**

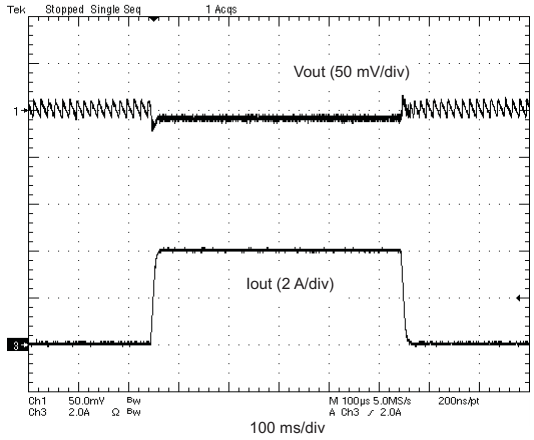


**Figure 6.**


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## TYPICAL CHARACTERISTICS (continued)

**STARTUP WAVEFORM**

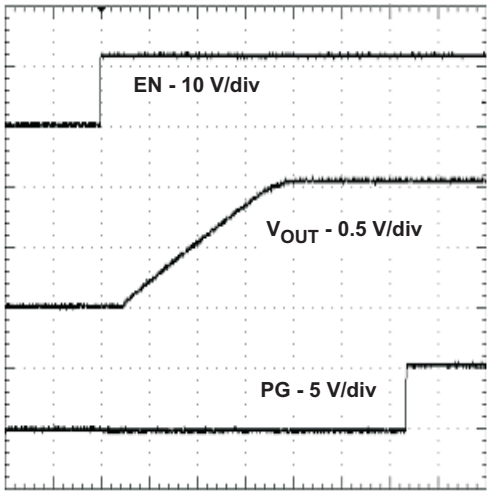


**Figure 7.**

**EFFICIENCY vs OUTPUT CURRENT**

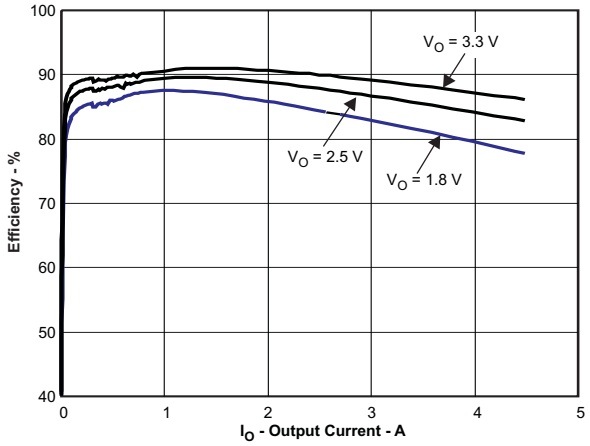


**Figure 8.**

**LIGHT LOAD EFFICIENCY vs OUTPUT CURRENT**

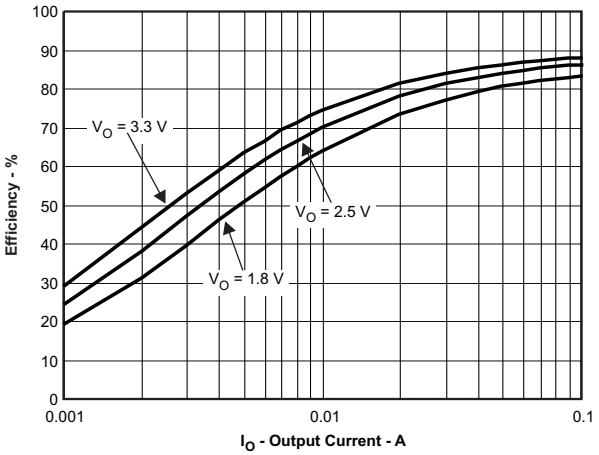


**Figure 9.**

**SWITCHING FREQUENCY vs INPUT VOLTAGE (IO=1A)**

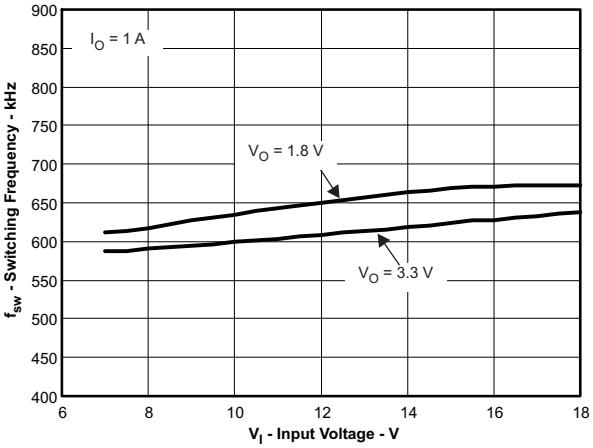


**Figure 10.**

## TYPICAL CHARACTERISTICS (continued)

**SWITCHING FREQUENCY VS OUTPUT CURRENT**

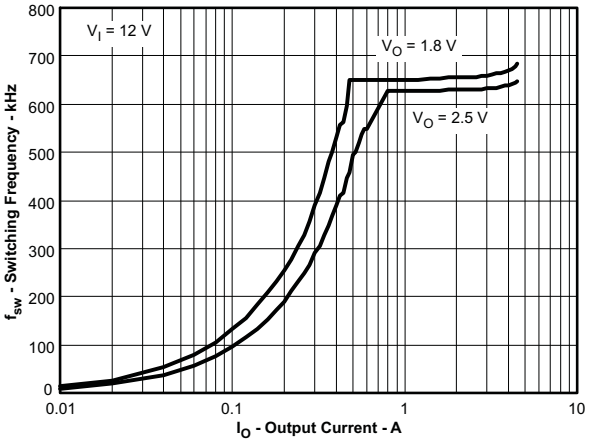


**Figure 11.**

**VOLTAGE RIPPLE AT OUTPUT (IO=4A)**

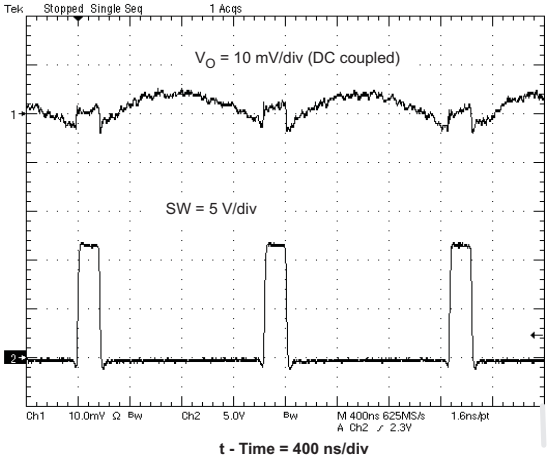


**Figure 12.**

**VOLTAGE RIPPLE AT INPUT (IO=4A)**

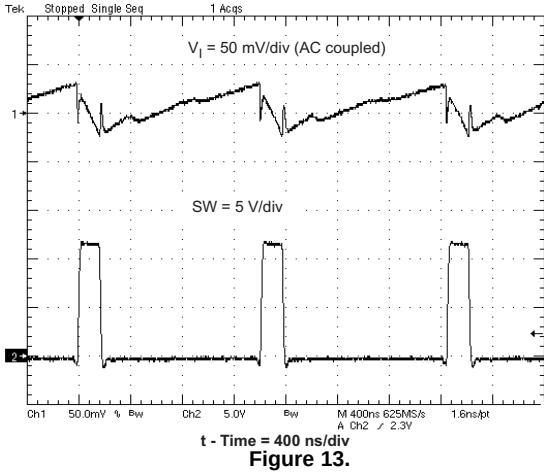


**Figure 13.**


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## DESIGN GUIDE

### Step By Step Design Procedure

To begin the design process, you must know a few application parameters:

- Input voltage range
- Output voltage
- Output current
- Output voltage ripple
- Input voltage ripple

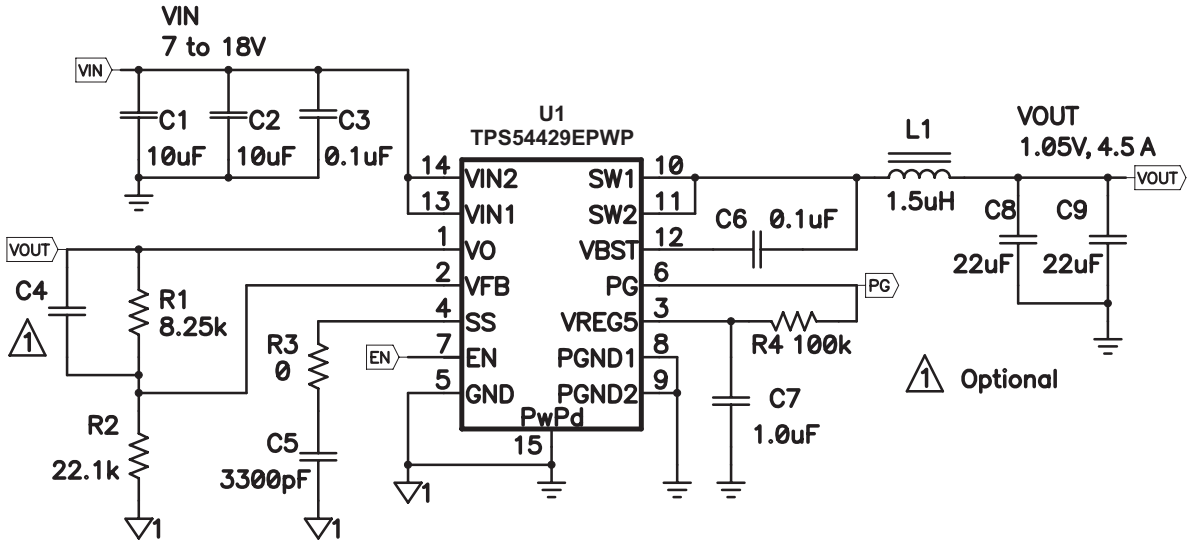


**Figure 14. Schematic Diagram for This Design Example**

### Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. It is recommended to use 1% tolerance or better divider resistors. Start by using Equation 3 and Equation 4 to calculate $V_{OUT}$

To improve efficiency at very light loads consider using larger value resistors, too high of resistance will be more susceptible to noise and voltage errors from the VFB input current will be more noticeable

For output voltage from 0.76 V to 2.5 V:

$$V_{OUT} = 0.765 \bullet \left(1 + \frac{R1}{R2}\right) \tag{3}$$

For output voltage over 2.5 V:

$$V_{OUT} = (0.763 + 0.0017 \bullet V_{OUT\_SET}) \bullet \left(1 + \frac{R1}{R2}\right) \tag{4}$$

Where:

$V_{OUT\_SET}$ = Target $V_{OUT}$ voltage

### Output Filter Selection

The output filter used with the TPS54429E is an LC circuit. This LC filter has double pole at:

$$F_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \tag{5}$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS54429E. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a -40 dB per decade rate and the phase drops rapidly. D-CAP2™ introduces a high frequency zero that reduces the gain roll off to -20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor selected for the output filter must be selected so that the double pole of Equation 5 is located below the high frequency zero but close enough that the phase boost provided be the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in Table 1

**Table 1. Recommended Component Values**

| Output Voltage (V) | R1 (kΩ) | R2 (kΩ) | C4 (pF)(1) | L1 (µH) | C8 + C9 (µF) |
|---|---|---|---|---|---|
| 1 | 6.81 | 22.1 | | 1.5 | 22 - 68 |
| 1.05 | 8.25 | 22.1 | | 1.5 | 22 - 68 |
| 1.2 | 12.7 | 22.1 | | 1.5 | 22 - 68 |
| 1.5 | 23.2 | 22.1 | | 1.5 | 22 - 68 |
| 1.8 | 30.1 | 22.1 | 10 - 22 | 2.2 | 22 - 68 |
| 2.5 | 49.9 | 22.1 | 10 - 22 | 2.2 | 22 - 68 |
| 3.3 | 73.2 | 22.1 | 10 - 22 | 2.2 | 22 - 68 |
| 5 | 121 | 22.1 | 10 - 22 | 3.3 | 22 - 68 |

(1) Optional

For higher output voltages at or above 1.8 V, additional phase boost can be achieved by adding a feed forward capacitor (C4) in parallel with R1.

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using Equation 6, Equation 7 and Equation 8. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current. Use 700 kHz for $f_{SW}$.

$$Ilp\text{-}p = \frac{V_{OUT}}{V_{IN\,(max)}} \bullet \frac{V_{IN\,(max)} - V_{OUT}}{L_O \bullet f_{SW}} \tag{6}$$

$$I_{lpeak} = I_O + \frac{Ilp\text{-}p}{2} \tag{7}$$

$$I_{Lo(RMS)} = \sqrt{I_O^2 + \frac{1}{12} Ilp\text{-}p^2} \tag{8}$$

For this design example, the calculated peak current is 4.97A and the calculated RMS current is 4.508 A. The inductor used is a TDK SPM6530-1R5M100 with a peak current rating of 11.5 A and an RMS current rating of 11 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS54429E is intended for use with ceramic or other low ESR capacitors. Recommended values range from 22uF to 68uF. Use Equation 9 to determine the required RMS current rating for the output capacitor

$$I_{CO(RMS)} = \frac{V_{OUT} \bullet (V_{IN} - V_{OUT})}{\sqrt{12} \bullet V_{IN} \bullet L_O \bullet f_{SW}} \tag{9}$$

For this design two TDK C3216X5R0J226M 22uF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is .271A and each output capacitor is rated for 4A.

### Input Capacitor Selection

The TPS54429E requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A ceramic capacitor over 10 µF is recommended for the decoupling capacitor. An additional 0.1 µF capacitor from pin 14 to ground is recommended to improve the stability of the over-current limit function. The capacitor voltage rating needs to be greater than the maximum input voltage.


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### Bootstrap Capacitor Selection

A 0.1 µF ceramic capacitor must be connected between the VBST to SW pin for proper operation. It is recommended to use a ceramic capacitor.

### VREG5 Capacitor Selection

A 1.0 µF ceramic capacitor must be connected between the VREG5 to GND pin for proper operation. It is recommended to use a ceramic capacitor.

## THERMAL INFORMATION

This PowerPad™ package incorporates an exposed thermal pad that is designed to be directly to an external heatsink. The thermal pad must be soldered directly to the printed board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD™ package and how to use the advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD™ Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD™ Made Easy, Texas Instruments Literature No. SLMA004.

The exposed thermal pad dimensions for this package are shown in the following illustration.

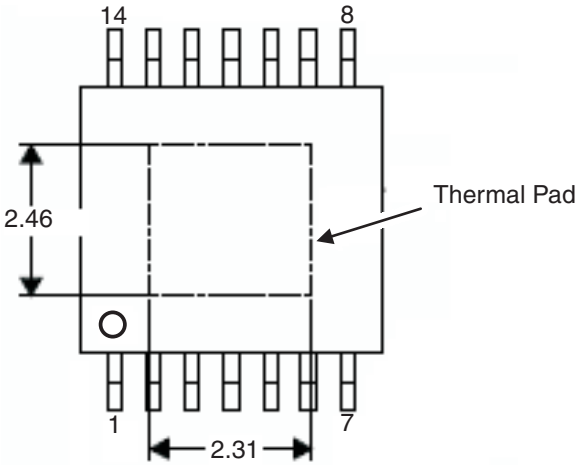


**Figure 15. Thermal Pad Dimensions**

## LAYOUT CONSIDERATIONS

1. Keep the input switching current loop as small as possible.
2. Keep the SW node as physically small and short as possible to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections should be brought from the output to the feedback pin of the device.
3. Keep analog and non-switching components away from switching components.
4. Make a single point connection from the signal ground to power ground.
5. Do not allow switching current to flow under the device.
6. Keep the pattern lines for VIN and PGND broad.
7. Exposed pad of device must be connected to PGND with solder.
8. VREG5 capacitor should be placed near the device, and connected PGND.
9. Output capacitor should be connected to a broad pattern of the PGND.
10. Voltage feedback loop should be as short as possible, and preferably with ground shield.
11. Lower resistor of the voltage divider which is connected to the VFB pin should be tied to SGND.
12. Providing sufficient via is preferable for VIN, SW and PGND connection.
13. PCB pattern for VIN, SW, and PGND should be as broad as possible.
14. VIN Capacitor should be placed as near as possible to the device.

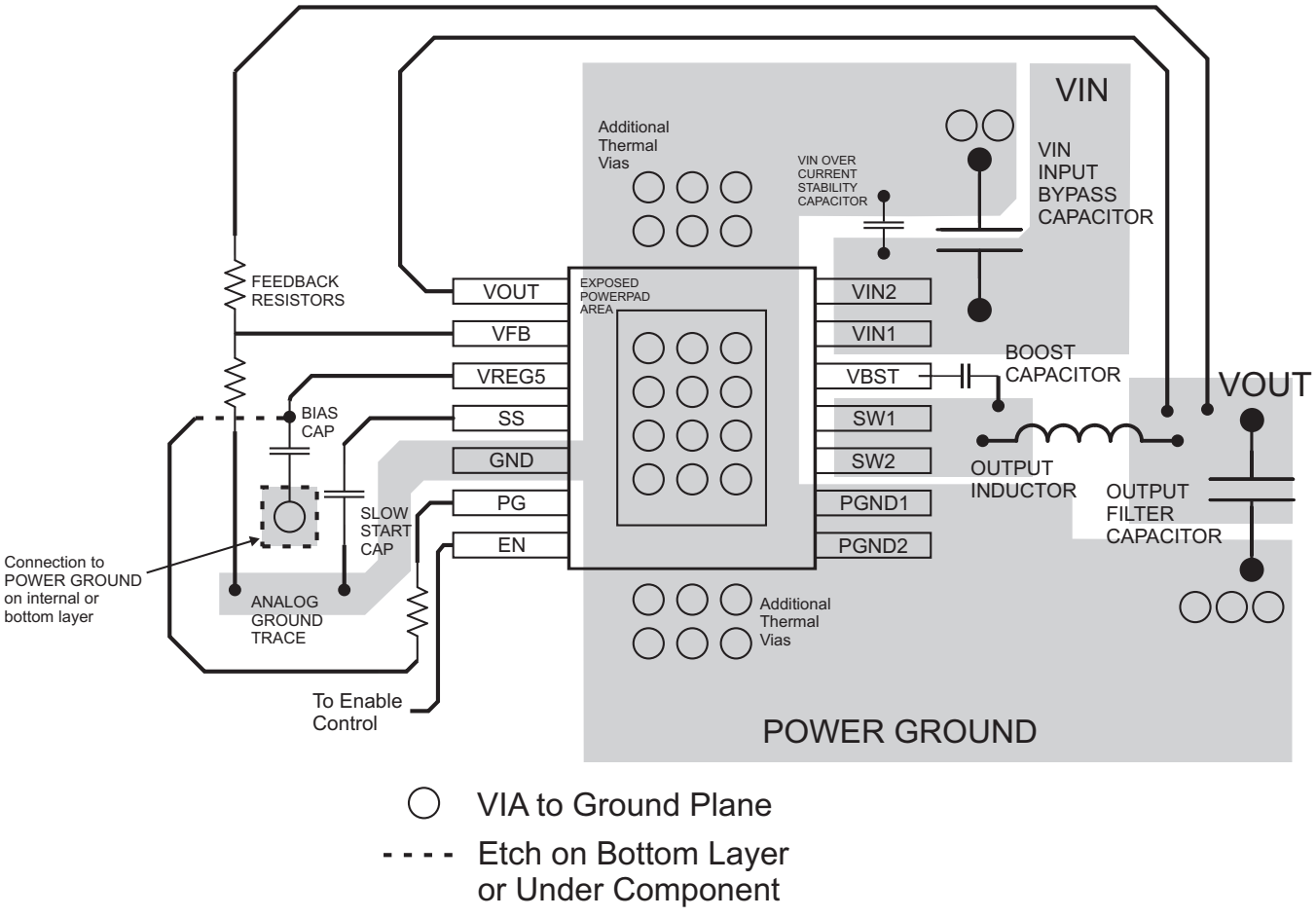


**Figure 16. PCB Layout**


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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS54429EPWP | ACTIVE | HTSSOP | PWP | 14 | | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -20 to 85 | 54429E | Samples |
| TPS54429EPWPR | ACTIVE | HTSSOP | PWP | 14 | 2000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -20 to 85 | 54429E | Samples |
| TPS54429ERSAR | ACTIVE | QFN | RSA | 16 | 3000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -20 to 85 | TPS 54429E | Samples |
| TPS54429ERSAT | ACTIVE | QFN | RSA | 16 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -20 to 85 | TPS 54429E | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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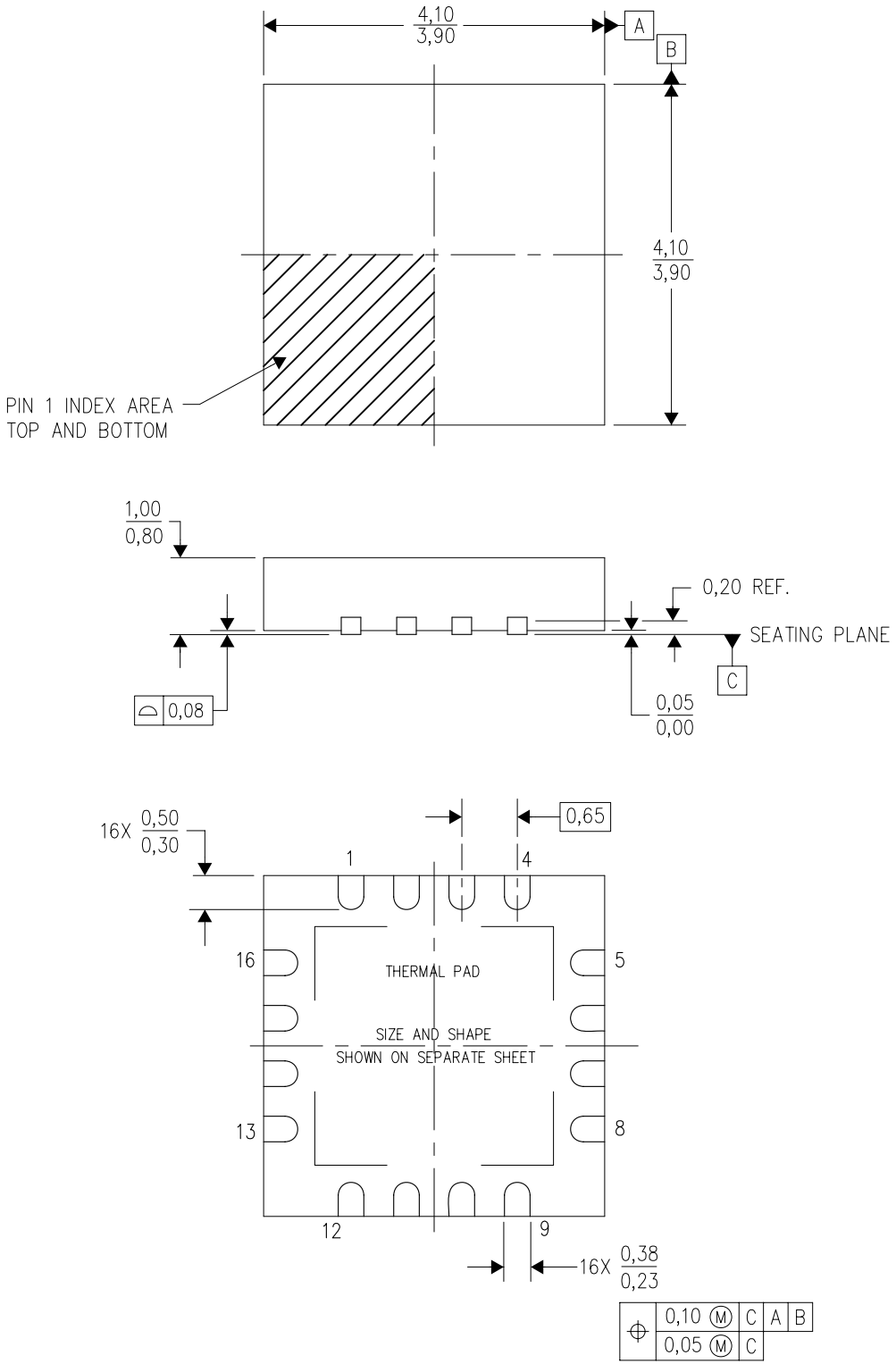
RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

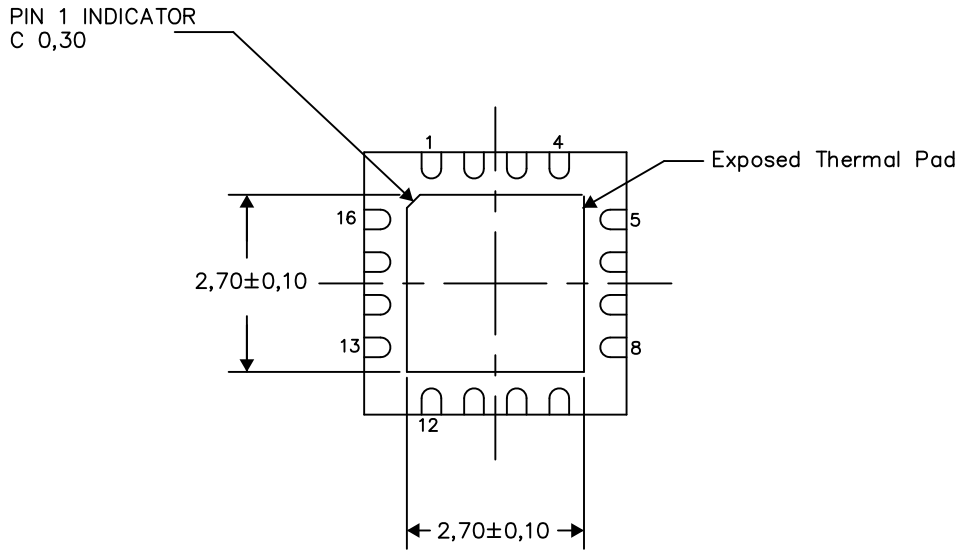
RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



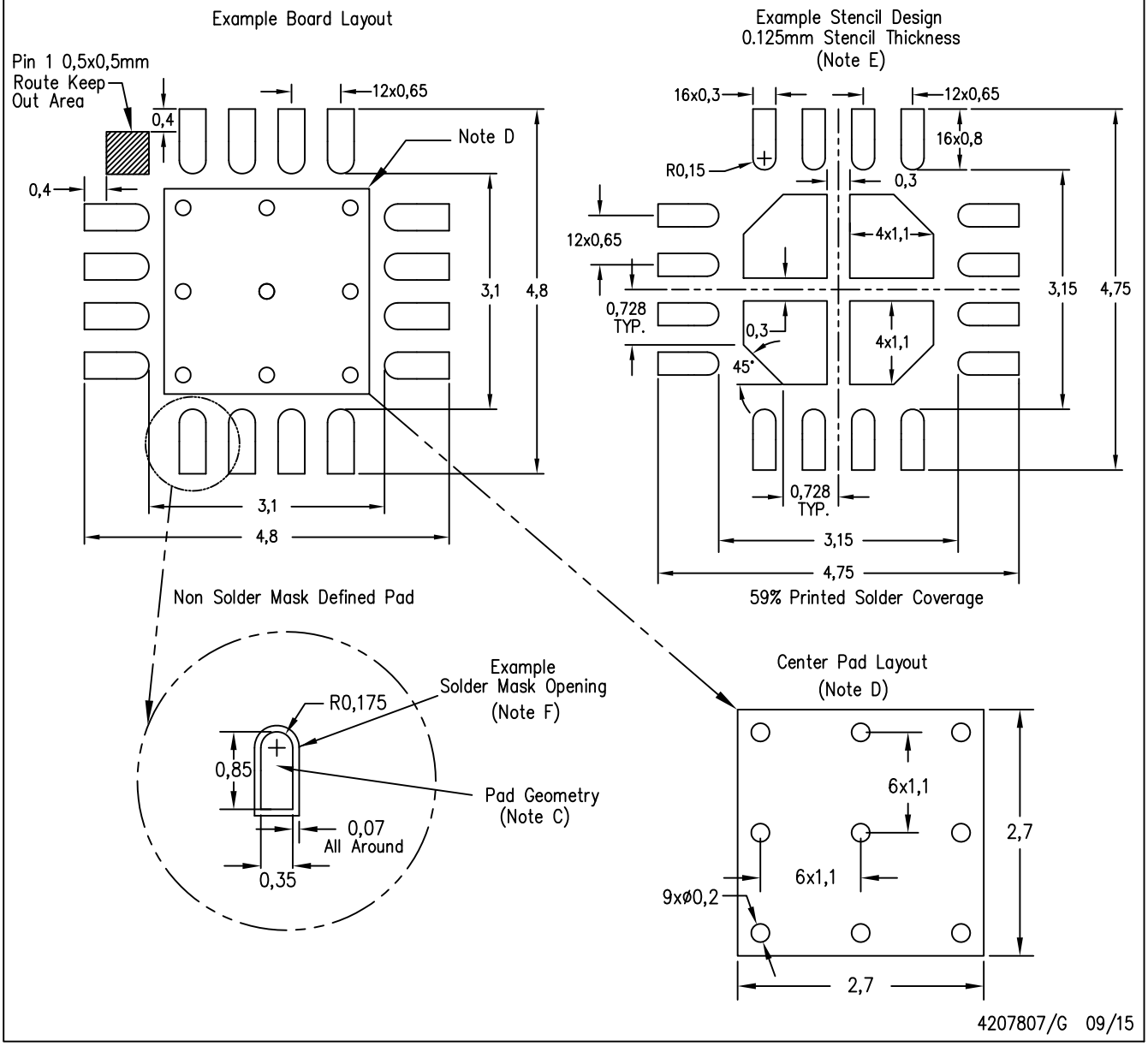

Bottom View

Exposed Thermal Pad Dimensions

4206364–2/0 09/15

NOTES:
A. All linear dimensions are in millimeters

# RSA (S–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

# GENERIC PACKAGE VIEW

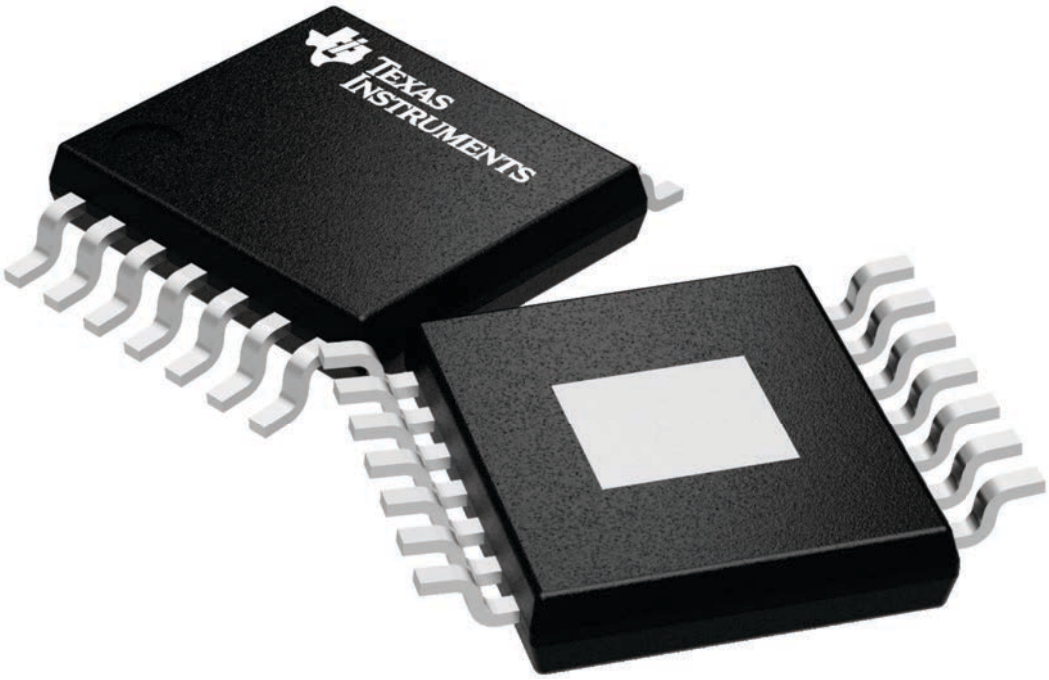
## PWP 14

## PowerPAD TSSOP - 1.2 mm max height

**4.4 x 5.0, 0.65 mm pitch**

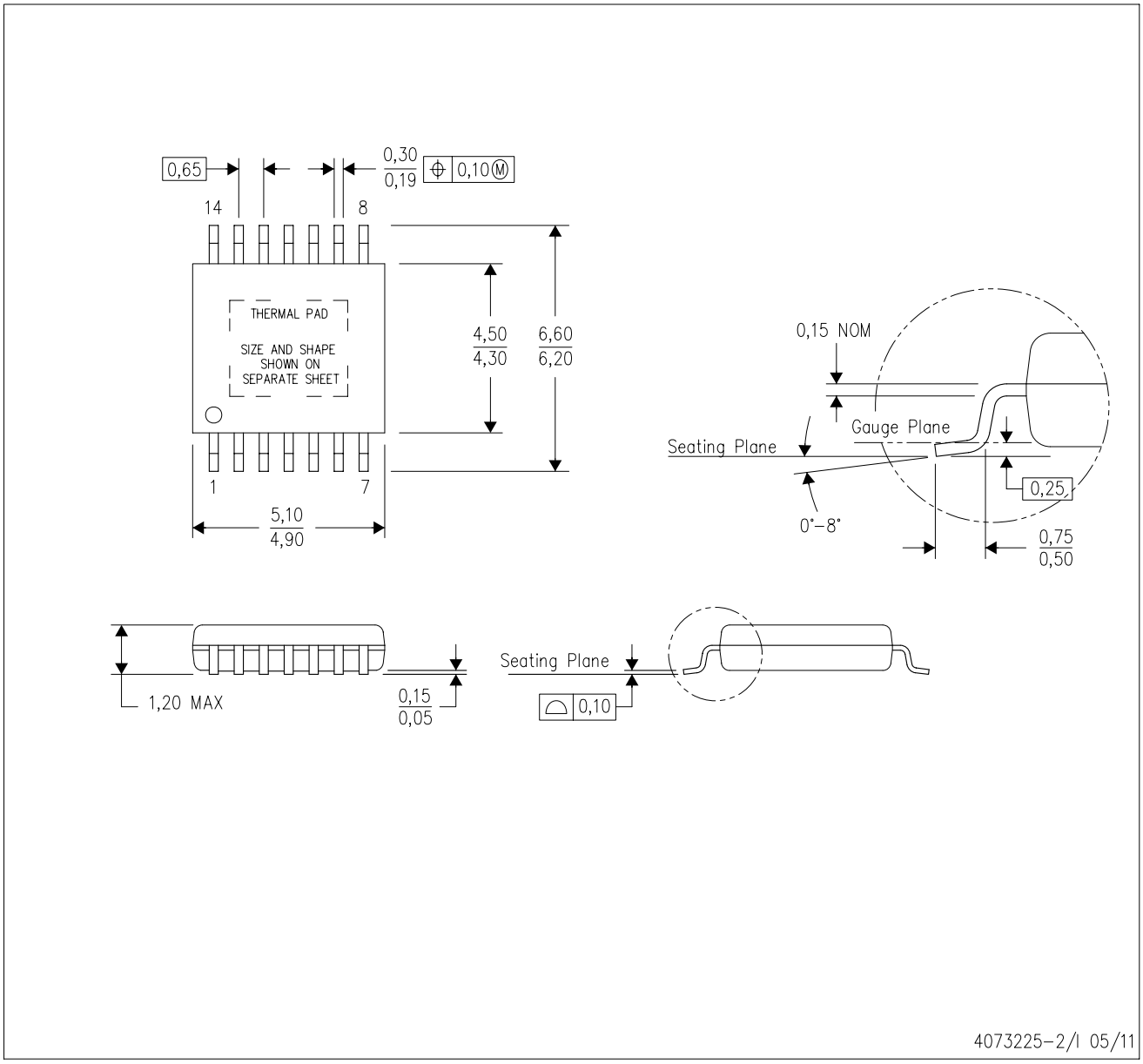
PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.




4224995/A

PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

**PowerPAD is a trademark of Texas Instruments.**

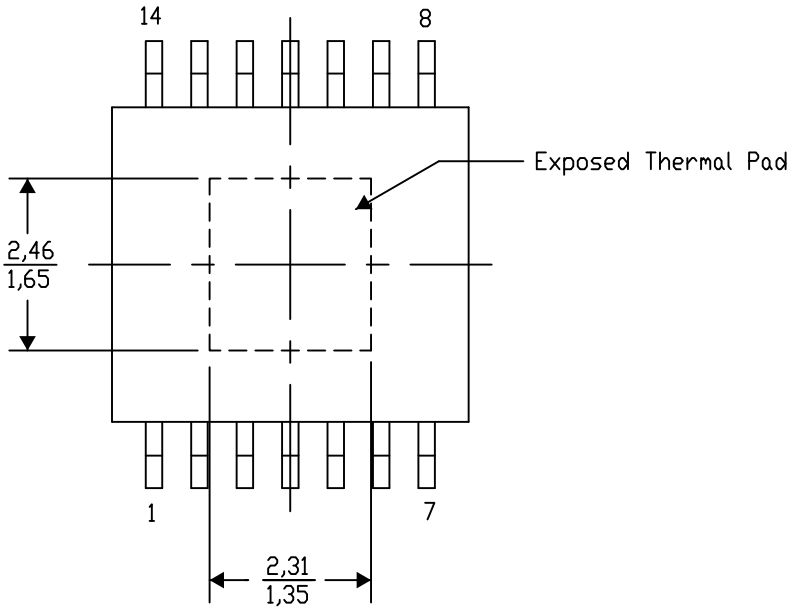
PWP (R–PDSO–G14) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.




Top View

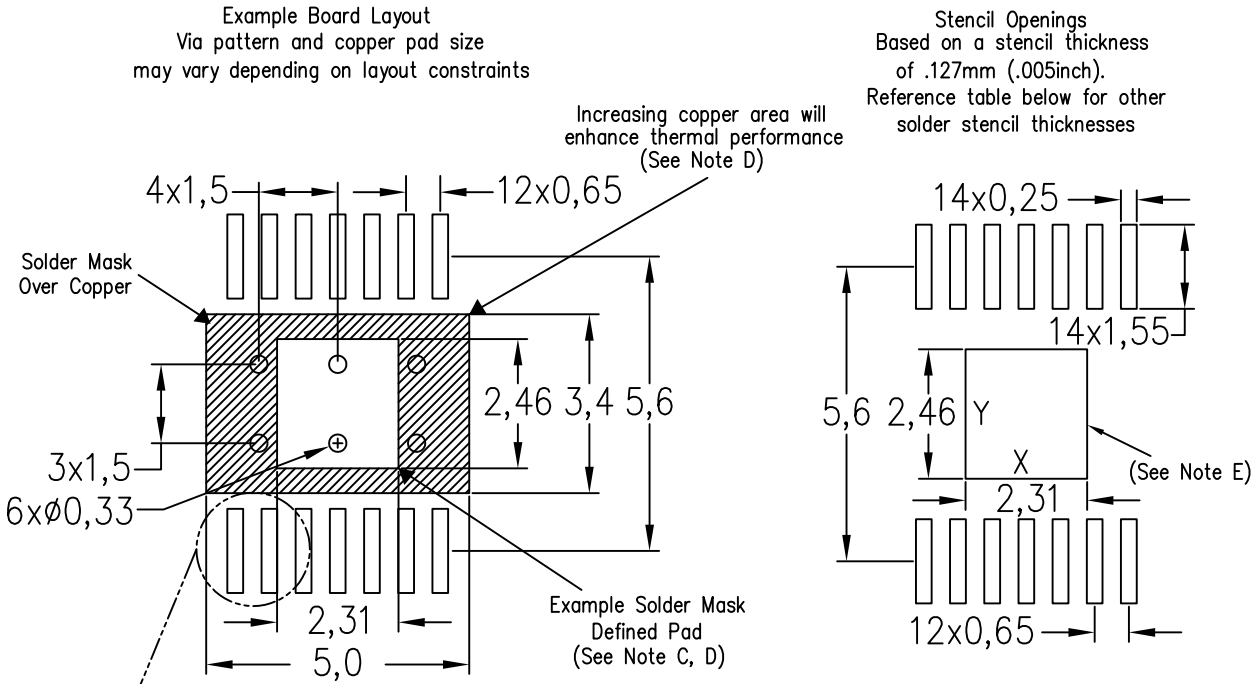
Exposed Thermal Pad Dimensions

4206332–2/AO 01/16

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

## PWP (R–PDSO–G14) PowerPAD™ PLASTIC SMALL OUTLINE




| Center Power Pad Solder Stencil Opening | | |
|---|---|---|
| Stencil Thickness | X | Y |
| 0.1mm | 2.5 | 2.65 |
| 0.127mm | 2.31 | 2.46 |
| 0.152mm | 2.15 | 2.3 |
| 0.178mm | 2.05 | 2.15 |

4207609–2/W 09/15

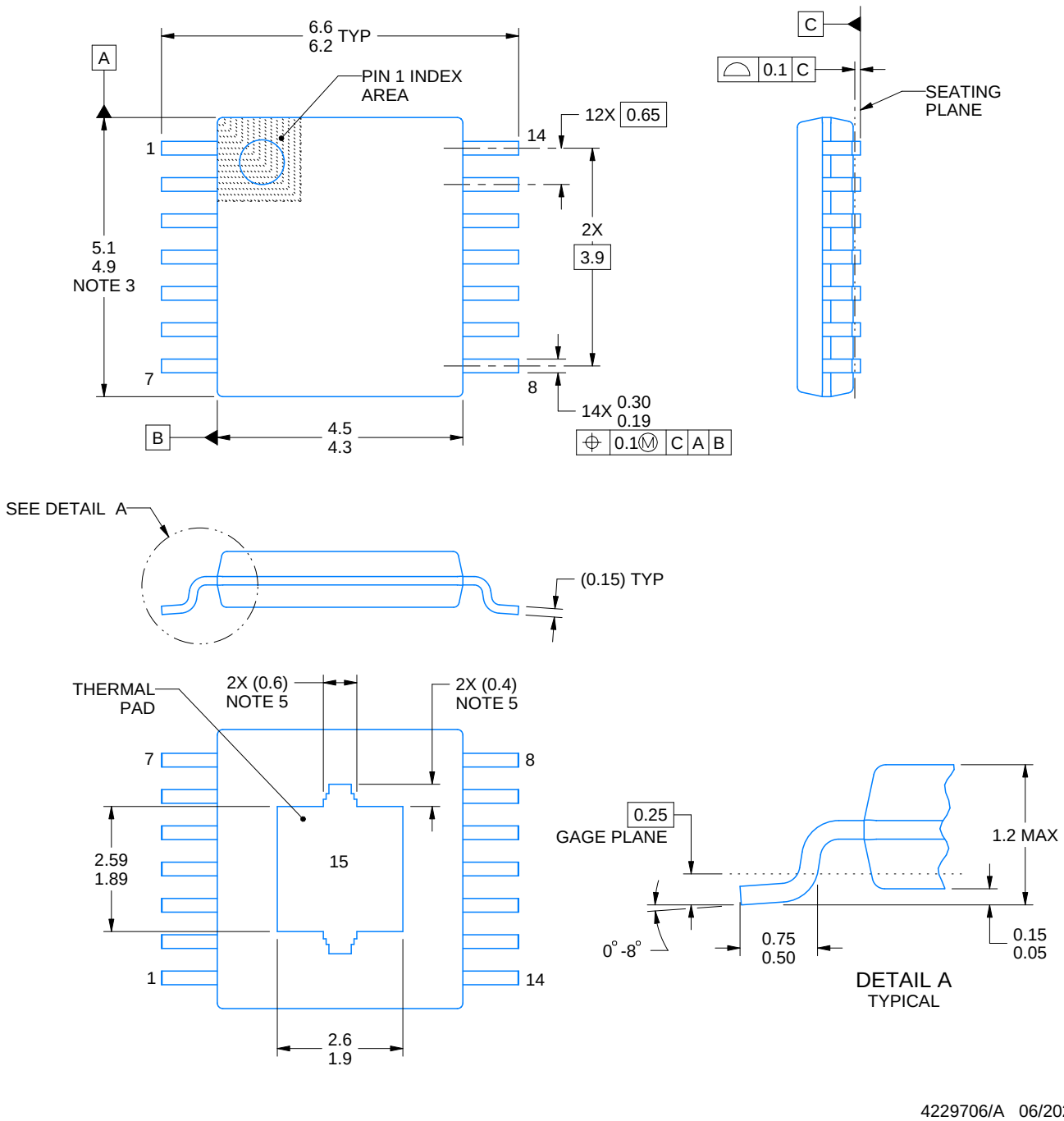
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# PACKAGE OUTLINE

## PWP0014K

## PowerPAD™ TSSOP - 1.2 mm max height

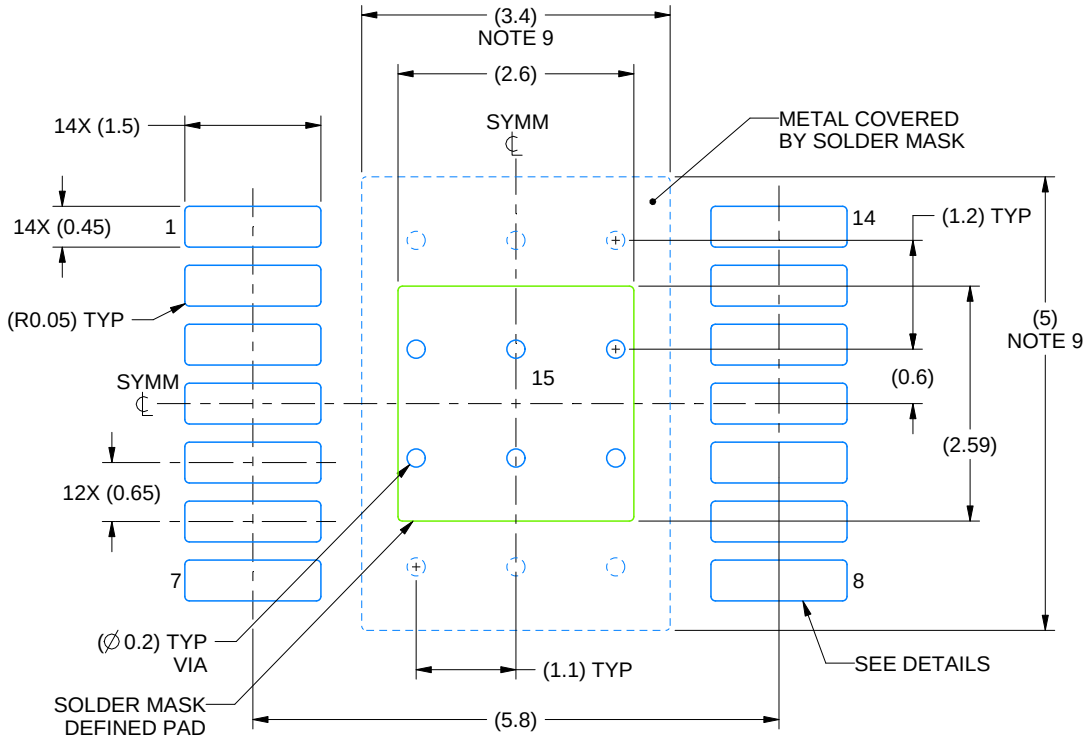
SMALL OUTLINE PACKAGE



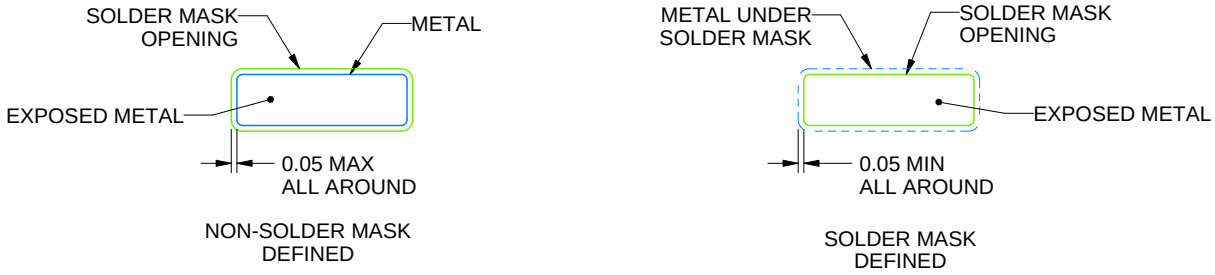

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 12X

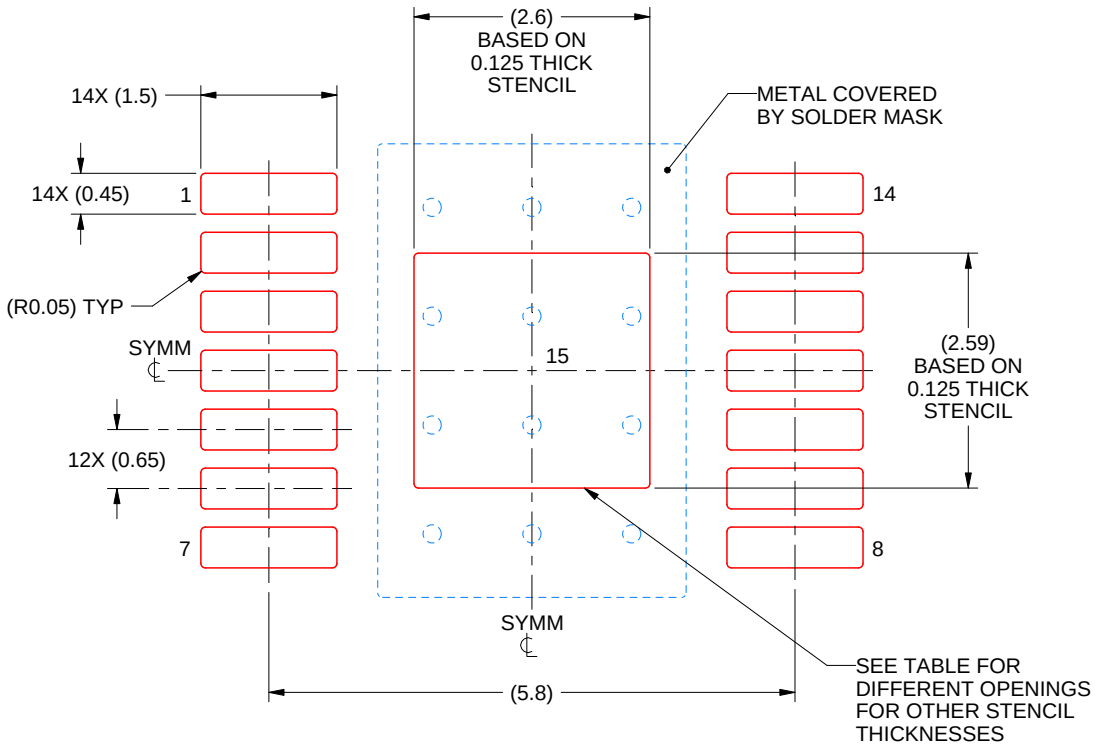



SOLDER MASK DETAILS

4229706/A 06/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 12X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 2.91 X 2.90 |
| 0.125 | 2.60 X 2.59 (SHOWN) |
| 0.15 | 2.37 X 2.36 |
| 0.175 | 2.20 X 2.19 |

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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