TPS54541 具有软启动和 Eco-mode™ 的 4.5V 至 42V 输入、5A、降压 DC-DC 转换器

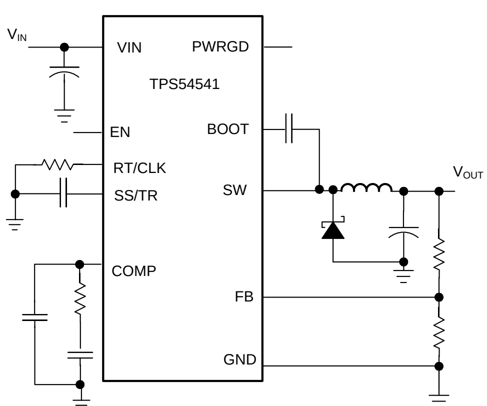
1 特性

- 轻负载条件下使用脉冲跳跃实现的高效率 Eco-mode。™
- 87mΩ 高侧金属氧化物半导体场效应晶体管 (MOSFET)
- 152μA 静态运行电流和 2μA 关断电流
- 100kHz 至 2.5MHz 可调开关频率
- 同步至外部时钟
- 轻负载条件下使用集成型引导 (BOOT) 再充电场效应晶体管 (FET) 实现的低压降
- 可调欠压闭锁 (UVLO) 电压和滞后
- 欠压 (UV) 和过压 (OV) 电源正常输出
- 可调软启动和定序
- 0.8V 1% 内部电压基准
- 带有散热焊盘的 10 引脚晶圆级小外形无引线 (WSON) 封装
- T_J 运行范围为 -40°C 至 150°C
- 使用 TPS54541 并借助 WEBENCH Power Designer 创建定制设计方案

2 应用

- 工业自动化和电机控制
- 车辆附件：全球卫星定位 (GPS)（请参见 SLVA412），娱乐系统
- USB 专用充电端口和电池充电器（请参见 SLVA464）
- 12V 和 24V 工业、汽车和通信电源系统

简化电路原理图



3 说明

TPS54541 器件是一款 42V 5A 降压型稳压器，此稳压器具有一个集成型高侧 MOSFET。按照 ISO 7637 标准，此器件能够耐受高达 45V 的抛负载脉冲。电流模式控制提供了简单的外部补偿和灵活的组件选择。一个低纹波脉冲跳跃模式将无负载输出电源电流减小至 152μA。使能引脚下拉为低电平后，关断电源电流降至 2μA。

欠压闭锁在内部设定为 4.3V，但可用一个使能引脚上的外部电阻分压器将之提高。输出电压启动斜坡受控于软启动引脚，该引脚还可被配置用来控制电源排序和跟踪。一个开漏电源正常信号表示输出处于标称电压值的 93% 至 106% 之内。

宽可调开关频率范围可针对效率或者外部组件尺寸进行优化。逐周期电流限制、频率折返和热关断功能可在过载情况下保护内部和外部组件。

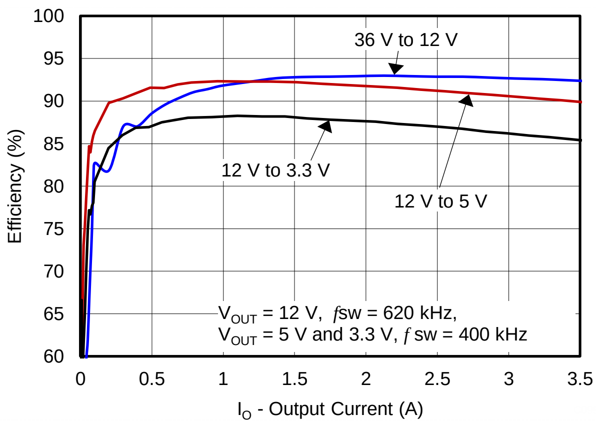
TPS54541 器件采用 10 引脚 4mm x 4mm WSON 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS54541	WSON (10)	4.00mm x 4.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

效率与负载电流间的关系



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (February 2016) to Revision C **Page**

- WEBENCH 信息至*特性*，*详细设计流程*和*器件支持部分* 1
- Changed Equation 10 and Equation 11 21
- Changed Equation 30 30
- Changed From: "power pad" To: "thermal pad" in the *Layout Guidelines* section 43

Changes from Revision A (August 2015) to Revision B **Page**

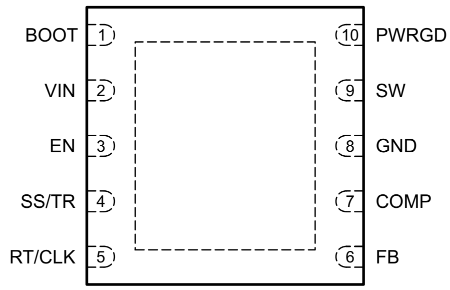
- Added: SW, 5-ns Transient to the Absolute Maximum Ratings 5
- Changed text in the *Application Information* From: "iterative design procedure" To: "interactive design procedure" 29

Changes from Original (October 2013) to Revision A **Page**

- 已添加 *ESD 额定值表，特性 描述部分，器件功能模式，应用和实施部分，电源相关建议部分，布局部分，器件和文档支持部分以及机械、封装和可订购信息部分* 1

5 Pin Configuration and Functions

DPR Package
10-Pin WSON With Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT	1	O	A bootstrap capacitor is required between BOOT and SW. If the voltage on this capacitor is below the minimum required to operate the high-side MOSFET, the gate drive is switched off until the capacitor is refreshed.
COMP	7	O	Error amplifier output and input to the output switch current (PWM) comparator. Connect frequency compensation components to this pin.
EN	3	I	Enable pin, with an internal pullup current source. Pull below 1.2 V to disable. Float to enable. Adjust the input undervoltage lockout with two resistors. See the *Enable and Adjusting Undervoltage Lockout* section.
FB	6	I	Inverting input of the transconductance (gm) error amplifier.
GND	8	–	Ground
PWRGD	10	O	Power Good is an open drain output that asserts low if the output voltage is out of regulation due to thermal shutdown, dropout, over-voltage or EN shut down.
RT/CLK	5	I	Resistor Timing and External Clock. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency. If the pin is pulled above the PLL upper threshold, a mode change occurs and the pin becomes a synchronization input. The internal amplifier is disabled and the pin is a high impedance clock input to the internal PLL. If clocking edges stop, the internal amplifier is re-enabled and the operating mode returns to resistor frequency programming.
SS/TR	4	I	Soft-start and Tracking. An external capacitor connected to this pin sets the output rise time. Because the voltage on this pin overrides the internal reference, SS/TR can be used for tracking and sequencing.
SW	9	O	The source of the internal high-side power MOSFET and switching node of the converter.
VIN	2	I	Input supply voltage with 4.5-V to 42-V operating range.
Thermal Pad	11	–	The GND pin must be electrically connected to the exposed pad on the printed circuit board for proper operation.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Voltage	VIN	–0.3	45	V
	EN	–0.3	8.4	
	BOOT–SW	–0.3	8	
	FB	–0.3	3	
	COMP	–0.3	3	
	PWRGD	–0.3	6	
	SS/TR	–0.3	3	
	RT/CLK	–0.3	3.6	
	SW	–0.6	45	
	SW, 5-ns Transient	–7	65	
	SW, 10-ns Transient	–2	45	
Operating junction temperature		–40	150	°C
Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VIN}	Supply input voltage	4.5		42	V
V_O	Output voltage	0.8		41.1	V
I_O	Output current	0		5	A
T_J	Operating junction temperature	–40		150	°C

6.4 Thermal Information

THERMAL METRIC[1][2]		TPS54541 DPR (WSON) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (standard board)	35.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	34.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	12.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	12.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	2.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Power rating at a specific ambient temperature T_A should be determined with a junction temperature of 150°C. This is the point where distortion starts to substantially increase. See *Power Dissipation Estimate* for more information.

6.5 Electrical Characteristics

T_J = –40°C to 150°C, VIN = 4.5 V to 42 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)					
Operating input voltage		4.5		42	V
Internal undervoltage lockout threshold	Rising	4.1	4.3	4.48	V
Internal undervoltage lockout threshold hysteresis			325		mV
Shutdown supply current	EN = 0 V, 25°C, 4.5 V ≤ VIN ≤ 42 V		2.25	4.5	µA
Operating: nonswitching supply current	FB = 0.9 V, T_A = 25°C		152	200	µA
ENABLE AND UVLO (EN PIN)					
Enable threshold voltage	No voltage hysteresis, rising and falling	1.1	1.2	1.3	V
Input current	Enable threshold +50 mV		–4.6		µA
Input current	Enable threshold –50 mV	–0.58	–1.2	-1.8	µA
Hysteresis current		–2.2	–3.4	-4.5	µA
Enable to COMP active	VIN = 12 V, T_A = 25°C		540		µs
VOLTAGE REFERENCE					
Voltage reference		0.792	0.8	0.808	V
HIGH-SIDE MOSFET					
On-resistance	VIN = 12 V, BOOT-SW = 6 V		87	185	mΩ
ERROR AMPLIFIER					
Input current			50		nA
Error amplifier transconductance (gm)	–2 µA < I_{COMP} < 2 µA, V_{COMP} = 1 V		350		µS
Error amplifier transconductance (gm) during soft-start	–2 µA < I_{COMP} < 2 µA, V_{COMP} = 1 V, V_{FB} = 0.4 V		77		µS
Error amplifier dc gain	V_{FB} = 0.8 V		10,000		V/V
Min unity gain bandwidth			2500		kHz
Error amplifier source/sink	$V_{(COMP)}$ = 1 V, 100 mV overdrive		±30		µA
COMP to SW current transconductance			17		A/V
CURRENT LIMIT					
Current limit threshold	All VIN and temperatures, Open Loop(1)	6.3	7.5	8.8	A
Current limit threshold	All temperatures, VIN = 12 V, Open Loop(1)	6.3	7.5	8.3	A
Current limit threshold	VIN = 12 V, T_A = 25°C, Open Loop(1)	7.1	7.5	7.9	A
Current limit threshold delay			60		ns
THERMAL SHUTDOWN					
Thermal shutdown			176		°C
Thermal shutdown hysteresis			12		°C
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)					
RT/CLK high threshold			1.55	2	V
RT/CLK low threshold		0.5	1.2		V
SOFT START AND TRACKING (SS/TR PIN)					
Charge current	$V_{SS/TR}$ = 0.4 V		1.7		µA
SS/TR-to-FB matching	$V_{SS/TR}$ = 0.4 V		42		mV
SS/TR-to-reference crossover	98% nominal		1.16		V
SS/TR discharge current (overload)	FB = 0 V, $V_{SS/TR}$ = 0.4 V		354		µA
SS/TR discharge voltage	FB = 0 V		54		mV
POWER GOOD (PWRGD PIN)					
FB threshold for PWRGD low	FB falling		90%		
FB threshold for PWRGD high	FB rising		93%		
FB threshold for PWRGD low	FB rising		108%		

(1) Open Loop current limit measured directly at the SW pin and is independent of the inductor value and slope compensation.

Electrical Characteristics (continued)

T_J = –40°C to 150°C, VIN = 4.5 V to 42 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
FB threshold for PWRGD high	FB falling		106%		
Hysteresis	FB falling		2.5%		
Output high leakage	V_{PWRGD} = 5.5 V, T_A = 25°C		10		nA
On resistance	I_{PWRGD} = 3 mA, V_{FB} < 0.79 V		45		Ω
Minimum VIN for defined output	V_{PWRGD} < 0.5 V, I_{PWRGD} = 100 µA		0.9	2	V

6.6 Timing Requirements

T_J = –40°C to 150°C, VIN = 4.5 V to 42 V (unless otherwise noted)

	MIN	NOM	MAX	UNIT
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)				
Minimum CLK input pulse width		15		ns
RT/CLK falling edge to SW rising edge delay – Measured at 500 kHz with RT resistor in series		55		ns

6.7 Switching Requirements

T_J = –40°C to 150°C, VIN = 4.5 V to 42 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)						
f_{SW}	Switching frequency	R_T = 200 kΩ	450	500	550	kHz
	Switching frequency range using RT mode		100		2500	kHz
	Switching frequency range using CLK mode		160		2300	kHz
	PLL lock in time	Measured at 500 kHz		78		µs

6.8 Typical Characteristics

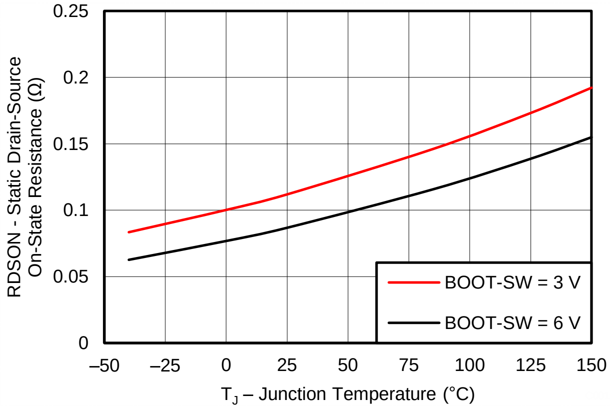


Figure 1. ON Resistance vs Junction Temperature

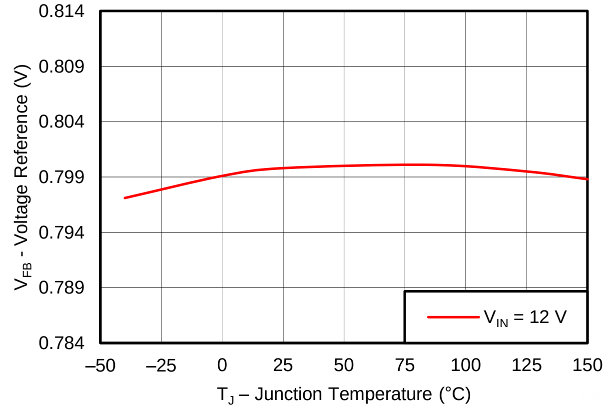


Figure 2. Voltage Reference vs Junction Temperature

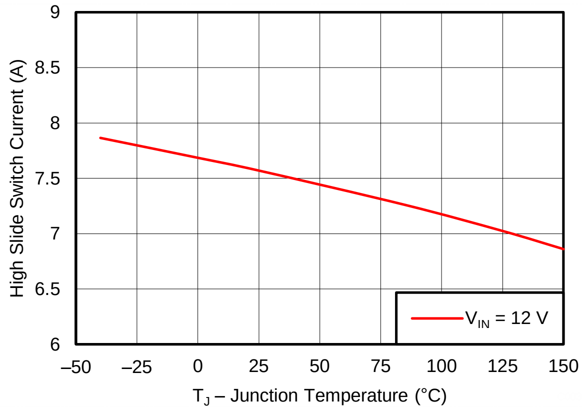


Figure 3. Switch Current Limit vs Junction Temperature

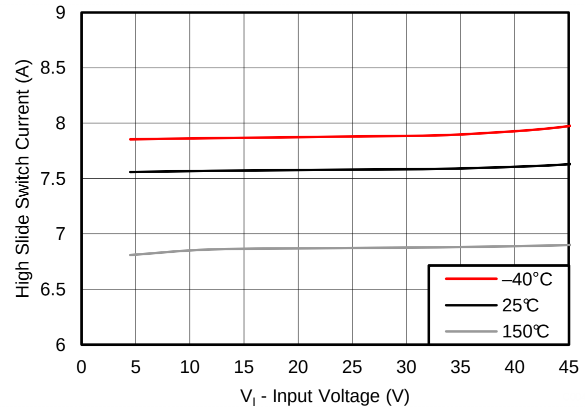


Figure 4. Switch Current Limit vs Input Voltage

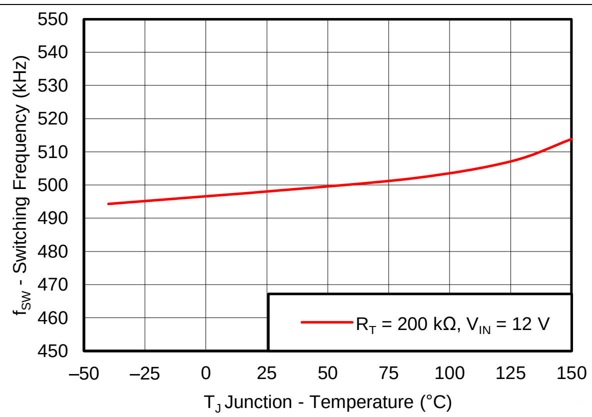


Figure 5. Switching Frequency vs Junction Temperature

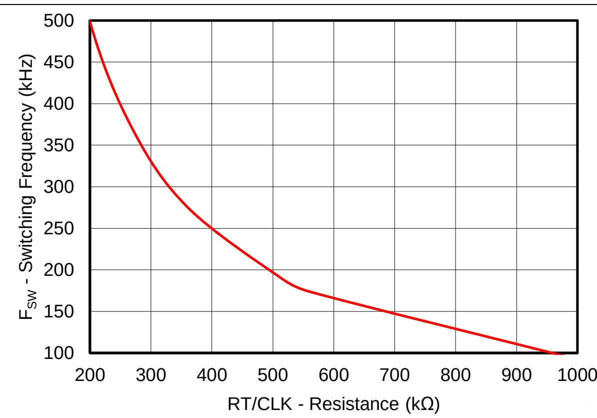


Figure 6. Switching Frequency vs RT/CLK Resistance Low Frequency Range

Typical Characteristics (continued)

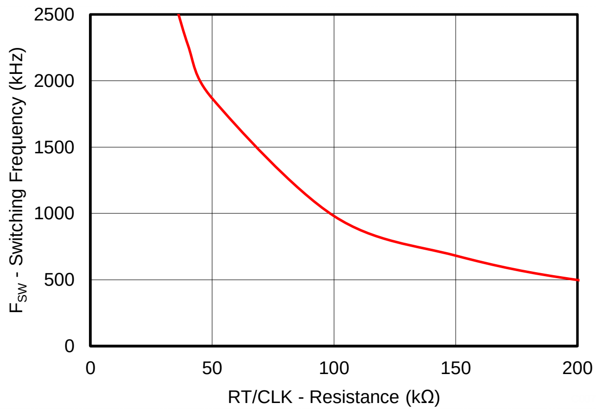


Figure 7. Switching Frequency vs RT/CLK Resistance High Frequency Range

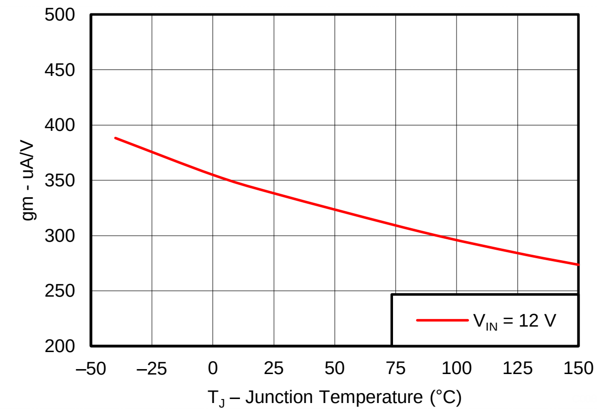


Figure 8. EA Transconductance vs Junction Temperature

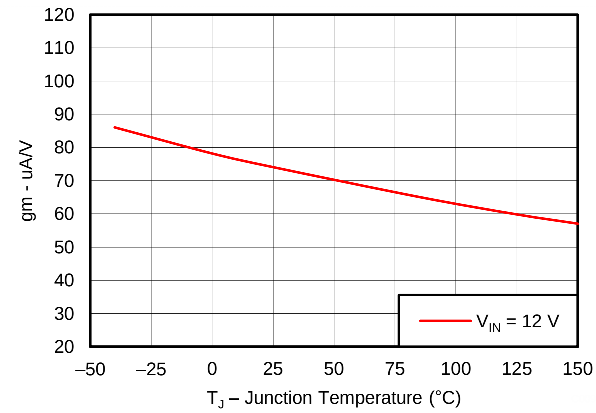


Figure 9. EA Transconductance During Soft-Start vs Junction Temperature

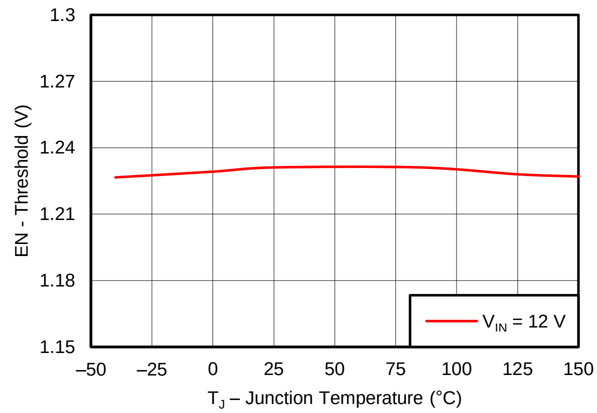


Figure 10. EN Pin Voltage vs Junction Temperature

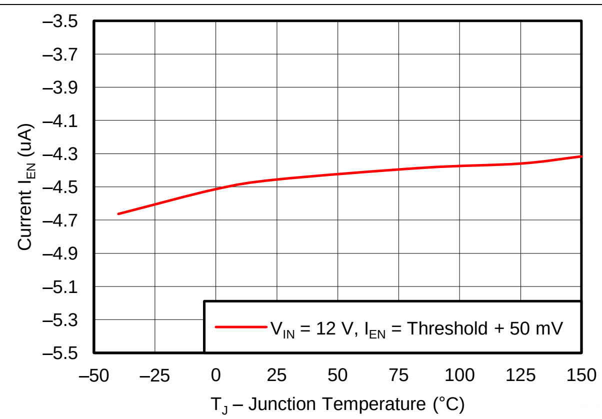


Figure 11. EN Pin Current vs Junction Temperature

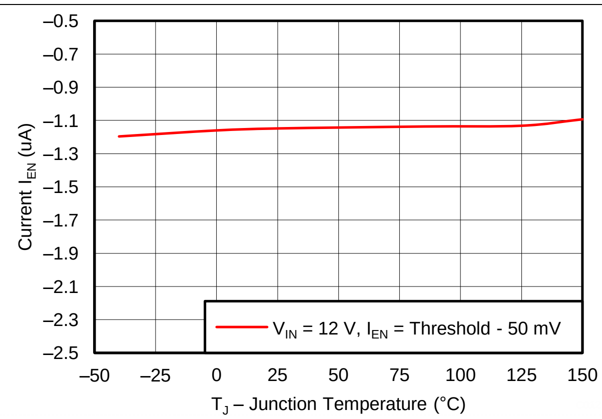


Figure 12. EN Pin Current vs Junction Temperature

Typical Characteristics (continued)

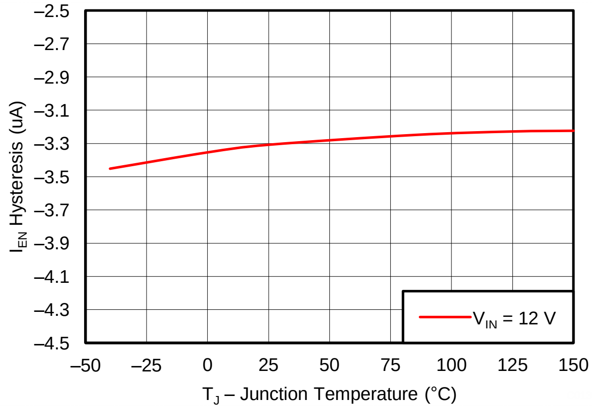


Figure 13. EN Pin Current Hysteresis vs Junction Temperature

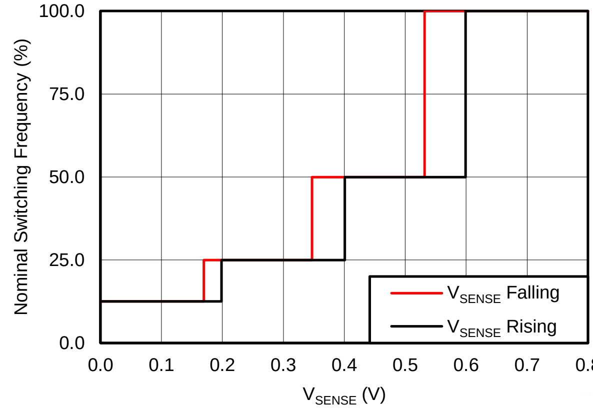


Figure 14. Switching Frequency vs FB

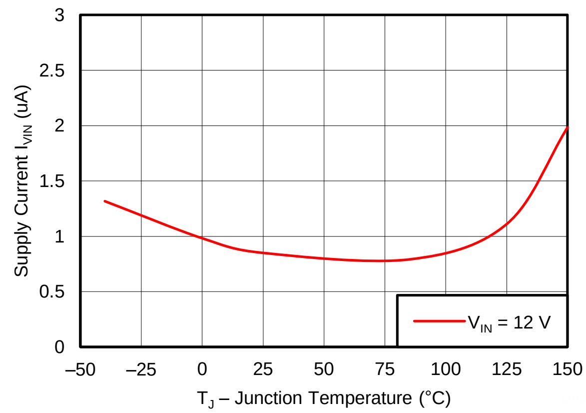


Figure 15. Shutdown Supply Current vs Junction Temperature

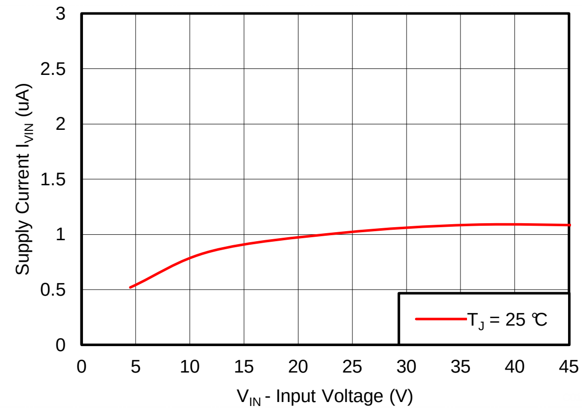


Figure 16. Shutdown Supply Current vs Input Voltage (VIN)

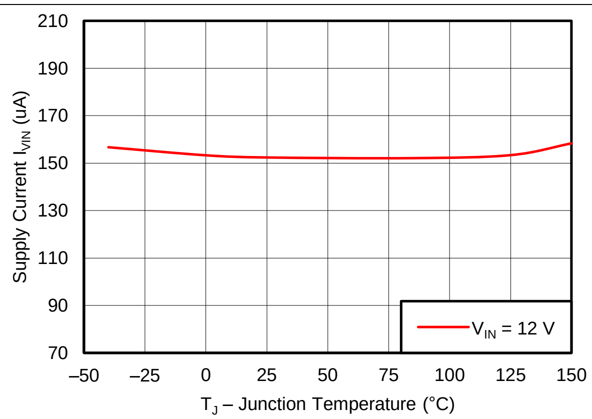


Figure 17. VIN Supply Current vs Junction Temperature

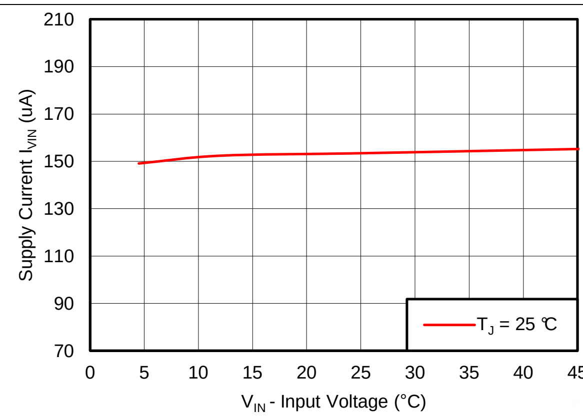


Figure 18. VIN Supply Current vs Input Voltage

Typical Characteristics (continued)

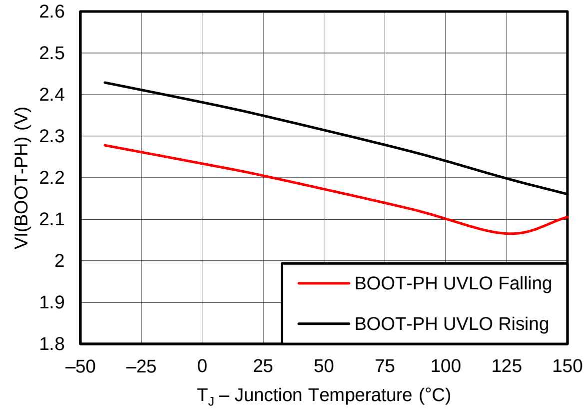


Figure 19. BOOT-SW UVLO vs Junction Temperature

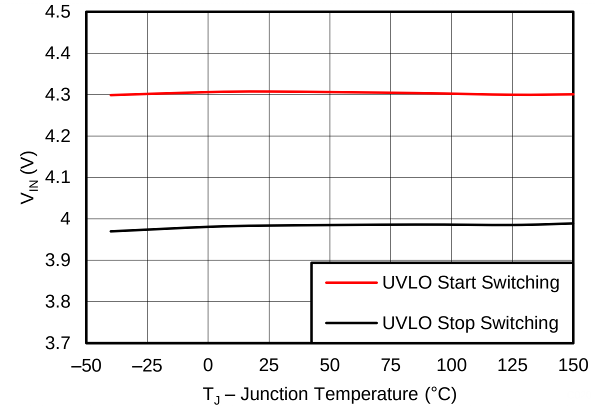


Figure 20. Input Voltage UVLO vs Junction Temperature

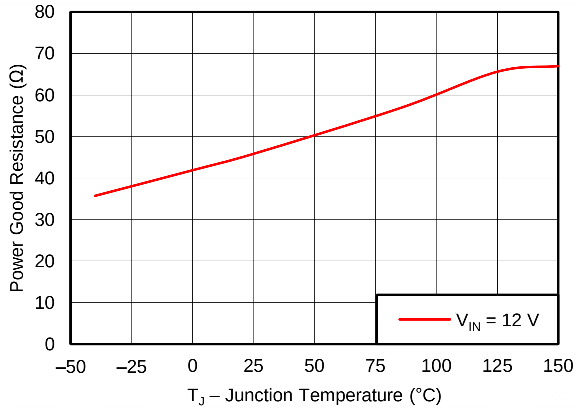


Figure 21. PWRGD ON Resistance vs Junction Temperature

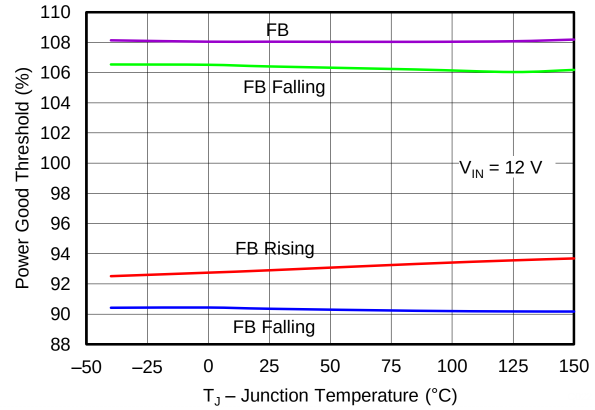


Figure 22. PWRGD Threshold vs Junction Temperature

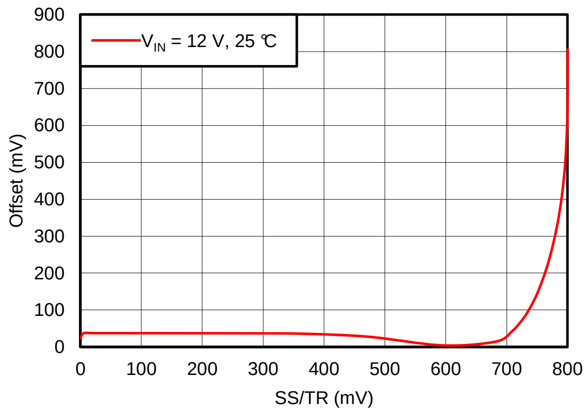


Figure 23. SS/TR to FB Offset vs FB

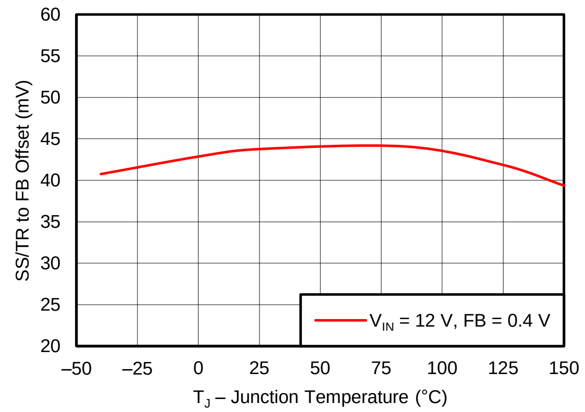


Figure 24. SS/TR to FB Offset vs Temperature

Typical Characteristics (continued)

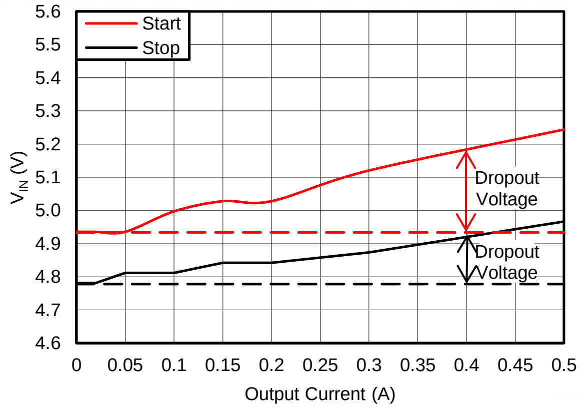


Figure 25. 5-V Start and Stop Voltage
(see *Low Dropout Operation and Bootstrap Voltage (BOOT)*)

7 Detailed Description

7.1 Overview

The TPS54541 is a 42-V 5-A, step-down (buck) regulator with an integrated high-side n-channel MOSFET. The device implements constant-frequency current-mode control which reduces output capacitance and simplifies external frequency compensation. The wide switching frequency range of 100 to 2500 kHz allows for either efficiency or size optimization when selecting the output filter components. The switching frequency is adjusted using a resistor to ground connected to the RT/CLK pin. The device has an internal phase-locked loop (PLL) connected to the RT/CLK pin that synchronizes the power switch turn-on to a falling edge of an external clock signal.

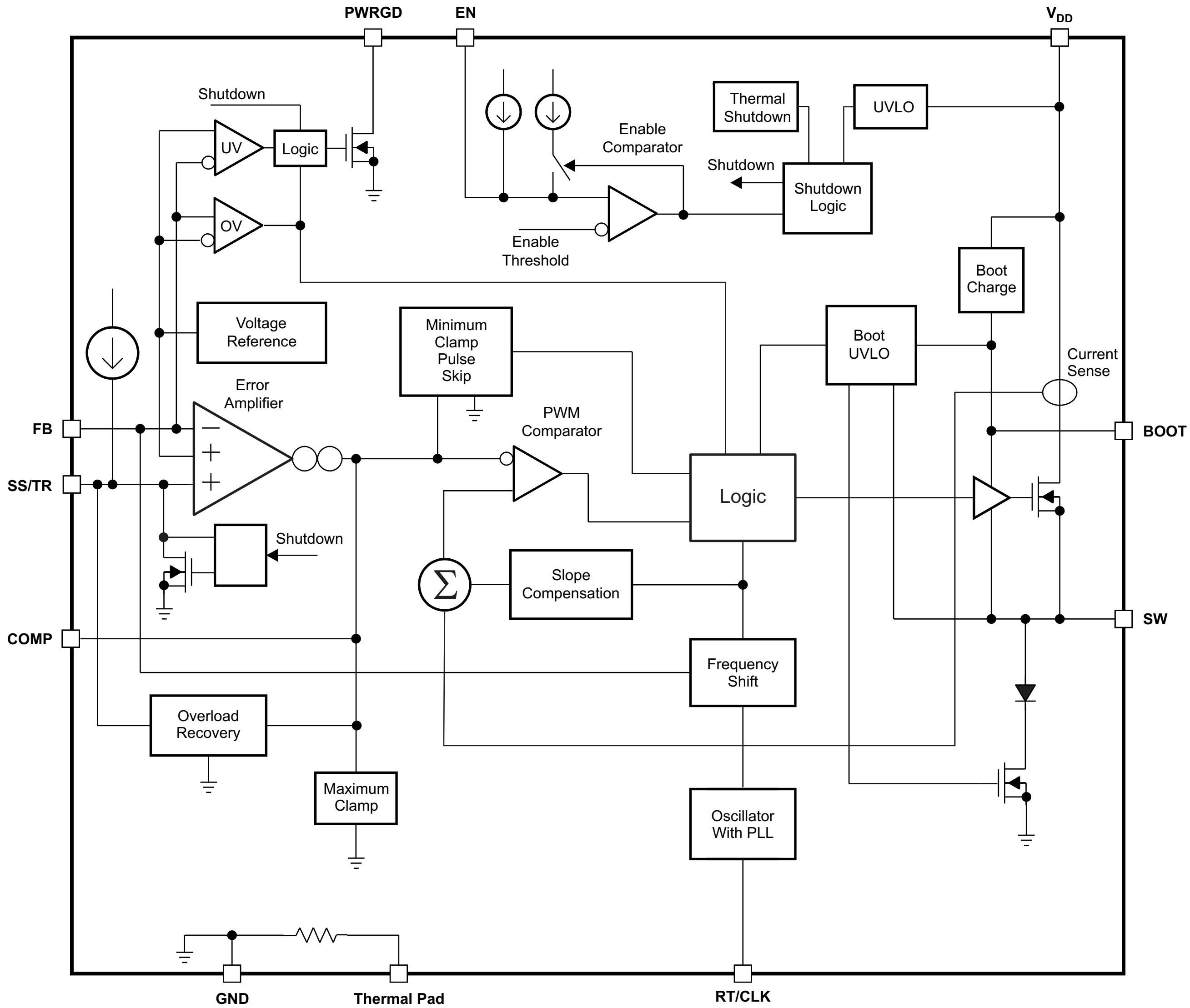
The TPS54541 device has a default input start-up voltage of 4.3 V typical. The EN pin adjusts the input-voltage undervoltage-lockout (UVLO) threshold with two external resistors. An internal-pullup current source enables operation when the EN pin is floating. The operating current is 152 μA under a no-load condition when not switching. When the device is disabled, the supply current is 2 μA.

The integrated 87-mΩ high-side MOSFET supports high-efficiency power-supply designs capable of delivering 5 A of continuous current to a load. The gate-drive bias voltage for the integrated high-side MOSFET is supplied by a bootstrap capacitor connected from the BOOT to SW pins. The TPS54541 device reduces the external component count by integrating the bootstrap recharge diode. The BOOT pin capacitor voltage is monitored by a UVLO circuit which turns off the high-side MOSFET when the BOOT to SW voltage falls below a preset threshold. An automatic BOOT capacitor recharge circuit allows the TPS54541 device to operate at high duty cycles approaching 100%. Therefore, the maximum output voltage is near the minimum input supply voltage of the application. The minimum output voltage is the internal 0.8-V feedback reference.

Output overvoltage transients are minimized by an overvoltage protection (OVP) comparator. When the OVP comparator is activated, the high-side MOSFET turns off and remains off until the output voltage is less than 106% of the desired output voltage.

The SS/TR (soft-start/tracking) pin minimizes inrush currents or provides power-supply sequencing during power up. A small value capacitor must be connected to the pin to adjust the soft-start time. A resistor divider can be connected to the pin for critical power supply sequencing requirements. The SS/TR pin is discharged before the output powers up. This discharging ensures a repeatable restart after an overtemperature fault, UVLO fault, or a disabled condition. When the overload condition is removed, the soft-start circuit controls the recovery from the fault output level to the nominal regulation voltage. A frequency-foldback circuit reduces the switching frequency during startup and overcurrent fault conditions to help maintain control of the inductor current.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Fixed-Frequency PWM Control

The TPS54541 device uses fixed-frequency peak-current-mode control with adjustable switching frequency. The output voltage is compared through external resistors connected to the FB pin to an internal voltage reference by an error amplifier. An internal oscillator initiates the turn-on of the high-side power switch. The error amplifier output at the COMP pin controls the high-side power switch current. When the high-side MOSFET switch current reaches the threshold level set by the COMP voltage, the power switch turns off. The COMP pin voltage increases and decreases as the output current increases and decreases. The device implements current limiting by clamping the COMP pin voltage to a maximum level. The pulse skipping Eco-mode is implemented with a minimum voltage clamp on the COMP pin.

7.3.2 Slope Compensation Output Current

The TPS54541 device adds a compensating ramp to the MOSFET switch current-sense signal. This slope compensation prevents sub-harmonic oscillations at duty cycles greater than 50%. The peak current limit of the high-side switch is not affected by the slope compensation and remains constant over the full duty-cycle range.

Feature Description (continued)

7.3.3 Pulse Skip Eco-mode

The TPS54541 device operates in a pulse-skipping Eco-mode at light-load currents to improve efficiency by reducing switching and gate drive losses. If the output voltage is within regulation and the peak switch current at the end of any switching cycle is below the pulse-skipping current threshold, the device enters Eco-mode. The pulse-skipping current threshold is the peak switch-current level corresponding to a nominal COMP voltage of 600 mV.

When in Eco-mode, the COMP pin voltage is clamped at 600 mV and the high-side MOSFET is inhibited. Because the device is not switching, the output voltage begins to decay. The voltage-control loop responds to the falling output voltage by increasing the COMP pin voltage. The high-side MOSFET is enabled and switching resumes when the error amplifier lifts COMP above the pulse skipping threshold. The output voltage recovers to the regulated value, and COMP eventually falls below the Eco-mode pulse-skipping threshold at which time the device again enters Eco-mode. The internal PLL remains operational when in Eco-mode. When operating at light load currents in Eco-mode, the switching transitions occur synchronously with the external clock signal.

During Eco-mode operation, the TPS54541 device senses and controls peak switch current, not the average load current. Therefore the load current at which the device enters Eco-mode is dependent on the output inductor value. As the load current approaches zero, the device enters a pulse skip mode during which it draws only 152-μA input quiescent current. The circuit in Figure 46 enters Eco-mode at about 18-mA output current and with no external load has an average input current of 260 μA.

7.3.4 Low Dropout Operation and Bootstrap Voltage (BOOT)

The TPS54541 device provides an integrated bootstrap voltage regulator. A small capacitor between the BOOT and SW pins provides the gate-drive voltage for the high-side MOSFET. The BOOT capacitor refreshes when the high-side MOSFET is off and the external low-side diode conducts. The recommended value of the BOOT capacitor is 0.1 μF. TI recommends a ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher for stable performance over temperature and voltage.

When operating with a low voltage difference from input to output, the high-side MOSFET of the TPS54541 device operates at 100% duty cycle as long as the BOOT to SW pin voltage is greater than 2.1 V. When the voltage from BOOT to SW drops below 2.1 V, the high-side MOSFET turns off and an integrated low-side MOSFET pulls SW low to recharge the BOOT capacitor. To reduce the losses of the small low-side MOSFET at high output voltages, the low-side MOSFET is disabled at 24-V output and re-enabled when the output reaches 21.5 V.

Because the gate-drive current sourced from the BOOT capacitor is small, the high-side MOSFET remains on for many switching cycles before the MOSFET turns off to refresh the capacitor. Thus the effective duty cycle of the switching regulator can be high, approaching 100%. The effective duty cycle of the converter during dropout is mainly influenced by the voltage drops across the power MOSFET, the inductor resistance, the low-side diode voltage, and the printed circuit-board resistance.

The start and stop voltage for a typical 5-V output application is shown in Figure 25 where the input voltage is plotted versus load current. The start voltage is defined as the input voltage required to regulate the output within 1% of nominal. The stop voltage is defined as the input voltage at which the output drops by 5% or where switching stops.

During high duty-cycle (low dropout) conditions, the inductor current ripple increases when the BOOT capacitor recharges resulting in an increase in output voltage ripple. Increased ripple occurs when the off-time required to recharge the BOOT capacitor is longer than the high-side off-time associated with cycle-by-cycle PWM control.

Feature Description (continued)

At heavy loads, the minimum input voltage must increase to ensure a monotonic start-up. Use Equation 1 to calculate the minimum input voltage for this condition.

$$V_O max = Dmax \times (V_{VIN} min - I_O max \times R_{DS(on)} + V_d) - V_d - I_O max \times R_{dc} \quad (1)$$

where

- Dmax ≥ 0.9
- V_d = forward drop of the catch diode
- $R_{DS(on)} = 1 / (-0.3 \times VB2SW^2 + 3.577 \times VB2SW - 4.246)$
  - VB2SW = VBOOT + Vd
  - $VBOOT = (1.41 \times V_{VIN} - 0.554 - V_d \times f_{SW} - 1.847 \times 10^3 \times IB2SW) / (1.41 + f_{SW})$
  - $IB2SW = 100 \times 10^{-6}$ A

7.3.5 Error Amplifier

The TPS54541 voltage-regulation loop is controlled by a transconductance error amplifier. The error amplifier compares the FB pin voltage to the lower of the internal soft-start voltage or the internal 0.8-V voltage reference. The transconductance (gm) of the error amplifier is 350 µA/V during normal operation. During soft-start operation, the transconductance is reduced to 78 µA/V and the error amplifier is referenced to the internal soft-start voltage.

The frequency-compensation components (capacitor, series resistor, and capacitor) connect between the error amplifier output COMP pin and GND pin.

7.3.6 Adjusting the Output Voltage

The internal voltage reference produces a precise 0.8-V ±1% voltage reference over the operating temperature and voltage range by scaling the output of a bandgap-reference circuit. A resistor divider from the output node to the FB pin sets the output voltage. Using 1% tolerance or better divider resistors is recommended. Select the low-side resistor R_{LS} for the desired divider current and use Equation 2 to calculate R_{HS}. To improve efficiency at light loads consider using larger value resistors. However, if the values are too high, the regulator is more susceptible to noise and voltage errors from the FB input current could become noticeable.

$$R_{HS} = R_{LS} \times \left(\frac{V_{OUT} - 0.8\ V}{0.8\ V} \right) \quad (2)$$

7.3.7 Enable and Adjusting Undervoltage Lockout

The TPS54541 device enables when the VIN pin voltage rises above 4.3 V and the EN pin voltage exceeds the enable threshold of 1.2 V. The TPS54541 device disables when the VIN pin voltage falls below 4 V or when the EN pin voltage is below 1.2 V. The EN pin has an internal pullup current source, I_1, of 1.2 µA enabling operation of the TPS54541 device when the EN pin floats.

If an application requires a higher UVLO threshold, use the circuit shown in Figure 26 to adjust the input voltage UVLO with two external resistors. When the EN pin voltage exceeds 1.2 V, an additional 3.4 µA of hysteresis current, I_{HYS}, is sourced out of the EN pin. When the EN pin is pulled below 1.2 V, the 3.4-µA I_{HYS} current is removed. This additional current facilitates adjustable input-voltage UVLO hysteresis. Use Equation 3 to calculate R_{UVLO1} for the desired UVLO hysteresis voltage. Use Equation 4 to calculate R_{UVLO2} for the desired VIN start voltage.

In applications designed to start at relatively low input voltages (that is, from 4.5 to 9 V) and withstand high input voltages (for example, 40 V), the EN pin can experience a voltage greater than the absolute maximum voltage of 8.4 V during the high input-voltage condition. To avoid exceeding this voltage when using the EN resistors, the EN pin is clamped internally with a 5.8-V Zener diode capable of sinking up to 150 µA.

$$R_{UVLO1} = \frac{V_{START} - V_{STOP}}{I_{HYS}} \quad (3)$$

$$R_{UVLO2} = \frac{V_{ENA}}{\frac{V_{START} - V_{ENA}}{R_{UVLO1}} + I_1} \quad (4)$$

Feature Description (continued)

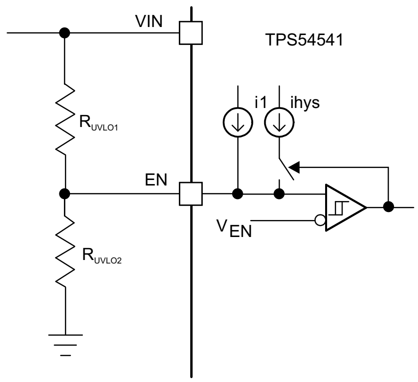


Figure 26. Adjustable Undervoltage Lockout (UVLO)

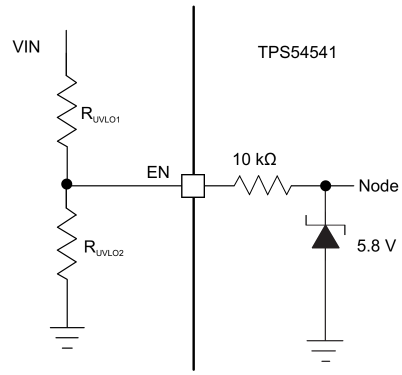


Figure 27. Internal EN Pin Clamp

7.3.8 Soft-Start/Tracking Pin (SS/TR)

The TPS54541 device effectively uses the lower voltage of the internal voltage reference or the SS/TR pin voltage as the reference voltage of the power supply and regulates the output accordingly. A capacitor on the SS/TR pin to ground implements a soft-start time. The TPS54541 device has an internal pullup current source of 1.7 µA that charges the external soft-start capacitor. The calculations for the soft start time (10% to 90%) are shown in Equation 5. The voltage reference (V_{REF}) is 0.8 V and the soft-start current (I_{SS}) is 1.7µA. The soft-start capacitor should remain lower than 0.47 µF and greater than 0.47 nF.

$$C_{SS}\ (nF) = \frac{T_{SS}\ (ms) \times I_{SS}\ (\mu A)}{V_{REF}\ (V) \times 0.8} \tag{5}$$

At power up, the TPS54541 device does not begin switching until the soft start pin is discharged to less than 54 mV to ensure a proper power-up, see Figure 28.

Also, during normal operation, the TPS54541 device stops switching, the SS/TR must discharge to 54 mV, and, when the VIN UVLO is exceeded, the EN pin must pull below 1.2 V, otherwise a thermal shutdown event occurs.

The FB voltage follows the SS/TR pin voltage with a 42-mV offset up to 85% of the internal voltage reference. When the SS/TR voltage is greater than 85% on the internal reference voltage the offset increases as the effective system reference transitions from the SS/TR voltage to the internal voltage reference (see Figure 23). The SS/TR voltage ramps linearly until clamped at 2.7 V typically as shown in Figure 28.

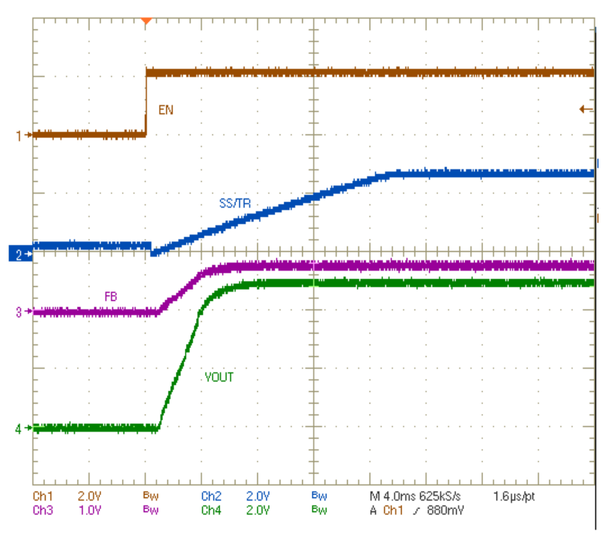


Figure 28. Operation of SS/TR Pin when Starting

Feature Description (continued)

7.3.9 Sequencing

Many of the common power supply sequencing methods are implemented using the SS/TR, EN, and PWRGD pins. The sequential method is implemented using an open-drain output of a power on the reset pin of another device. The sequential method is illustrated in Figure 29 using two TPS54541 devices. The power good is connected to the EN pin on the TPS54541 device which enables the second power supply once the primary supply reaches regulation. If needed, a 1-nF ceramic capacitor on the EN pin of the second power supply provides a 1-ms startup delay. Figure 30 shows the results of Figure 29.

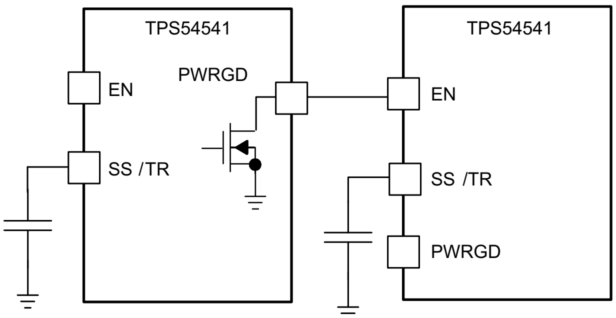


Figure 29. Schematic for Sequential Startup Sequence

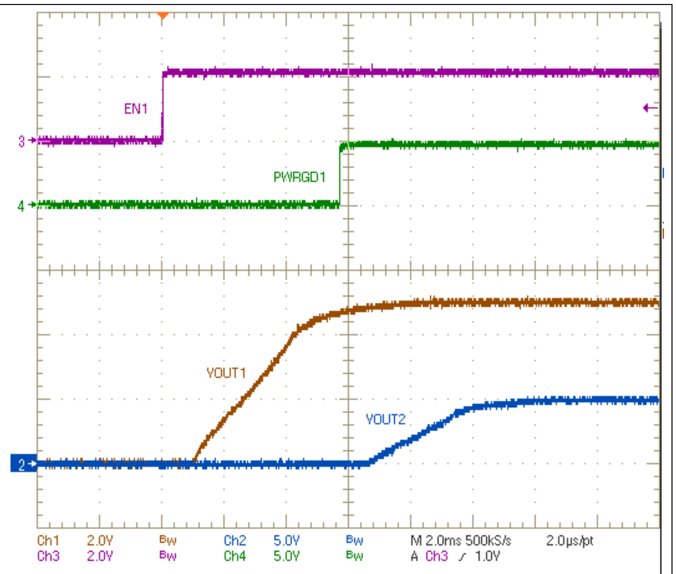


Figure 30. Sequential Startup using EN and PWRGD

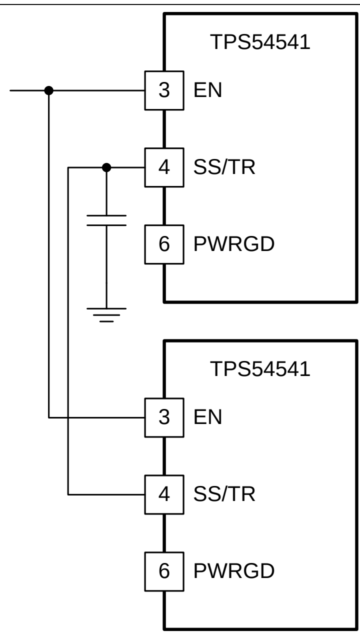


Figure 31. Schematic for Ratiometric Startup Sequence

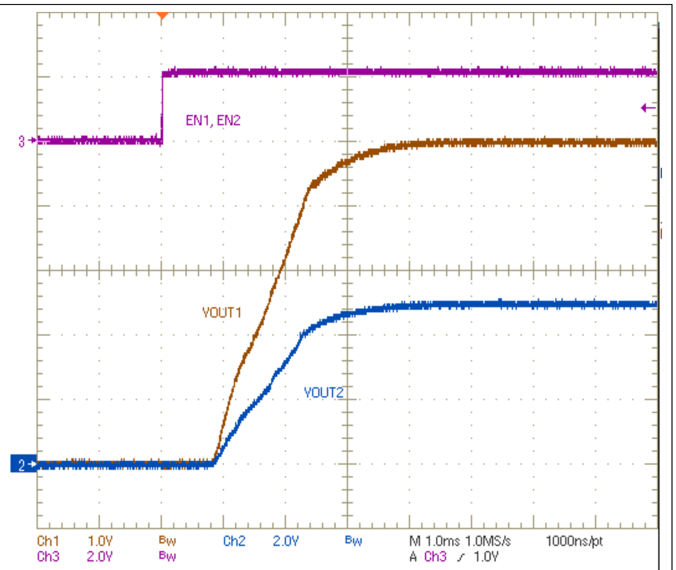


Figure 32. Ratiometric Startup Using Coupled SS/TR pins

Feature Description (continued)

Figure 31 shows a method for ratiometric start-up sequence by connecting the SS/TR pins together. The regulator outputs ramp up and reach regulation at the same time. When calculating the soft-start time the pullup current source must be doubled in Equation 5. Figure 32 shows the results of Figure 31.

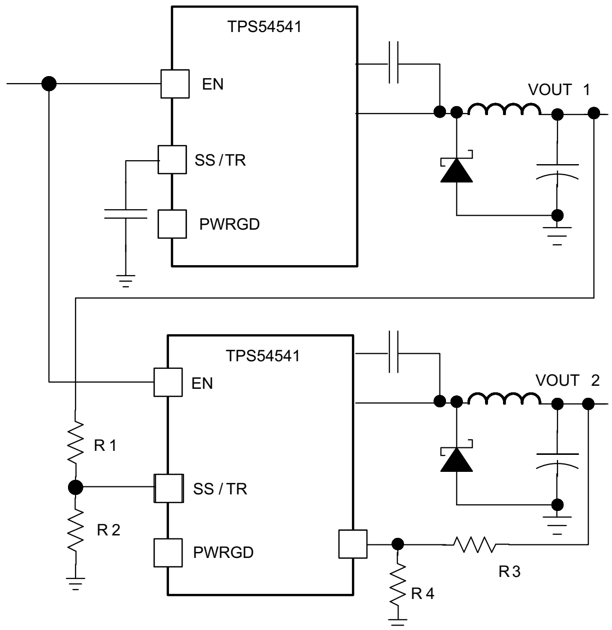


Figure 33. Schematic for Ratiometric and Simultaneous Startup Sequence

Ratiometric and simultaneous power-supply sequencing are implemented by connecting the resistor network of R1 and R2 shown in Figure 33 to the output of the power supply that must be tracked or another voltage reference source. Using Equation 6 and Equation 7, calculate the tracking resistors to initiate the V_{OUT2} slightly before, after or at the same time as V_{OUT1}. Equation 8 is the voltage difference between V_{OUT1} and V_{OUT2} at the 95% of nominal output regulation.

The ΔV variable is 0 V for simultaneous sequencing. To minimize the effect of the inherent SS/TR to FB offset ($V_{SSoffset}$) in the soft-start circuit and the offset created by the pullup-current source (I_{SS}) and tracking resistors, the $V_{SSoffset}$ and I_{SS} are included as variables in the equations.

To design a ratio-metric start-up in which the V_{OUT2} voltage is slightly greater than the V_{OUT1} voltage when V_{OUT2} reaches regulation, use a negative number in Equation 6 through Equation 8 for ΔV. Equation 8 results in a positive number for applications which the V_{OUT2} is slightly lower than V_{OUT1} when V_{OUT2} regulation is achieved.

Because the SS/TR pin must be pulled below 54 mV before starting after an EN, UVLO, or thermal shutdown fault, careful selection of the tracking resistors ensures that the device restarts after a fault. The calculated R1 value from Equation 6 must be greater than the value calculated in Equation 9 to ensure the device recovers from a fault.

As the SS/TR voltage becomes more than 85% of the nominal reference voltage, the $V_{SSoffset}$ becomes larger as the soft-start circuits gradually hands-off the regulation reference to the internal voltage reference. The SS/TR pin voltage must be greater than 1.5 V for a complete handoff to the internal voltage reference as shown in Figure 23.

$$R1 = \frac{V_{OUT2} + \Delta V}{V_{REF}} \times \frac{V_{SSoffset}}{I_{SS}} \tag{6}$$

$$R2 = \frac{V_{REF} \times R1}{V_{OUT2} + \Delta V - V_{REF}} \tag{7}$$

$$\Delta V = V_{OUT1} - V_{OUT2} \tag{8}$$

Feature Description (continued)

$$R1 > 2800 \times V_{OUT1} - 180 \times \Delta V \quad (9)$$

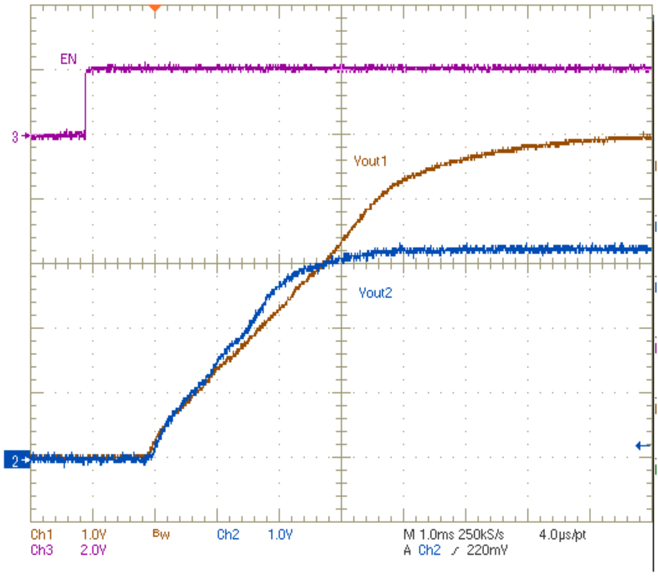


Figure 34. Ratiometric Startup with Tracking Resistors

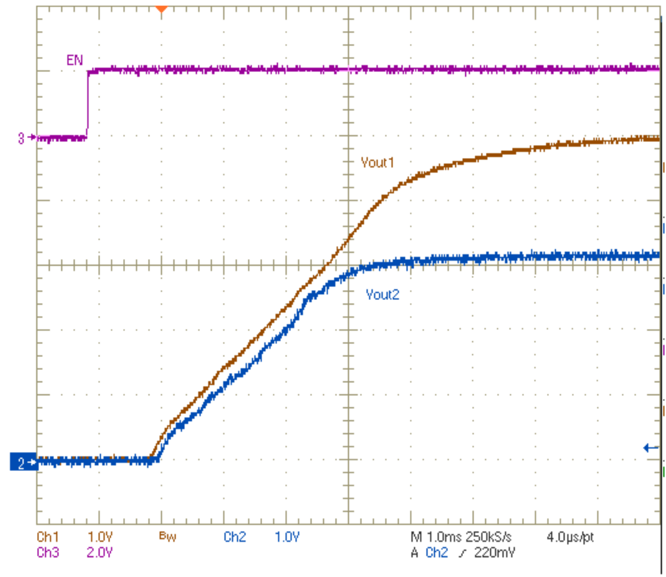


Figure 35. Ratiometric Startup with Tracking Resistors

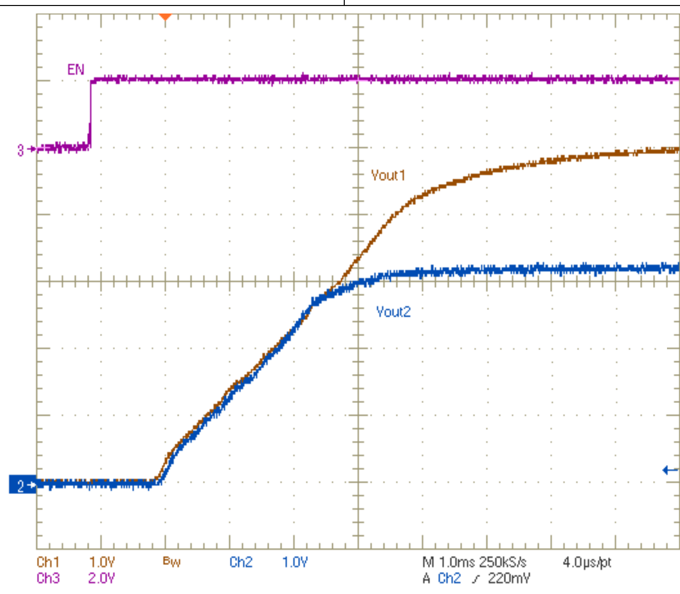


Figure 36. Simultaneous Startup With Tracking Resistor

Feature Description (continued)

7.3.10 Constant Switching Frequency and Timing Resistor (RT/CLK) Pin

The switching frequency of the TPS54541 device is adjustable over a wide range from 100 to 2500 kHz by placing a resistor between the RT/CLK pin and GND pin. The RT/CLK pin voltage is typically 0.5 V and must have a resistor to ground to set the switching frequency. To determine the timing resistance for a given switching frequency, use Equation 10 or Equation 11 or the curves in Figure 5 and Figure 6. To reduce the solution size typically set the switching frequency as high as possible. Consider the tradeoffs of the conversion efficiency, maximum input voltage, and minimum controllable on time. The minimum controllable on time is typically 135 ns, which limits the maximum operating frequency in applications with high input to output step-down ratios. The maximum switching frequency is also limited by the frequency-foldback circuit. A more detailed discussion of the maximum switching frequency is provided in the next section.

$$R_T\ (k\Omega) = \frac{101756}{f sw\ (kHz)^{1.008}} \tag{10}$$

$$f sw\ (kHz) = \frac{92417}{RT\ (k\Omega)^{0.991}} \tag{11}$$

7.3.11 Synchronization to RT/CLK Pin

The RT/CLK pin can receive a frequency synchronization signal from an external system clock. To implement this synchronization feature, connect a square wave to the RT/CLK pin through either circuit network shown in Figure 37. The square wave applied to the RT/CLK pin must switch lower than 0.5 V and higher than 2.0 V and have a pulsewidth greater than 15 ns. The synchronization frequency range is 160 to 2300 kHz. The rising edge of the SW synchronizes to the falling edge of RT/CLK pin signal. Design the external synchronization circuit such that the default-frequency set resistor connects from the RT/CLK pin to ground when the synchronization signal is off. When using a low impedance signal source, the frequency set resistor connects in parallel with an AC-coupling capacitor to a termination resistor (for example, 50 Ω) as shown in Figure 37. The two resistors in the series provide the default-frequency-setting resistance when the signal source is turned off. The sum of the resistance sets the switching frequency close to the external CLK frequency. AC-coupling the synchronization signal through a 10-pF ceramic capacitor to RT/CLK pin is recommended.

The first time the RT/CLK is pulled above the PLL threshold, the TPS54541 device switches from the RT-resistor free-running frequency mode to the PLL-synchronized mode. The internal 0.5-V voltage source is removed and the RT/CLK pin becomes high impedance as the PLL begins to lock onto the external signal. The switching frequency can be higher or lower than the frequency set with the RT/CLK resistor. The device transitions from the resistor mode to the PLL mode and locks onto the external clock frequency within 78 µs. During the transition from the PLL mode to the resistor programmed mode, the switching frequency falls to 150 kHz and then increases or decreases to the resistor programmed frequency when the 0.5-V bias voltage is reapplied to the RT/CLK resistor.

The switching frequency is divided by 8, 4, 2, and 1 as the FB pin voltage ramps from 0 to 0.8 V. The device implements a digital frequency foldback enables synchronization to an external clock during normal startup and fault conditions. Figure 38, Figure 39 and Figure 40 show the device synchronized to an external system clock in continuous conduction mode (CCM), discontinuous conduction (DCM), and pulse skip mode (Eco-Mode).

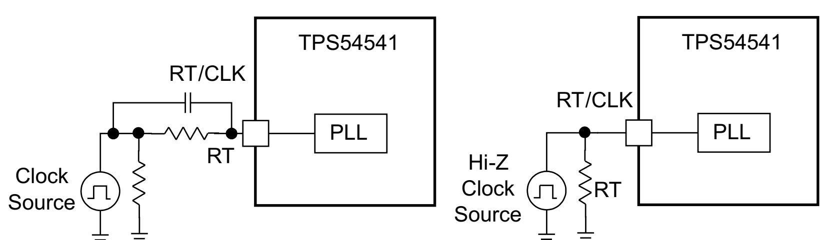


Figure 37. Synchronizing to a System Clock

Feature Description (continued)

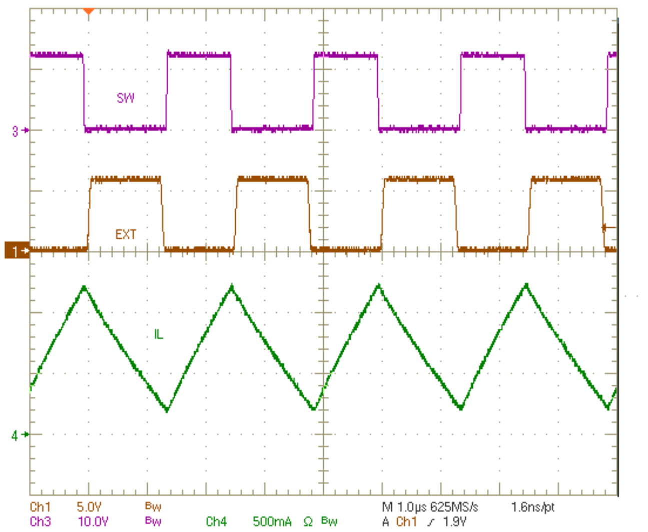


Figure 38. Plot of Synchronizing in CCM

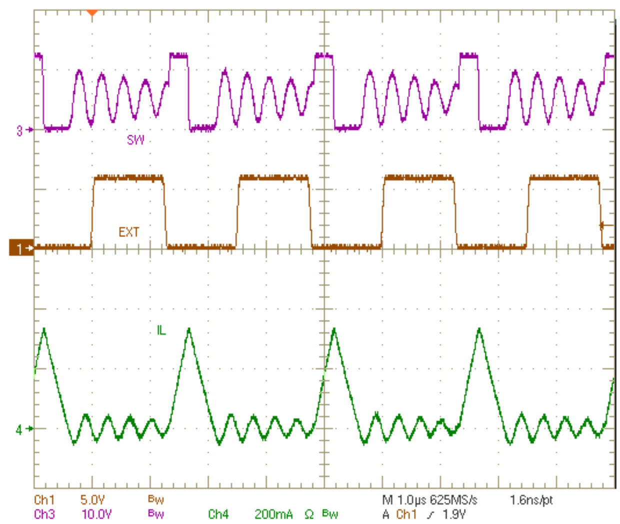


Figure 39. Plot of Synchronizing in DCM

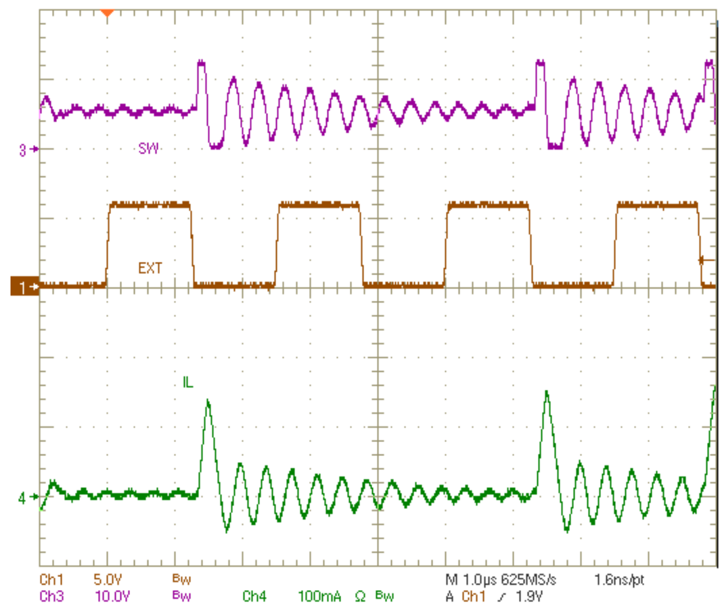


Figure 40. Plot of Synchronizing in Eco-mode

Feature Description (continued)

7.3.12 Maximum Switching Frequency

To protect the converter in overload conditions at higher switching frequencies and input voltages, the TPS54541 device implements a frequency foldback. The oscillator frequency is divided by 1, 2, 4, and 8 as the FB pin voltage falls from 0.8 V to 0 V. The TPS54541 device uses a digital frequency foldback to enable synchronization to an external clock during normal startup and fault conditions. During short-circuit events, the inductor current can exceed the peak current-limit because of the high-input voltage and the minimum controllable on time. When the output voltage is forced low by the shorted load, the inductor current decreases slowly during the switch off time. The frequency foldback effectively increases the off time by increasing the period of the switching cycle providing more time for the inductor current to ramp down.

With a maximum frequency-foldback ratio of 8, there is a maximum frequency at which the inductor current is controlled by frequency-foldback protection. Equation 13 calculates the maximum switching frequency at which the inductor current remains under control when V_{OUT} is forced to $V_{OUT(SC)}$. The selected operating frequency must not exceed the calculated value.

Equation 12 calculates the maximum switching-frequency limitation set by the minimum controllable on time and the input to output step-down ratio. Setting the switching frequency above this value causes the regulator to skip switching pulses to achieve the low duty cycle required to regulate the output voltage at maximum input voltage.

$$f_{SW(max\,skip)} = \frac{1}{t_{ON}} \times \left(\frac{I_O \times R_{dc} + V_{OUT} + V_d}{V_{IN} - I_O \times R_{DS(on)} + V_d} \right) \tag{12}$$

$$f_{SW(shift)} = \frac{f_{DIV}}{t_{ON}} \times \left(\frac{I_{CL} \times R_{dc} + V_{OUT(sc)} + V_d}{V_{IN} - I_{CL} \times R_{DS(on)} + V_d} \right) \tag{13}$$

where (for Equation 12 and Equation 13)

- I_O = output current
- I_{CL} = current limit
- R_{dc} = inductor resistance
- V_{IN} = maximum input voltage
- V_{OUT} = output voltage
- $V_{OUT(SC)}$ = output voltage during short
- V_d = diode voltage drop
- $R_{DS(on)}$ = switch on resistance
- t_{ON} = controllable on time
- f_{DIV} = frequency divide equals (1, 2, 4, or 8)

7.3.13 Accurate Current Limit Operation

The TPS54541 device implements peak current-mode control in which the COMP pin voltage controls the peak current of the high-side MOSFET. A signal proportional to the high-side switch current and the COMP pin voltage are compared each cycle. When the peak switch current intersects the COMP control voltage, the high-side switch turns off. During overcurrent conditions that pull the output voltage low, the error amplifier increases switch current by driving the COMP pin high. The error amplifier output is clamped internally at a level, which sets the peak switch current limit. The TPS54541 device provides an accurate current limit threshold with a typical current limit delay of 60 ns. With smaller inductor values, the delay results in a higher peak inductor current. The relationship between the inductor value and the peak inductor current is shown in Figure 41.

Feature Description (continued)

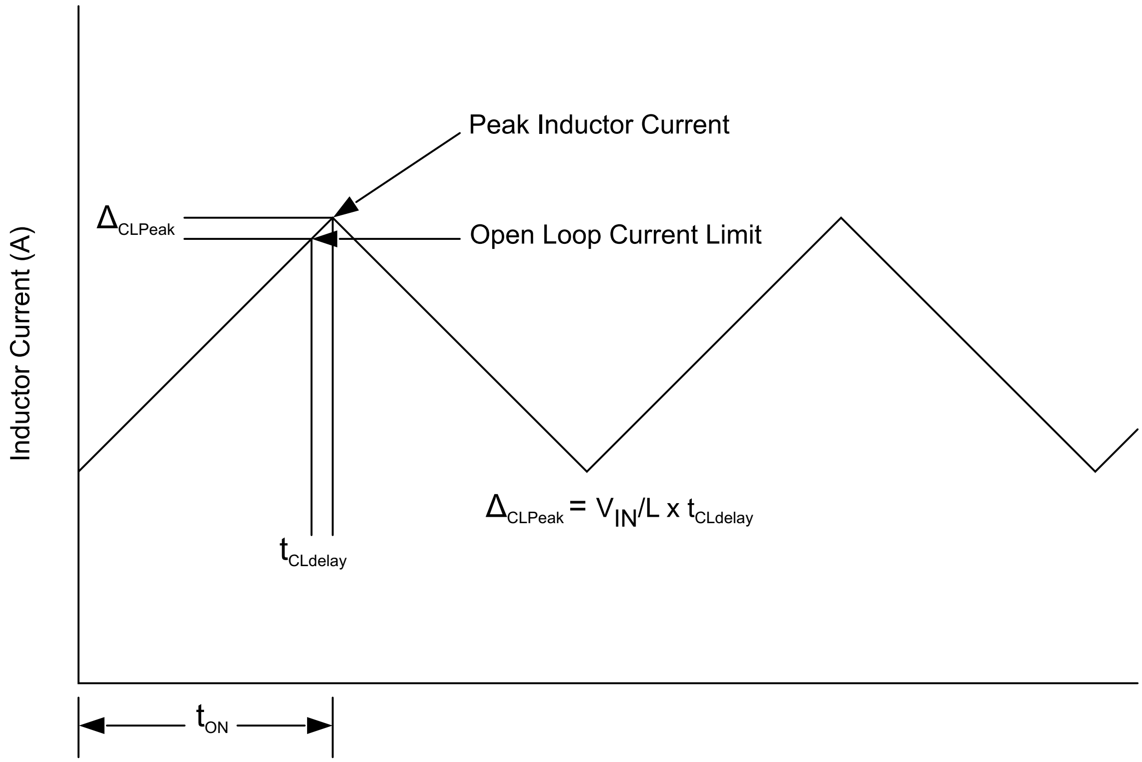


Figure 41. Current Limit Delay

7.3.14 Power Good (PWRGD Pin)

The PWRGD pin is an open-drain output. When the FB pin is between 93% and 106% of the internal voltage reference the PWRGD pin is de-asserted and the pin floats. A pull-up resistor of 1 kΩ to a voltage source that is 5.5 V or less is recommended. A higher pullup resistance reduces the amount of current drawn from the pullup voltage source when the PWRGD pin is asserted low. A lower pullup resistance reduces the switching noise seen on the PWRGD signal. The PWRGD is in a defined state once the VIN input voltage is greater than 2 V but with reduced current sinking capability. The PWRGD achieves full current sinking capability as VIN input voltage approaches 3 V.

The PWRGD pin is pulled low when the FB is lower than 90% or greater than 108% of the nominal internal reference voltage. If the UVLO or thermal shutdown are asserted or the EN pin pulled low, the PWRGD is pulled low.

7.3.15 Overvoltage Protection

The TPS54541 device incorporates an output overvoltage-protection (OVP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients in designs with low-output capacitance. For example, when the power supply output is overloaded the error amplifier compares the actual output voltage to the internal reference voltage. If the FB pin voltage is lower than the internal reference voltage for a considerable time, the output of the error amplifier increases to a maximum voltage corresponding to the peak current limit threshold. When the overload condition is removed, the regulator output rises and the error amplifier output transitions to the normal operating level. In some applications, the power-supply output voltage increases faster than the response of the error amplifier output resulting in an output overshoot.

The OVP feature minimizes output overshoot when using a low-value output capacitor by comparing the FB pin voltage to the rising OVP threshold which is nominally 108% of the internal voltage reference. If the FB pin voltage is greater than the rising OVP threshold, the high-side MOSFET immediately disables to minimize output overshoot. When the FB voltage drops below the falling OVP threshold which is nominally 106% of the internal voltage reference, the high-side MOSFET resumes normal operation.

Feature Description (continued)

7.3.16 Thermal Shutdown

The TPS54541 device provides an internal thermal shutdown to protect the device when the junction temperature exceeds 176°C. The high-side MOSFET stops switching when the junction temperature exceeds the thermal trip threshold. When the die temperature falls below 164°C, the device reinitiates the power-up sequence controlled by discharging the SS/TR pin.

7.3.17 Small-Signal Model for Loop Response

Figure 42 shows a simplified equivalent model for the TPS54541 control loop which can be simulated to check the frequency response and dynamic load response. The error amplifier is a transconductance amplifier with a gm_{EA} of 350 μA/V. The error amplifier is modeled using an ideal voltage-controlled current source. The resistor R_O and capacitor C_O model the open-loop gain and frequency response of the amplifier. The 1-mV AC-voltage source between the nodes a and b effectively breaks the control loop for the frequency response measurements. Plotting c/a provides the small signal response of the frequency compensation. Plotting a/b provides the small signal response of the overall loop. The dynamic loop response is evaluated by replacing R_L with a current source with the appropriate load-step amplitude and step rate in a time-domain analysis. This equivalent model is only valid for CCM operation.

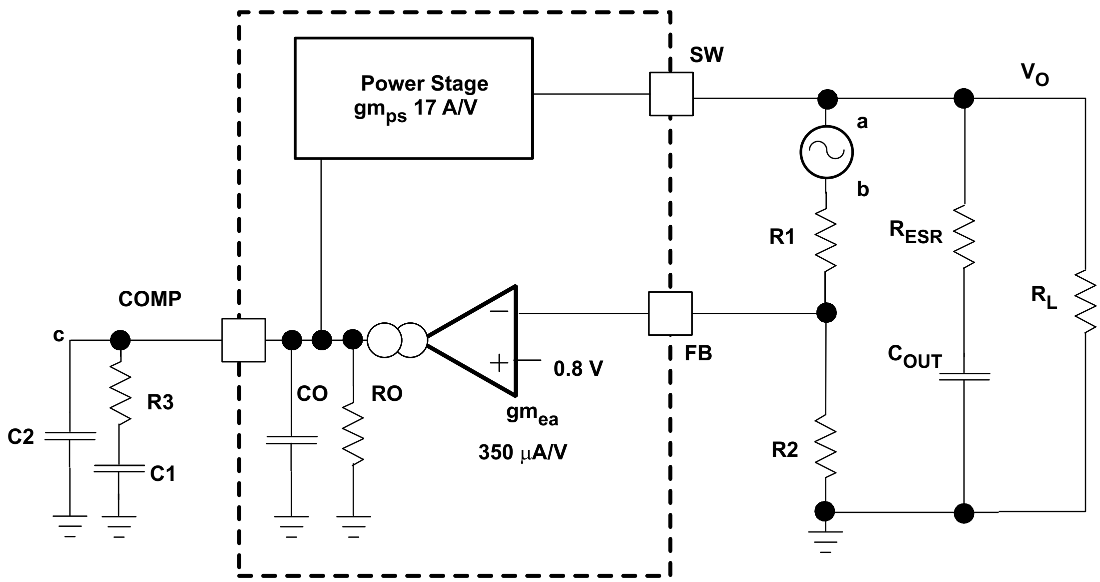


Figure 42. Small-Signal Model for Loop Response

7.3.18 Simple Small-Signal Model for Peak-Current-Mode Control

Figure 43 describes a simple small-signal model used to design the frequency compensation. The TPS54541 power stage is approximated by a voltage-controlled current source (duty-cycle modulator) supplying current to the output capacitor and load resistor. Equation 14 shows the control to output transfer function. The control to output transfer function consists of a DC gain, one dominant pole, and one equivalent-series-resistor (ESR) zero. The quotient of the change in switch current and the change in COMP pin voltage (node c in Figure 42) is the power stage transconductance, gm_{PS}. The gm_{PS} for the TPS54541 device is 17 A/V. The low-frequency gain of the power stage is the product of the transconductance and the load resistance as shown in Equation 15.

As the load current increases and decreases, the low-frequency gain decreases and increases, respectively. This variation with the load may seem problematic, but the dominant pole moves with the load current (see Equation 16). The combined effect is highlighted by the dashed line in the right half of Figure 43. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0-dB crossover frequency the same with varying load conditions. The type of output capacitor chosen determines whether the ESR zero has a profound effect on the frequency compensation design. Using high ESR aluminum electrolytic capacitors can reduce the number of frequency compensation components required to stabilize the overall loop because the phase margin is increased by the ESR zero of the output capacitor (see Equation 17).

Feature Description (continued)

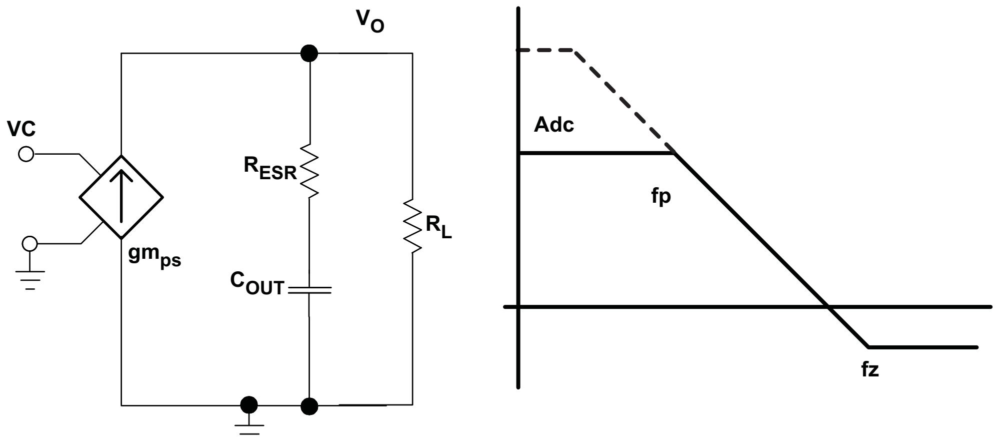


Figure 43. Simple Small-Signal Model and Frequency Response for Peak Current-Mode Control

$$\frac{V_{OUT}}{VC} = Adc \times \frac{\left(1 + \frac{s}{2\pi \times f_Z}\right)}{\left(1 + \frac{s}{2\pi \times f_P}\right)} \quad (14)$$

$$Adc = gm_{ps} \times R_L \quad (15)$$

$$f_P = \frac{1}{C_{OUT} \times R_L \times 2\pi} \quad (16)$$

$$f_Z = \frac{1}{C_{OUT} \times R_{ESR} \times 2\pi} \quad (17)$$

7.3.19 Small Signal Model for Frequency Compensation

The TPS54541 device uses a transconductance amplifier for the error amplifier and supports three of the commonly-used frequency compensation circuits. Figure 44 shows compensation circuits Type 2A, Type 2B, and Type 1 . Type 2 circuits are typically implemented in high-bandwidth power-supply designs using low-ESR output capacitors. The Type 1 circuit is implemented with power-supply designs with high-ESR aluminum electrolytic or tantalum capacitors. Equation 18 and Equation 19 relate the frequency response of the amplifier to the small signal model in Figure 44. The open-loop gain and bandwidth are modeled using the R_O and C_O shown in Figure 44. See Figure 44 for a design example using a Type 2A network with a low-ESR output capacitor.

Equation 18 through Equation 27 are provided as references. An alternative is to use WEBENCH® software tools to create a design based on the power-supply requirements (go to www.ti.com/WEBENCH for more information).

Feature Description (continued)

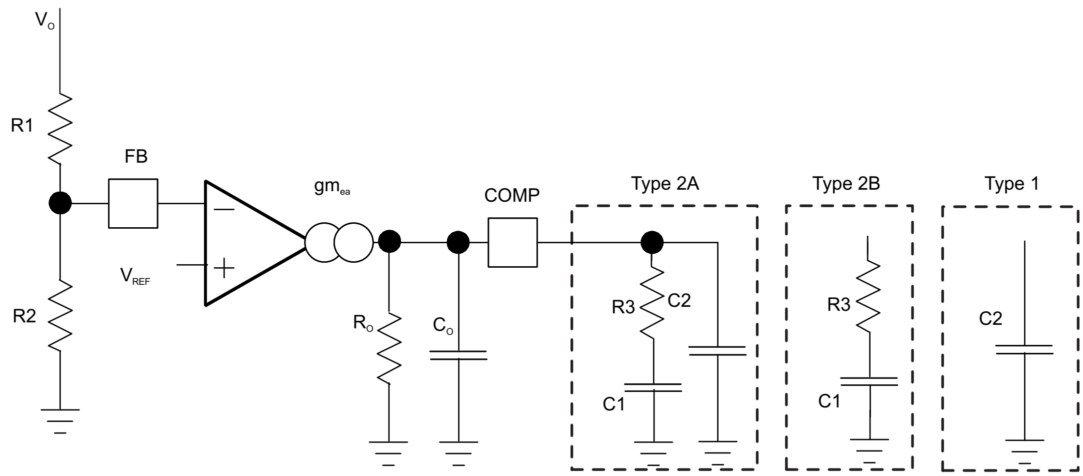


Figure 44. Types of Frequency Compensation

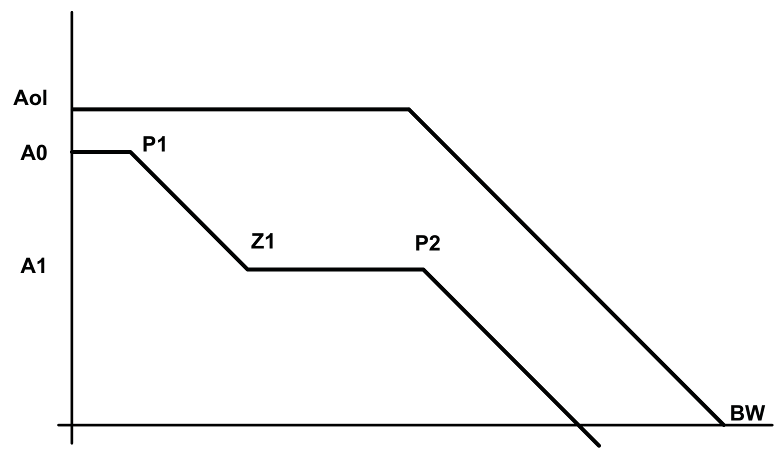


Figure 45. Frequency Response of the Type 2A and Type 2B Frequency Compensation

$$R_O = \frac{Aol(V/V)}{gm_{ea}} \tag{18}$$

$$C_O = \frac{gm_{ea}}{2\pi \times BW\,(Hz)} \tag{19}$$

$$EA = A0 \times \frac{\left(1 + \frac{s}{2\pi \times f_{Z1}}\right)}{\left(1 + \frac{s}{2\pi \times f_{P1}}\right) \times \left(1 + \frac{s}{2\pi \times f_{P2}}\right)} \tag{20}$$

$$A0 = gm_{ea} \times R_O \times \frac{R2}{R1 + R2} \tag{21}$$

$$A1 = gm_{ea} \times R_O \,||\, R3 \times \frac{R2}{R1 + R2} \tag{22}$$

$$P1 = \frac{1}{2\pi \times Ro \times C1} \tag{23}$$

Feature Description (continued)

$$Z1 = \frac{1}{2\pi \times R3 \times C1} \quad (24)$$

$$P2 = \frac{1}{2\pi \times R3 || R_O \times (C2 + C_O)} \text{Type 2A} \quad (25)$$

$$P2 = \frac{1}{2\pi \times R3 || R_O \times C_O} \text{Type 2B} \quad (26)$$

$$P2 = \frac{1}{2\pi \times R_O \times (C2 + C_O)} \text{Type 1} \quad (27)$$

7.4 Device Functional Modes

TI designed the TPS54541 to operate with input voltages above 4.5 V. When the VIN voltage is above the 4.3-V typical rising UVLO threshold and the EN voltage is above the 1.2-V typical threshold, the device is active. If the VIN voltage falls below the typical 4-V UVLO turnoff threshold, the device stops switching. If the EN voltage falls below the 1.2-V threshold, the device stops switching and enters shutdown mode with a low-supply current of 2 µA typical.

The TPS54541 operates in CCM when the output current is enough to keep the inductor current above 0 A at the end of each switching period. As a non-synchronous converter, the device enters DCM at low-output currents when the inductor current falls to 0 A before the end of a switching period. At very-low output current, the COMP voltage drops to the pulse-skipping threshold and the device operates in a pulse-skipping Eco-mode. In this mode, the high-side MOSFET does not switch every switching period. This operating mode reduces power loss, while regulating the output voltage. For more information on Eco-mode, see the *Pulse Skip Eco-mode* section.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS54541 device is a 42-V, 5-A, step-down regulator with an integrated high-side MOSFET. This device typically converts a higher-dc voltage to a lower-dc voltage with a maximum available output current of 5 A. Example applications are the following: 12-V and 24-V industrial, automotive, and communication power systems. Use the following design procedure to select component values for the TPS54541 device. The spreadsheet (SLVC452) on the product page can help with all calculations. Alternatively, use the WEBENCH software to generate a complete design. The WEBENCH software uses an interactive design procedure and accesses a comprehensive database of components when generating a design.

8.2 Typical Applications

8.2.1 Buck Converter for 6-V to 42-V Input and 3.3-V at 5-A Output

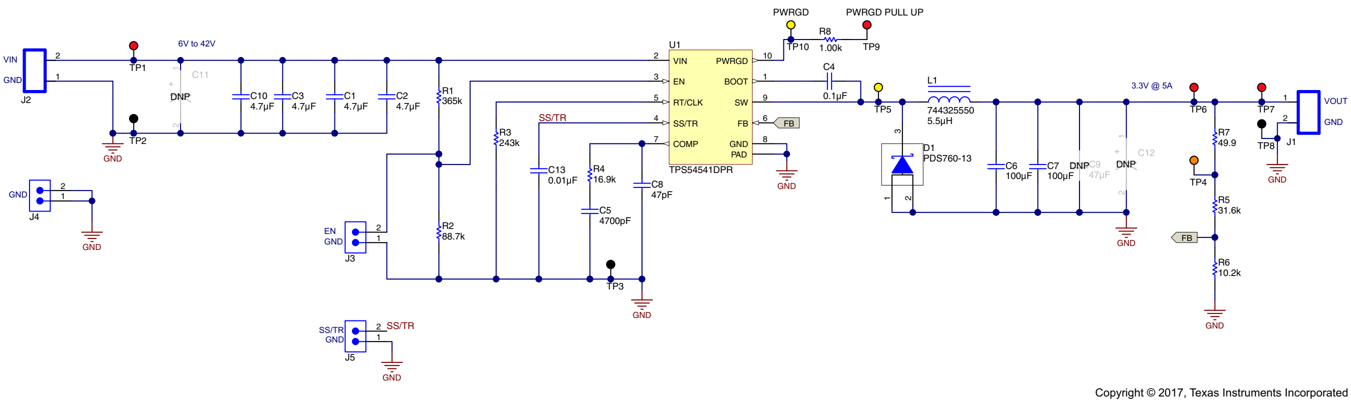


Figure 46. 3.3-V Output TPS54541 Design Example

8.2.1.1 Design Requirements

This guide illustrates the design of a high-frequency switching regulator using ceramic output capacitors. A few parameters must be known to start the design process. These requirements are typically determined at the system level. Calculations can be done with WEBENCH or the excel spreadsheet (SLVC452) located on the product page. TI designed this example to the known parameters listed in Table 1.

Table 1. Design Parameters

PARAMETER	VALUE
Output Voltage	3.3 V
Transient Response 1.25 A to 3.75 A load step	ΔV_{OUT} = 4 %
Maximum Output Current	5 A
Input Voltage	12 V nominal 6 V to 42 V
Output Voltage Ripple	0.5% of V_{OUT}
Start Input Voltage (rising VIN)	5.75 V
Stop Input Voltage (falling VIN)	4.5 V

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design with WEBENCH® Tools

Click here to create a custom design using the TPS54541 device with the WEBENCH® Power Designer.

1. Start by entering your V_{IN}, V_{OUT}, and I_{OUT} requirements.
2. Optimize your design for key parameters like efficiency, footprint and cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.
3. The WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real time pricing and component availability.
4. In most cases, you will also be able to:
   – Run electrical simulations to see important waveforms and circuit performance
   – Run thermal simulations to understand the thermal performance of your board
   – Export your customized schematic and layout into popular CAD formats
   – Print PDF reports for the design, and share your design with colleagues
5. Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.1.2.2 Selecting the Switching Frequency

Choose a switching frequency for the regulator. Typically, a designer uses the highest switching frequency possible because this produces the smallest solution size. High-switching frequency allows for lower-value inductors and smaller-output capacitors compared to a power supply that switches at a lower frequency. The switching frequency that can be selected is limited by the minimum on-time of the internal power switch, the input voltage, the output voltage, and the frequency-foldback protection.

Use Equation 12 and Equation 13 to calculate the upper limit of the switching frequency for the regulator. Choose the lower value result from the two equations. Switching frequencies higher than these values results in pulse skipping or the lack of overcurrent protection during a short circuit.

The typical minimum on time, t_{onmin}, is 135 ns for the TPS54541 device. For this example, the output voltage is 3.3 V and the maximum input voltage is 42 V. Assuming a diode voltage of 0.52 V, inductor DC resistance of 10.3 mΩ, typical switch resistance of 87 mΩ and 5-A load, from Equation 12 the maximum switch frequency to avoid pulse skipping is 680 kHz. To ensure overcurrent runaway is not a concern during short circuits, use Equation 10 to determine the maximum switching frequency for frequency foldback protection. With a current-limit value of 6.3 A and short circuit output voltage of 0.1 V, the maximum switching frequency is 960 kHz.

For this design, TI chose a lower-switching frequency of 400 kHz to operate below the calculated maximums. To determine the timing resistance for a given switching frequency, use Equation 10 or the curve in Figure 6. Figure 46 shows resistor R_3, which sets the switching frequency . For 400-kHz operation, the closest standard value resistor is 243 kΩ.

$$f_{SW(max\,skip)} = \frac{1}{135\text{ns}} \times \left(\frac{5\text{ A x }10.3\text{ m}\Omega + 3.3\text{ V} + 0.52\text{ V}}{42\text{ V} - 5\text{ A x }87\text{ m}\Omega + 0.52\text{ V}} \right) = 680\text{ kHz} \quad (28)$$

$$f_{SW(shift)} = \frac{8}{135\text{ ns}} \times \left(\frac{6.3\text{ A x }10.3\text{ m}\Omega + 0.1\text{ V} + 0.52\text{ V}}{42\text{ V} - 6.3\text{ A x }87\text{ m}\Omega + 0.52\text{ V}} \right) = 960\text{ kHz} \quad (29)$$

$$R_T\ (\text{k}\Omega) = \frac{101756}{400\ (\text{kHz})^{1.008}} = 242\text{ k}\Omega \quad (30)$$

8.2.1.2.3 Output Inductor Selection (L_O)

To calculate the minimum value of the output inductor, use Equation 31.

K_{IND} is a ratio that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Choosing high inductor ripple currents impacts the selection of the output capacitor because the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. The inductor ripple value is at the discretion of the designer, but the following guidelines may be used.

For designs using low-ESR output capacitors such as ceramics, use a value as high as K_{IND} = 0.3. When using higher-ESR output capacitors, K_{IND} = 0.2 yields better results. Because the inductor ripple current is part of the current mode PWM control system, the inductor ripple current should always be greater than 150 mA for stable PWM operation. In a wide input voltage regulator, choose a relatively large inductor ripple current. This provides sufficient ripple current with the input voltage at the minimum.

For this design example, K_{IND} = 0.3 and the inductor value is calculated to be 5.1 µH. It is important that the RMS current and saturation current ratings of the inductor not be exceeded. See Equation 33 and Equation 34 for the RMS and peak inductor current. For this design, the RMS inductor current is 5 A and the peak inductor current is 5.79 A. The chosen inductor is a WE 744325550, which has a saturation current rating of 12 A and an RMS current rating of 10 A. This inductor also has a typical inductance of 5.5 µH at no load and 4.8 µH at 5-A load. Lastly, the inductor has a DCR of 10.3 mΩ.

As the equation set demonstrates, lower-ripple currents reduce the output voltage ripple of the regulator but require a larger value of inductance. Selecting higher-ripple currents increases the output voltage ripple of the regulator but allow for a lower-inductance value.

The current flowing through the inductor is the inductor ripple current plus the output current. During powerup, faults, or transient load conditions, the inductor current can increase above the peak inductor current level calculated previously. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative design approach is to choose an inductor with a saturation current rating equal to or greater than the switch current limit of the TPS54541 device, which is nominally 7.5 A.

$$L_{O(min)} = \frac{V_{IN(max)} - V_{OUT}}{I_{OUT} \times K_{IND}} \times \frac{V_{OUT}}{V_{IN(max)} \times f_{SW}} = \frac{42\ \text{V} - 3.3\ \text{V}}{5\ \text{A} \times 0.3} \times \frac{3.3\ \text{V}}{42\ \text{V} \times 400\ \text{kHz}} = 5.1\ \mu\text{H} \tag{31}$$

$$I_{RIPPLE} = \frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{V_{IN(max)} \times L_O \times f_{SW}} = \frac{3.3\ \text{V} \times (42\ \text{V} - 3.3\ \text{V})}{42\ \text{V} \times 4.8\ \mu\text{H} \times 400\ \text{kHz}} = 1.58\ \text{A} \tag{32}$$

$$I_{L(rms)} = \sqrt{(I_{OUT})^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times (V_{IN(max)} - V_{OUT})}{V_{IN(max)} \times L_O \times f_{SW}}\right)^2} = \sqrt{(5\ \text{A})^2 + \frac{1}{12} \times \left(\frac{3.3\ \text{V} \times (42\ \text{V} - 3.3\ \text{V})}{42\ \text{V} \times 4.8\ \mu\text{H} \times 400\ \text{kHz}}\right)^2} = 3.5\ \text{A} \tag{33}$$

$$I_{L(peak)} = I_{OUT} + \frac{I_{RIPPLE}}{2} = 5\ \text{A} + \frac{1.58\ \text{A}}{2} = 5.79\ \text{A} \tag{34}$$

8.2.1.2.4 Output Capacitor

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the following:

- The modulator pole
- The output voltage ripple
- How the regulator responds to a large change in load current

Select the output capacitance based on the most stringent of these three criteria.

The desired response to a large change in the load current is the first criteria. The output capacitor must to supply the increased load current until the regulator responds to the load step. A regulator does not respond immediately to a large, fast increase in the load current such as transitioning from no load to a full load. The regulator usually requires two or more clock cycles for the control loop to sense the change in output voltage and adjust the peak switch current in response to the higher load. The output capacitance must be large enough to supply the difference in current for two clock cycles to maintain the output voltage within the specified range. Equation 35 shows the minimum output capacitance necessary, where ΔI_{OUT} is the change in output current, f_{SW} is the switching frequency of the regulators and ΔV_{OUT} is the allowable change in the output voltage. For this example, the transient load response is specified as a 4% change in V_{OUT} for a load step from 1.25 A to 3.75 A. ΔI_{OUT} is 3.75 A – 1.25 A = 2.5 A and ΔV_{OUT} = 0.04 × 3.3 V = 0.13 V. These values provide a minimum capacitance of 95 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to be ignored. Aluminum electrolytic and tantalum capacitors have higher ESR that must be included in load step calculations.

The output capacitor must also be sized to absorb energy stored in the inductor when transitioning from a high to low load current. The catch diode of the regulator can not sink current so energy stored in the inductor can produce an output voltage overshoot when the load current rapidly decreases. Figure 51 shows a typical load step response. The excess energy absorbed in the output capacitor increases the voltage on the capacitor. The capacitor must be sized to maintain the output voltage during these transient periods. Equation 36 calculates the minimum capacitance required to keep the output voltage overshoot to a desired value, where L_O is the value of the inductor, I_{OH} is the output current under heavy load, I_{OL} is the output under light load, V_f is the peak output voltage and Vi is the initial voltage. For this example, the worst case load step is from 3.75 A to 1.25 A. The output voltage increases during this load transition and the stated maximum in our specification is 4% of the output voltage. This makes V_f = 1.04 × 3.3 V = 3.43 V. V_I is the initial capacitor voltage which is the nominal output voltage of 3.3 V. The values in Equation 36 yield a minimum capacitance of 68 µF.

Equation 37 calculates the minimum output capacitance needed to meet the output voltage ripple specification, where $f$sw is the switching frequency, $V_{ORIPPLE}$ is the maximum allowable output voltage ripple, and I_{RIPPLE} is the inductor ripple current. Equation 37 yields 30 µF.

Equation 38 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. Equation 38 indicates the equivalent ESR should be less than 10 mΩ.

The most stringent criteria for the output capacitor is 95 µF required to maintain the output voltage within regulation tolerance during a load transient.

Capacitance de-ratings for aging, temperature, and DC bias increases this minimum value. For this example, two 100-µF 6.3-V type X5R ceramic capacitors with 2 mΩ of ESR are used. The derated capacitance is 130 µF, well above the minimum required capacitance of 95 µF.

Capacitors are generally rated for a maximum ripple current that can be filtered without degrading capacitor reliability, especially non ceramic capacitors. Some capacitor data sheets specify the Root Mean Square (RMS) value of the maximum ripple current. Equation 39 can calculate the RMS ripple current that the output capacitor must support. For this example, Equation 39 yields 460 mA.

$$C_{OUT} > \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}} = \frac{2 \times 2.5\ \text{A}}{400\ \text{kHz x } 0.13\ \text{V}} = 95\ \mu\text{F} \tag{35}$$

$$C_{OUT} > L_O \times \frac{\left((I_{OH})^2 - (I_{OL})^2\right)}{\left((V_f)^2 - (V_I)^2\right)} = 4.8\ \mu\text{H x } \frac{\left(3.75\ \text{A}^2 - 1.25\ \text{A}^2\right)}{\left(3.43\ \text{V}^2 - 3.3\ \text{V}^2\right)} = 68\ \mu\text{F} \tag{36}$$

$$C_{OUT} > \frac{1}{8 \times f_{SW}} \times \frac{1}{\left(\frac{V_{ORIPPLE}}{I_{RIPPLE}}\right)} = \frac{1}{8\ \text{x } 400\ \text{kHz}}\ \text{x } \frac{1}{\left(\frac{16\ \text{mV}}{1.58\ \text{A}}\right)} = 30\ \mu\text{F} \tag{37}$$

$$R_{ESR} < \frac{V_{ORIPPLE}}{I_{RIPPLE}} = \frac{16\ \text{mV}}{1.58\ \text{A}} = 10\ \text{m}\Omega \tag{38}$$

$$I_{COUT(rms)} = \frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT}\right)}{\sqrt{12} \times V_{IN(max)} \times L_O \times f_{SW}} = \frac{3.3\ \text{V} \times (42\ \text{V} - 3.3\ \text{V})}{\sqrt{12} \times 42\ \text{V} \times 4.8\ \mu\text{H} \times 400\ \text{kHz}} = 460\ \text{mA} \tag{39}$$

8.2.1.2.5 Catch Diode

The TPS54541 device requires an external catch diode between the SW pin and GND. The selected diode must have a reverse voltage rating equal to or greater than $V_{IN(max)}$. The peak current rating of the diode must be greater than the maximum inductor current. Schottky diodes are typically a good choice for the catch diode due to their low forward voltage. The lower the forward voltage of the diode, the higher the efficiency of the regulator.

Typically, diodes with higher voltage and current ratings have higher forward voltages. TI recommends a diode with a minimum of 42-V reverse voltage to allow input voltage transients up to the rated voltage of the TPS54541 device.

For the example design, the PDS760 Schottky diode is selected for its lower forward voltage and good thermal characteristics compared to smaller devices. The typical forward voltage of the PDS760 is 0.52 V at 5 A and 25°C.

The diode must also be selected with an appropriate power rating. The diode conducts the output current during the off-time of the internal power switch. The off-time of the internal switch is a function of the maximum input voltage, the output voltage, and the switching frequency. The output current during the off-time is multiplied by the forward voltage of the diode to calculate the instantaneous conduction losses of the diode. At higher switching frequencies, consider the AC losses of the diode. The AC losses of the diode are due to the charging and discharging of the junction capacitance and reverse recovery charge. Equation 40 calculates the total power dissipation, including conduction losses and AC losses of the diode.

The PDS760 diode has a junction capacitance of 180 pF. Using Equation 40, the total loss in the diode at the nominal input voltage is 1.89 W.

If the power supply spends a significant amount of time at light load currents or in sleep mode, consider using a diode, which has a low leakage current and slightly higher forward voltage drop.

$$P_D = \frac{(V_{IN} - V_{OUT}) \times I_{OUT} \times Vfd}{V_{IN}} + \frac{C_j \times f_{SW} \times (V_{IN} + Vfd)^2}{2} =$$

$$\frac{(12\,V - 3.3\,V) \times 5\,A \times 0.52\,V}{12\,V} + \frac{180\,pF \times 400\,kHz \times (12\,V + 0.52\,V)^2}{2} = 1.89\,W \tag{40}$$

8.2.1.2.6 Input Capacitor

The TPS54541 device requires a high-quality ceramic-type X5R or X7R input decoupling capacitor with at least 3 μF of effective capacitance. Some applications benefit from additional bulk capacitance. The effective capacitance includes any loss of capacitance due to DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS54541 device. Use Equation 41 to calculate the input ripple current.

The value of a ceramic capacitor varies significantly with temperature and the DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is more stable over temperature. X5R and X7R ceramic dielectrics are usually selected for switching regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The input capacitor must also be selected with consideration for the DC bias. The effective value of a capacitor decreases as the DC bias across a capacitor increases.

For this example design, a ceramic capacitor with at least a 42-V voltage rating is required to support transients up to the maximum input voltage. Common standard ceramic capacitor voltage ratings include 4 V, 6.3 V, 10 V, 16 V, 25 V, 50 V, or 100 V. This example uses four 4.7-μF 50-V capacitors in parallel. Table 2 shows several choices of high-voltage capacitors.

The input capacitance value determines the input ripple voltage of the regulator. The maximum input voltage ripple occurs at 50% duty cycle and can be calculated using Equation 42. Using the design example values, I_{OUT} = 5 A, C_{IN} = 18.8 μF, f_{SW} = 400 kHz, yields an input voltage ripple of 170 mV and a rms input ripple current of 2.5 A.

$$I_{CI(rms)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN(min)}} \times \frac{\left(V_{IN(min)} - V_{OUT}\right)}{V_{IN(min)}}} = 5\,A \sqrt{\frac{3.3\,V}{6\,V} \times \frac{(6\,V - 3.3\,V)}{6\,V}} = 2.5\,A \tag{41}$$

$$\Delta V_{IN} = \frac{I_{OUT} \times 0.25}{C_{IN} \times f_{SW}} = \frac{5\,A \times 0.25}{18.8\,\mu F \times 400\,kHz} = 170\,mV \tag{42}$$

Table 2. Capacitor Types

VENDOR	VALUE (μF)	EIA Size	VOLTAGE (V)	DIALECTRIC	COMMENTS
Murata	1 to 2.2	1210	100	X7R	GRM32 series
	1 to 4.7		50		
	1	1206	100		GRM31 series
	1 to 2.2		50		
Vishay	1 to 1.8	2220	50		VJ X7R series
	1 to 1.2		100		
	1 to 3.9	2225	50		
	1 to 1.8		100		
TDK	1 to 2.2	1812	100		C series C4532
	1.5 to 6.8		50		
	1 to 2.2	1210	100		C series C3225
	1 to 3.3		50		
AVX	1 to 4.7	1210	50		X7R dielectric series
	1		100		
	1 to 4.7	1812	50		
	1 to 2.2		100		

8.2.1.2.7 Slow-Start Capacitor

The slow-start capacitor determines the minimum amount of time for the output voltage to reach its nominal programmed value during power up. This is useful if a load requires a controlled voltage slew rate. This capacitor is also used if the output capacitance is large and would require large amounts of current to quickly charge the capacitor to the output voltage level. The large currents necessary to charge the capacitor may make the TPS54541 device reach the current limit or excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output voltage slew rate solves both of these problems.

The slow start time must be long enough to allow the regulator to charge the output capacitor up to the output voltage without drawing excessive current. Equation 43 can be used to find the minimum slow\-start time, T_{ss}, necessary to charge the output capacitor, C_{OUT}, from 10% to 90% of the output voltage, V_{OUT}, with an average slow start current of I_{SSavg}. In the example, to charge the effective output capacitance of 130 µF up to 3.3 V with an average current of 1 A requires a 0.3-ms slow-start time.

When the slow-start time is known, the slow-start capacitor value can be calculated using Equation 5. For the example circuit, the slow-start time is not critical because the output capacitor value is two-times 100 μF which does not require much current to charge to 3.3 V. The example circuit has the slow-start time set to an arbitrary value of 3.5 ms which requires a 9.3-nF slow-start capacitor calculated with Equation 44. For this design, the next larger standard value of 10 nF is used.

$$tss > \frac{Cout \times Vout \times 0.8}{Issavg} \tag{43}$$

$$C_{SS}\ (nF) = \frac{T_{SS}\ (ms) \times I_{SS}\ (\mu A)}{V_{REF}\ (V) \times 0.8} = 3.5\ ms \times \frac{1.7\ \mu A}{(0.8\ V \times 0.8)} = 9.3\ nF \tag{44}$$

8.2.1.2.8 Bootstrap Capacitor Selection

A 0.1-μF ceramic capacitor must be connected between the BOOT and SW pins. TI recommends a ceramic capacitor with X5R or better grade dielectric. The capacitor must have a 10 V or higher voltage rating.

8.2.1.2.9 Undervoltage Lockout Set Point

The Undervoltage Lockout (UVLO) can be adjusted using an external voltage divider on the EN pin of the TPS54541 device. The UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. For the example design, the supply must turn on and start switching when the input voltage increases above 5.75 V (UVLO start). After the regulator starts switching, it must continue until the input voltage falls below 4.5 V (UVLO stop).

Programmable UVLO threshold voltages are set using the resistor divider of R_{UVLO1} and R_{UVLO2} between VIN and ground connected to the EN pin. Equation 3 and Equation 4 calculate the resistance values. For the example application, a 365 kΩ between V_{IN} and EN (R_{UVLO1}) and a 88.7 kΩ between EN and ground (R_{UVLO2}) are required to produce the 5.75-V and 4.5-V start and stop voltages.

$$R_{UVLO1} = \frac{V_{START} - V_{STOP}}{I_{HYS}} = \frac{5.75\ V - 4.5\ V}{3.4\ \mu A} = 368\ k\Omega \tag{45}$$

$$R_{UVLO2} = \frac{V_{ENA}}{\frac{V_{START} - V_{ENA}}{R_{UVLO1}} + I_1} = \frac{1.2\ V}{\frac{5.75\ V - 1.2\ V}{365\ k\Omega} + 1.2\ \mu A} = 88.7\ k\Omega \tag{46}$$

8.2.1.2.10 Output Voltage and Feedback Resistors Selection

The voltage divider of R5 and R6 sets the output voltage. For the example design, 10.2 kΩ was selected for R6. Using Equation 2, R5 is calculated as 31.9 kΩ. The nearest standard 1% resistor is 31.6 kΩ. Due to the input current of the FB pin, the current flowing through the feedback network must be greater than 1 μA to maintain the accuracy of the output voltage. If the value of R6 is less than 800 kΩ, this requirement is satisfied. Choosing higher-resistor values decreases quiescent current and improves efficiency at low-output currents but may also introduce noise immunity problems.

$$R_{HS} = R_{LS} \text{ x } \frac{V_{OUT} - 0.8\ V}{0.8\ V} = 10.2\ k\Omega \text{ x } \left(\frac{3.3\ V - 0.8\ V}{0.8\ V}\right) = 31.9\ k\Omega \tag{47}$$

8.2.1.2.11 Compensation

There are several methods to design compensation for DC-DC regulators. The method is simple to calculate and ignores the effects of the slope compensation that is internal to the device. Because the slope compensation is ignored, the actual crossover frequency is lower than the crossover frequency in the calculations. This method assumes the crossover frequency is between the modulator pole and the ESR zero and the ESR zero is at least ten-times greater the modulator pole.

To get started, calculate the modulator pole, $f_{p(mod)}$, and the ESR zero, f_{z1} using Equation 48 and Equation 49. For C_{OUT}, use a derated value of 130 μF. Use equations Equation 50 and Equation 51 to estimate a starting point for the crossover frequency, f_{co}. For the example, design, $f_{p(mod)}$ is 1850 Hz and $f_{z(mod)}$ is 610 kHz. Equation 49 is the geometric mean of the modulator pole and the ESR zero and Equation 51 is the mean of modulator pole and half of the switching frequency. Equation 50 yields 34 kHz and Equation 51 gives 19 kHz. Use the geometric mean value of Equation 50 and Equation 51 for an initial crossover frequency. For this example, after lab measurement, the crossover frequency target increased to 30 kHz for an improved transient response.

Next, calculate the compensation components. A resistor in series with a capacitor creates a compensating zero. In parallel to these two components, a capacitor forms the compensating pole.

$$f_{P(mod)} = \frac{I_{OUT(max)}}{2 \times \pi \times V_{OUT} \times C_{OUT}} = \frac{5\ A}{2 \times \pi \times 3.3\ V \times 130\ \mu F} = 1850\ Hz \tag{48}$$

$$f_{Z(mod)} = \frac{1}{2 \times \pi \times R_{ESR} \times C_{OUT}} = \frac{1}{2 \times \pi \times 1\ m\Omega \times 130\ \mu F} = 610\ kHz \tag{49}$$

$$f_{co1} = \sqrt{f_{p(mod)} \text{ x } f_{z(mod)}} = \sqrt{1850\ Hz \text{ x } 610\ kHz} = 34\ kHz \tag{50}$$

$$f_{co2} = \sqrt{f_{p(mod)} \text{ x } \frac{f_{SW}}{2}} = \sqrt{1850\ Hz \text{ x } \frac{400\ kHz}{2}} = 19\ kHz \tag{51}$$

To determine the compensation resistor, R4, use Equation 52. The typical power stage transconductance, gmps, is 17 A/V. The output voltage, V_O, reference voltage, V_{REF}, and amplifier transconductance, gmea, are 3.3 V, 0.8 V and 350 μA/V, respectively. R4 is calculated to be 17 kΩ and a standard value of 16.9 kΩ is selected. Use Equation 53 to set the compensation zero to the modulator pole frequency. Equation 53 yields 5100 pF for compensating capacitor C5. 4700 pF is used for this design.

$$R4 = \left(\frac{2 \times \pi \times f_{co} \times C_{OUT}}{gm_{ps}}\right) \times \left(\frac{V_{OUT}}{V_{REF} \text{ x } gm_{ea}}\right) = \left(\frac{2 \times \pi \times 30\ kHz \times 130\ \mu F}{17\ A / V}\right) \times \left(\frac{3.3\ V}{0.8\ V \times 350\ \mu A / V}\right) = 17\ k\Omega$$

(52)

$$C5 = \frac{1}{2 \times \pi \times R4 \text{ x } f_{p(mod)}} = \frac{1}{2 \times \pi \times 16.9 \text{ k}\Omega \text{ x } 1850 \text{ Hz}} = 5100 \text{ pF}$$ (53)

A compensation pole can be implemented by adding capacitor C8 in parallel with the series combination of R4 and C5. Use the larger value calculated from Equation 54 and Equation 55 for C8 to set the compensation pole. The value of C8 is 47 pF for this design example.

$$C8 = \frac{C_{OUT} \text{ x } R_{ESR}}{R4} = \frac{130 \text{ }\mu\text{F x } 1 \text{ m}\Omega}{16.9 \text{ k}\Omega} = 15 \text{ pF}$$ (54)

$$C8 = \frac{1}{R4 \times f_{sw} \times \pi} = \frac{1}{16.9 \text{ k}\Omega \times 400 \text{ kHz} \times \pi} = 47 \text{ pF}$$ (55)

8.2.1.2.12 Power Dissipation Estimate

The following formulas estimate the TPS54541 power dissipation under CCM operation. Do not use these equations if the device is operating in DCM.

The power dissipation of the IC includes conduction loss (P_{COND}), switching loss (P_{SW}), gate drive loss (P_{GD}), and supply current (P_Q). Example calculations are shown with the 12-V typical input voltage of the design example.

$$P_{COND} = (I_{OUT})^2 \times R_{DS(on)} \times \left(\frac{V_{OUT}}{V_{IN}}\right) = 5 \text{ A}^2 \times 87 \text{ m}\Omega \times \frac{5 \text{ V}}{12 \text{ V}} = 0.958 \text{ W}$$ (56)

$$P_{SW} = V_{IN} \times f_{SW} \times I_{OUT} \times t_{rise} = 12 \text{ V} \times 400 \text{ kHz} \times 5 \text{ A} \times 4.9 \text{ ns} = 0.118 \text{ W}$$ (57)

$$P_{GD} = V_{IN} \times Q_G \times f_{SW} = 12 \text{ V} \times 3\text{nC} \times 400 \text{ kHz} = 0.014 \text{ W}$$ (58)

$$P_Q = V_{IN} \times I_Q = 12 \text{ V} \times 146 \text{ }\mu\text{A} = 0.0018 \text{ W}$$

where (for Equation 56, Equation 57, Equation 58, and Equation 59)

- I_{OUT} is the output current (A)
- $R_{DS(on)}$ is the on-resistance of the high-side MOSFET (Ω)
- V_{OUT} is the output voltage (V)
- V_{IN} is the input voltage (V)
- f_{sw} is the switching frequency (Hz)
- t_{rise} is the SW pin voltage rise time and can be estimated by trise = V_{IN} x 0.16 ns/V + 3 ns
- Q_G is the total gate charge of the internal MOSFET
- I_Q is the operating nonswitching supply current (59)

Therefore,

$$P_{TOT} = P_{COND} + P_{SW} + P_{GD} + P_Q = 0.958 \text{ W} + 0.118 \text{ W} + 0.014 \text{ W} + 0.0018 \text{ W} = 1.092 \text{ W}$$ (60)

For given T_A,

$$T_J = T_A + R_{TH} \times P_{TOT}$$ (61)

For given $T_{J(MAX)}$ = 150°C

$$T_{A(max)} = T_{J(max)} - R_{TH} \times P_{TOT}$$

where (for Equation 60, Equation 61, and Equation 62)

- P_{TOT} is the total device power dissipation (W)
- T_A is the ambient temperature (°C)
- T_J is the junction temperature (°C)
- R_{TH} is the thermal resistance from junction to ambient for a given PCB layout (°C/W)
- $T_{J(MAX)}$ is maximum junction temperature (°C)
- $T_{A(MAX)}$ is maximum ambient temperature (°C) (62)

Additional power loss occurs in the regulator circuit due to the inductor ac and dc losses and the catch diode and PCB trace resistance impacting the overall efficiency of the regulator.

8.2.1.2.13 Safe Operating Area

Figure 47 shows the safe operating area (SOA) of a typical design, through Figure 50 for 3.3-V, 5-V, and 12-V outputs and varying amounts of forced air flow. The temperature-derating curves represent the conditions at which the internal components and external components are at or below the maximum operating temperatures of the manufacturer. Derating limits apply to devices soldered directly to a double-sided PCB with 2-oz copper, similar to the EVM. Pay attention to the other components chosen for the design, especially the catch diode. In most applications, the thermal performance is limited by the catch diode. When operating at high-duty cycles or in the high end of the switching frequency range, the thermal performance of the TPS54541 can be the limiting factor.

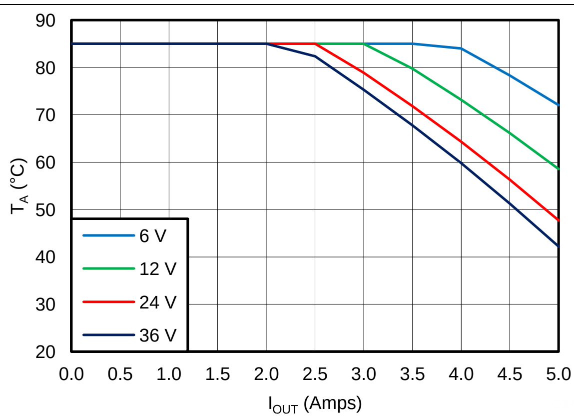


Figure 47. 3.3-V Outputs

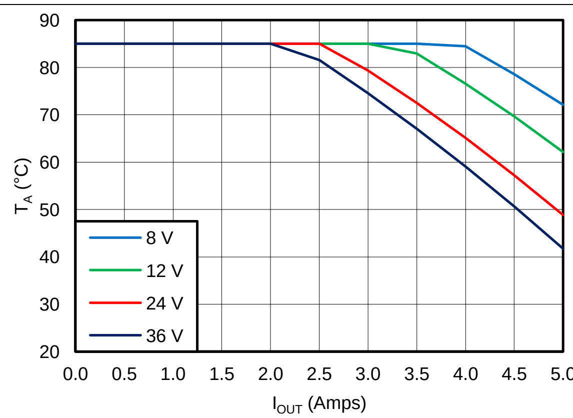


Figure 48. 5-V Outputs

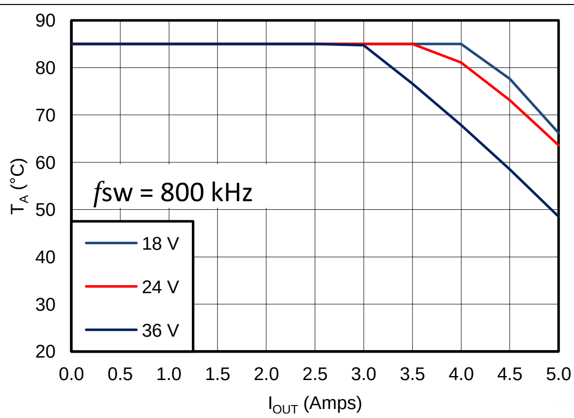


Figure 49. 12-V Outputs

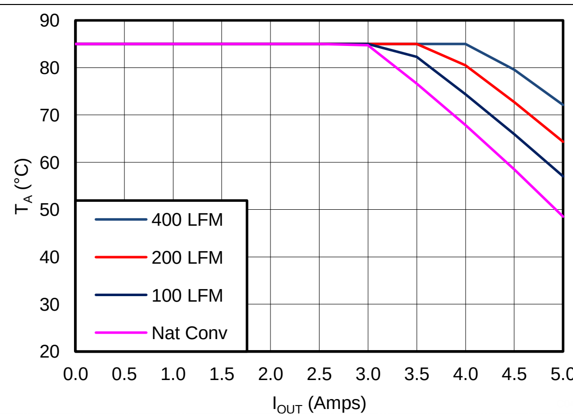


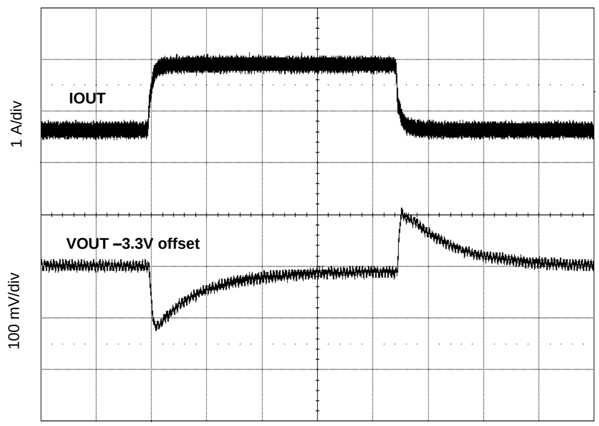
Figure 50. Air Flow Conditions
V_{IN} = 36 V, V_O = 12 V, fsw = 800 kHz

8.2.1.2.14 Discontinuous Conduction Mode and Eco-mode Boundary

With an input voltage of 12 V, the power supply enters discontinuous conduction mode when the output current is less than 560 mA. The power supply enters Eco-mode when the output current is lower than 18 mA. The input current draw is 260 μA with no load.

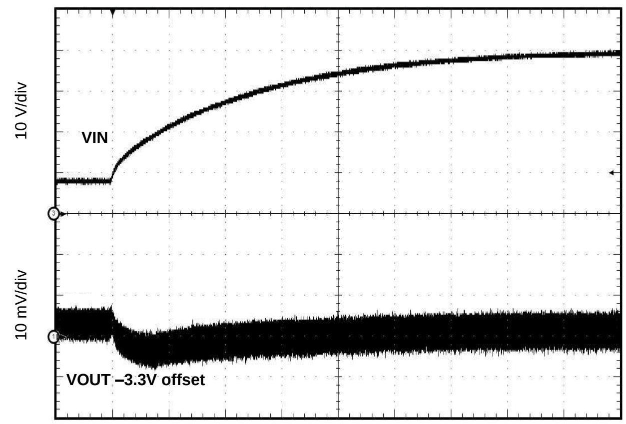
8.2.1.3 Application Curves

Measurements are taken with standard EVM using a 12-V input, 3.3-V output, and 5-A load unless otherwise noted.



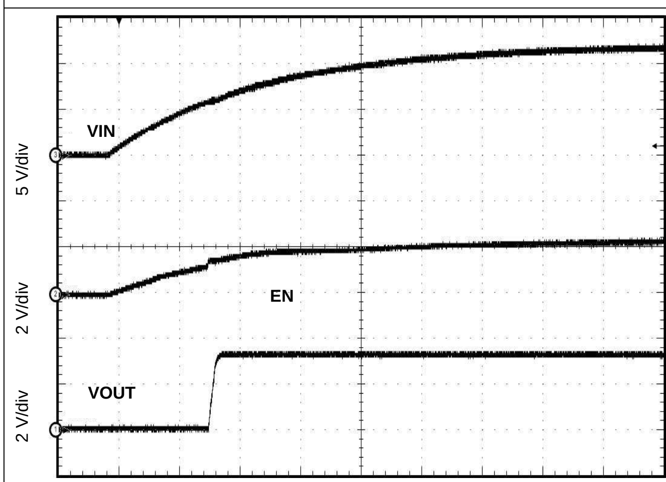
Time = 100 μs/div

Figure 51. Load Transient



Time = 4 ms/div

Figure 52. Line Transient (8 V to 40 V)



Time = 20 ms/div

Figure 53. Start-up With VIN

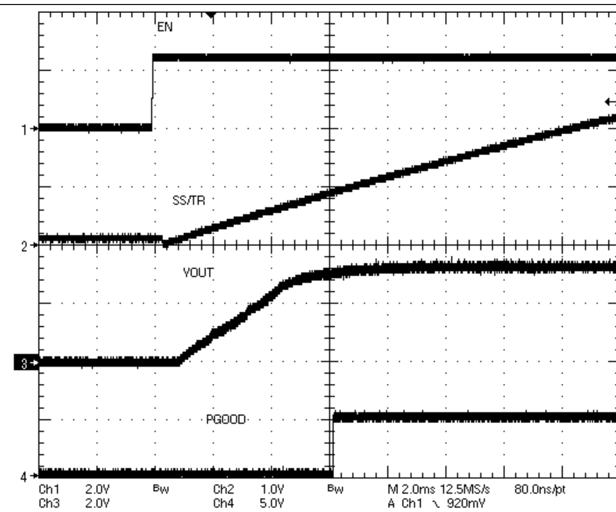


Figure 54. Start-up With EN

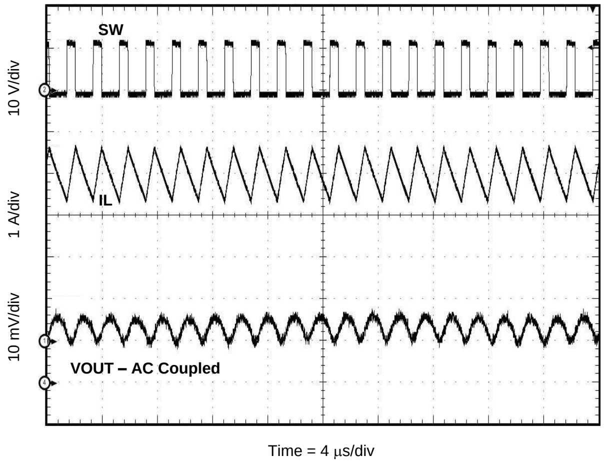


Figure 55. Output Ripple CCM

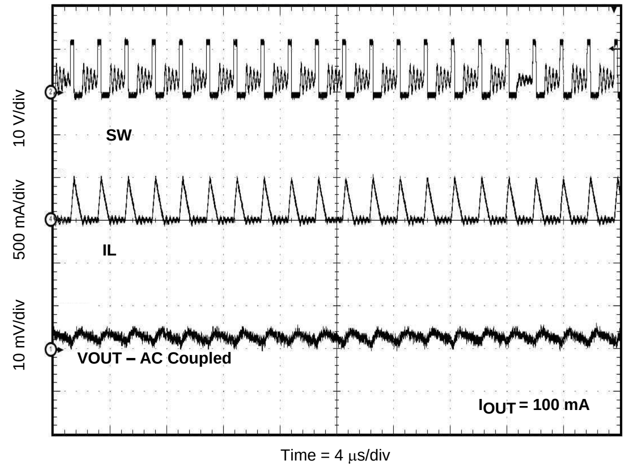


Figure 56. Output Ripple DCM

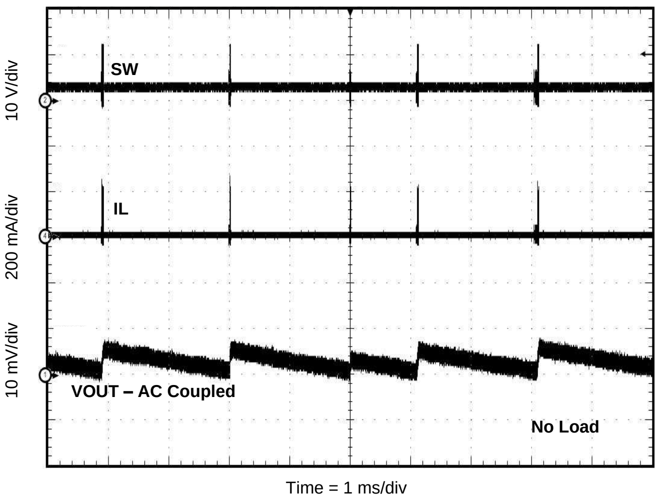


Figure 57. Output Ripple PSM

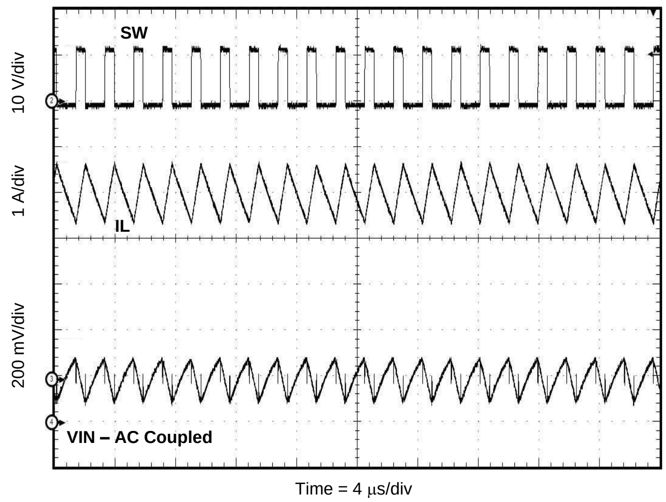


Figure 58. Input Ripple CCM

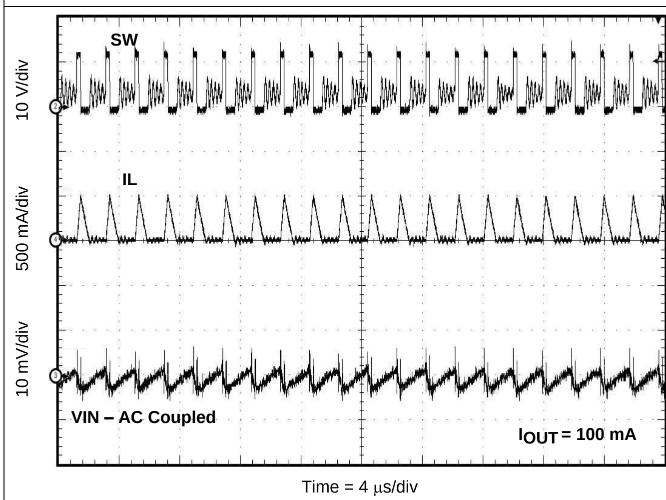


Figure 59. Input Ripple DCM

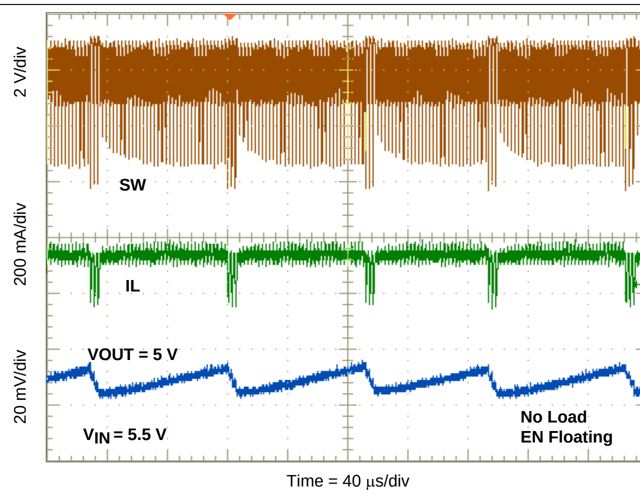


Figure 60. Low Dropout Operation

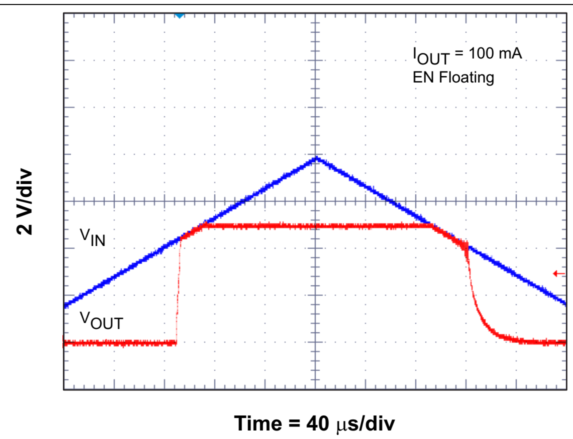


Figure 61. Low Dropout Operation

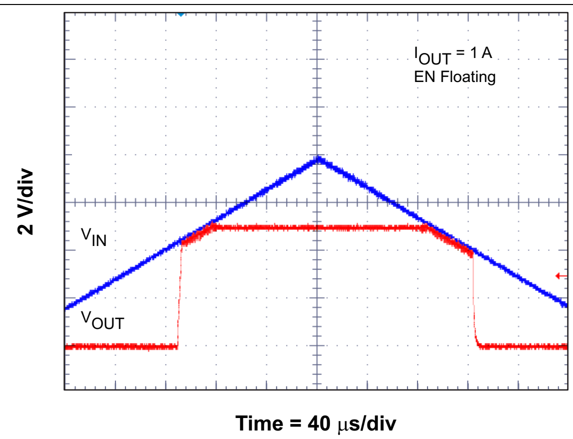


Figure 62. Low Dropout Operation

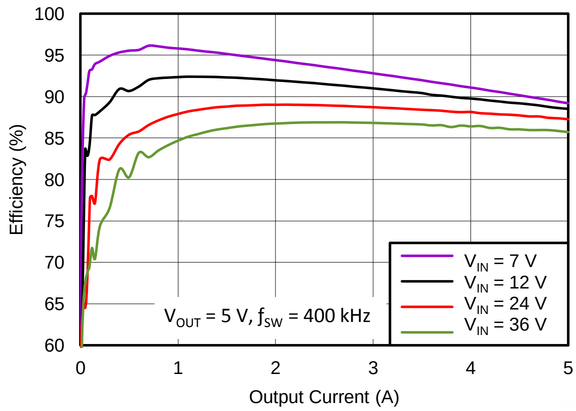


Figure 63. Efficiency vs Load Current

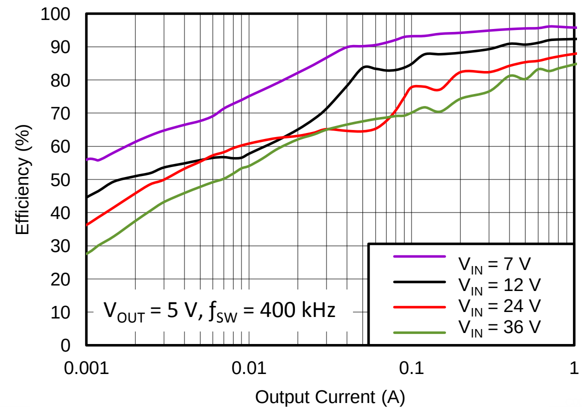


Figure 64. Light Load Efficiency

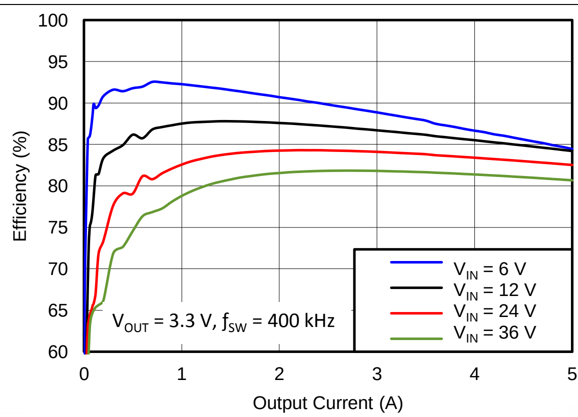


Figure 65. Efficiency vs Load Current

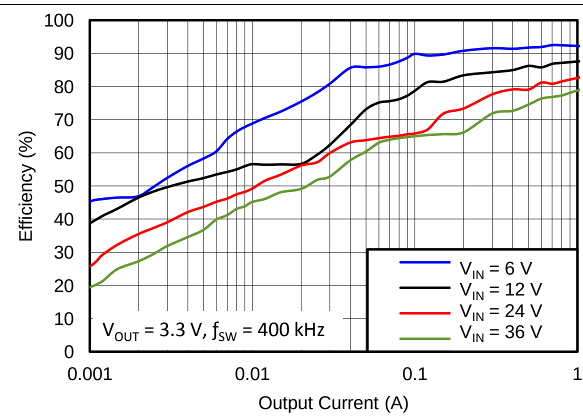


Figure 66. Light Load Efficiency

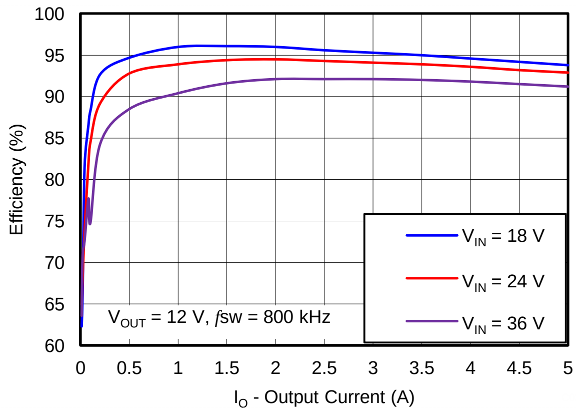


Figure 67. Efficiency vs Output Current

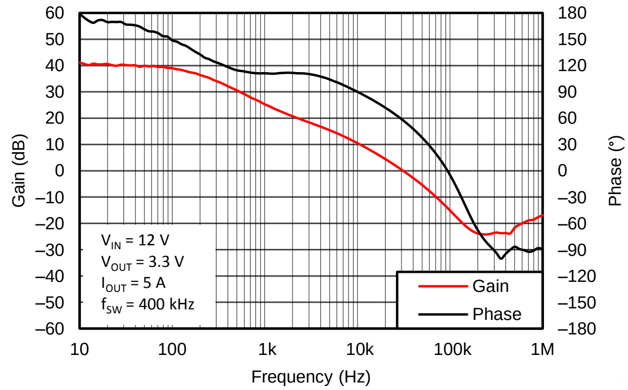


Figure 68. Overall Loop Frequency Response

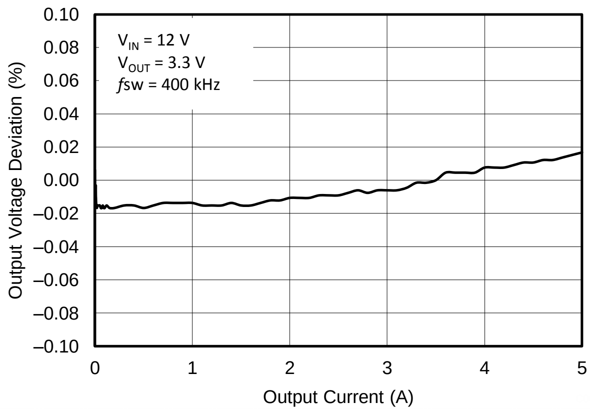


Figure 69. Regulation vs Load Current

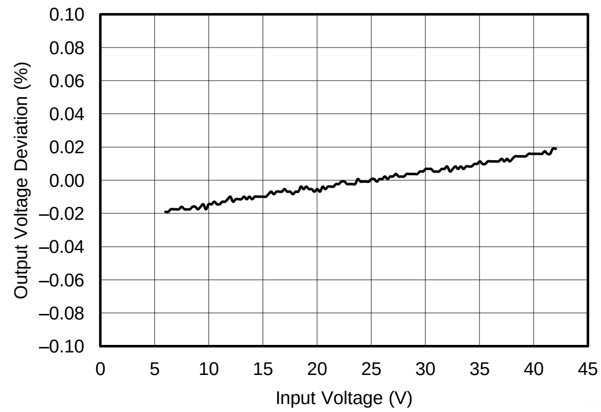


Figure 70. Regulation vs Input Voltage

8.2.2 Inverting Buck-Boost Topology for Positive Input to Negative Output

The TPS54541 can be used to convert a positive input voltage to a negative output voltage. An example application is an amplifier requiring a negative power supply. For a more detailed example, see SLVA317.

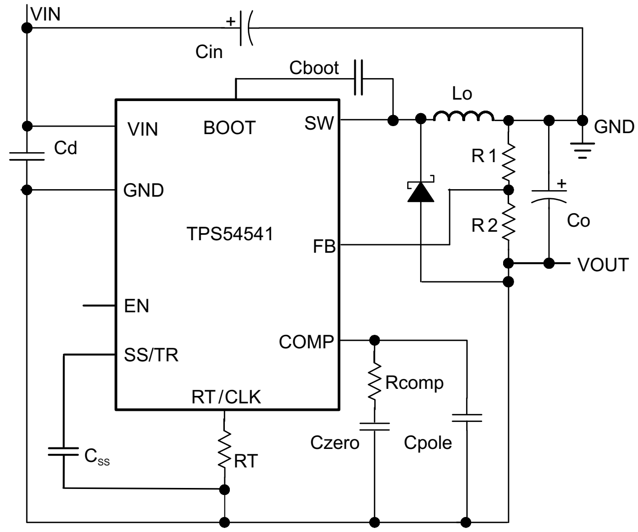


Figure 71. TPS54541 Inverting Power Supply Based on the Application Note, SLVA317

8.2.3 Split-Rail Topology for Positive Input to Negative and Positive Output

The TPS54541 can be used to convert a positive input voltage to a split rail positive and negative output voltage by using a coupled inductor. An example application is an amplifier requiring a split rail positive and negative voltage power supply. For a more detailed example, see SLVA369.

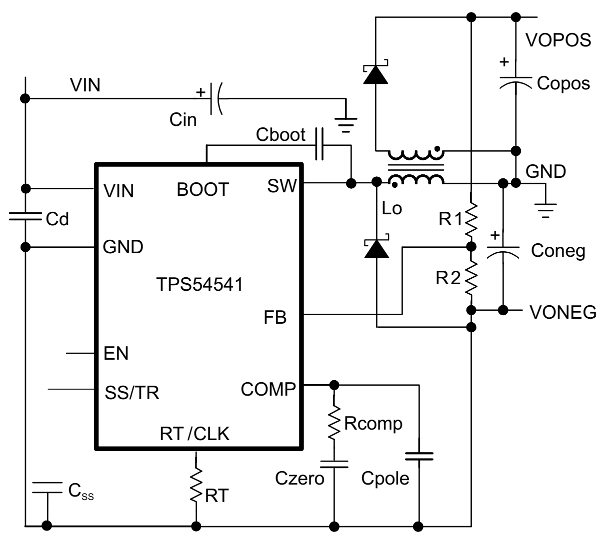


Figure 72. TPS54541 Split Rail Power Supply Based on the Application Note, SLVA369

9 Power Supply Recommendations

The design of the device is for operation from an power supply range between 4.5 V and 42 V. The power supply voltage must remain within this range. If the power supply is more distant than a few inches from the TPS54541 converter, the circuit may require additional bulk capacitance besides the ceramic bypass capacitors. An electrolytic capacitor with a value of 100 µF is a typical choice.

10 Layout

10.1 Layout Guidelines

Layout is a critical portion of good power supply design. There are several signal paths that conduct fast-changing currents or voltages that interact with stray inductance or parasitic capacitance to generate noise or degrade performance. To reduce parasitic effects, bypass the VIN pin to ground with a low-ESR ceramic bypass-capacitor with X5R or X7R dielectric. Minimize the loop area formed by the bypass-capacitor connections, the VIN pin, and the anode of the catch diode. See Figure 73 for a PCB layout example. Tie the GND pin directly to the thermal pad under the IC.

Connect the thermal pad to internal PCB ground planes using multiple vias directly under the IC. Route the SW pin to the cathode of the catch diode and to the output inductor. Because the SW connection is the switching node, locate the catch diode and output inductor close to the SW pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. For operation at full rated load, ensure the top-side ground area provides adequate heat dissipating area. The RT/CLK pin is sensitive to noise so locate and rout the RT resistor as close as possible to the IC with minimal lengths of trace, respectively. The additional external components are placed approximately as shown. Obtaining acceptable performance with alternate PCB layouts is possible, however this layout produces good results and TI intends it as a guideline.

10.2 Layout Example

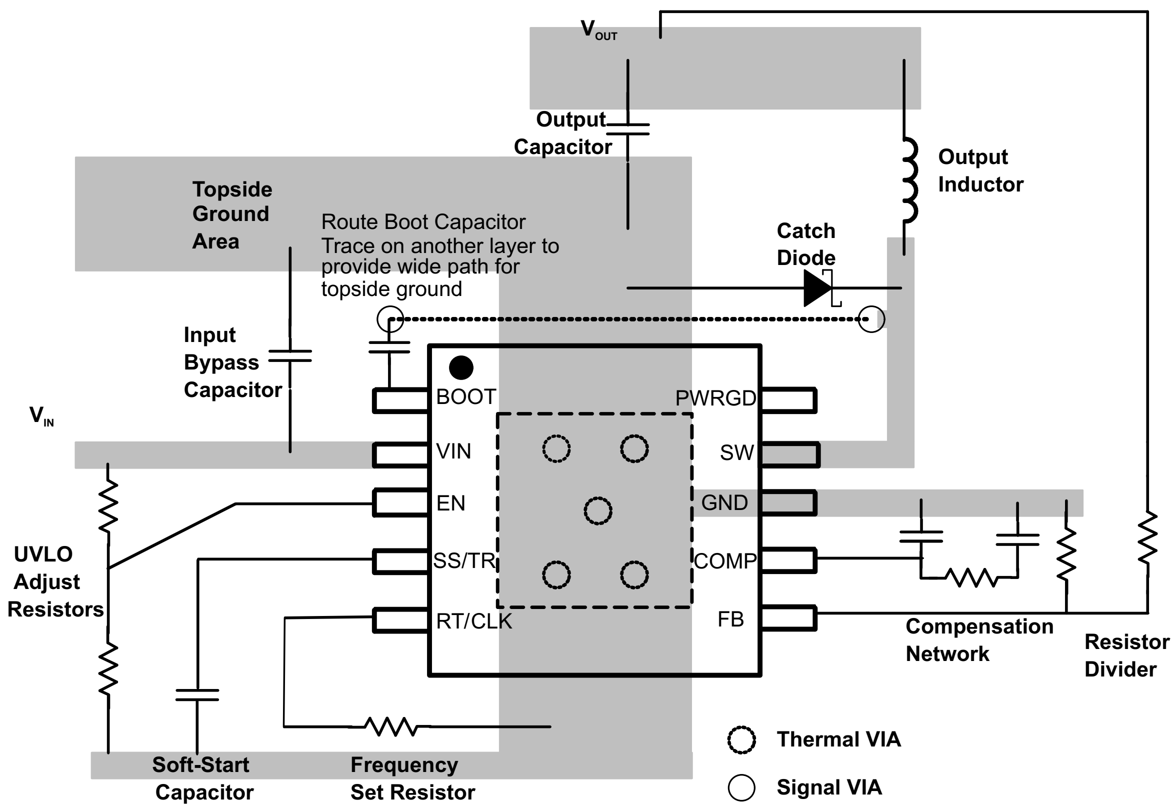


Figure 73. PCB Layout Example

10.3 Estimated Circuit Area

Boxing in the components in the design of Figure 46 the estimated printed circuit board area is 1.025 in^2 (661 mm^2). This area does not include test points or connectors.

11 器件和文档支持

11.1 器件支持

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.1.2 开发支持

有关 TPS54540、TPS54541 和 TPS54541-Q1 系列 Excel 设计工具的信息，请参见 SLVC452。

11.2 文档支持

11.2.1 相关文档

相关文档如下：

- *《使用降压稳压器创建反向电源》*，SLVA317
- *《使用宽范围输入电压降压稳压器创建分离轨电源》*，SLVA369
- *《针对 TPS54541 降压转换器的评估模块》*，SLVU990
- *《利用 TPS54240 和 TPS2511 制作供 USB 设备使用的通用车载充电器》*，SLVA464
- *《基于 TPS54260 创建 GSM/GPRS 电源》*，SLVA412

11.2.2 《使用 **WEBENCH®** 工具定制设计方案》

请单击此处，借助 WEBENCH®Power Designer 并使用 TPS54541 器件定制设计方案。

1. 首先输入您的 V_{IN}、V_{OUT} 和 I_{OUT} 要求。
2. 使用优化器拨盘可优化效率、封装和成本等关键设计参数并将您的设计与德州仪器 (TI) 的其他可行解决方案进行比较。
3. WEBENCH Power Designer 提供一份定制原理图以及罗列实时价格和组件可用性的物料清单。
4. 在多数情况下，您还可以：
   – 运行电气仿真，观察重要波形以及电路性能
   – 运行热性能仿真，了解电路板热性能
   – 将定制原理图和布局方案导出至常用 CAD 格式
   – 打印设计方案的 PDF 报告并与同事共享
5. 有关 WEBENCH 工具的详细信息，请访问 www.ti.com/WEBENCH。

11.3 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

11.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 商标

11.5 商标 (接下页)

Eco-mode。, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.

11.6 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54541DPRR	ACTIVE	WSON	DPR	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 54541	Samples
TPS54541DPRT	ACTIVE	WSON	DPR	10	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS 54541	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

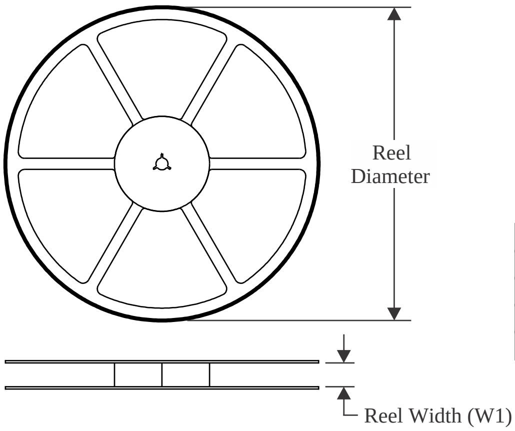
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

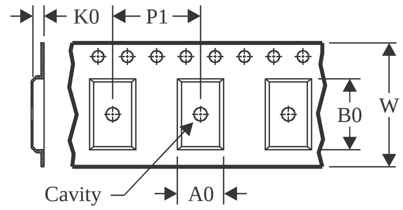
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

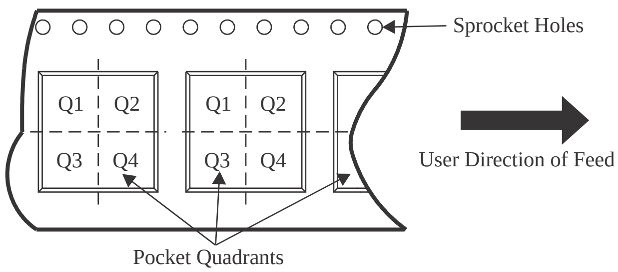


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

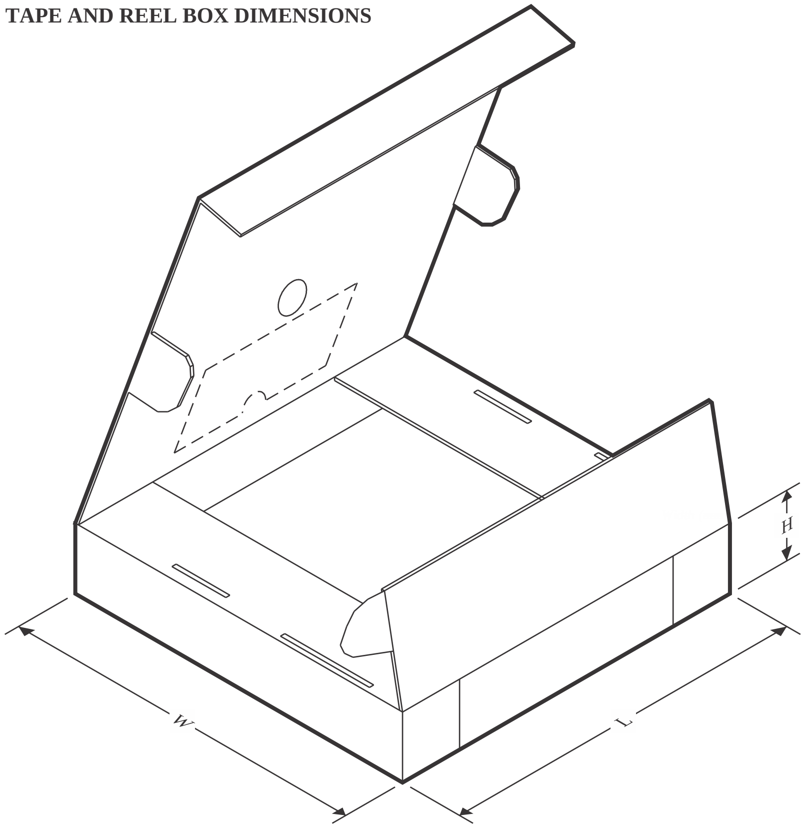
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

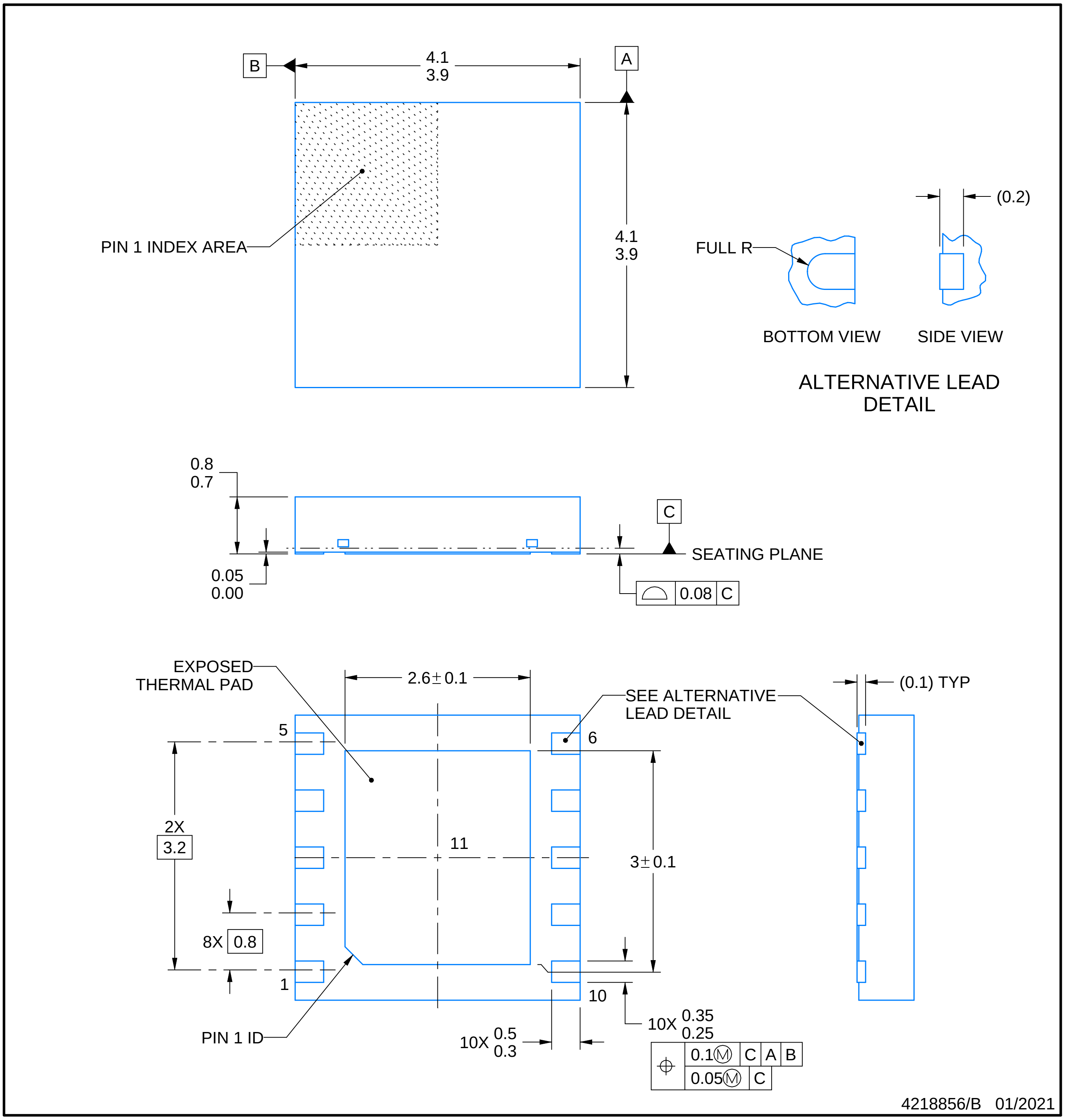
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54541DPRR	WSON	DPR	10	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS54541DPRT	WSON	DPR	10	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



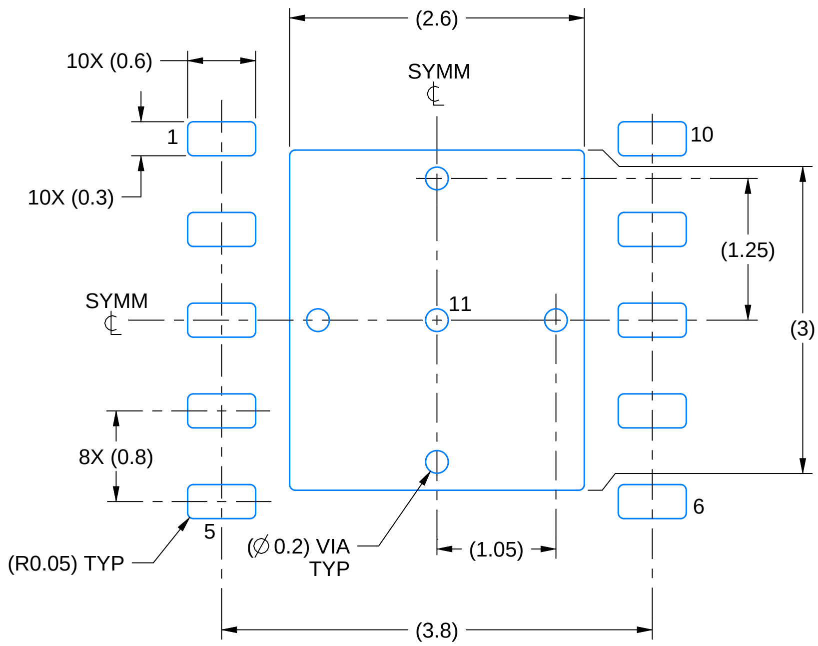
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54541DPRR	WSON	DPR	10	3000	346.0	346.0	33.0
TPS54541DPRT	WSON	DPR	10	250	210.0	185.0	35.0

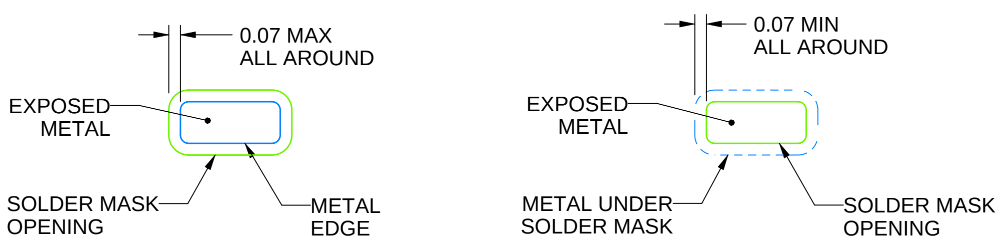


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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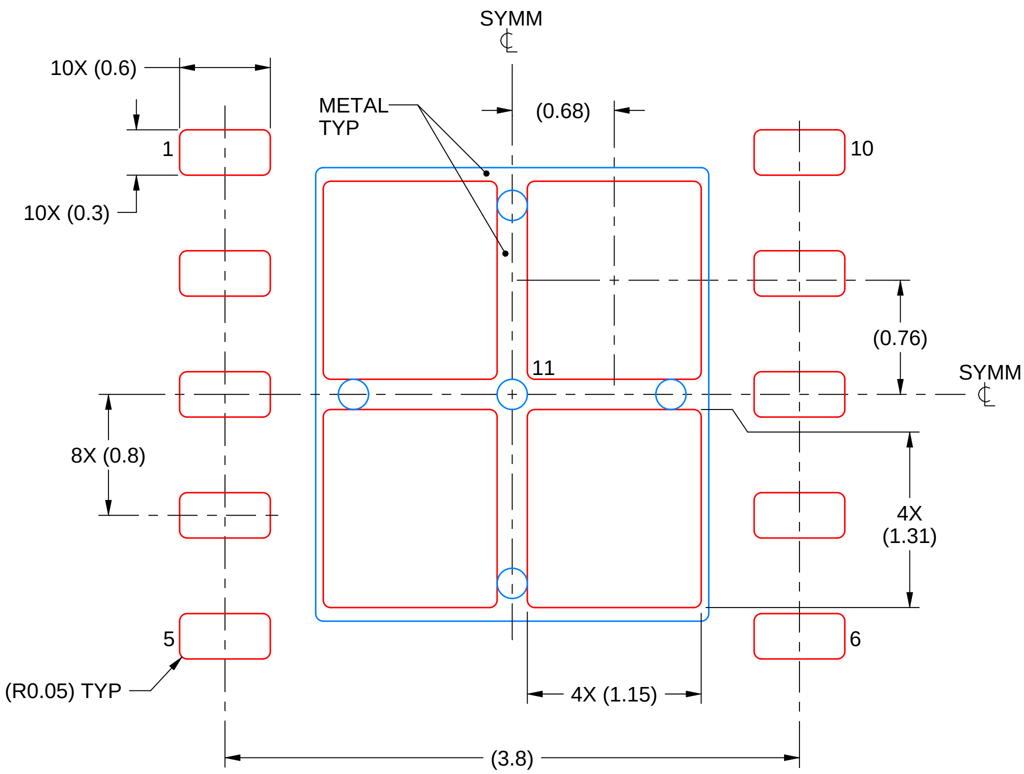
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
77% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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