TPS61093 低输入升压转换器，具有集成式功率二极管和输入/输出隔离功能

1 特性

- 输入范围：1.6V 至 6V
- 集成式功率二极管和隔离 FET
- 1.1A、20V 内部开关 FET
- 1.2MHz 固定开关频率
- 15V 输出电压时，效率高达 88%
- 过载和过压保护
- 可编程软启动
- IC 关断之后的负载放电路径
- 2.5mm × 2.5mm × 0.8mm WSON 封装
- 使用 TPS61093 并借助 WEBENCH® 电源设计器进行定制设计

2 应用

- 血糖仪
- OLED 电源
- 3.3V 至 12V、5V 至 12V 升压转换器

3 说明

TPS61093 是一款兼具高集成度和高可靠性的 1.2MHz 固定频率升压转换器。该集成电路 (IC) 集成有 20V 电源开关、输入/输出隔离开关以及功率二极管。当输出电流超过过载限制时，IC 的隔离开关打开，以将输出与输入断开，从而保护 IC 和输入电源。在关断期间，隔离开关也会断开输出与输入之间的连接，以更大限度降低泄漏电流。当 IC 关断时，输出电容会通过内部二极管放电至低电压电平。其他保护 特性 包括每个周期 1.1A 峰值过流保护 (OCP)、输出过压保护 (OVP)、热关断以及欠压锁定 (UVLO)。

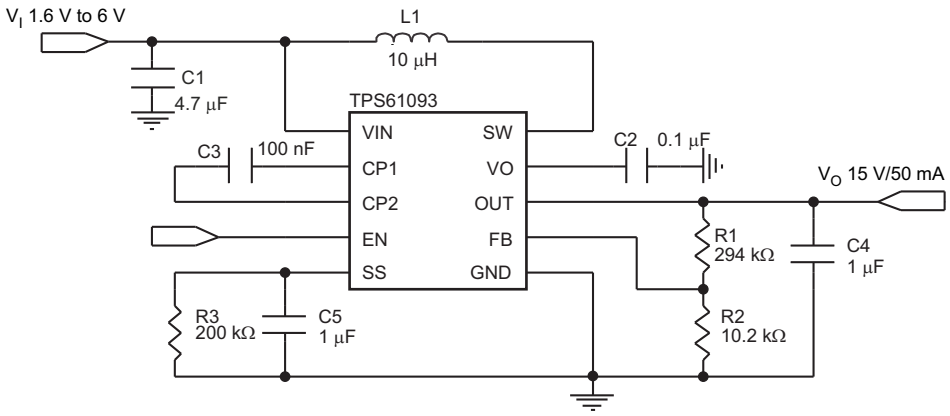
IC 的最低输入电压为 1.6V，可通过两个碱性电池、单个锂离子电池或者 3.3V 和 5V 稳压电源供电运行。输出电压最高可升压至 17V。TPS61093 可采用带有散热垫的 2.5mm × 2.5mm VSON 封装。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS61093	WSON (10)	2.50mm x 2.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



目录

4 修订历史记录

Changes from Revision C (June 2015) to Revision D **Page**

- 已添加 Webench 链接 ... 1
- Changed *Shutdown and Load Discharge* output voltage value from "3.3 V" to "4.3 V" ... 8

Changes from Revision B (December 2014) to Revision C **Page**

- 将*特性* 中的“VSON 封装”更改为“WSON 封装” ... 1
- Changed the pinout title From "QFN Package 10 Pins" To: "DSK Package 10 Pins (WSON)" ... 3
- Changed "VSON" to "WSON" in the *Thermal Information* table ... 5
- Deleted the *Dissipation Ratings* table ... 5

Changes from Revision A (October 2009) to Revision B **Page**

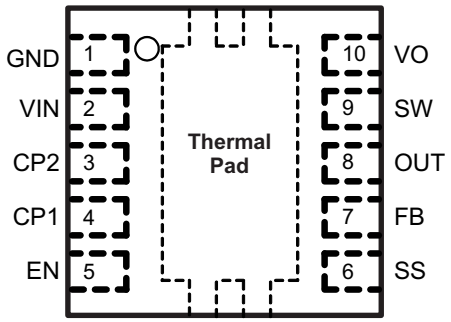
- 已添加 *ESD 额定值* 表、*特性 说明* 部分、*器件功能模式*、*应用和实施* 部分、*电源建议* 部分、*布局* 部分、*器件和文档支持* 部分以及*机械、封装和可订购信息* 部分 ... 1

Changes from Original (September 2009) to Revision A **Page**

- Added information to OPERATION description ... 7
- Changed *Output Program* description ... 10
- Changed *Output Program* equations ... 10

5 Pin Configuration and Functions

DSK Package
10 Pins (WSON)
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
CP1, CP2	3, 4		Connect to flying capacitor for internal charge pump.
EN	5	I	Enable pin (HIGH = enable). When the pin is pulled low for 1 ms, the IC turns off and consumes less than 1-μA current.
FB	7	I	Voltage feedback pin for output regulation, 0.5-V regulated voltage. An external resistor divider connected to this pin programs the regulated output voltage.
GND	1	–	Ground of the IC.
OUT	8	O	Isolation switch is between this pin and VO pin. Connect load to this pin for input/output isolation during IC shutdown. See *Without Isolation FET* for the tradeoff between isolation and efficiency.
SS	6	I	Soft start pin. A RC network connecting to the SS pin programs soft start timing. See *Start-Up*.
SW	9	I	Switching node of the IC where the internal PWM switch operates.
Thermal Pad	–	–	It should be soldered to the ground plane. If possible, use thermal via to connect to ground plane for ideal power dissipation.
VIN	2	I	IC Supply voltage input.
VO	10	O	Output of the boost converter. When the output voltage exceeds the overvoltage protection (OVP) threshold, the power switch turns off until VO drops below the overvoltage protection hysteresis.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) (1)

		MIN	MAX	UNIT
	Supply voltage on pin VIN (2)	–0.3	7	V
	Voltage on pins CP2, EN, and SS (2)	–0.3	7	V
	Voltage on pin CP1 and FB (2)	–0.3	3	V
	Voltage on pin SW, VO, and OUT (2)	–0.3	20	V
T_A	Operating temperature	–40	85	°C
T_J	Maximum operating junction temperature		150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_i	Input voltage range	1.6		6	V
V_o	Output voltage range at VO pin			17	V
L	Inductor (1)	2.2	4.7	10	µH
C_{in}	Input capacitor	4.7			µF
C_o	Output capacitor at OUT pin (1)	1		10	µF
C_{fly}	Flying capacitor at CP1 and CP2 pins	10			nF
T_J	Operating junction temperature	–40		125	°C
T_A	Operating free-air temperature	–40		85	°C

(1) These values are recommended values that have been successfully tested in several applications. Other values may be acceptable in other applications but should be fully tested by the user.

6.4 Thermal Information

THERMAL METRIC (1)		TPS61093 WSON 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	23.4	
ψ_{JT}	Junction-to-top characterization parameter	1.1	
ψ_{JB}	Junction-to-board characterization parameter	23.0	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

VIN = 3.6 V, EN = VIN, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_{IN}	Input voltage range, VIN		1.6		6	V
I_Q	Operating quiescent current into VIN	Device PWM switching no load		0.9	1.5	mA
I_{SD}	Shutdown current	EN = GND, VIN = 6 V			1	µA
UVLO	Undervoltage lockout threshold	VIN falling		1.5	1.55	V
V_{hys}	Undervoltage lockout hysterisis			50		mV
ENABLE AND PWM CONTROL						
V_{ENH}	EN logic high voltage	VIN = 1.6 V to 6 V	1.2			V
V_{ENL}	EN logic low voltage	VIN = 1.6 V to 6 V			0.3	V
R_{EN}	EN pull down resistor		400	800	1600	kΩ
T_{off}	EN pulse width to shutdown	EN high to low			1	ms
VOLTAGE CONTROL						
V_{REF}	Voltage feedback regulation voltage		0.49	0.5	0.51	V
I_{FB}	Voltage feedback input bias current				100	nA
f_S	Oscillator frequency		1.0	1.2	1.4	MHz
D_{max}	Maximum duty cycle	V_{FB} = 0.1 V, T_A = 85°C	90%	93%		
T_{min_on}	Minimum on pulse width			65		ns
POWER SWITCH, ISOLATION FET						
$R_{DS(ON)N}$	N-channel MOSFET on-resistance	VIN = 3 V		0.25	0.4	Ω
$R_{DS(ON)iso}$	Isolation FET on-resistance	VO = 5 V		2.5	4	Ω
		VO = 3.5 V		4.5		
I_{LN_N}	N-channel leakage current	V_{DS} = 20 V, T_A = 25°C			1	µA
I_{LN_iso}	Isolation FET leakage current	V_{DS} = 20 V, T_A = 25°C			1	µA
V_F	Power diode forward voltage	Current = 500 mA		0.8		V
OC, ILIM, OVP SC AND SS						
I_{LIM}	N-Channel MOSFET current limit		0.9	1.1	1.5	A
V_{ovp}	Overvoltage protection threshold	Measured on the VO pin	18	19		V
V_{ovp_hys}	Overvoltage protection hysteresis			0.6		V
I_{OL}	Overload protection		200	300		mA
THERMAL SHUTDOWN						
$T_{shutdown}$	Thermal shutdown threshold			150		°C
$T_{hysteresis}$	Thermal shutdown hysteresis			15		°C

6.6 Typical Characteristics

Table 1. Table Of Graphs

Figure 1, L = TOKO #A915_Y-100M, unless otherwise noted			FIGURE
η	Efficiency	vs Load current at OUT = 15 V	Figure 1
η	Efficiency	vs Load current at OUT = 10 V	Figure 2
V_{FB}	FB voltage	vs Free-air temperature	Figure 3
V_{FB}	FB voltage	vs Input voltage	Figure 4
I_{LIM}	Switch current limit	vs Free-air temperature	Figure 5

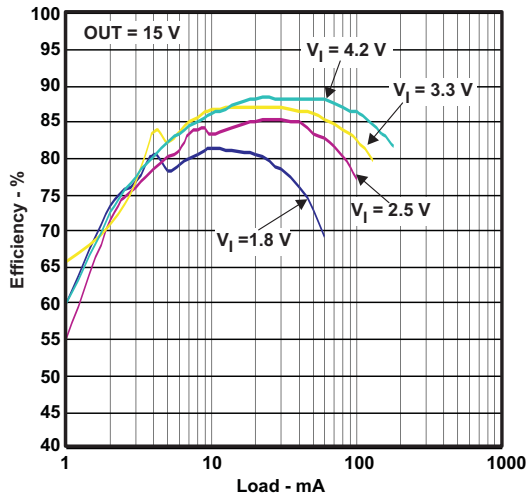


Figure 1. Efficiency vs Load

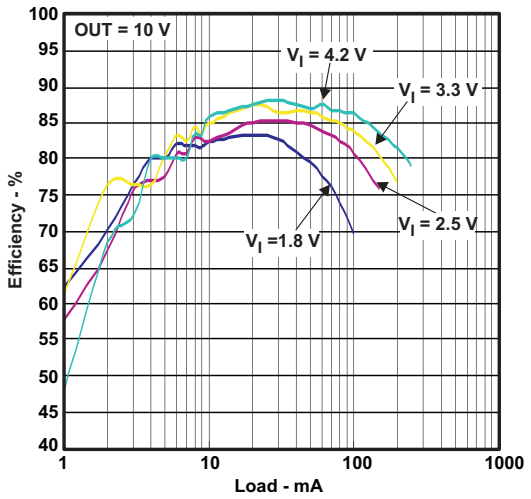


Figure 2. Efficiency vs Load

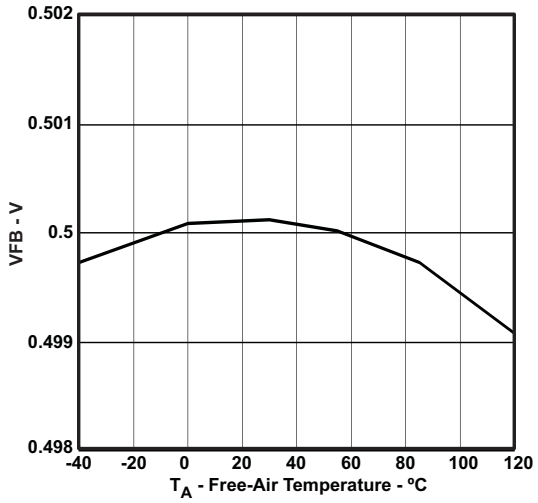


Figure 3. FB Voltage vs Free-Air Temperature

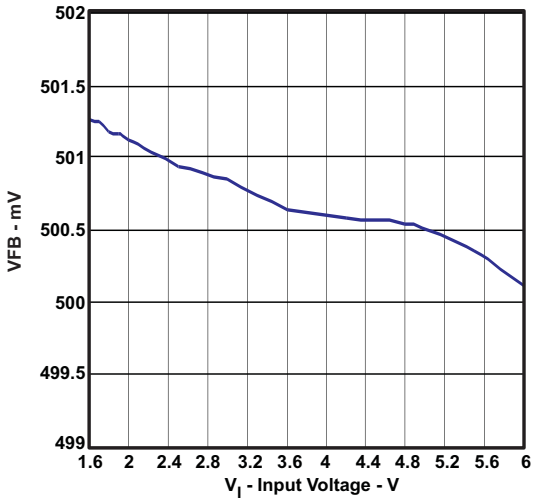


Figure 4. FB Voltage vs Input Voltage

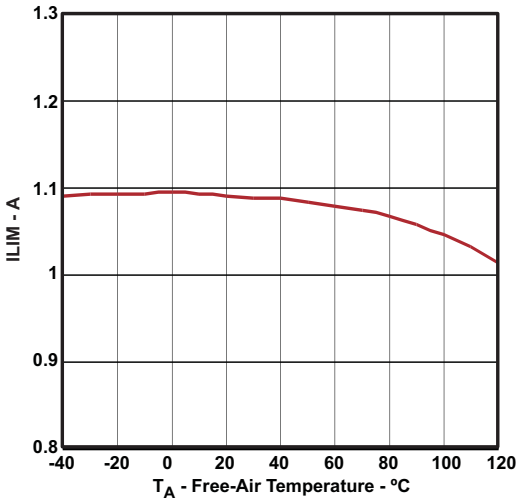


Figure 5. Switch Current Limit vs Free-Air Temperature

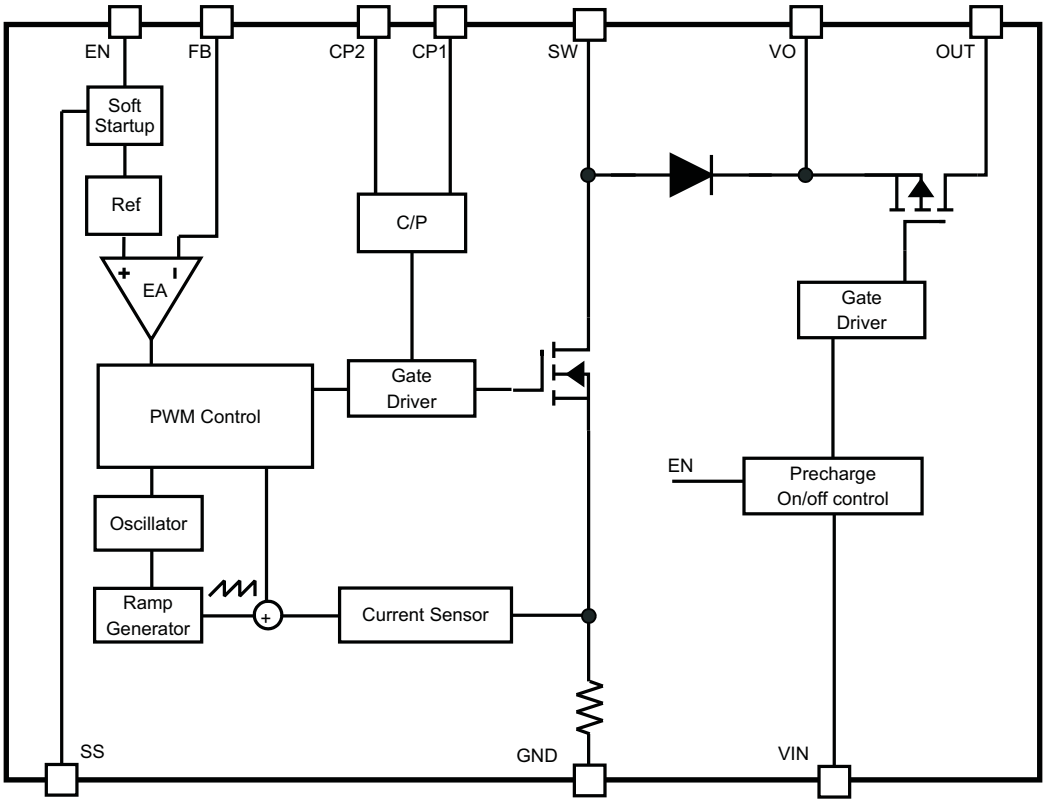
7 Detailed Description

7.1 Overview

The TPS61093 is a highly integrated boost regulator for up to 17-V output. In addition to the on-chip 1-A PWM switch and power diode, this IC also integrates an output-side isolation switch as shown in the functional block diagram. One common issue with conventional boost regulators is the conduction path from input to output even when the PWM switch is turned off. It creates three problems, which are inrush current during start-up, output leakage current during shutdown, and excessive overload current. In the TPS61093, the isolation switch turns off under shutdown-mode and overload conditions, thereby opening the current path. However, shorting the VO and OUT pins bypasses the isolation switch and enhances efficiency. Because the isolation switch is on the output side, the IC's VIN pin and power stage input power (up to 10 V) can be separated.

The TPS61093 adopts current-mode control with constant pulse-width-modulation (PWM) frequency. The switching frequency is fixed at 1.2 MHz typical. PWM operation turns on the PWM switch at the beginning of each switching cycle. The input voltage is applied across the inductor and the inductor current ramps up. In this mode, the output capacitor is discharged by the load current. When the inductor current hits the threshold set by the error amplifier output, the PWM switch is turned off, and the power diode is forward-biased. The inductor transfers its stored energy to replenish the output capacitor. This operation repeats in the next switching cycle. The error amplifier compares the FB-pin voltage with an internal reference, and its output determines the duty cycle of the PWM switching. This closed-loop system requires frequency compensation for stable operation. The device has a built-in compensation circuit that can accommodate a wide range of input and output voltages. To avoid the sub-harmonic oscillation intrinsic to current-mode control, the IC also integrates slope compensation, which adds an artificial slope to the current ramp.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Shutdown and Load Discharge

When the EN pin is pulled low for 1 ms, the IC stops the PWM switch and turns off the isolation switch, providing isolation between input and output. The internal current path consisting of the isolation switch's body diode and several parasitic diodes quickly discharges the output voltage to less than 4.3 V. Afterwards, the voltage is slowly discharged to zero by the leakage current. This protects the IC and the external components from high voltage in shutdown mode.

In shutdown mode, less than 1 μA of input current is consumed by the IC.

7.3.2 Overload and Overvoltage Protection

If the overload current passing through the isolation switch is above the overload limit (I_{OL}) for 3-μs (typical), the TPS61093 is switched off until the fault is cleared and the EN pin toggles. The function only is triggered 52 ms after the IC is enabled.

To prevent the PWM switch and the output capacitor from exceeding maximum voltage ratings, an overvoltage protection circuit turns off the boost switch as soon as the output voltage at the VO pin exceeds the OVP threshold. Simultaneously, the IC opens the isolation switch. The regulator resumes PWM switching after the VO pin voltage falls 0.6 V below the threshold.

7.3.3 UVLO

An undervoltage lockout prevents improper operation of the device for input voltages below 1.55 V. When the input voltage is below the undervoltage threshold, the entire device, including the PWM and isolation switches, remains off.

7.3.4 Thermal Shutdown

An internal thermal shutdown turns off the isolation and PWM switches when the typical junction temperature of 150°C is exceeded. The thermal shutdown has a hysteresis of 15°C, typical.

7.4 Device Functional Modes

The converter operates in continuous conduction mode (CCM) as soon as the input current increases above half the ripple current in the inductor, for lower load currents it switches into discontinuous conduction mode (DCM). If the load is further reduced, the part starts to skip pulses to maintain the output voltage.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The device is a step up DC-DC converter with a PWM switch, a power diode and an input/output isolation switch integrated. TPS61093 supports up to 17-V output with the input range from 1.6 V to 6 V. The TPS61093 adopts the current-mode control with constant pulse-width-modulation (PWM) frequency. The switching frequency is fixed at 1.2 MHz typical. The isolation switch disconnects the output from the input during shutdown to minimize leakage current. However, shorting the VO and OUT pins bypasses the isolation switch and enhances efficiency. The following design procedure can be used to select component values for the TPS61093.

8.2 Typical Applications

8.2.1 15 V Output Boost Converter

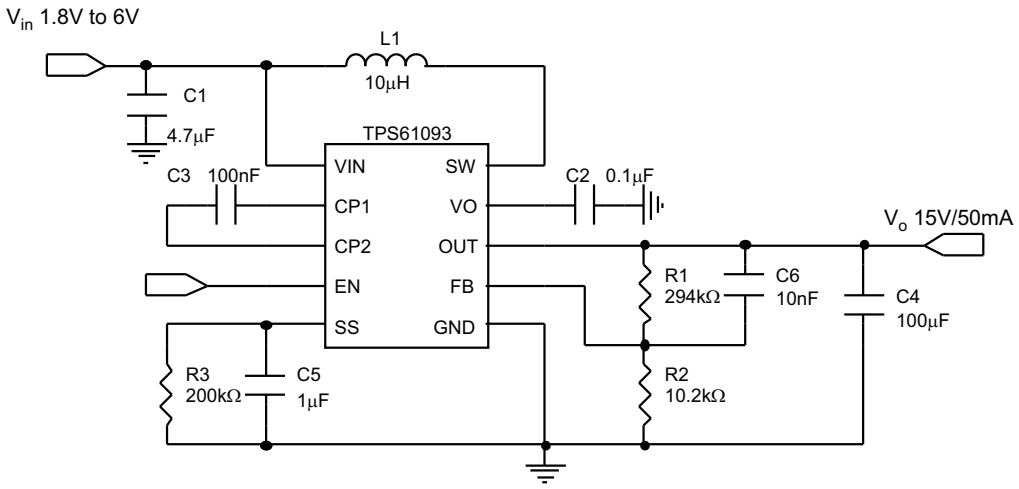


Figure 6. 15 V Boost Converter with 100 µF Output Capacitor

8.2.1.1 Design Requirements

Table 2. Design Parameters

PARAMETERS	VALUES
Input voltage	4.2 V
Output voltage	15 V
Operating frequency	1.2 MHz

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS61093 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.1.2.2 Output Program

To program the output voltage, select the values of R1 and R2 (see Figure 7) according to Equation 1.

$$Vout = 0.5\ V \times \left(\frac{R1}{R2} + 1\right)$$

$$R1 = R2 \times \left(\frac{Vout}{0.5\ V} - 1\right) \quad (1)$$

A recommended value for R2 is approximately 10 kΩ which sets the current in the resistor divider chain to 0.5 V/10 kΩ = 50 μA. The output voltage tolerance depends on the VFB accuracy and the resistor divider.

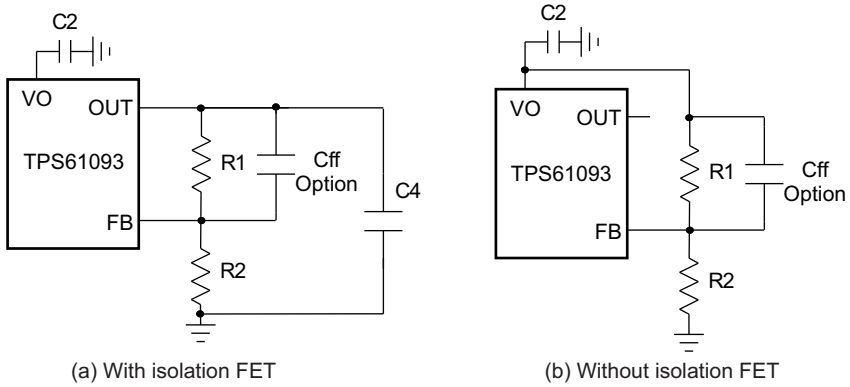


Figure 7. Resistor Divider to Program Output Voltage

8.2.1.2.3 Without Isolation FET

The efficiency of the TPS61093 can be improved by connecting the load to the VO pin instead of the OUT pin. The power loss in the isolation FET is then negligible, as shown in Figure 8. The tradeoffs when bypassing the isolation FET are:

- Leakage path between input and output causes the output to be a diode drop below the input voltage when the IC is in shutdown
- No overload circuit protection

When the load is connected to the VO pin, the output capacitor on the VO pin must be above 1 μF.

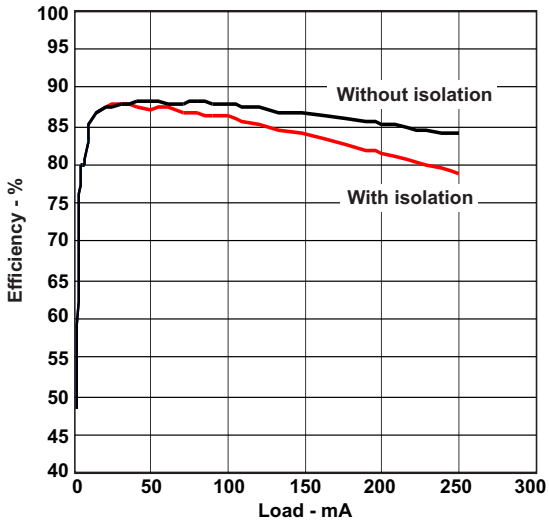


Figure 8. Efficiency vs Load

8.2.1.2.4 Start-Up

The TPS61093 turns on the isolation FET and PWM switch when the EN pin is pulled high. During the soft-start period, the R and C network on the SS pin is charged by an internal bias current of 5 μA (typical). The RC network sets the reference voltage ramp up slope. Because the output voltage follows the reference voltage via the FB pin, the output voltage rise time follows the SS pin voltage until the SS pin voltage reaches 0.5 V. The soft-start time is given by Equation 2.

$$t_{SS} = \frac{0.5\ V \times C5}{5\ \mu A} \quad (2)$$

where

- C5 is the capacitor connected to the SS pin

When the EN pin is pulled low to switch the IC off, the SS pin voltage is discharged to zero by the resistor R3. The discharge period depends on the RC time constant. Note that if the SS pin voltage is not discharged to zero before the IC is enabled again, the soft start circuit may not slow the output voltage startup and may not reduce the startup inrush current.

8.2.1.2.5 Switch Duty Cycle

The maximum switch duty cycle (D) of the TPS61093 is 90% (minimum). The duty cycle of a boost converter under continuous conduction mode (CCM) is given by:

$$D = \frac{Vout + 0.8\ V - Vin}{Vout + 0.8\ V} \quad (3)$$

The duty cycle must be lower than the specification in the application; otherwise the output voltage cannot be regulated.

The TPS61093 has a minimum ON pulse width once the PWM switch is turned on. As the output current drops, the device enters discontinuous conduction mode (DCM). If the output current drops extremely low, causing the ON time to be reduced to the minimum ON time, the TPS61093 enters pulse-skipping mode. In this mode, the device keeps the power switch off for several switching cycles to keep the output voltage in regulation. See Figure 14. The output current when the IC enters skipping mode is calculated with Equation 4.

$$I_{out\_skip} = \frac{Vin^2 \times T_{min\_on}^2 \times f_{SW}}{2 \times (Vout + 0.8V - Vin) \times L} \quad (4)$$

where

- T_{min_on} = Minimum ON pulse width specification (typically 65-ns);
- L = Selected inductor value;
- f_{SW} = Converter switching frequency (typically 1.2-MHz)

8.2.1.2.6 Inductor Selection

Because the selection of the inductor affects steady state operation, transient behavior, and loop stability, the inductor is the most important component in power regulator design. There are three important inductor specifications, inductor value, saturation current, and dc resistance. Considering inductor value alone is not enough.

The saturation current of the inductor should be higher than the peak switch current as calculated in Equation 5.

$$I_{L\_peak} = I_{L\_DC} + \frac{\Delta I_L}{2}$$

$$I_{L\_DC} = \frac{Vout \times Iout}{Vin \times \eta}$$

$$\Delta I_L = \frac{1}{\left[L \times f_{SW} \times \left(\frac{1}{Vout + 0.8\ V - VIN} + \frac{1}{VIN}\right)\right]} \quad (5)$$

where

- I_{L_peak} = Peak switch current
- I_{L_DC} = Inductor average current
- ΔI_L = Inductor peak to peak current
- η = Estimated converter efficiency

Normally, it is advisable to work with an inductor peak-to-peak current of less than 30% of the average inductor current. A smaller ripple from a larger valued inductor reduces the magnetic hysteresis losses in the inductor and EMI. But in the same way, load transient response time is increased. Also, the inductor value should not be outside the 2.2 µH to 10 µH range in the recommended operating conditions table. Otherwise, the internal slope compensation and loop compensation components are unable to maintain small signal control loop stability over the entire load range. Table 3 lists the recommended inductor for the TPS61093.

Table 3. Recommended Inductors for the TPS61093

PART NUMBER	L (µH)	DCR MAX (mΩ)	SATURATION CURRENT (A)	SIZE (L×W×H mm)	VENDOR
#A915_Y-4R7M	4.7	45	1.5	5.2x5.2x3.0	Toko
#A915_Y-100M	10	90	1.09	5.2x5.2x3.0	Toko
VLS4012-4R7M	4.7	132	1.1	4.0x4.0x1.2	TDK
VLS4012-100M	10	240	0.82	4.0x4.0x1.2	TDK
CDRH3D23/HP	10	198	1.02	4.0x4.0x2.5	Sumida
LPS5030-103ML	10	127	1.4	5.0x5.0x3.0	Coilcraft

8.2.1.2.7 Input and Output Capacitor Selection

The output capacitor is mainly selected to meet the requirements for output ripple and loop stability. This ripple voltage is related to the capacitor's capacitance and its equivalent series resistance (ESR). Assuming a ceramic capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by:

$$C_{out} = \frac{D \times I_{out}}{Fs \times V_{ripple}} \quad (6)$$

where

- V_{ripple} = peak to peak output ripple

The ESR impact on the output ripple must be considered if tantalum or electrolytic capacitors are used.

Care must be taken when evaluating a ceramic capacitor's derating under dc bias, aging, and ac signal. For example, larger form factor capacitors (in 1206 size) have their self resonant frequencies in the range of the switching frequency. So the effective capacitance is significantly lower. The dc bias can also significantly reduce capacitance. A ceramic capacitor can lose as much as 50% of its capacitance at its rated voltage. Therefore, always leave margin on the voltage rating to ensure adequate capacitance at the required output voltage.

A 4.7-μF (minimum) input capacitor is recommended. The output requires a capacitor in the range of 1 μF to 10 μF. The output capacitor affects the small signal control loop stability of the boost regulator. If the output capacitor is below the range, the boost regulator can potentially become unstable.

The popular vendors for high value ceramic capacitors are:

- TDK (http://www.component.tdk.com/components.php)
- Murata (http://www.murata.com/cap/index.html)

8.2.1.2.8 Small Signal Stability

The TPS61093 integrates slope compensation and the RC compensation network for the internal error amplifier. Most applications are control loop stable if the recommended inductor and input/output capacitors are used. For those few applications that require components outside the recommended values, the internal error amplifier's gain and phase are presented in Figure 9.

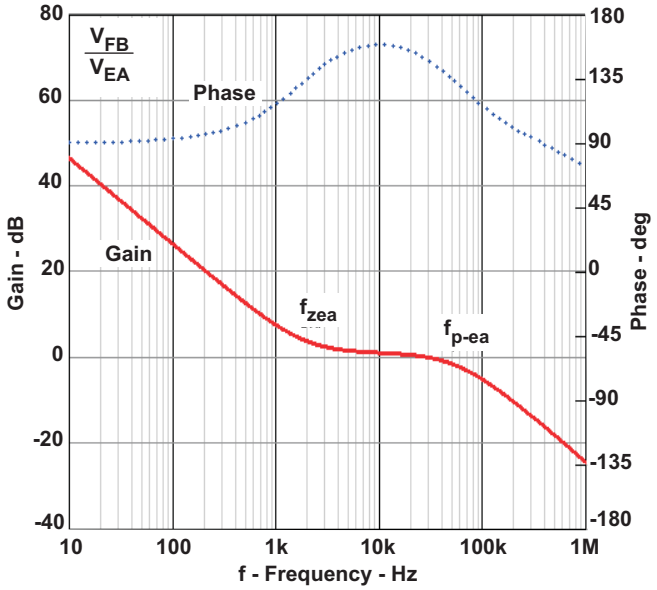


Figure 9. Bode Plot of Error Amplifier Gain and Phase

The RC compensation network generates a pole f_{p-ea} of 57 kHz and a zero f_{z-ea} of 1.9 kHz, shown in Figure 9. Use Equation 7 to calculate the output pole, f_P, of the boost converter. If f_P << f_{z-ea}. due to a large capacitor beyond 10 µF, for example, a feed forward capacitor on the resistor divider, as shown in Figure 9, is necessary to generate an additional zero f_{z-f}. to improve the loop phase margin and improve the load transient response. The low frequency pole f_{p-f} and zero f_{z-f} generated by the feed forward capacitor are given by Equation 8 and Equation 9:

$$f_P = \frac{1}{\pi \times R_o \times C_O} \quad \text{(a)} \tag{7}$$

$$f_{p-f} = \frac{1}{2\pi \times R2 \times C_{ff}} \quad \text{(b)} \tag{8}$$

$$f_{z-f} = \frac{1}{2\pi \times R1 \times C_{ff}} \quad \text{(c)} \tag{9}$$

where

- C_{ff} = the feed-forward capacitor

For example, in the typical application circuitry (see Figure 7), the output pole f_P is approximately 1 kHz. When the output capacitor is increased to 100 µF, then the f_P is reduced to 10 Hz. Therefore, a feed-forward capacitor of 10 nF compensates for the low frequency pole.

A feed-forward capacitor that sets f_{z-f} near 10 kHz improves the load transient response in most applications, as shown in Figure 11.

8.2.1.3 Application Curves

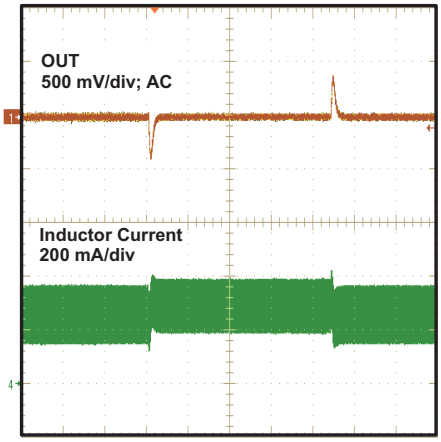


Figure 10. 3.3 V to 3.6 V Line Transient Response

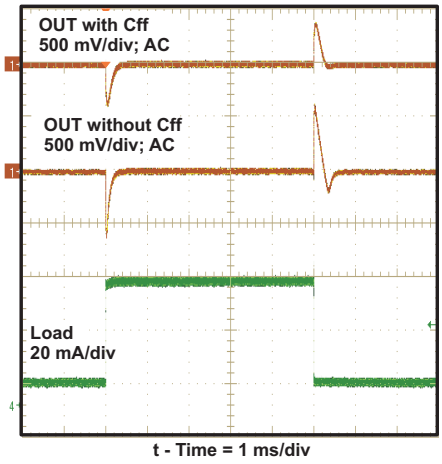


Figure 11. 10 mA to 50 mA Load Transient Response

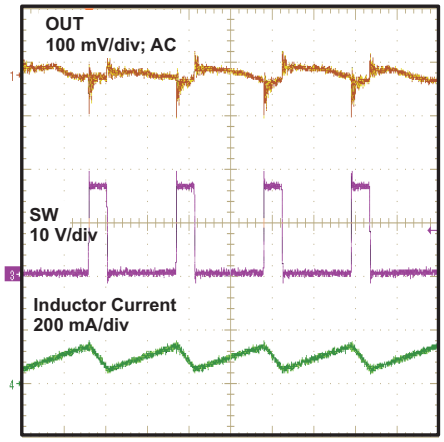


Figure 12. PWM Control in CCM

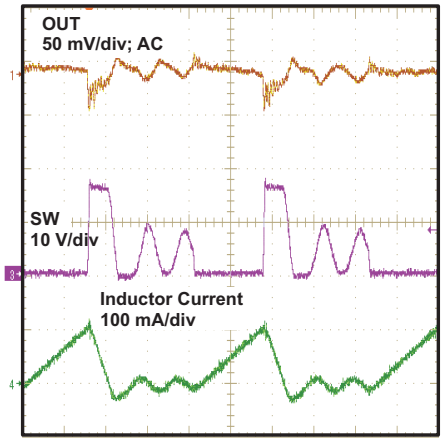


Figure 13. PWM Control in DCM

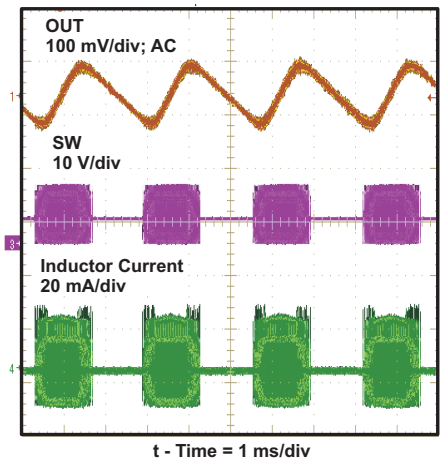


Figure 14. Pulse Skip Mode at Light Load

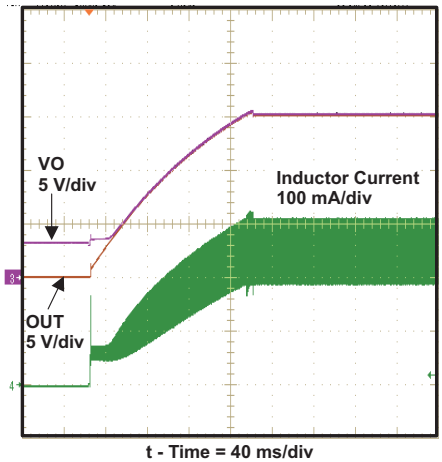


Figure 15. Soft Start-Up

8.2.2 10 V, –10 V Dual Output Boost Converter

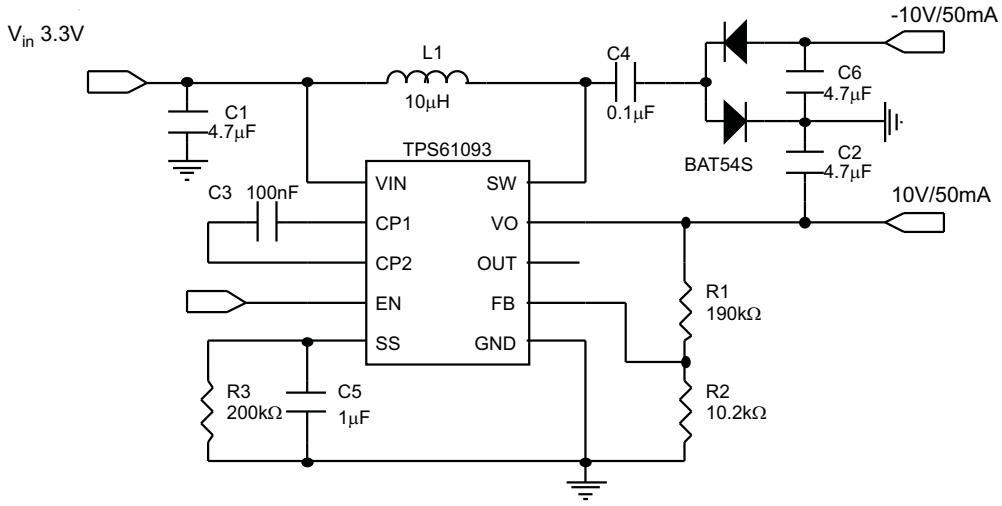


Figure 16. 10 V, –10 V Dual Output Boost Converter Schematic

8.2.2.1 Design Requirements

Table 4. Design Parameters

PARAMETERS	VALUES
Input voltage	3.3 V
Output voltage	10 V/–10 V
Operating frequency	1.2 MHz

8.2.2.2 Detailed Design Procedure

Refer to *Detailed Design Procedure* for the 15-V output boost converter.

8.2.2.3 Application Curve

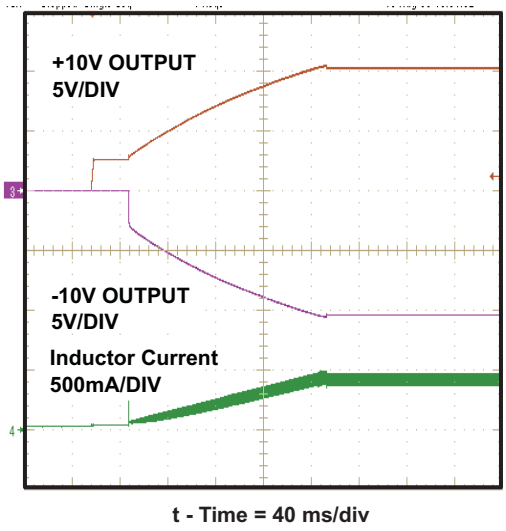


Figure 17. Soft Start-up Waveform, 10 V, -10 V Dual Output Boost Converter

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 1.6 V to 6 V. The input power supply's output current needs to be rated according to the supply voltage, output voltage and output current of the TPS61093.

10 Layout

10.1 Layout Guidelines

As for all switching power supplies, especially those running at high switching frequency and high currents, layout is an important design step. If layout is not carefully done, the regulator could suffer from instability as well as noise problems. To maximize efficiency, switch rise and fall times are very fast. To prevent radiation of high frequency noise (for example, EMI), proper layout of the high frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin and always use a ground plane under the switching regulator to minimize interplane coupling. The high current path including the switch and output capacitor contains nanosecond rise and fall times and should be kept as short as possible. The input capacitor needs not only to be close to the VIN pin, but also to the GND pin in order to reduce input supply ripple.

10.2 Layout Example

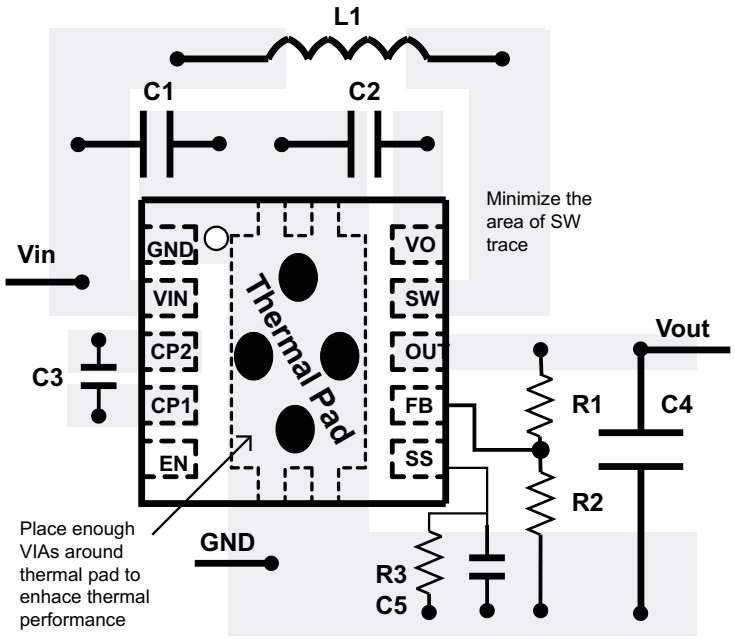


Figure 18. TPS61093QFN Board Layout

11 器件和文档支持

11.1 器件支持

11.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

11.1.2 开发支持

11.1.2.1 使用 WEBENCH® 工具创建定制设计

单击此处，使用 TPS61093 器件并借助 WEBENCH® 电源设计器创建定制设计方案。

1. 首先输入输入电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
2. 使用优化器拨盘优化该设计的关键参数，如效率、尺寸和成本。
3. 将生成的设计与德州仪器 (TI) 的其他可行的解决方案进行比较。

WEBENCH 电源设计器可提供定制原理图以及罗列实时价格和组件供货情况的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案以常用 CAD 格式导出
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com.cn/WEBENCH。

11.2 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的*通知我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商标

E2E is a trademark of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61093DSKR	ACTIVE	SON	DSK	10	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OAP	Samples
TPS61093DSKT	ACTIVE	SON	DSK	10	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OAP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

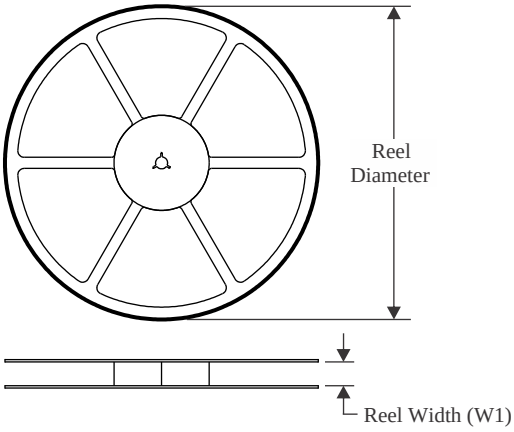
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

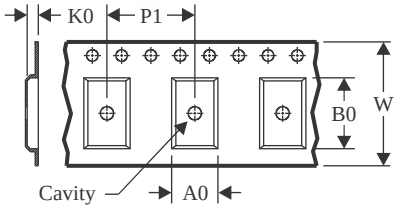
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

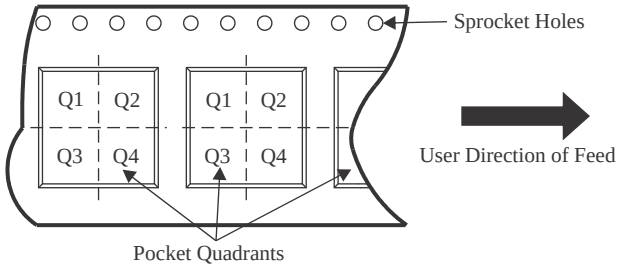


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

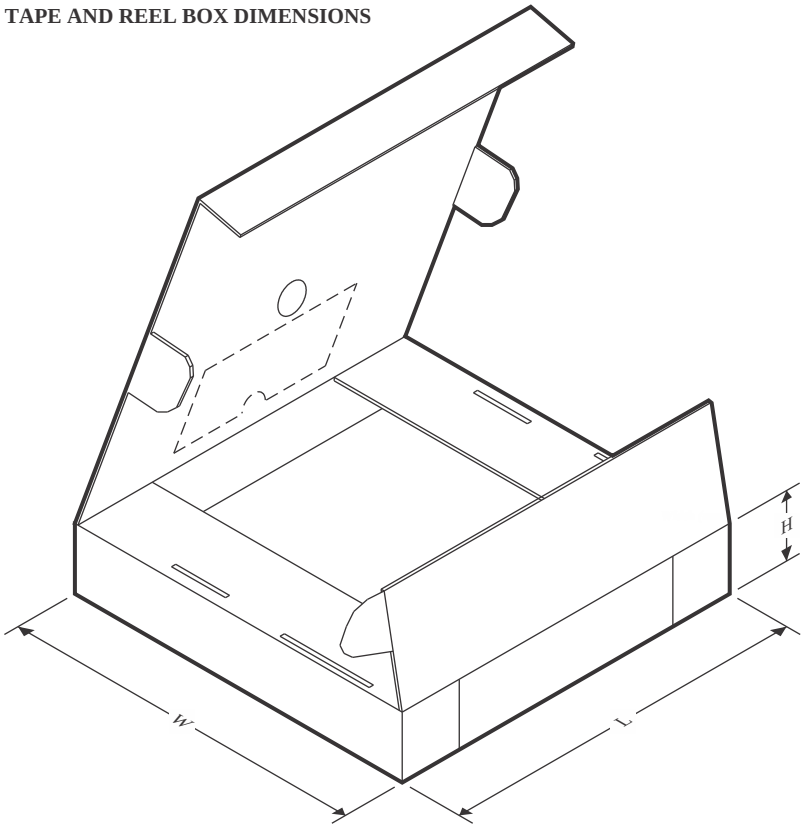
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61093DSKR	SON	DSK	10	3000	180.0	8.4	2.8	2.8	1.0	4.0	8.0	Q2
TPS61093DSKT	SON	DSK	10	250	180.0	8.4	2.8	2.8	1.0	4.0	8.0	Q2
TPS61093DSKT	SON	DSK	10	250	178.0	8.4	2.75	2.75	0.95	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



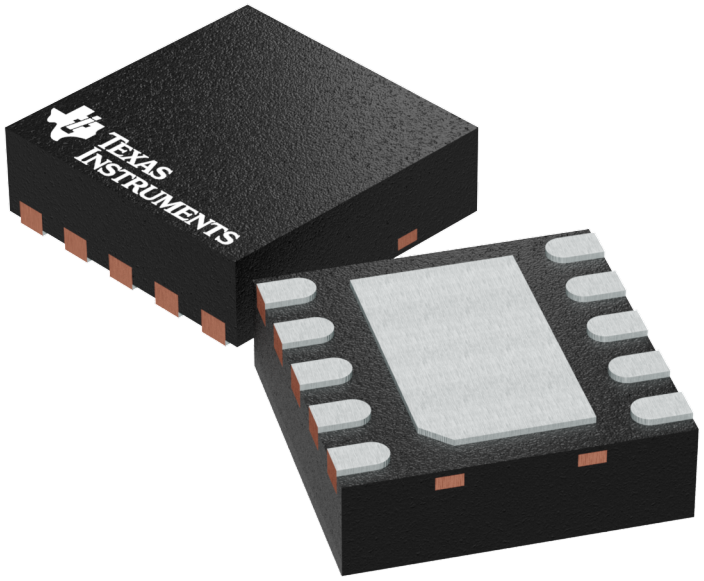
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61093DSKR	SON	DSK	10	3000	182.0	182.0	20.0
TPS61093DSKT	SON	DSK	10	250	182.0	182.0	20.0
TPS61093DSKT	SON	DSK	10	250	205.0	200.0	33.0

DSK 10 WSON - 0.8 mm max height

2.5 x 2.5 mm, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD



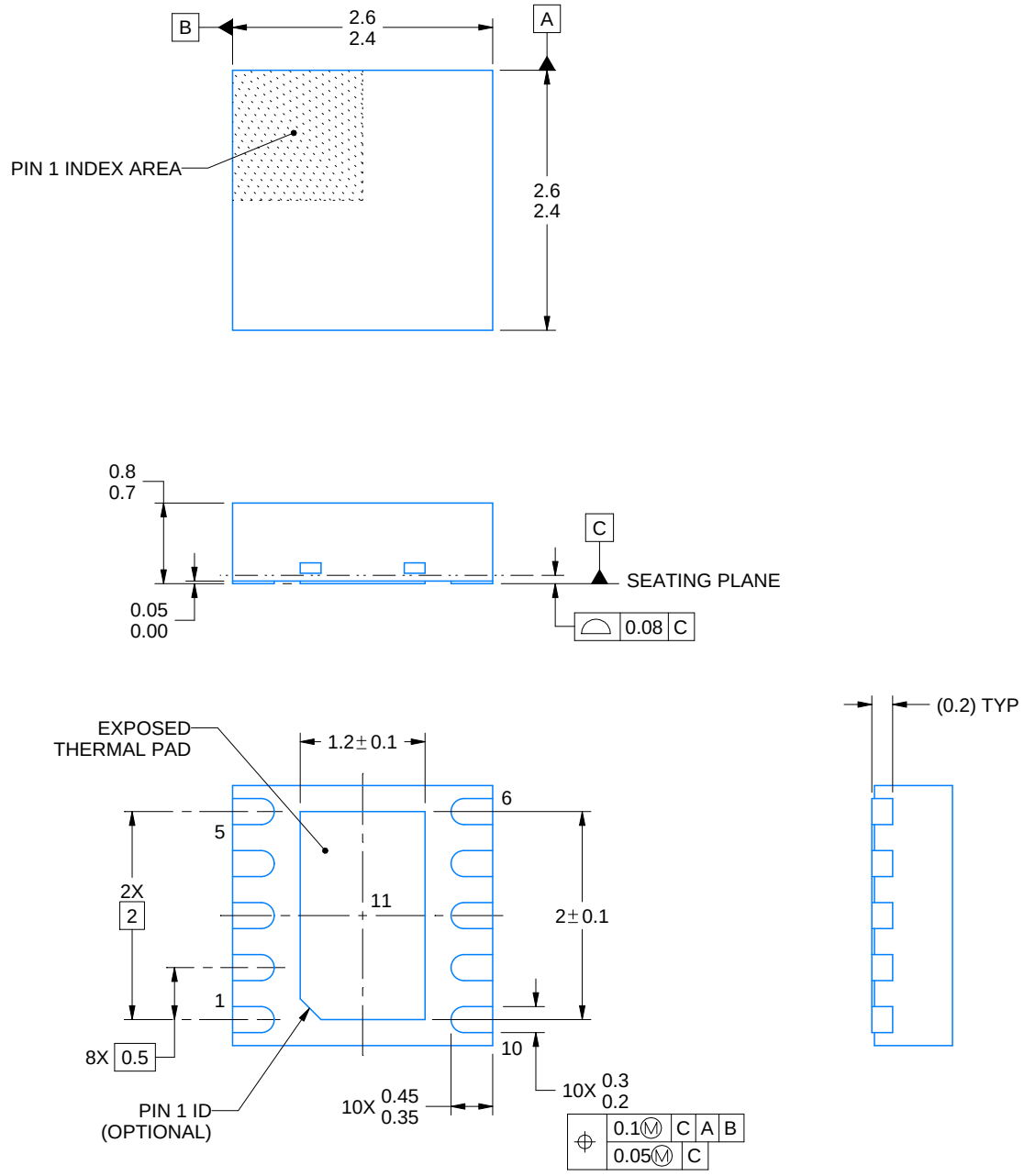
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PACKAGE OUTLINE

DSK0010A

WSON - 0.8 mm max height

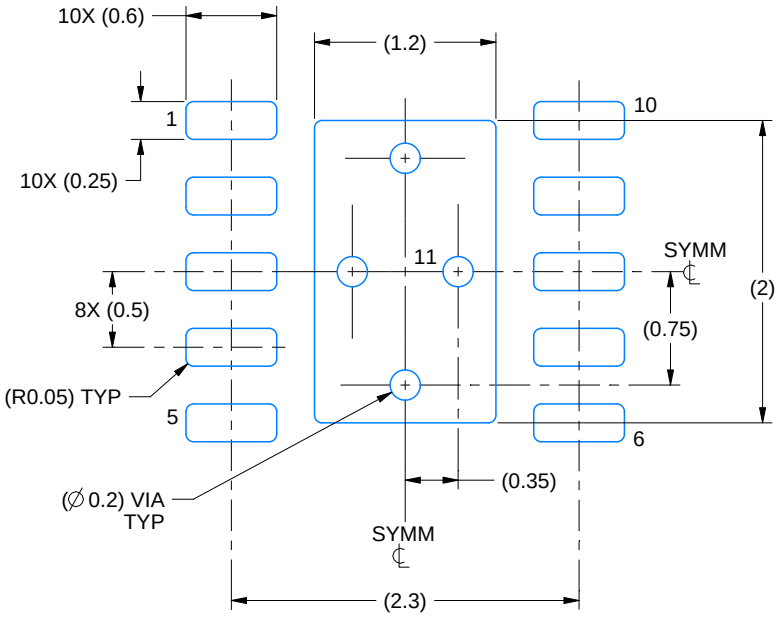
PLASTIC SMALL OUTLINE - NO LEAD



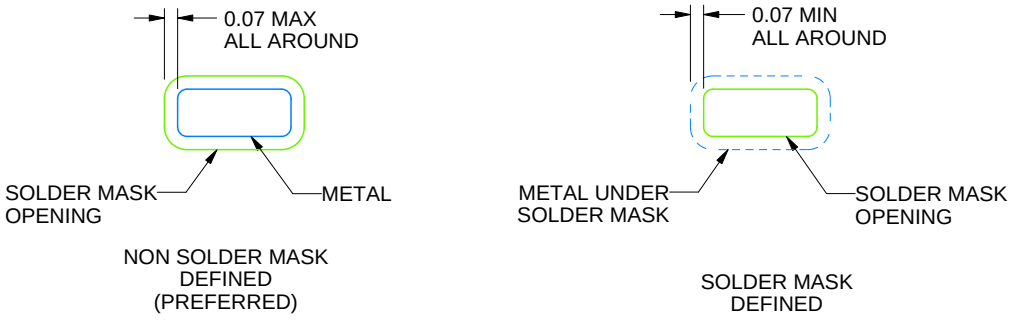
4218903/B 10/2020

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

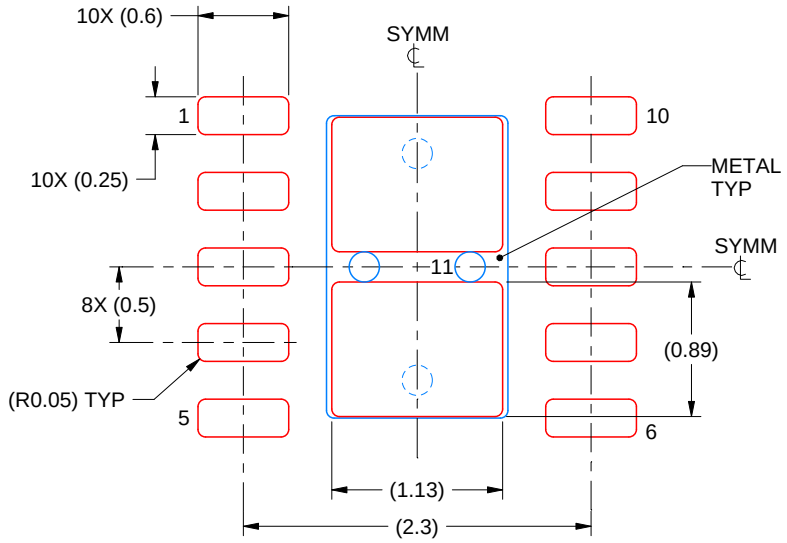


SOLDER MASK DETAILS

4218903/B 10/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4218903/B 10/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265