用于智能手机的双通道白光发光二级管 (WLED) 驱动器

查询样品: TPS61163

特性

- **2.7V** 至 **6.5V** 输入电压
- 集成型 **1.5A/40V** 金属氧化物半导体场效应晶体管 **(MOSFET)**
- **1.2MHz** 开关频率
- 每个通道上高达 **30mA** 的双电流吸收能力
- **1%** 的典型电流匹配及准确度
- **37.5V** 过压保护 **(OVP)** 阀值
- 自适应升压输出至 **WLED** 电压
- 极低电压净空控制 **(90mV)**
- 灵活的数字和脉宽调制 **(PWM)** 亮度控制
- **1** 线制控制接口 **(EasyScale)**
- **PWM** 亮度调节控制接口
- 高达 **100:1 PWM** 调光比
- 高达 **10** 位的调光分辨率
- 效率高达 **90%**
- 内置软起动功能
- 具有过压保护功能
- 内置 **WLED** 开路/短路保护
- 热关断
- 支持 **4.7uH** 电感器应用
- **9L 1.31mm x 1.31mm** 芯片级封装 **(CSP)**

应用范围

- 智能电话
- 掌上电脑 **(PDA)**，手持计算机
- **GPS** 接收器
- 针对具有单节电池输入的小型、媒体尺寸 **LCD** 显示屏的背光

说明

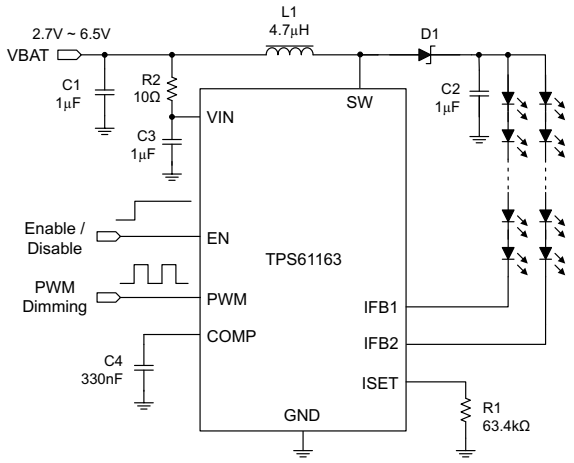
TPS61163 是一款双通道 WLED 驱动器，此驱动器为单节锂离子电池供电的智能手机背光提供高度集成的解决方案。 此器件具有一个带有集成 1.5A/40V 功率 MOSFET 的内置高效升压稳压器并支持低至 2.7V 的输入电压。 借助于两个高电流匹配能力的电流吸收稳压器，此器件能够驱动高达十串两并 (10s2p) 的 WLED 二极管。 升压输出能够自动调节至 WLED 正向电压并且可实现极低的电压净空控制，从而有效提升 LED 灯串的效率。

TPS61163 支持 PWM 调光接口和 1 线制数字 EasyScale™ 调光接口并能够实现 9 位亮度代码编程。

TPS61163 集成了内置软启动、过压/过流保护和热关断保护。

此器件采用节省空间的 1.31mm x 1.31mm 芯片级封装 (CSP)。

典型应用



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	PART NUMBER	OPEN LED PROTECTION	PACKAGE	ORDERING(2)	PACKAGE MARKING
–40°C to 85°C	TPS61163	37.5V (typical)	9-ball WSCP	TPS61163YFF	TPS61163

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) The YFF package is available in tape and reel. Add a R suffix (e.g. TPS61163YFFR) to order quantities of 3000 parts. Add a T suffix (e.g. TPS61163YFFT) to order quantities of 250 parts.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE		UNIT
		MIN	MAX	
Voltage range(2)	VIN, EN, PWM, IFB1, IFB2	–0.3	7	V
	COMP, ISET	–0.3	3	V
	SW	–0.3	40	V
ESD rating	Human Body Mode – (HBM)		2	kV
	Machine Mode – (MM)		200	V
	Charge Device Mode – (CDM)		750	V
P_D	Continuous power dissipation	See Thermal Information Table		
T_J	Operating junction temperature range	–40	150	°C
T_{STG}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS61163 YFF (9-ball WSCP)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	107	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(3)	0.9	
θ_{JB}	Junction-to-board thermal resistance(4)	18.1	
ψ_{JT}	Junction-to-top characterization parameter(5)	4.0	
ψ_{JB}	Junction-to-board characterization parameter(6)	18	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(7)	NA	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

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RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	2.7		6.5	V
V_{OUT}	Output voltage range	V_{IN}		38	V
L	Inductor	4.7		10	µH
C_I	Input capacitor	1.0			µF
C_O	Output capacitor	1.0		2.2	µF
C_{COMP}	Compensation capacitor		330		nF
F_{PWM}	PWM dimming signal frequency	40		100	kHz
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

ELECTRICAL CHARACTERISTICS

V_{IN} = 3.6V, EN = high, PWM = high, IFB current = 20mA, T_A = -40°C to +85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	Input voltage range		2.7		6.5	V
V_{VIN_UVLO}	Under voltage lockout threshold	V_{IN} falling		2.2	2.3	V
		V_{IN} rising			2.45	
V_{VIN_HYS}	VIN UVLO hysteresis			100		mV
I_q	Operating quiescent current into VIN	Device enable, switching 1.2 MHz and no load, V_{IN} = 3.6V		1.2	2	mA
I_{SD}	Shutdown current	EN = low		1	2	µA
EN and PWM						
V_H	EN Logic high		1.2			V
V_L	EN Logic Low				0.4	V
V_H	PWM Logic high		1.2			V
V_L	PWM Logic Low				0.4	V
R_{PD}	EN pin and PWM pin internal pull-down resistor		400	800	1600	kΩ
t_{PWM_SD}	PWM logic low width to shutdown	PWM high to low	20			ms
t_{EN_SD}	EN logic low width to shutdown	EN high to low	2.5			ms
CURRENT REGULATION						
V_{ISET_full}	ISET pin voltage	Full brightness	1.204	1.229	1.253	V
K_{ISET_full}	Current multiplier	Full brightness		1030		
I_{FB_avg}	Current accuracy	I_{ISET} = 20 µA, D = 100%, 0°C to 70°C	–2%		2%	
		I_{ISET} = 20 µA, D = 100%, –40°C to 85°C	–2.3%		2.3%	
K_M	$(I_{MAX} – I_{AVG}) / I_{AVG}$	D = 100%		1%	2%	
		D = 25%		1%		
I_{IFB_max}	Current sink max output current	I_{ISET} = 35 µA, each IFBx pin	30			mA

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ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 3.6V, EN = high, PWM = high, IFB current = 20mA, T_A = -40°C to +85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SWITCH						
$R_{DS(on)}$	Switch MOSFET on-resistance	V_{IN} = 3.6 V		0.25		Ω
		V_{IN} = 3.0 V		0.3		
I_{LEAK_SW}	Switch MOSFET leakage current	V_{SW} = 35 V, T_A = 25°C			1	µA
OSCILLATOR						
f_{SW}	Oscillator frequency		1000	1200	1500	kHz
D_{max}	Maximum duty cycle	Measured on the drive signal of switch MOSFET	91	95		%
BOOST VOLTAGE CONTROL						
V_{IFB_reg}	IFBx feedback regulation voltage	I_{IFBx} = 20mA, measured on IFBx pin which has a lower voltage		90		mV
I_{sink}	COMP pin sink current			12		µA
I_{source}	COMP pin source current			5		µA
G_{ea}	Error amplifier transconductance		30	55	80	µmho
R_{ea}	Error amplifier output resistance			45.5		MΩ
f_{ea}	Error amplifier crossover frequency	5pF connected to COMP pin		1.65		MHz
PROTECTION						
I_{LIM}	Switch MOSFET current limit	D = D_{max}, 0°C to 70°C	1	1.5	2	A
I_{LIM_Start}	Switch MOSFET start up current limit	D = D_{max}		0.7		A
t_{Half_LIM}	Time window for half current limit			5		ms
V_{OVP_SW}	SW pin over voltage threshold		36	37.5	39	V
V_{OVP_IFB}	IFBx pin over voltage threshold	Measured on IFBx pin	4.2	4.5	4.8	V
EASYSCALE INTERFACE						
t_{es_delay}	EasyScale detection delay	Measured from EN low to high	100			µs
t_{es_det}	EasyScale detection time	EN pin low time	260			µs
t_{es_win}	EasyScale detection window(1)	Measured from EN low to high	1			ms
t_{start}	Start time of program stream		2			µs
t_{EOS}	End time of program stream		2		360	µs
t_{H_LB}	High time of low bit (Logic 0)		2		180	µs
t_{L_LB}	Low time of low bit (Logic 0)		2 x t_{H_LB}		360	µs
t_{H_HB}	High time of high bit (Logic 1)		2 x t_{L_HB}		360	µs
t_{L_HB}	Low time high bit (Logic 1)		2		180	µs
$t_{valACKN}$	Acknowledge valid time				2	µs
t_{ACKN}	Duration of acknowledge condition				512	µs
V_{ACKNL}	Acknowledge output voltage low(2)	Open drain, R_{pullup} = 15 kΩ to VIN			0.4	V
THERMAL SHUTDOWN						
$T_{shutdown}$	Thermal shutdown threshold			160		°C
T_{hys}	Thermal shutdown hysteresis			15		°C

(1) To select EasyScale interface, after t_{es_delay} delay from EN low to high, drive EN pin to low for more than t_{es_det} before t_{es_win} expires
(2) Acknowledge condition active 0, this condition is only applied when the RFA bit is set to 1. To use this feature, master must have an open drain output, and the data line needs to be pulled up by the master with a resistor load.

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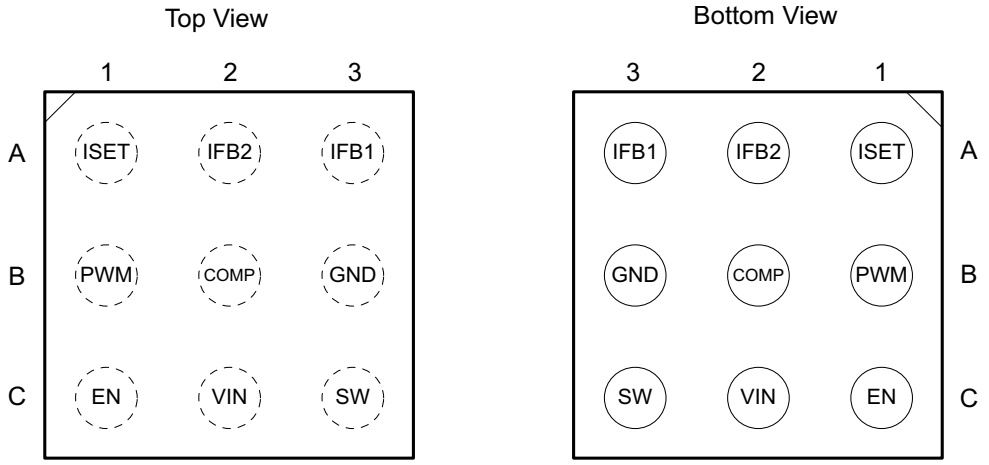
DEVICE INFORMATION

PIN ASSIGNMENT
9 BALL 1.31mm x 1.31mm YFF PACKAGE



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NUMBER	NAME		
A1	ISET	I	Full-scale LED current set pin. Connecting a resistor to the pin programs the full-scale LED current
A2	IFB2	I	Regulated current sink input pin
A3	IFB1	I	Regulated current sink input pin
B1	PWM	I	PWM dimming signal input
B2	COMP	O	Output of the transconductance error amplifier. Connect external capacitor to this pin to compensate the boost loop
B3	GND	O	Ground
C1	EN	I	Enable control, and 1-wire digital signal input
C2	VIN	I	Supply input pin
C3	SW	I	Drain connection of the internal power MOSFET

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TYPICAL CHARACTERISTICS

Table 1. TABLE OF GRAPHS

TITLE	DESCRIPTION	FIGURE
Dimming Efficiency	V_{IN} = 3V, 3.6V, 4.2V, 5V; V_O = 15V, 5s2p, 20mA/string; PWM Freq = 40kHz; L = 10µH	Figure 1
Dimming Efficiency	V_{IN} = 3V, 3.6V, 4.2V, 5V; V_O = 18V, 6s2p, 20mA/string; PWM Freq = 40kHz; L = 10µH	Figure 2
Dimming Efficiency	V_{IN} = 3V, 3.6V, 4.2V, 5V; V_O = 21V, 7s2p, 20mA/string; PWM Freq = 40kHz; L = 10µH	Figure 3
Dimming Efficiency	V_{IN} = 3V, 3.6V, 4.2V, 5V; V_O = 24V, 8s2p, 20mA/string; PWM Freq = 40kHz; L = 10µH	Figure 4
Dimming Efficiency	V_{IN} = 3V, 3.6V, 4.2V, 5V; V_O = 27V, 9s2p, 20mA/string; PWM Freq = 40kHz; L = 10µH	Figure 5
Dimming Efficiency	V_{IN} = 3V, 3.6V, 4.2V, 5V; V_O = 30V, 10s2p, 20mA/string; PWM Freq = 40kHz; L = 10µH	Figure 6
Dimming Linearity	V_{IN} = 3V, 3.6V, 4.2V, 5V; V_O = 21V, 7s2p; R_{ISET} = 63.4kΩ; PWM Freq = 40kHz	Figure 7
Switching Waveform	V_{IN} = 3.6V; V_O = 21V, 7s2p, 20mA/string; Duty = 100%; L = 4.7µH	Figure 8
Switching Waveform	V_{IN} = 3.6V; V_O = 21V, 7s2p, 20mA/string; PWM Freq = 40kHz, Duty = 20%; L = 4.7µH	Figure 9
Startup Waveform	V_{IN} = 3.6V; V_O = 21V, 7s2p, 20mA/string; Duty = 100%; L = 4.7µH	Figure 10
Startup Waveform	V_{IN} = 3.6V; V_O = 21V, 7s2p, 20mA/string; PWM Freq = 40kHz, Duty = 50%; L = 4.7µH	Figure 11
Shutdown Waveform	V_{IN} = 3.6V; V_O = 21V, 7s2p, 20mA/string; Duty = 100%; L = 4.7µH	Figure 12
Shutdown Waveform	V_{IN} = 3.6V; V_O = 21V, 7s2p, 20mA/string; PWM Freq = 40kHz, Duty = 50%; L = 4.7µH	Figure 13

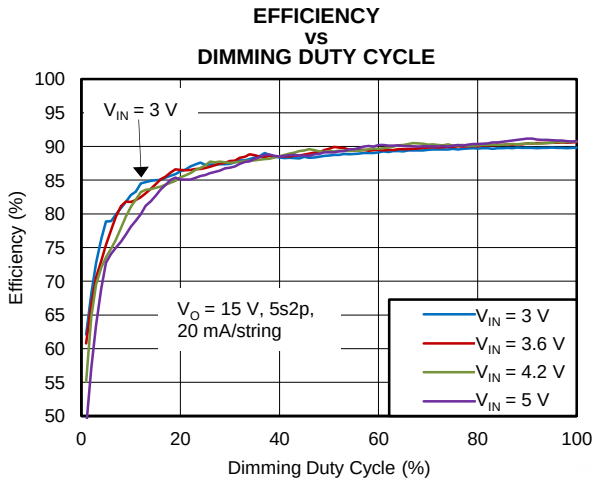

Figure 1.

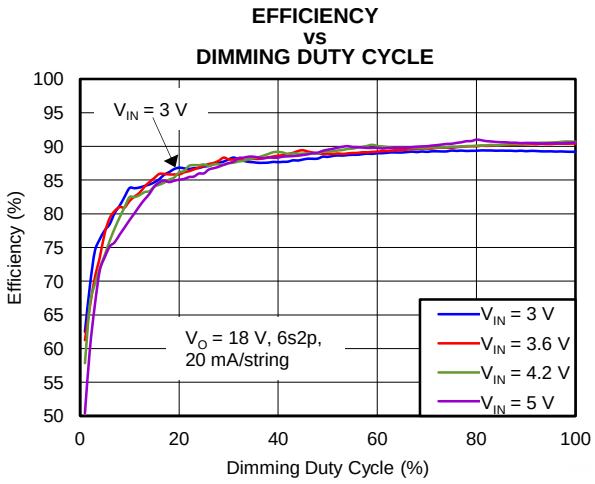

Figure 2.

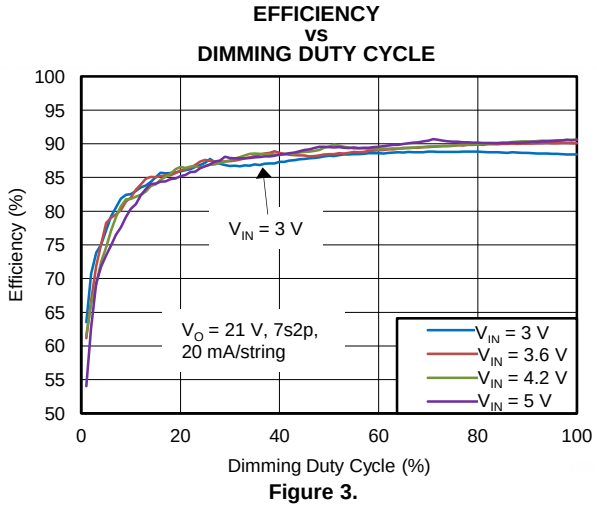

Figure 3.

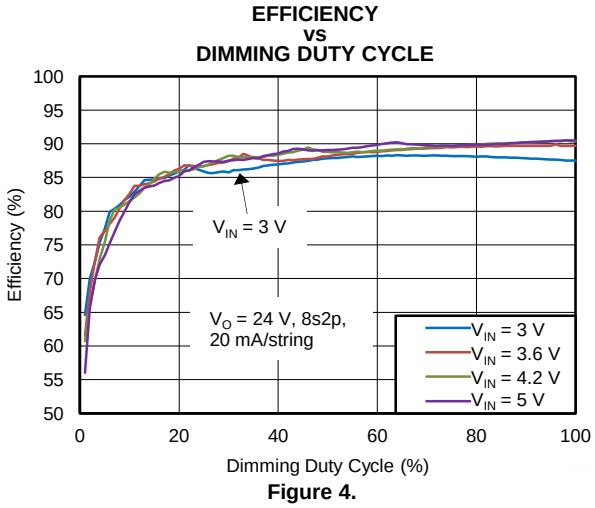

Figure 4.

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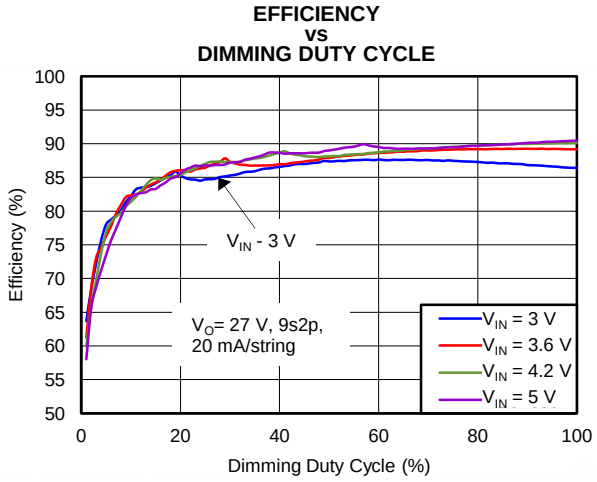

Figure 5.

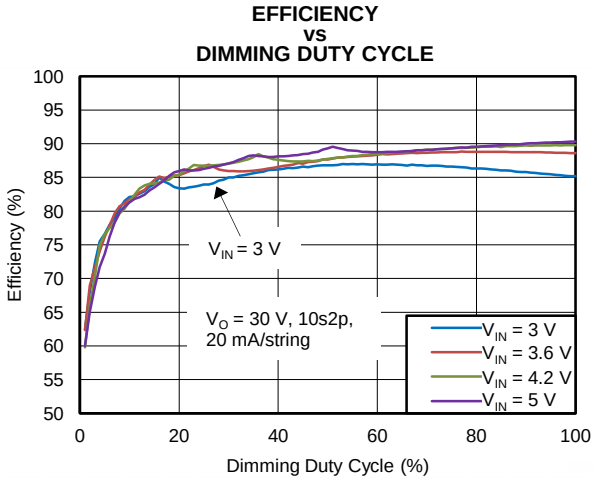

Figure 6.

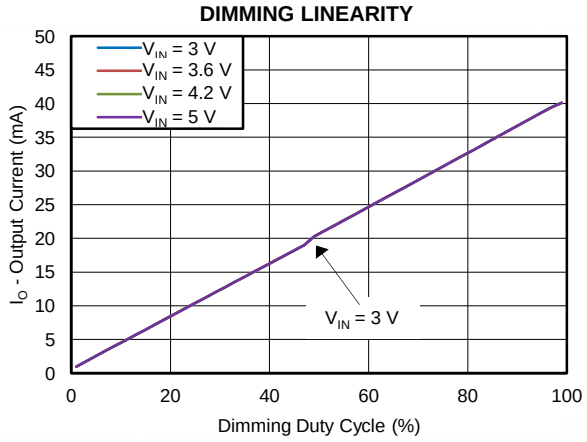

Figure 7.

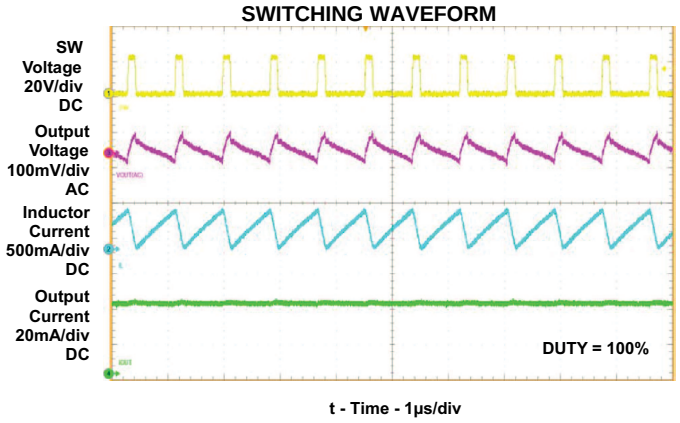

Figure 8.

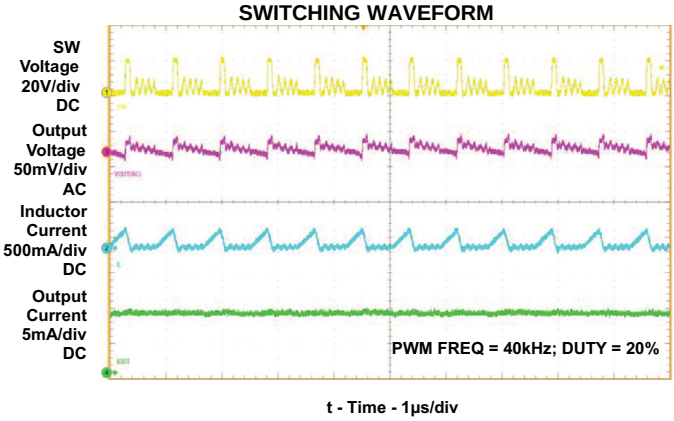

Figure 9.

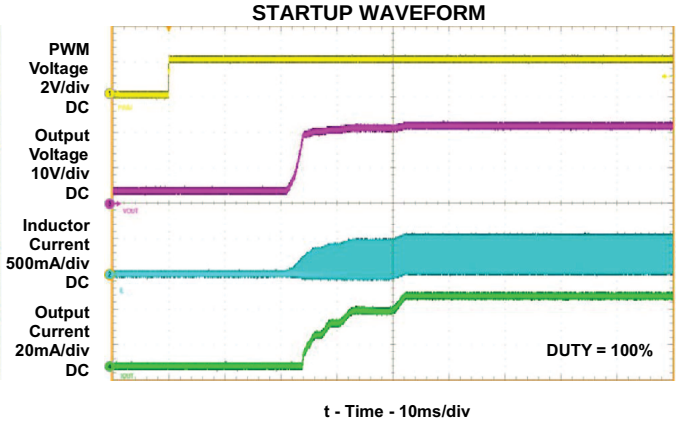

Figure 10.

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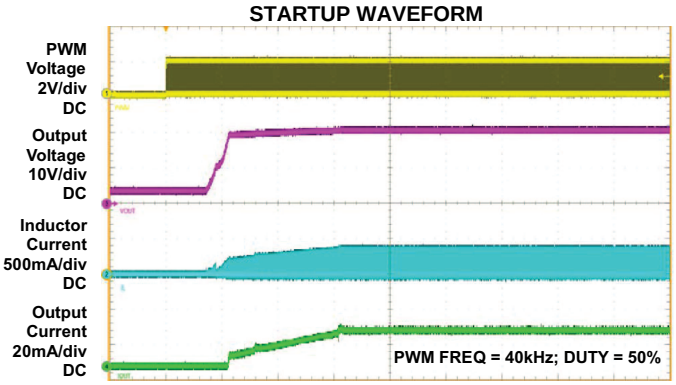

Figure 11.

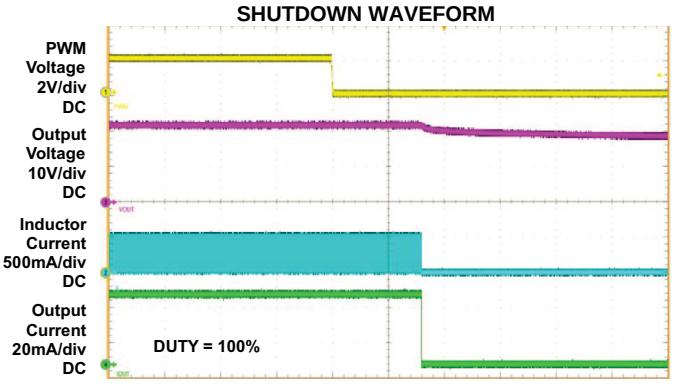

Figure 12.

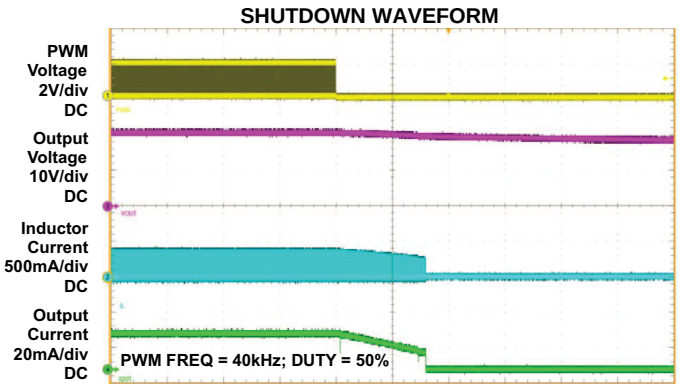

Figure 13.

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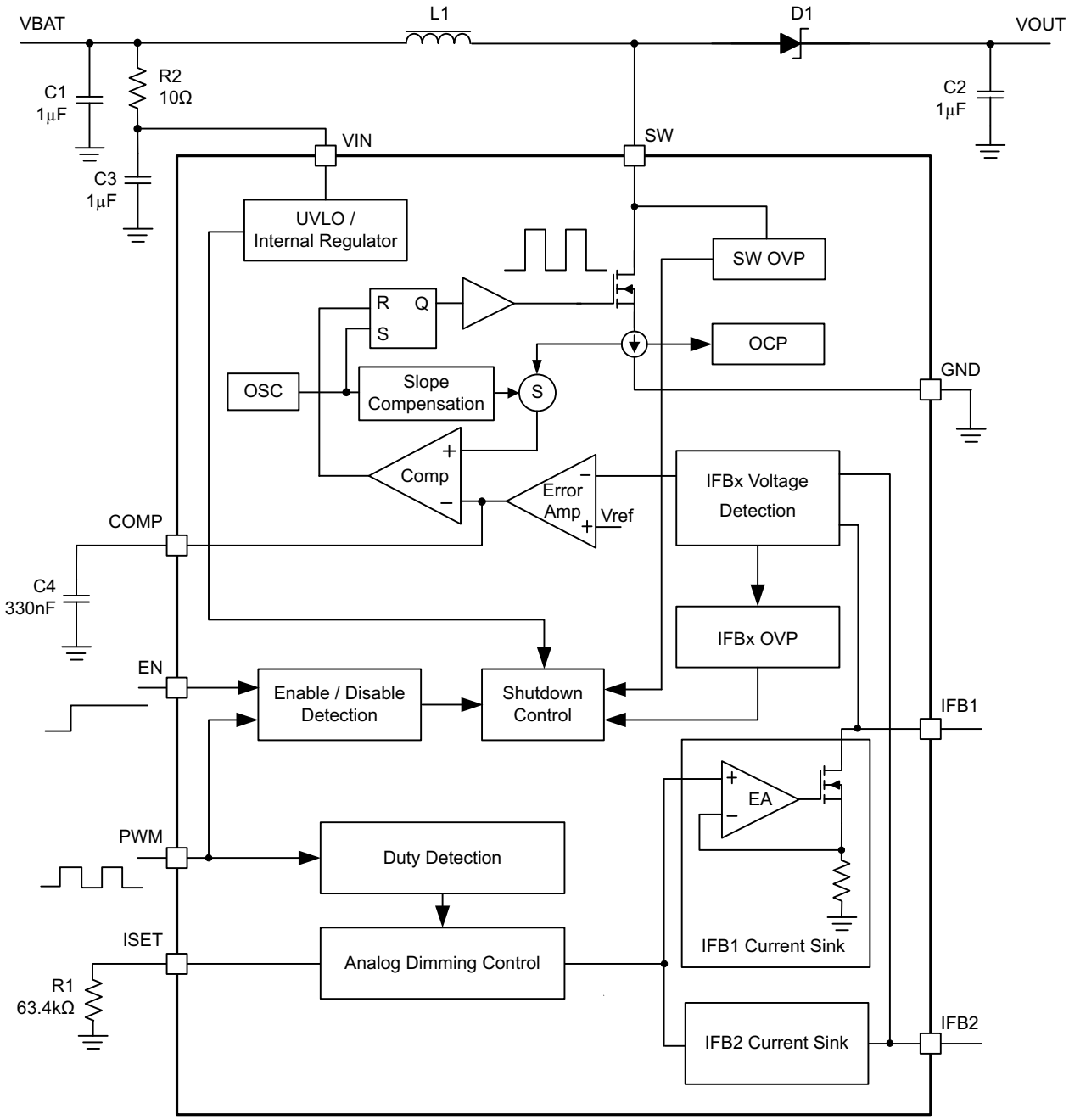
FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

NORMAL OPERATION

In order to provide high brightness backlighting for big size or high resolution smartphone panels, more and more white LED diodes are used. Having all LED diodes in a string improves overall current matching; however, the output voltage of a boost converter will be limited when input voltage is low, and normally the efficiency will drop when output voltage goes very high. Thus the LED diodes are arranged in two parallel strings.

The TPS61163 is a high efficiency, dual-channel white LED driver for such smart phone backlighting applications. Two current sink regulators of high current-matching capability are integrated in the TPS61163 to support dual LED strings connection and to improve the current balance and protect the LED dioeds when either LED string is open or short.

TPS61163 has integrated all of the key function blocks to power and control up to 20 white LED diodes. It includes a 40V/1.5A boost converter, two current sink regulators and protection circuit for over-current, over-voltage and thermal shutdown protection.

BOOST CONVERTER

The boost converter of the TPS61163 integrates 40V 1.5A low side switch MOSFET and has a fixed switching frequency of 1.2MHz. The control architecture is based on traditional current-mode PWM control. For operation see the block diagram. Two current sinks regulate the dual-channel current and the boost output is automatically set by regulating IFBx pin's voltage. The output of error amplifier and the sensed current of switch MOSFET are applied to a control comparator to generate the boost switching duty cycle; slope compensation is added to the current signal to allow stable operation for duty cycles larger than 50%.

The forward voltages of two LED strings are normally different due to the LED diode forward voltage inconsistency, thus the IFB1 and IFB2 voltages are normally different. The TPS61163 can select out the IFBx pin which has a lower voltage than the other and regulates its voltage to a very low value (90mV typical), which is enough for the two current sinks' headroom. In this way, the output voltage of the boost converter is automatically set and adaptive to LED strings' forward voltages, and the power dissipation of the current sink regulators can be reduced remarkably with this very low headroom voltage.

IFBx PIN UNUSED

If only one channel is needed, a user can easily disable the unused channel by connecting its IFBx pin to ground. If both IFBx pins are connected to ground, the IC will not start up.

ENABLE AND STARTUP

In order to enable the IC from shutdown mode, three conditions have to be met: 1. POR (Power On Reset, that is, VIN voltage is higher than UVLO threshold), 2. Logic high on EN pin, 3. PWM signal (logic high or PWM pulses) on PWM pin. When these conditions are all met, an internal LDO linear regulator is enabled to provide supply to internal circuits and the IC can start up.

The TPS61163 supports two dimming interfaces: 1-wire digital interface (EasyScale interface) and PWM interface. TPS61163 begins an EasyScale detection window after startup to detect which interface is selected. If the EasyScale interface is needed, signals of a specific pattern should be input into EN pin during the EasyScale detection window; otherwise, PWM dimming interface will be enabled (see details in 1-Wire Digital Interface (EasyScale Interface)).

After the EasyScale detection window, the TPS61163 checks the status of IFBx pins. If one IFBx pin is detected to connect to ground, the corresponding channel will be disabled and removed from the control loop. Then the soft-start begins and the boost converter starts switching. If both IFBx pins are shorted to ground, the TPS61163 will not start up.

Either pulling EN pin low for more than 2.5ms or pulling PWM pin low for more than 20ms can disable the device and the TPS61163 enters into shutdown mode.

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SOFTSTART

Soft-start is implemented internally to prevent voltage over-shoot and in-rush current. After the IFBx pin status detection, the COMP pin voltage starts ramp up and the boost starts switching. During the beginning 5ms (t_{Half_LIM}) of the switching, the peak current of the switch MOSFET is limited at I_{LIM_Start} (0.7A typical) to avoid the input inrush current. After the 5ms, the current limit is changed to I_{LIM} (1.5A typical) to allow the normal operation of the boost converter.

FULL-SCALE CURRENT PROGRAM

The dual channels of the TPS61163 can provide up to 30 mA current each. No matter either EasyScale interface or PWM interface is selected, the full-scale current (current when dimming duty cycle is 100%) of each channel should be programmed by an external resistor R_{ISET} at ISET pin according to Equation 1.

$$I_{FB_full} = \frac{V_{ISET_full}}{R_{ISET}} \times K_{ISET_full} \quad (1)$$

Where:

I_{FB_full}, full-scale current of each channel
K_{ISET_full} = 1030 (Current multiple when dimming duty cycle = 100%)
V_{ISET_full} = 1.229V (ISET pin voltage when dimming duty cycle = 100%)
R_{ISET} = ISET pin resistor

BRIGHTNESS CONTROL

The TPS61163 controls the DC current of the dual channels to realize the brightness dimming. The DC current control is normally referred to as analog dimming mode. When the DC current of LED diode is reduced, the brightness is dimmed.

The TPS61163 can receive either the PWM signals at the PWM pin (PWM interface) or digital commands at the EN pin (EasyScale interface) for brightness dimming. If the EasyScale interface is selected, the PWM pin should be kept high; if PWM interface is selected, the EN pin should be kept high.

1-Wire Digital Interface (EasyScale Interface)

The EN pin features a simple digital interface to allow digital brightness control. The digital dimming interface can save the processor power and battery life as it does not require PWM signals all the time, and the processor can enter idle mode if possible. In order to enable the EasyScale interface, the following conditions must be satisfied and the specific digital pattern on the EN pin must be recognized by the IC every time the TPS61163 starts up from shutdown mode.

1. VIN voltage is higher than UVLO threshold and PWM pin is pulled high
2. Pull EN pin from low to high to enable the TPS61163. At this moment, the EasyScale detection window starts
3. After EasyScale detection delay time (t_{es_delay}, 100µs), drive EN to low for more than EasyScale detection time (t_{es_detect}, 260µs).

The third step must be finished before the EasyScale detection window (t_{es_win}, 1ms) expires, and once this step is finished, the EasyScale interface is enabled and the EasyScale communication can start. Refer to the Figure 14 for a graphical explanation.

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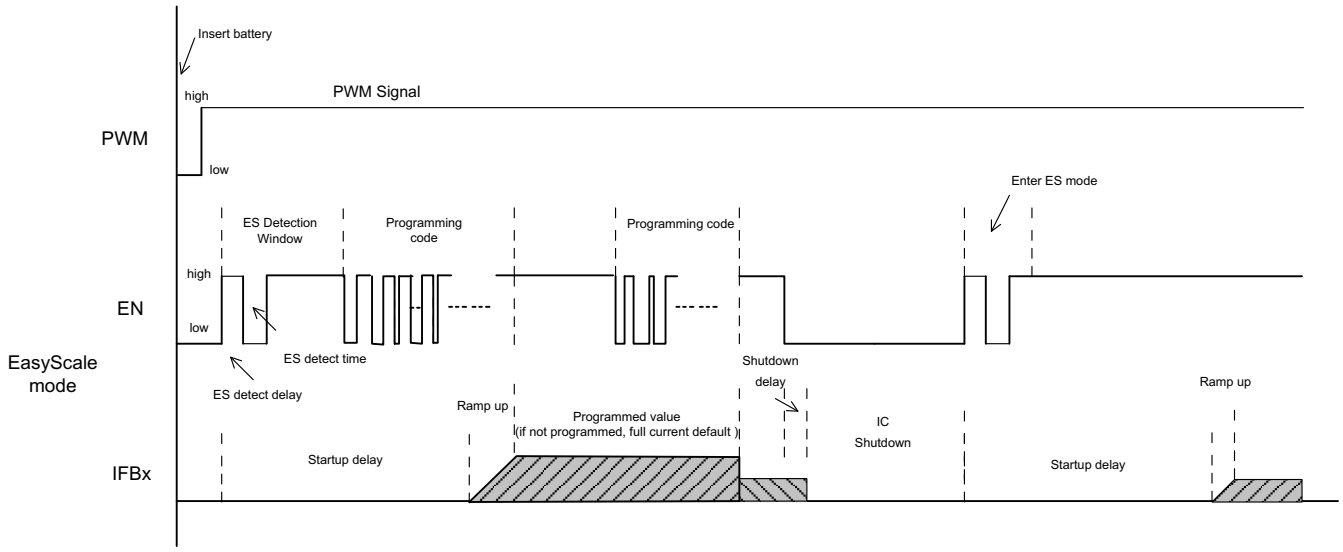

Figure 14. EasyScale Interface Detection

The TPS61163 supports 9-bit brightness code programming. By the EasyScale interface, a master can program the 9-bit code D8(MSB) to D0(LSB) to any of 511 steps with a single command. The default code value of D8~D0 is “111111111” when the device is first enabled, and the programmed value will be stored in an internal register and set the dual-channel current according to Equation 2. The code will be reset to default value when the IC is shut down or disabled.

$$I_{FBx} = I_{FB_full} \times \frac{Code}{511} \quad (2)$$

Where

I_{FB_full}: the full-scale LED current set by the R_{ISET} at ISET pin

Code: the 9-bit brightness code D8~D0 programmed by EasyScale interface

When the 1-wire digital interface at EN pin is selected, the PWM pin can be connected to either VIN pin or a GPIO (refer to ADDITIONAL APPLICATION CIRCUITS). If PWM pin is connected to VIN pin, EN pin alone can enable and disable the IC: pulling EN pin low for more than 2.5ms disables the IC; if PWM pin is connected to a GPIO, both PWM and EN signals should be high to enable the IC, and either pulling EN pin low for more than 2.5ms or pulling PWM pin low for more than 20ms disables the IC.

EasyScale Programming

EasyScale is a simple but flexible one pin interface to configure the current of the dual channels. The interface is based on a master-slave structure, where the master is typically a microcontroller or application processor and the IC is the slave. Figure 15 and Table 2 give an overview of the protocol used by TPS61163. A command consists of 24 bits, including an 8-bit device address byte and a 16-bit data byte. All of the 24 bits should be transmitted together each time, and the LSB bit should be transmitted first. The device address byte D7(MSB)~D0(LSB) is fixed to 0x8F. The data byte includes 9 bits D8(MSB)~D0(LSB) for brightness information and an RFA bit. The RFA bit set to "1" indicates the Request for Acknowledge condition. The Acknowledge condition is only applied when the protocol is received correctly. The advantage of EasyScale compared with other one pin interfaces is that its bit detection is in a large extent independent from the bit transmission rate. It can automatically detect bit rates between 1.7kBit/sec and up to 160kBit/sec.

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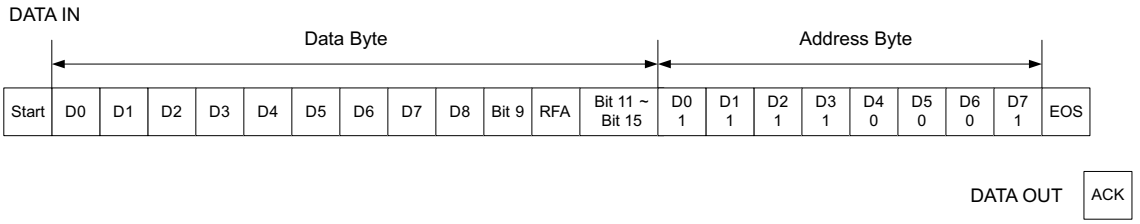

Figure 15. EasyScale™ Protocol Overview

Table 2. EasyScale™ Bit Description

BYTE	BIT NUMBER	NAME	TRANSMISSION DIRECTION	DESCRIPTION
Device Address Byte (0x8F)	23 (MSB)	DA7	IN	DA7 = 1, MSB of device address
	22	DA6		DA6 = 0
	21	DA5		DA5 = 0
	20	DA4		DA4 = 0
	19	DA3		DA3 = 1
	18	DA2		DA2 = 1
	17	DA1		DA1 = 1
	16	DA0		DA0 = 1, LSB of device address
Data Byte	15	Bit 15	IN	No information. Write 0 to this bit.
	14	Bit 14		No information. Write 0 to this bit.
	13	Bit 13		No information. Write 0 to this bit.
	12	Bit 12		No information. Write 0 to this bit.
	11	Bit 11		No information. Write 0 to this bit.
	10	RFA		Request for acknowledge. If set to 1, IC will pull low the data line when it receives the command well. This feature can only be used when the master has an open drain output stage and the data line needs to be pulled high by the master with a pullup resistor; otherwise, acknowledge condition is not allowed and don't set this bit to 1.
	9	Bit 9		No information. Write 0 to this bit.
	8	D8		Data bit 8, MSB of brightness code
	7	D7		Data bit 7
	6	D6		Data bit 6
	5	D5		Data bit 5
	4	D4		Data bit 4
	3	D3		Data bit 3
	2	D2		Data bit 2
	1	D1		Data bit 1
	0 (LSB)	D0		Data bit 0, LSB of brightness code

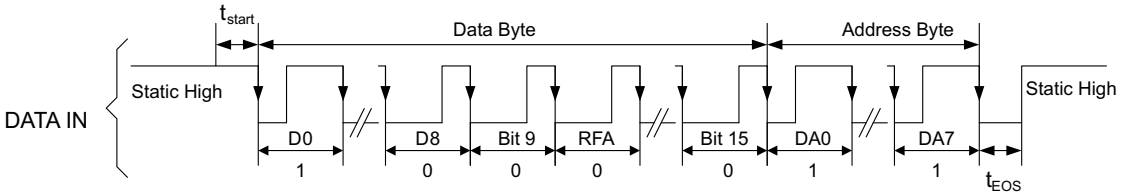

Figure 16. EasyScale Timing, with RFA = 0

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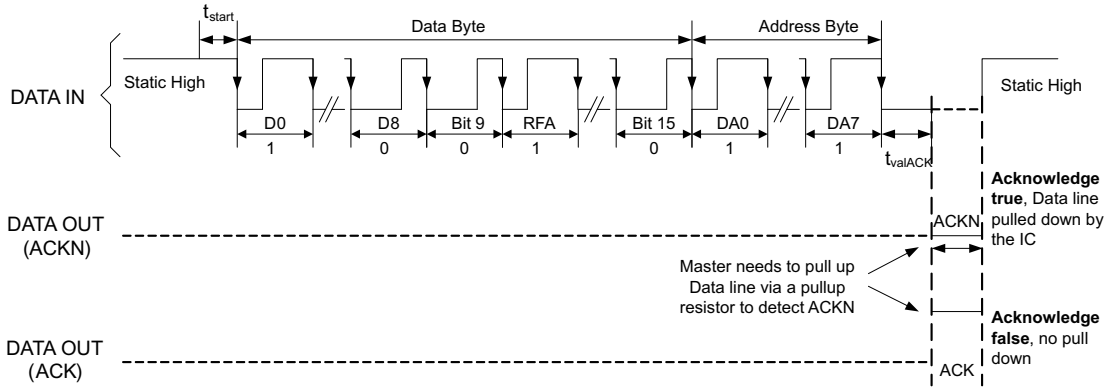

Figure 17. EasyScale Timing, with RFA = 1

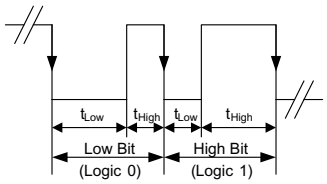

Figure 18. EasyScale — Bit Coding

The 24-bit command should be transmitted with LSB first and MSB last. Figure 16 shows the protocol without acknowledge request (Bit RFA = 0), Figure 17 with acknowledge request (Bit RFA = 1). Before the command transmission, a start condition must be applied. For this, the EN pin must be pulled high for at least t_{start} (2µs) before the bit transmission starts with the falling edge. If the EN pin is already at high level, no start condition is needed. The transmission of each command is closed with an End of Stream condition for at least t_{EOS} (2µs).

The bit detection is based on a Logic Detection scheme, where the criterion is the relation between t_{LOW} and t_{HIGH} (refer to Figure 18). It can be simplified to:

Low Bit (Logic 0): $t_{LOW} \geq 2 \times t_{HIGH}$

High Bit (Logic 1): $t_{HIGH} \geq 2 \times t_{LOW}$

The bit detection starts with a falling edge on the EN pin and ends with the next falling edge. Depending on the relation between t_{HIGH} and t_{LOW}, the logic 0 or 1 is detected.

The acknowledge condition is only applied if:

- Acknowledge is requested by setting RFA bit to 1.
- The transmitted device address matches with the device address of the IC.
- Total 24 bits are received correctly.

If above conditions are met, after t_{valACK} delay from the moment when the last falling edge of the protocol is detected, an internal ACKN-MOSFET is turned on to pull the EN pin low for the time t_{ACKN}, which is 512µs maximum, then the Acknowledge condition is valid. During the t_{valACK} delay, the master controller keeps the line low; after the delay, it should release the line by outputting high impedance and then detect the acknowledge condition. If it reads back a logic 0, it means the IC has received the command correctly. The EN pin can be used again by the master when the acknowledge condition ends after t_{ACKN} time.

Note that the acknowledge condition can only be requested when the master device has an open drain output. For a push-pull output stage, the use of a series resistor in the EN line to limit the current to 500µA is recommended to for such cases as:

- An accidentally requested acknowledge, or
- To protect the internal ACKN-MOSFET.

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PWM Control Interface

The PWM control interface is automatically enabled if the EasyScale interface fails to be enabled during startup. In this case, the TPS61163 receives PWM dimming signals on the PWM pin to control the backlight brightness. When using PWM interface, the EN pin can be connected to VIN pin or a GPIO (refer to ADDITIONAL APPLICATION CIRCUITS). If EN pin is connected to VIN pin, PWM pin alone is used to enable and disable the IC: pulling PWM pin high or apply PWM signals at PWM pin to enable the IC and pulling PWM pin low for more than 20ms to disable the IC; if EN pin is connected to a GPIO, either pulling EN pin low for more than 2.5ms or pulling PWM pin low for more than 20ms can disable the IC. Only after both EN and PWM signals are applied, the TPS61163 can start up. Refer to Figure 19 for a graphical explanation.

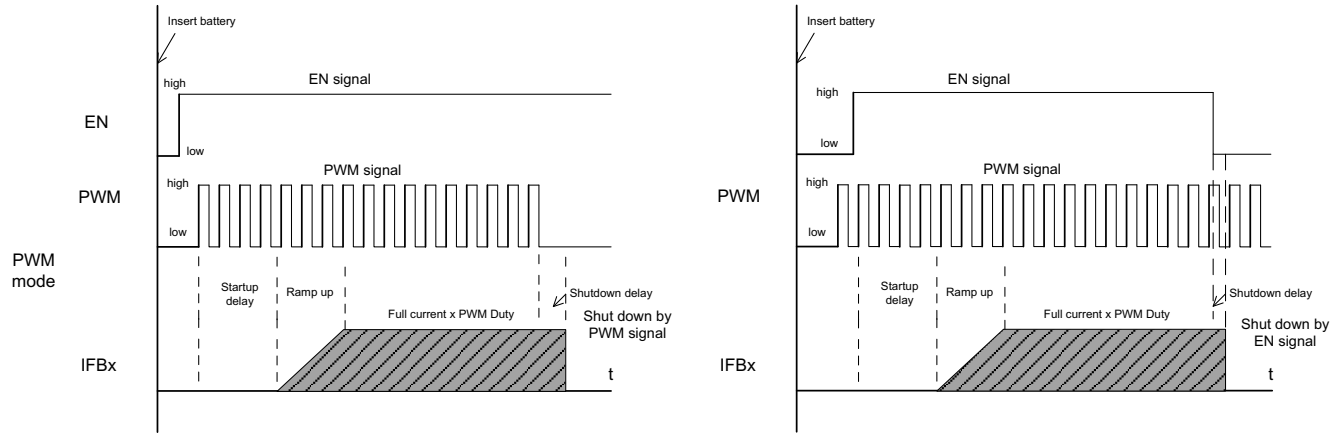

Figure 19. PWM Control Interface Detection

When the PWM pin is constantly high, the dual channel current is regulated to full-scale according to Equation 1. The PWM pin allows PWM signals to reduce this regulation current according to the PWM duty cycle; therefore, it achieves LED brightness dimming. The relationship between the PWM duty cycle and IFBx current is given by Equation 3.

$$I_{FBx} = I_{FB_full} \times Duty \quad (3)$$

Where I_{FBx} is the current of each current sink, I_{FB_full} is the full-scale LED current, Duty is the duty cycle information detected from the PWM signals.

UNDERVOLTAGE LOCKOUT

An undervoltage lockout circuit prevents the operation of the device at input voltages below undervoltage threshold (2.2V typical). When the input voltage is below the threshold, the device is shutdown. If the input voltage rises by undervoltage lockout hysteresis, the IC restarts.

OVERVOLTAGE PROTECTION

Over voltage protection circuitry prevents IC damage as the result of white LED string disconnection or shortage.

The TPS61163 monitors the voltages at SW pin and IFBx pin during each switching cycle. No matter either SW OVP threshold V_{OVP_SW} or IFBx OVP threshold V_{OVP_FB} is reached due to the LED string open or short issue, the protection circuitry will be triggered. Refer to Figure 20 and Figure 21 for the protection actions.

If one LED string is open, its IFBx pin voltage drops, and the boost output voltage is increased by the control loop as it tries to regulate this lower IFBx voltage to the target value (90mV typical). For the normal string, its current is still under regulation but its IFBx voltage increases along with the output voltage. During the process, either the SW voltage reaches its OVP threshold V_{OVP_SW} or the normal string's IFBx pin voltage reaches the IFBx OVP threshold V_{OVP_FB}, then the protection circuitry will be triggered accordingly.

If both LED strings are open, both IFBx pins' voltages drop to ground, and the boost output voltage is increased by the control loop until reaching the SW OVP threshold V_{OVP_SW}, the SW OVP protection circuitry is triggered, and the IC is latched off. Only VIN POR or EN/PWM pin toggling can restart the IC.

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One LED diode short in a string is allowed for the TPS61163. If one LED diode in a string is short, the normal string's IFBx voltage is regulated to about 90mV, and the abnormal string's IFBx pin voltage will be higher. Normally with only one diode short, the higher IFBx pin voltage does not reach the IFBx OVP threshold V_{OVP_FB}, so the protection circuitry will not be triggered.

If more than one LED diodes are short in a string, as the boost loop regulates the normal string's IFBx voltage to 90mV, this abnormal string's IFBx pin voltage is much higher and will reach V_{OVP_FB}, then the protection circuitry is triggered.

The SW OVP protection will also be triggered when the forward voltage drop of an LED string exceeds the SW OVP threshold. In this case, the device turns off the switch FET and shuts down.

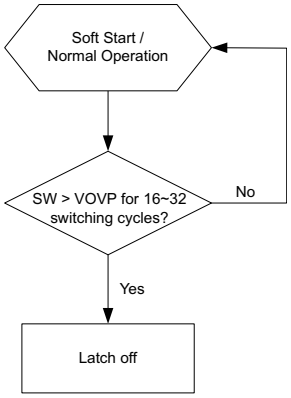

Figure 20. SW OVP Protection Action

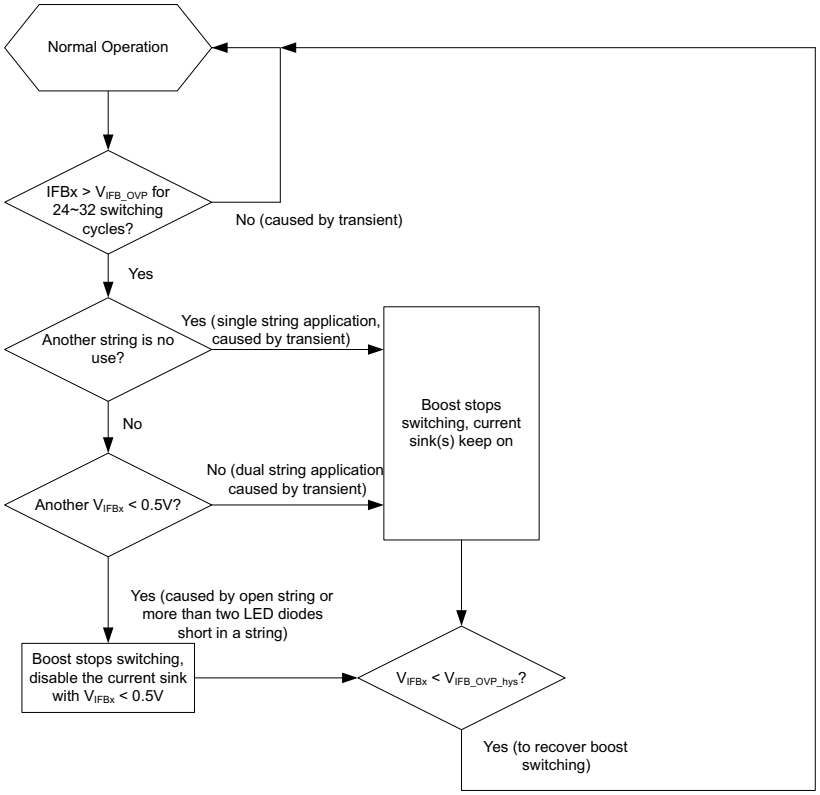

Figure 21. VIFBx OVP Protection Action

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OVER CURRENT PROTECTION

The TPS61163 has a pulse-by-pulse over-current limit. The boost switch turns off when the inductor current reaches this current threshold and it remains off until the beginning of the next switching cycle. This protects the TPS61163 and external component under overload conditions.

THERMAL SHUTDOWN

An internal thermal shutdown turns off the device when the typical junction temperature of 160°C is exceeded. The device is released from shutdown automatically when the junction temperature decreases by 15°C.

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APPLICATION INFORMATION

INDUCTOR SELECTION

Because the selection of inductor affects power supply's steady state operation, transient behavior, loop stability and the boost converter efficiency, the inductor is one of the most important components in switching power regulator design. There are three specifications most important to the performance of the inductor: inductor value, DC resistance, and saturation current. The TPS61163 is designed to work with inductor values from 4.7µH to 10µH to support all applications. A 4.7µH inductor is typically available in a smaller or lower profile package, while a 10µH inductor produces lower inductor ripple. If the boost output current is limited by the over-current protection of the IC, using a 10µH inductor may maximize the controller's output current capability. A 22uH inductor can also be used for some applications, such as 6s2p and 7s2p, but may cause stability issue when more than eight WLED diodes are connected per string. Therefore, customers need to verify the inductor in their application if it is different from the values in RECOMMENDED OPERATING CONDITIONS.

Inductor values can have ±20% or even ±30% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the 0A value depending on how the inductor vendor defines saturation. When selecting an inductor, please make sure its rated current, especially the saturation current, is larger than its peak current during the operation.

Follow Equation 4 to Equation 6 to calculate the inductor's peak current. To calculate the current in the worst case, use the minimum input voltage, maximum output voltage and maximum load current of the application. In order to leave enough design margin, the minimum switching frequency (1MHz for TPS61163), the inductor value with -30% tolerance, and a low power conversion efficiency, such as 80% or lower are recommended for the calculation.

In a boost regulator, the inductor DC current can be calculated as Equation 4.

$$I_{DC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \tag{4}$$

Where

V_{OUT} = boost output voltage
I_{OUT} = boost output current
V_{IN} = boost input voltage
η = boost power conversion efficiency

The inductor current peak to peak ripple can be calculated as Equation 5.

$$I_{PP} = \frac{1}{L \times \left(\frac{1}{V_{OUT} - V_{IN}} + \frac{1}{V_{IN}} \right) \times F_S} \tag{5}$$

Where

I_{PP} = inductor peak-to-peak ripple
L = inductor value
F_S = boost switching frequency
V_{OUT} = boost output voltage
V_{IN} = boost input voltage

Therefore, the peak current I_P seen by the inductor is calculated with Equation 6.

$$I_P = I_{DC} + \frac{I_{PP}}{2} \tag{6}$$

Select an inductor with saturation current over the calculated peak current. If the calculated peak current is larger than the switch MOSFET current limit I_{LIM}, use a larger inductor, such as 10µH, and make sure its peak current is below I_{LIM}.

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Boost converter efficiency is dependent on the resistance of its current path, the switching losses associated with the switch MOSFET and power diode and the inductor's core loss. The TPS61163 has optimized the internal switch resistance, however, the overall efficiency is affected a lot by the inductor's DC Resistance (DCR), Equivalent Series Resistance (ESR) at the switching frequency and the core loss. Core loss is related to the core material and different inductors have different core loss. For a certain inductor, larger current ripple generates higher DCR/ESR conduction losses as well as higher core loss. Normally a datasheet of an inductor does not provide the ESR and core loss information. If needed, consult the inductor vendor for detailed information. Generally, an inductor with lower DCR/ESR is recommended for TPS61163 application. However, there is a trade off among inductor's inductance, DCR/ESR resistance, and its footprint; furthermore, shielded inductors typically have higher DCR than unshielded ones. Table 3 lists some recommended inductors for the TPS61163. Verify whether the recommended inductor can support your target application by the calculations above as well as bench validation.

Table 3. Recommended Inductors

PART NUMBER	L (uH)	DCR MAX (mΩ)	SATURATION CURRENT (A)	Size (L x W x H mm)	VENDOR
LPS4018-472ML	4.7	125	1.9	4 x 4 x 1.8	Coilcraft
LPS4018-682ML	6.8	150	1.3	4 x 4 x 1.8	Coilcraft
LPS4018-103ML	10	200	1.3	4 x 4 x 1.8	Coilcraft
PCMB051B-4R7M	4.7	163	2.7	5.4 x 5.2 x 1.2	Cyntec
PCMB051B-6R8M	6.8	250	2.3	5.4 x 5.2 x 1.2	Cyntec

SCHOTTKY DIODE SELECTION

The TPS61163 demands a low forward voltage, high-speed and low capacitance schottky diode for optimum efficiency. Ensure that the diode average and peak current rating exceeds the average output current and peak inductor current. In addition, the diode's reverse breakdown voltage must exceed the open LED protection voltage. ONSemi MBR0540 and NSR05F40, and Vishay MSS1P4 are recommended for the TPS61163.

COMPENSATION CAPACITOR SELECTION

The compensation capacitor C4 (refer to ADDITIONAL APPLICATION CIRCUITS) connected from the COMP pin to GND, is used to stabilize the feedback loop of the TPS61163. A 330nF ceramic capacitor for C4 is suitable for most applications. A 470nF is also OK for some applications and customers are suggested to verify it in their applications.

OUTPUT CAPACITOR SELECTION

The output capacitor is mainly selected to meet the requirement for the output ripple and loop stability. A 1µF to 2.2µF capacitor is recommended for the loop stability consideration. This ripple voltage is related to the capacitor's capacitance and its equivalent series resistance (ESR). Due to its low ESR, V_{ripple_ESR} could be neglected for ceramic capacitors. Assuming a capacitor with zero ESR, the output ripple can be calculated with Equation 7.

$$V_{ripple} = \frac{(V_{OUT} - V_{IN}) \times I_{OUT}}{V_{OUT} \times F_S \times C_{OUT}} \quad (7)$$

Where: V_{ripple} = peak-to-peak output ripple. The additional part of ripple caused by the ESR is calculated using $V_{ripple_ESR} = I_{OUT} \times R_{ESR}$ and can be ignored for ceramic capacitors.

Note that capacitor degradation increases the ripple much. Select the capacitor with 50V rated voltage to reduce the degradation at the output voltage. If the output ripple is too large, change a capacitor with less degradation effect or with higher rated voltage could be helpful.

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LAYOUT CONSIDERATION

As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully done, the regulator could show instability as well as EMI problems. Therefore, use wide and short traces for high current paths. The input capacitor, C1 in ADDITIONAL APPLICATION CIRCUITS, needs to be close to the inductor, as well as the VIN pin and GND pin in order to reduce the input ripple seen by the IC. If possible, choose higher capacitance value for it. If the ripple seen at VIN pin is so large that it affects the boost loop stability or internal circuits operation, R2 and C3 are recommended to filter and decouple the noise. In this case, C3 should be placed as close as possible to the VIN and GND pins. The SW pin carries high current with fast rising and falling edges. Therefore, the connection between the SW pin to the inductor and schottky diode should be kept as short and wide as possible. The trace between schottky diode and the output capacitor C2 should also be as short and wide as possible. It is also beneficial to have the ground of the output capacitor C2 close to the GND pin since there is a large ground return current flowing between them. When laying out signal grounds, it is recommended to use short traces separated from power ground traces, and connect them together at a single point close to the GND pin.

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ADDITIONAL APPLICATION CIRCUITS

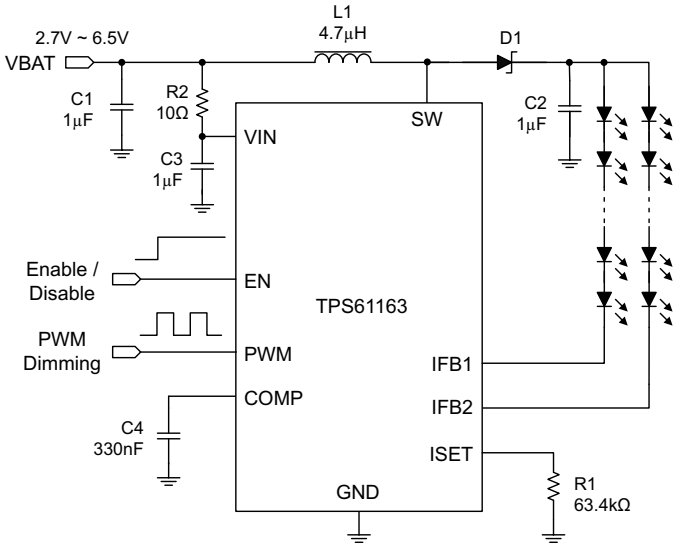

Figure 22. TPS61163 Typical Application (PWM interface enabled, EN pin can be used to enable or disable the IC)

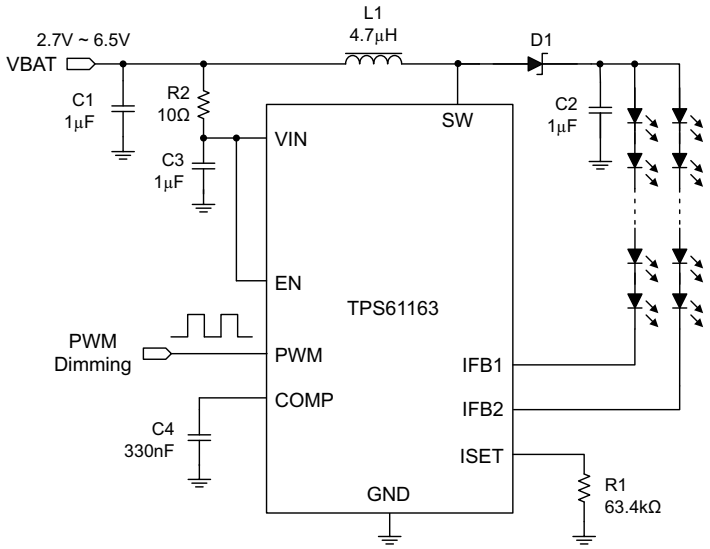

Figure 23. TPS61163 Typical Application (PWM interface enabled, EN pin connected to VIN, only PWM signal is used to enable or disable the IC)

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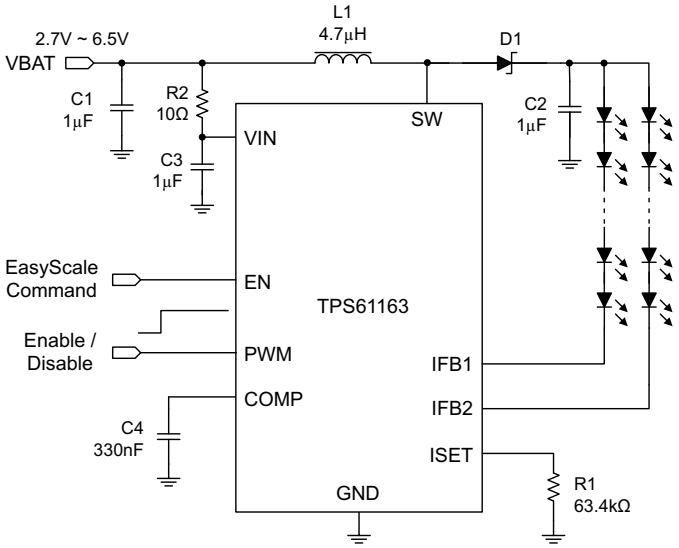

Figure 24. TPS61163 Typical Application (1-wire digital interface enabled, PWM pin can be used to enable or disable the IC)

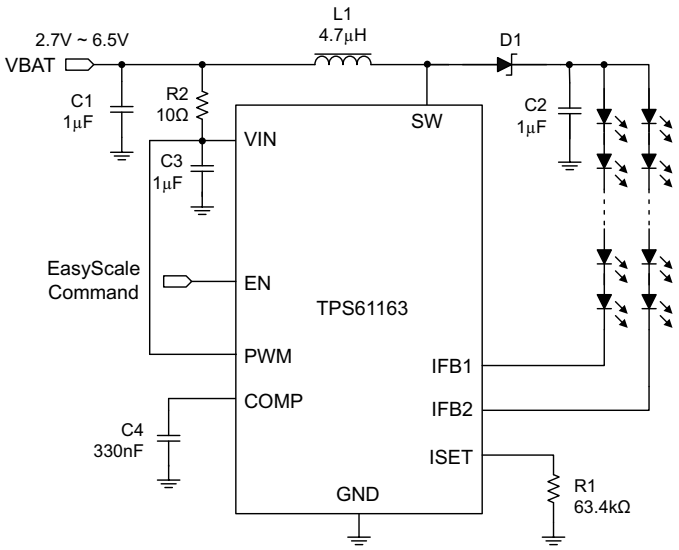

Figure 25. TPS61163 Typical Application (1-wire digital interface enabled, PWM pin connected to VIN, only EN signal is used to enable or disable the IC)

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REVISION HISTORY

Changes from Original (January 2013) to Revision A **Page**

- 更改为产品预览器件 1

Changes from Revision A (February 2013) to Revision B **Page**

- 1

Changes from Revision B (March 2013) to Revision C **Page**

- Deleted 数据表中 TPS61162 器件的首次发布 1
- Changed PWM Freq = 20kHz to PWM Freq = 40kHz in the descriptions of Figure 1 - Figure 7, Figure 9, Figure 11, and Figure 13 in Table 1 6
- Changed PWM FREQ = 20kHz to PWM FREQ = 40kHz in Figure 9 7
- Changed PWM FREQ = 20kHz to PWM FREQ = 40kHz in Figure 11 7
- Changed PWM FREQ = 20kHz to PWM FREQ = 40kHz in Figure 13 8

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61163YFFR	NRND	DSBGA	YFF	9	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 150	TPS 61163	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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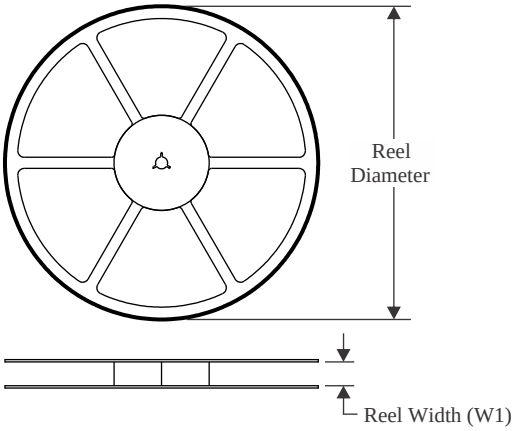
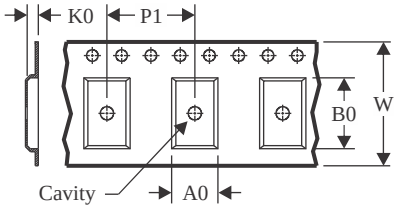
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

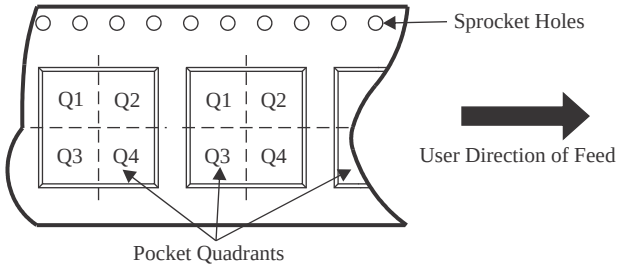


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

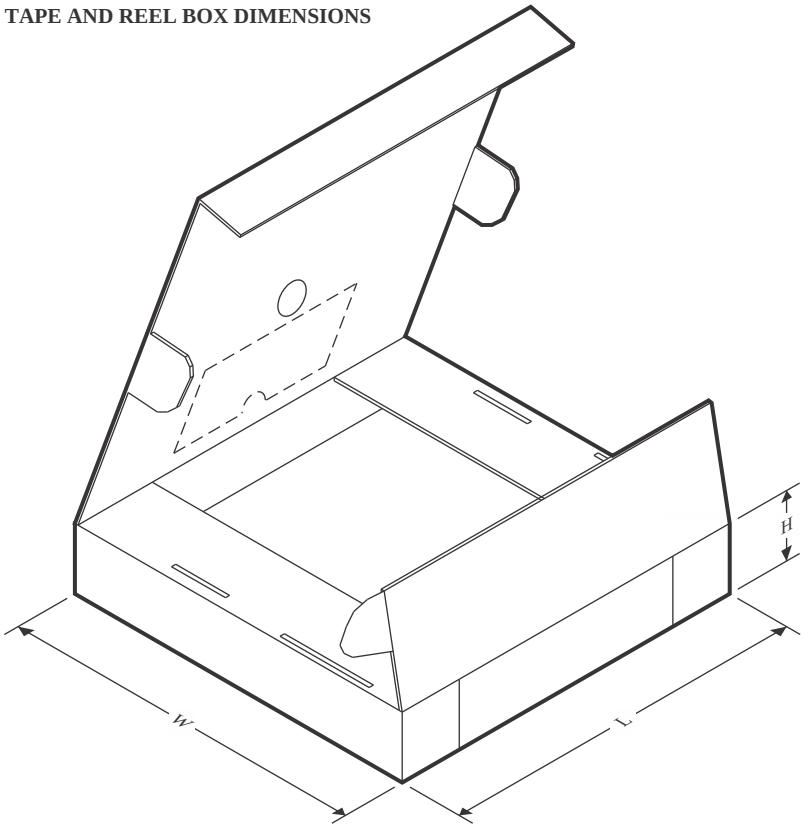
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61163YFFR	DSBGA	YFF	9	3000	180.0	8.4	1.45	1.45	0.8	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

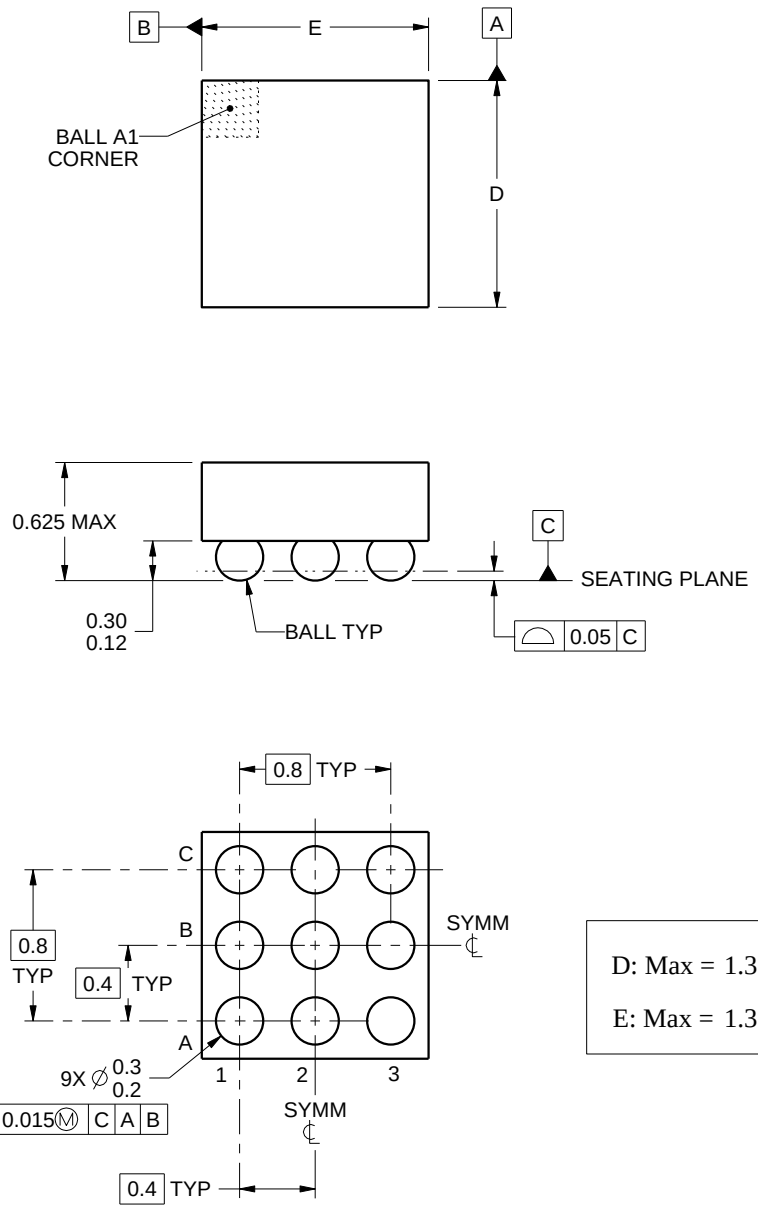
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61163YFFR	DSBGA	YFF	9	3000	182.0	182.0	20.0

PACKAGE OUTLINE

YFF0009

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



D: Max = 1.336 mm, Min =1.276 mm

E: Max = 1.336 mm, Min =1.276 mm

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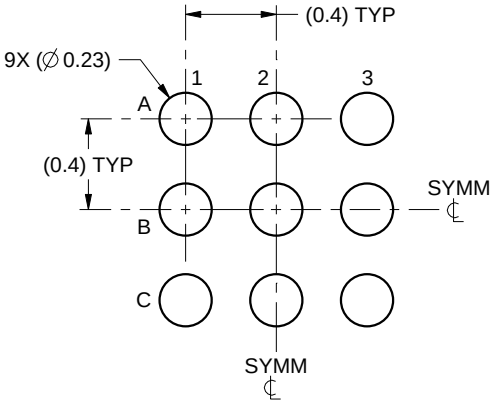
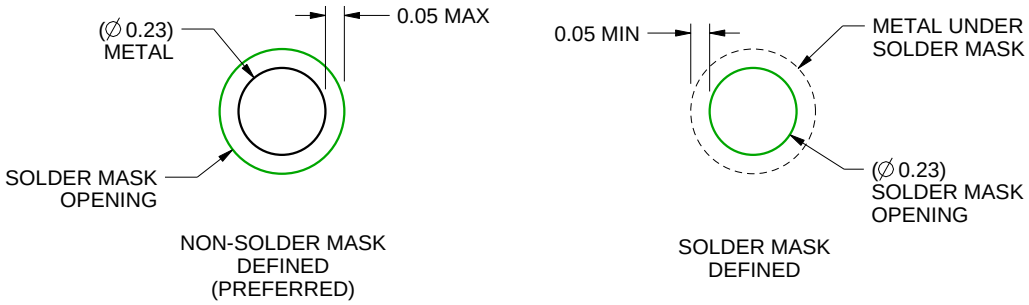
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X



SOLDER MASK DETAILS
NOT TO SCALE

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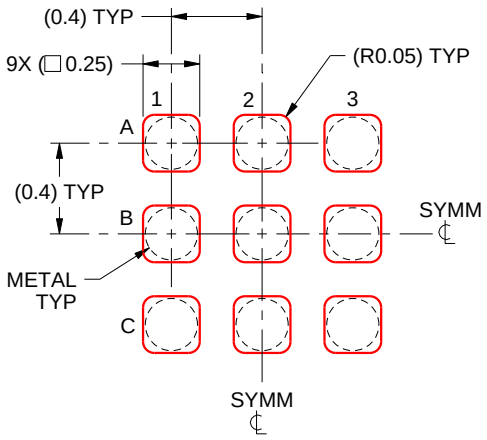
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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