TEXAS INSTRUMENTS

TPS62000, TPS62001, TPS62002, TPS62003
TPS62004, TPS62005, TPS62006, TPS62007, TPS62008

SLVS294F – SEPTEMBER 2000 – REVISED AUGUST 2015

TPS6200x High-Efficiency Step-Down Low Power DC-DC Converter

1 Features

- High-Efficiency Synchronous Step-Down Converter with More than 95% Efficiency
- 2-V to 5.5-V Operating Input Voltage Range
- Adjustable Output Voltage Range From 0.8 V to V_{IN}
- Fixed Output Voltage Options Available in 0.9 V, 1 V, 1.2 V, 1.5 V, 1.8 V, 1.9 V, 2.5 V, and 3.3 V
- Synchronizable to External Clock Signal up to 1 MHz
- Up to 600 mA Output Current
- Pin-Programmable Current Limit
- High Efficiency Over a Wide Load Current Range in Power Save Mode
- 100% Maximum Duty Cycle for Lowest Dropout
- Low-Noise Operation Antiringing Switch and PFM/PWM Operation Mode
- Internal Softstart
- 50-µA Quiescent Current (TYP)
- Available in the 10-Pin Microsmall Outline Package (VSSOP)
- Evaluation Module Available

2 Applications

- Low-Power CPUs and DSPs
- Cellular Phones
- Organizers, PDAs, and Handheld PCs
- MP-3 Portable Audio Players
- Digital Cameras
- USB-Based DSL Modems and Other Network Interface Cards

3 Description

The TPS6200x devices are a family of low-noise synchronous step-down DC/DC converters that are ideally suited for systems powered from a 1-cell Li-ion battery or from a 2- to 3-cell NiCd, NiMH, or alkaline battery. The TPS6200x operates typically down to an input voltage of 1.8 V, with a specified minimum input voltage of 2 V.

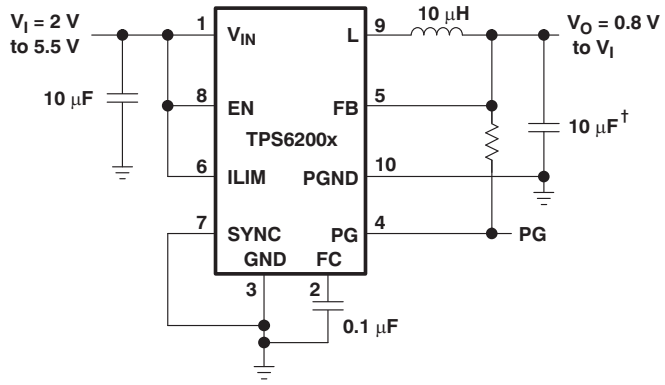
The TPS62000 operates over a free-air temperature range of –40°C to 85°C.The device is available in the 10-pin (DGS) microsmall outline package (VSSOP).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS6200x	VSSOP (10)	3.00 mm × 3.00 mm

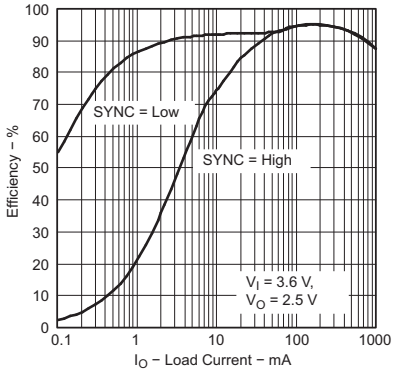
(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Schematic



† With V_O ≥1.8 V; C_o = 10 µF, V_O <1.8 V; C_o = 47 µF

Efficiency vs Load Current



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (August 2008) to Revision F	Page
• Added *Pin Configuration and Functions* section, *ESD Ratings*, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

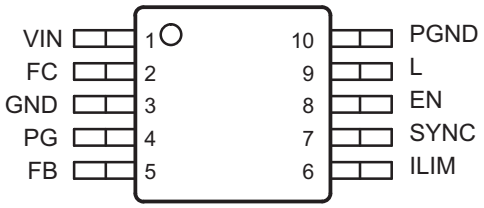
5 Device Comparison Table

VOLTAGE OPTIONS	PACKAGE(1)	MARKING
	VSSOP	DGS
Adjustable	TPS62000DGS	AIH
0.9 V	TPS62001DGS	AII
1 V	TPS62002DGS	AIJ
1.2 V	TPS62003DGS	AIK
1.5 V	TPS62004DGS	AIL
1.8 V	TPS62005DGS	AIM
1.9 V	TPS62008DGS	AJI
2.5 V	TPS62006DGS	AIN
3.3 V	TPS62007DGS	AIO

(1) For shipment quantities and additional package information see *Mechanical, Packaging, and Orderable Information*

6 Pin Configuration and Functions

DGS Package
10-Pin VSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	8	I	Enable. A logic high enables the converter, logic low forces the device into shutdown mode reducing the supply current to less than 1 µA.
FB	5	I	Feedback pin for the fixed output voltage option. For the adjustable version an external resistive divider is connected to FB. The internal voltage divider is disabled for the adjustable version.
FC	2	—	Supply bypass pin. A 0.1-µF coupling capacitor should be connected as close as possible to this pin for good high frequency input voltage supply filtering.
GND	3	—	Ground
ILIM	6	I	Switch current limit. Connect ILIM to GND to set the switch current limit to typically 600 mA, or connect this pin to V_{IN} to set the current limit to typically 1200 mA.
L	9	I/O	Connect the inductor to this pin. L is the switch pin connected to the drain of the internal power MOSFETS.
PG	4	O	Power good comparator output. This is an open-drain output. A pull-up resistor should be connected between PG and V_{OUT}. The output goes active high when the output voltage is greater than 92% of the nominal value.
PGND	10	—	Power ground. Connect all power grounds to PGND.
SYNC	7	I	Input for synchronization to external clock signal. Synchronizes the converter switching frequency to an external clock signal with CMOS level: SYNC = High: Low-noise mode enabled, fixed frequency PWM operation is forced SYNC = Low (GND): Power save mode enabled, PFM/PWM mode enabled
VIN	1	I	Supply voltage input

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
	Supply voltages on pin VIN and FC(2)	–0.3	6	V
	Voltages on pins EN, ILIM, SYNC, PG, FB, L(2)	–0.3	V_{IN} + 0.3	V
	Peak switch current		1.6	A
T_J	Operating junction temperature	–40	150	°C
	Lead temperature (soldering, 10 sec)		260	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage	2		5.5	V
V_{OUT}	Output voltage range for adjustable output voltage version	0.8		V_{IN}	V
I_{OUT}	Output current for 3-cell operation (V_{IN} ≥ 2.5 V; L = 10 µH, f = 750 kHz)			600	mA
I_{OUT}	Output current for 2-cell operation (V_{IN} ≥ 2 V; L = 10 µH, f = 750 kHz)			200	mA
L	Inductor(1) (see Note 2)		10		µH
C_{IN}	Input capacitor(1)	10			µF
C_{OUT}	Output capacitor(1) (V_{OUT} ≥ 1.8 V)	10			µF
C_{OUT}	Output capacitor(1) V_{OUT} < 1.8 V)	47			µF
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

(1) Refer to *Application Information* section for further information.

7.4 Thermal Information

THERMAL METRIC(1)		TPS6200x DGS [VSSOP] 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	160	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	73	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	72	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Over recommended operating free-air temperature range, V_{IN} = 3.6 V, V_{OUT} = 2.5 V, I_{OUT} = 300 mA, EN = V_{IN}, ILIM = V_{IN}, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
V_{IN}	Input voltage range		I_{OUT} = 0 mA to 600 mA	2.5		5.5	V
			I_{OUT} = 0 mA to 200 mA	2		5.5	
$I_{(Q)}$	Operating quiescent current		I_{OUT} = 0 mA, SYNC = GND (PFM-mode enabled)		50	75	µA
$I_{(SD)}$	Shutdown current		EN = GND		0.1	1	µA
ENABLE							
V_{IH}	EN high-level input voltage			1.3			V
V_{IL}	EN low-level input voltage					0.4	V
I_{lkg}	EN input leakage current		EN = GND or V_{IN}		0.01	0.1	µA
$V_{(UVLO)}$	Undervoltage lockout threshold			1.2	1.6	1.95	V
POWER SWITCH AND CURRENT LIMIT							
$R_{DS(on)}$	P-channel MOSFET on-resistance		V_{IN} = V_{GS} = 3.6 V, I = 200 mA	200	280	410	mΩ
			V_{IN} = V_{GS} = 2 V, I = 200 mA		480		
	P-channel leakage current		V_{DS} = 5.5 V			1	µA
	N-channel MOSFET on-resistance		V_{IN} = V_{GS} = 3.6 V, I_{OUT} = 200 mA	200	280	410	mΩ
			V_{IN} = V_{GS} = 2 V, I_{OUT} = 200 mA		500		
	N-channel leakage current		V_{DS} = 5.5 V			1	µA
$I_{(LIM)}$	P-channel current limit		2.5 V ≤ V_{IN} ≤ 5.5 V, ILIM = V_{IN}	800	1200	1600	mA
			2 V ≤ V_{IN} ≤ 5.5 V, ILIM = GND	390	600	900	
V_{IH}	ILIM high-level input voltage			1.3			V
V_{IL}	ILIM low-level input voltage					0.4	V
I_{lkg}	ILIM input leakage current		ILIM = GND or V_{IN}		0.01	0.1	µA
POWER GOOD OUTPUT (see (1))							
$V_{(PG)}$	Power good threshold		Feedback voltage falling	88% V_{OUT}	92% V_{OUT}	94% V_{OUT}	V
	Power good hysteresis				2.5% V_{OUT}		V
V_{OL}	PG output low voltage		$V_{(FB)}$ = 0.8 × V_{OUT} nominal, $I_{(sink)}$ = 10 µA			0.3	V
I_{lkg}	PG output leakage current		$V_{(FB)}$ = V_{OUT} nominal		0.01	1	µA
	Minimum supply voltage for valid power good signal			1.2			V
OSCILLATOR							
f_s	Oscillator frequency			500	750	1000	kHz
$f_{(SYNC)}$	Synchronization range		CMOS-logic clock signal on SYNC pin	500		1000	kHz
V_{IH}	SYNC high level input voltage			1.3			V
V_{IL}	SYNC low level input voltage					0.4	V
I_{lkg}	SYNC input leakage current		SYNC = GND or V_{IN}		0.01	0.1	µA
	Duty cycle of external clock signal			20%		60%	
V_O	Adjustable output voltage range	TPS62000		0.8		5.5	V
V_{ref}	Reference voltage	TPS6200x			0.45		V

(1) Power good is not valid for the first 100 µs after EN goes high. Refer to the application section for more information.

Electrical Characteristics (continued)

Over recommended operating free-air temperature range, V_{IN} = 3.6 V, V_{OUT} = 2.5 V, I_{OUT} = 300 mA, EN = V_{IN}, ILIM = V_{IN}, T_A = –40°C to 85°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Fixed output voltage	TPS62000 adjustable	V_{IN} = 2.5 V to 5.5 V; 0 mA ≤ I_{OUT} ≤ 600 mA	–3%		4%	V
			10 mA < I_{OUT} ≤ 600 mA	–3%		3%	
		TPS62001 0.9 V	V_{IN} = 2.5 V to 5.5 V; 0 mA ≤ I_{OUT} ≤ 600 mA	–3%		4%	
			10 mA < I_{OUT} ≤ 600 mA	–3%		3%	
		TPS62002 1 V	V_{IN} = 2.5 V to 5.5 V; 0 mA ≤ I_{OUT} ≤ 600 mA	–3%		4%	
			10 mA < I_{OUT} ≤ 600 mA	–3%		3%	
		TPS62003 1.2 V	V_{IN} = 2.5 V to 5.5 V; 0 mA ≤ I_{OUT} ≤ 600 mA	–3%		4%	
			10 mA < I_{OUT} ≤ 600 mA	–3%		3%	
		TPS62004 1.5 V	V_{IN} = 2.5 V to 5.5 V; 0 mA ≤ I_{OUT} ≤ 600 mA	–3%		4%	
			10 mA < I_{OUT} ≤ 600 mA	–3%		3%	
		TPS62005 1.8 V	V_{IN} = 2.5 V to 5.5 V; 0 mA ≤ I_{OUT} ≤ 600 mA	–3%		4%	
			10 mA < I_{OUT} ≤ 600 mA	–3%		3%	
		TPS62008 1.9 V	V_{IN} = 2.5 V to 5.5 V; 0 mA ≤ I_{OUT} ≤ 600 mA	–3%		4%	
			10 mA < I_{OUT} ≤ 600 mA	–3%		3%	
		TPS62006 2.5 V	V_{IN} = 2.7 V to 5.5 V; 0 mA ≤ I_{OUT} ≤ 600 mA	–3%		4%	
			10 mA < I_{OUT} ≤ 600 mA	–3%		3%	
		TPS62007 3.3 V	V_{IN} = 3.6 V to 5.5 V; 0 mA ≤ I_{OUT} ≤ 600 mA	–3%		4%	
			10 mA < I_{OUT} ≤ 600 mA	–3%		3%	
	Line regulation		V_{IN} = V_{OUT} + 0.5 V (min. 2 V) to 5.5 V, I_{OUT} = 10 mA		0.05		%/V
	Load regulation		V_{IN} = 5.5 V; I_{OUT} = 10 mA to 600 mA		0.6%		
η	Efficiency		V_{IN} = 5 V; V_{OUT} = 3.3 V; I_{OUT} = 300 mA		95%		
			V_{IN} = 3.6 V; V_{OUT} = 2.5 V; I_{OUT} = 200 mA				
	Start-up time		I_{OUT} = 0 mA, time from active EN to V_{OUT}	0.4		2	ms

7.6 Typical Characteristics

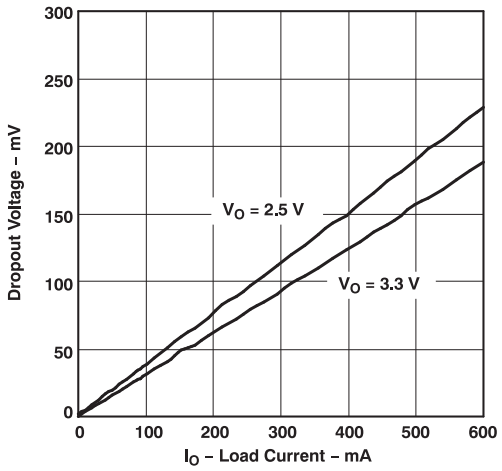


Figure 1. Dropout Voltage vs Load Current

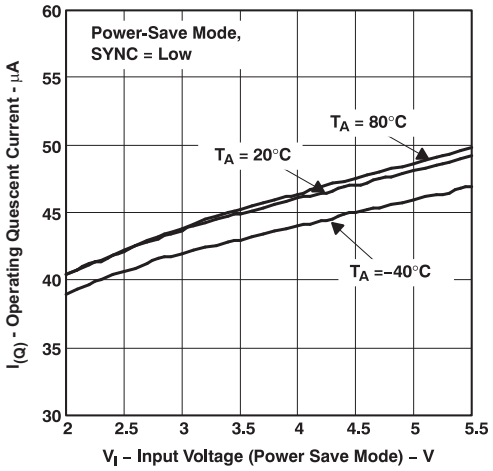


Figure 2. Operating Quiescent Current vs Input Voltage (Power Save Mode)

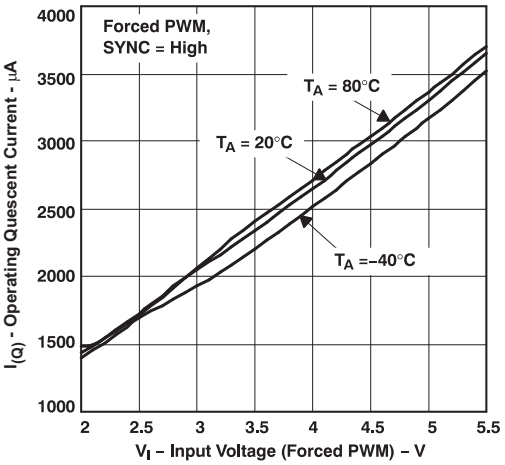


Figure 3. Operating Quiescent Current vs Input Voltage (Forced PWM)

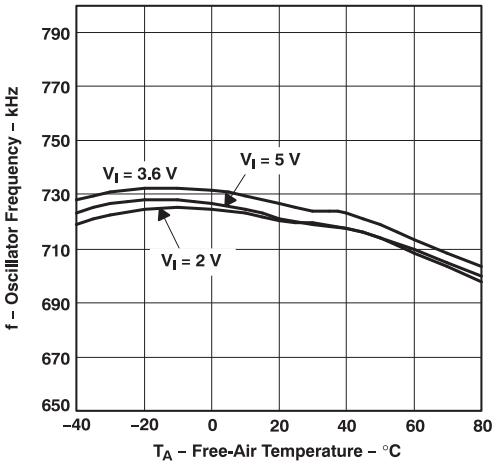


Figure 4. Oscillator Frequency vs Free-Air Temperature

8 Detailed Description

8.1 Overview

The TPS6200x is a step down converter operating in a current mode PFM/PWM scheme with a typical switching frequency of 750 kHz.

At moderate to heavy loads, the converter operates in the pulse width modulation (PWM) and at light loads the converter enters a power save mode (pulse frequency modulation, PFM) to keep the efficiency high.

In the PWM mode operation, the part operates at a fixed frequency of 750 kHz. At the beginning of each clock cycle, the high side P-channel MOSFET is turned on. The current in the inductor ramps up and is sensed via an internal circuit. The high side switch is turned off when the sensed current causes the PFM/PWM comparator to trip when the output voltage is in regulation or when the inductor current reaches the current limit (set by ILIM). After a minimum dead time preventing shoot through current, the low side N-channel MOSFET is turned on and the current ramps down again. As the clock cycle is completed, the low side switch is turned off and the next clock cycle starts.

In discontinuous conduction mode (DCM), the inductor current ramps to zero before the end of each clock cycle. In order to increase the efficiency the load comparator turns off the low side MOSFET before the inductor current becomes negative. This prevents reverse current flowing from the output capacitor through the inductor and low side MOSFET to ground that would cause additional losses.

As the load current decreases and the peak inductor current does not reach the power save mode threshold of typically 120 mA for more than 15 clock cycles, the converter enters a pulse frequency modulation (PFM) mode.

In the PFM mode, the converter operates with:

- Variable frequency
- Constant peak current that reduces switching losses
- Quiescent current at a minimum

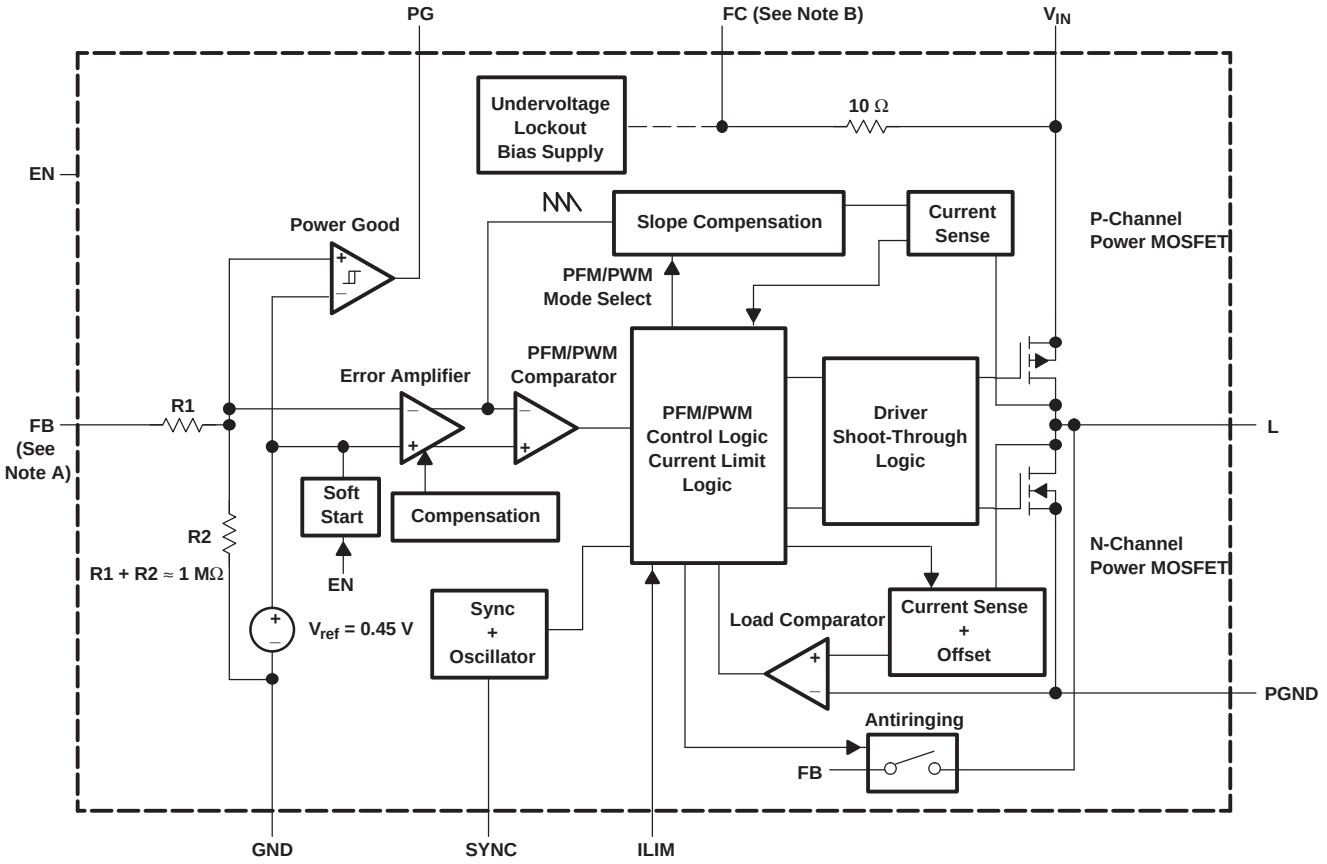
Thus maintaining the highest efficiency at light load currents. In this mode, the output voltage is monitored with the error amplifier. As soon as the output voltage falls below the nominal value, the high side switch is turned on and the inductor current ramps up. When the inductor current reaches the peak current of typical: 150 mA + 50 mA/V × (V_{IN} – V_{OUT}), the high side switch turns off and the low side switch turns on. As the inductor current ramps down, the low side switch is turned off before the inductor current becomes negative which completes the cycle. When the output voltage falls below the nominal voltage again, the next cycle is started.

The converter enters the PWM mode again as soon as the output voltage can not be maintained with the typical peak inductor current in the PFM mode.

The control loop is internally compensated reducing the amount of external components.

The switch current is internally sensed and the maximum current limit can be set to typical 600 mA by connecting ILIM to ground; or, to typically 1.2 A by connecting ILIM to V_{IN}.

8.2 Functional Block Diagram



A. The adjustable output voltage version does not use the internal feedback resistor divider. The FB pin is directly connected to the error amplifier.

B. Do not connect the FC pin to an external power source

8.3 Feature Description

8.3.1 Low Noise Antiringing Switch

An *antiringing* switch is implemented in order to reduce the EMI radiated from the converter during discontinuous conduction mode (DCM). In DCM, the inductor current ramps to zero before the end of each switching period. The internal load comparator turns off the low side switch at that instant thus preventing the current flowing backward through the inductance which increases the efficiency. An antiringing switch across the inductor prevents parasitic oscillation caused by the residual energy stored in the inductance (see Figure 11).

NOTE

The *antiringing* switch is only activated in the fixed output voltage versions. It is not enabled for the adjustable output voltage version TPS62000.

8.3.2 Enable

Logic low on EN forces the TPS6200x into shutdown. In shutdown, the power switch, drivers, voltage reference, oscillator, and all other functions are turned off. The supply current is reduced to less than 1 µA in the shutdown mode.

Feature Description (continued)

8.3.3 Undervoltage Lockout

An undervoltage lockout circuit provides the save operation of the device. It prevents the converter from turning on when the voltage on V_{IN} is less than typically 1.6 V.

8.3.4 Power Good Comparator

The power good (PG) comparator has an open drain output capable of sinking typically 10 µA. The PG is only active when the device is enabled (EN = high). When the device is disabled (EN = low), the PG pin is high impedance.

The PG output is only valid after a 100 µs delay after the device is enabled and the supply voltage is greater than 1.2 V. This is only important in cases where the pullup resistor of the PG pin is connected to an external voltage source which might cause an initial spike (false high signal) within the first 100 µs after the input voltage exceeds 1.2 V. This initial spike can be filtered with a small R-C filter to avoid false power good signals during start-up.

If the PG pin is connected to the output of the TPS62000 with a pullup resistor, no initial spike (false high signal) occurs and no precautions have to be taken during start-up.

The PG pin becomes active high when the output voltage exceeds typically 94.5% of its nominal value. Leave the PG pin unconnected when not used.

8.4 Device Functional Modes

The TPS6200x is a synchronous current-mode PWM converter with integrated – and P-channel power MOSFET switches. Synchronous rectification is used to increase efficiency and to reduce external component count. To achieve the highest efficiency over a wide load current range, the converter enters a power-saving pulse-frequency modulation (PFM) mode at light load currents. Operating frequency is typically 750 kHz, allowing the use of small inductor and capacitor values. The device can be synchronized to an external clock signal in the range of 500 kHz to 1 MHz. For low-noise operation, the converter can be operated in the PWM mode and the internal antiringing switch reduces noise and EMI. In the shutdown mode, the current consumption is reduced to less than 1 µA. The TPS62000 is available in the 10-pin (DGS) microsmall outline package (VSSOP). The device operates over a free-air temperature range of –40°C to 85°C.

8.4.1 Soft Start

As the enable pin (EN) goes high, the soft-start function generates an internal voltage ramp. This causes the start-up current to slowly rise preventing output voltage overshoot and high inrush currents. The soft-start duration is typical 1 ms (see Figure 12). When the soft-start function is completed, the error amplifier is connected directly to the internal voltage reference.

8.4.2 Synchronization, Power Save Mode, and Forced PWM Mode

If no clock signal is applied, the converter operates with a typical switching frequency of 750 kHz. It is possible to synchronize the converter to an external clock within a frequency range from 500 kHz to 1000 kHz. The device automatically detects the rising edge of the first clock and is synchronized immediately to the external clock. If the clock signal is stopped, the converter automatically switches back to the internal clock and continues operation without interruption. The switch over is initiated if no rising edge on the SYNC pin is detected for a duration of four clock cycles. Therefore, the maximum delay time can be 8 µs in case the internal clock has a minimum frequency of 500 kHz.

In case the device is synchronized to an external clock, the power save mode is disabled and the device stays in forced PWM mode.

Connecting the SYNC pin to the GND pin enables the power save mode. The converter operates in the PWM mode at moderate to heavy loads and in the PFM mode during light loads maintaining high efficiency over a wide load current range.

Connecting the SYNC pin to the VIN pin forces the converter to operate permanently in the PWM mode even at light or no load currents. The advantage is the converter operates with a fixed switching frequency that allows simple filtering of the switching frequency for noise sensitive applications. In this mode, the efficiency is lower compared to the power save mode during light loads (see).

Device Functional Modes (continued)

It is possible to switch from forced PWM mode to the power save mode during operation.

The flexible configuration of the SYNC pin during operation of the device allows efficient power management by adjusting the operation of the TPS6200x to the specific system requirements.

8.4.3 100% Duty Cycle Operation

As the input voltage approaches the output voltage and the duty cycle exceeds typical 95%, the converter turns the P-channel high side switch continuously on. In this mode, the output voltage is equal to the input voltage minus the voltage drop across the P-channel MOSFET.

8.4.4 No Load Operation

In case the converter operates in the forced PWM mode and there is no load connected to the output, the converter will regulate the output voltage by allowing the inductor current to reverse for a short period of time.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS6200x device family are highly efficient synchronous step down DC/DC converters providing adjustable output voltages from 0.9 V to V_{IN} and fixed output voltages.

9.2 Typical Application

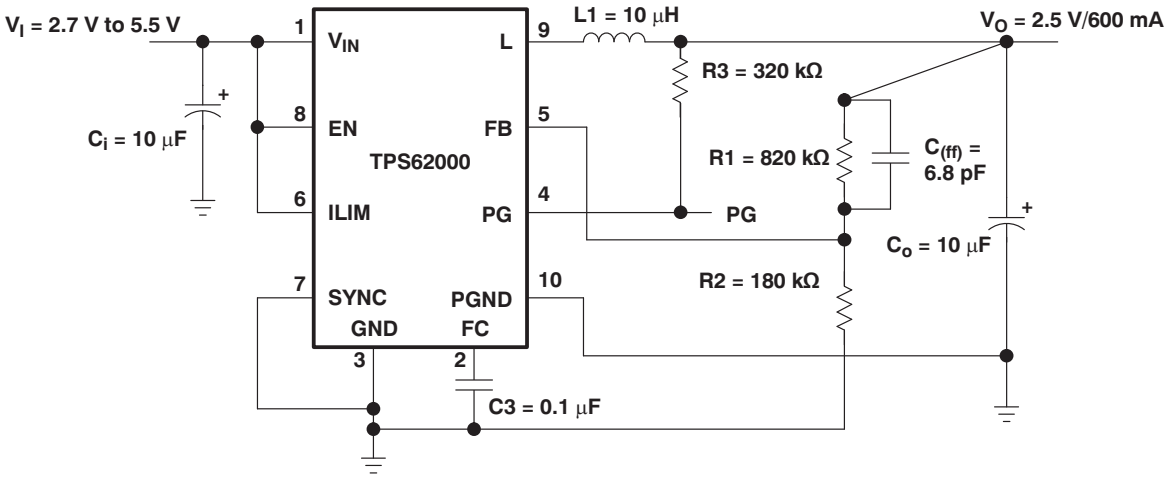


Figure 5. Typical Application Circuit for Adjustable Output Voltage Option

9.2.1 Design Requirements

When the adjustable output voltage version (TPS62000DGS) is used, the output voltage is set by the external resistor divider (see Figure 5).

The output voltage is calculated as:

$$V_O = 0.45\ V \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

with R1 + R2 ≤ 1 MΩ

R1 + R2 should not be greater than 1 MW because of stability reasons.

For stability reasons, a small bypass capacitor ($C_{(ff)}$) is required in parallel to the upper feedback resistor, refer to Figure 5. The bypass capacitor value can be calculated as:

$$C_{(ff)} = \frac{1}{2\pi \times 30000 \times R1} \text{ for } C_o < 47\mu F \quad (2)$$

$$C_{(ff)} = \frac{1}{2\pi \times 5000 \times R1} \text{ for } C_o \geq 47\mu F \quad (3)$$

R1 is the upper resistor of the voltage divider. For $C_{(ff)}$, choose a value which comes closest to the computed result.

Typical Application (continued)

9.2.2 Detailed Design Procedure

9.2.2.1 Inductor Selection

A 10 µH minimum output inductor is used with the TPS6200x. Values larger than 22 µH or smaller than 10 µH may cause stability problems because of the internal compensation of the regulator.

For output voltages greater than 1.8 V, a 22 µH inductance might be used in order to improve the efficiency of the converter.

After choosing the inductor value of typically 10 µH, two additional inductor parameters should be considered: first the current rating of the inductor and second the DC resistance.

The DC resistance of the inductance influences directly the efficiency of the converter. Therefore, an inductor with lowest DC resistance should be selected for highest efficiency.

In order to avoid saturation of the inductor, the inductor should be rated at least for the maximum output current plus the inductor ripple current which is calculated as:

$$\Delta I_L = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \qquad I_{L(max)} = I_{O(max)} + \frac{\Delta I_L}{2} \tag{4}$$

Where:

- f = Switching frequency (750 kHz typical)
- L = Inductor value
- ΔI_L = Peak-to-peak inductor ripple current
- $I_{L(max)}$ = Maximum inductor current

The highest inductor current occurs at maximum V_{IN}.

A more conservative approach is to select the inductor current rating just for the maximum switch current of the TPS6200x which is 1.6 A with ILIM = V_{IN} and 900 mA with ILIM = GND. See Table 1 for recommended inductors.

Table 1. Tested Inductors

OUTPUT CURRENT	INDUCTOR VALUE	COMPONENT SUPPLIER	COMMENTS
0 mA to 600 mA	10 µH	Coilcraft DO3316P-103 Coilcraft DT3316P-103 Sumida CDR63B-100 Sumida CDRH5D28-100	High efficiency
		Coilcraft DO1608C-103 Sumida CDRH4D28-100	Smallest solution
0 mA to 300 mA	10 µH	Coilcraft DO1608C-103	High efficiency
		Murata LQH4C100K04	Smallest solution

9.2.2.2 Output Capacitor Selection

For best performance, a low ESR output capacitor is needed. At output voltages greater than 1.8 V, ceramic output capacitors can be used to show the best performance. Output voltages below 1.8 V require a larger output capacitor and ESR value to improve the performance and stability of the converter.

Table 2. Capacitor Selection

OUTPUT VOLTAGE RANGE	OUTPUT CAPACITOR	OUTPUT CAPACITOR ESR
1.8 V ≤ V_{IN} ≤ 5.5 V	C_o ≥ 10 µF	ESR ≤ 120 mΩ
0.8 V ≤ V_{IN} < 1.8 V	C_o ≥ 47 µF	ESR > 50 mΩ

See Table 3 for recommended capacitors.

If an output capacitor is selected with an ESR value ≤ 120 mΩ, its RMS ripple current rating always meets the application requirements. Just for completeness, the RMS ripple current is calculated as:

$$I_{RMS(C_O)} = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (5)$$

The overall output ripple voltage is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta V_O = V_O \times \frac{1 - \frac{V_O}{V_I}}{L \times f} \times \left(\frac{1}{8 \times C_O \times f} + ESR \right) \quad (6)$$

Where the highest output voltage ripple occurs at the highest input voltage V_I.

Table 3. Tested Capacitors

CAPACITOR VALUE	ESR/mΩ	COMPONENT SUPPLIER	COMMENTS
10 µF	50	Taiyo Yuden JMK316BJ106KL	Ceramic
47 µF	100	Sanyo 6TPA47M	POSCAP
68 µF	100	Spraque 594D686X0010C2T	Tantalum

9.2.2.3 Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes.

The input capacitor should have a minimum value of 10 µF and can be increased without any limit for better input voltage filtering.

The input capacitor should be rated for the maximum input ripple current calculated as:

$$I_{RMS} = I_{O(max)} \times \sqrt{\frac{V_O}{V_I} \times \left(1 - \frac{V_O}{V_I}\right)} \quad (7)$$

The worst case RMS ripple current occurs at D = 0.5 and is calculated as: $I_{RMS} = \frac{I_O}{2}$

Ceramic capacitor show a good performance because of their low ESR value, and they are less sensitive against voltage transients compared to tantalum capacitors.

Place the input capacitor as close as possible to the input pin of the IC for best performance.

9.2.3 Application Curves

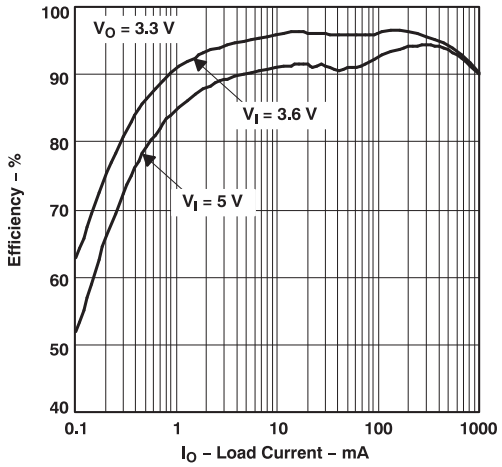


Figure 6. Efficiency vs Load Current

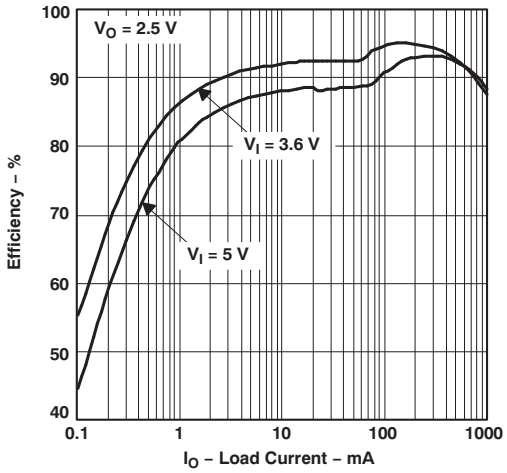


Figure 7. Efficiency vs Load Current

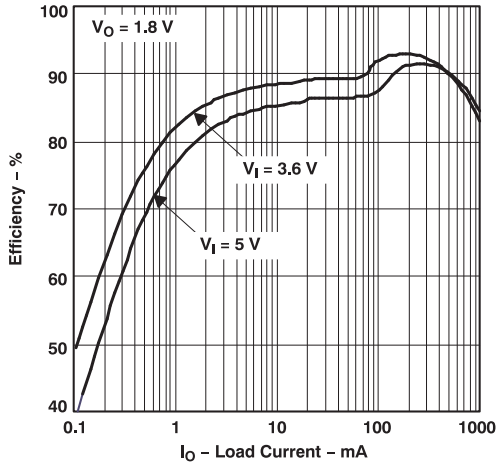


Figure 8. Efficiency vs Load Current

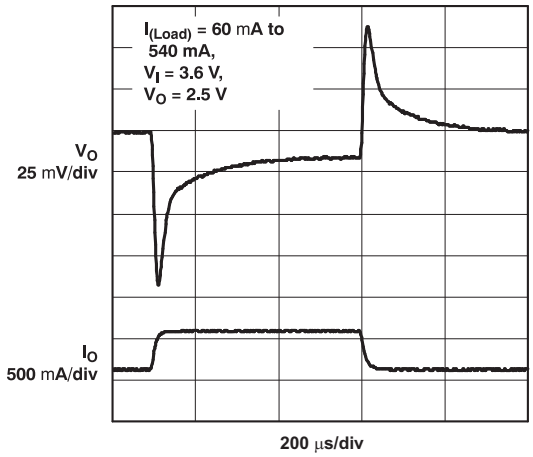


Figure 9. Load Transient Response

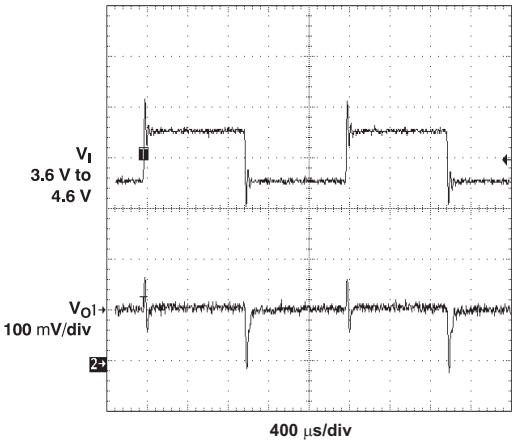


Figure 10. Line Transient Response

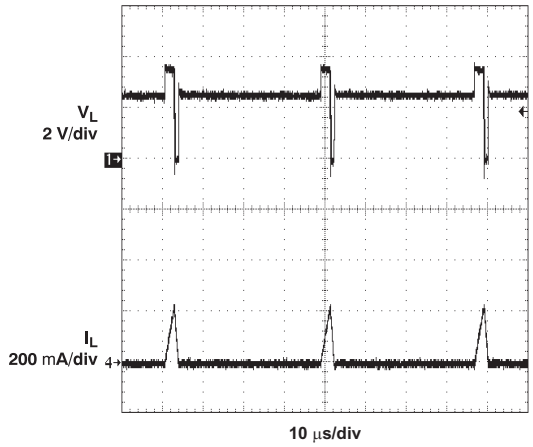


Figure 11. Power Save Mode Operation

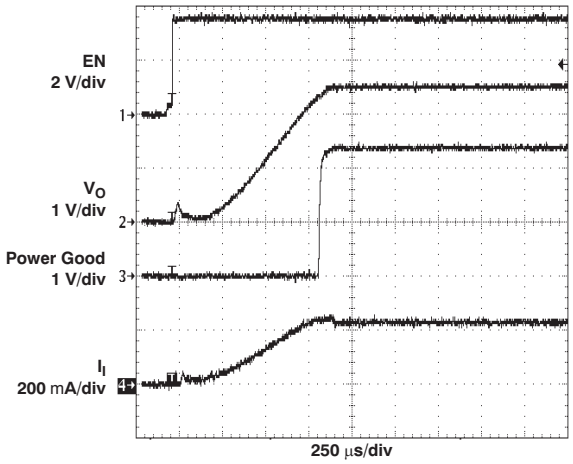


Figure 12. Start-Up vs Time

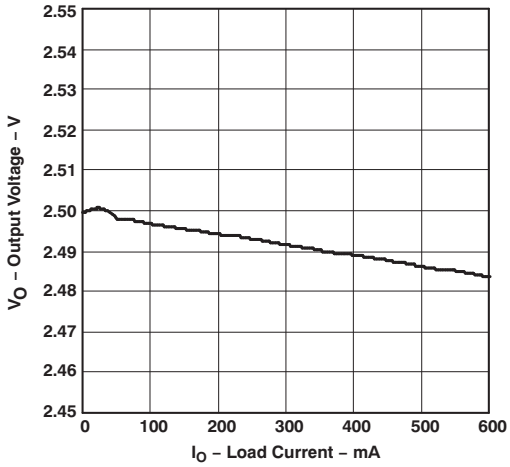


Figure 13. Output Voltage vs Load Current

9.3 System Examples

9.3.1 Standard 5-V to 3.3-V/600-mA Conversion; High Efficiency

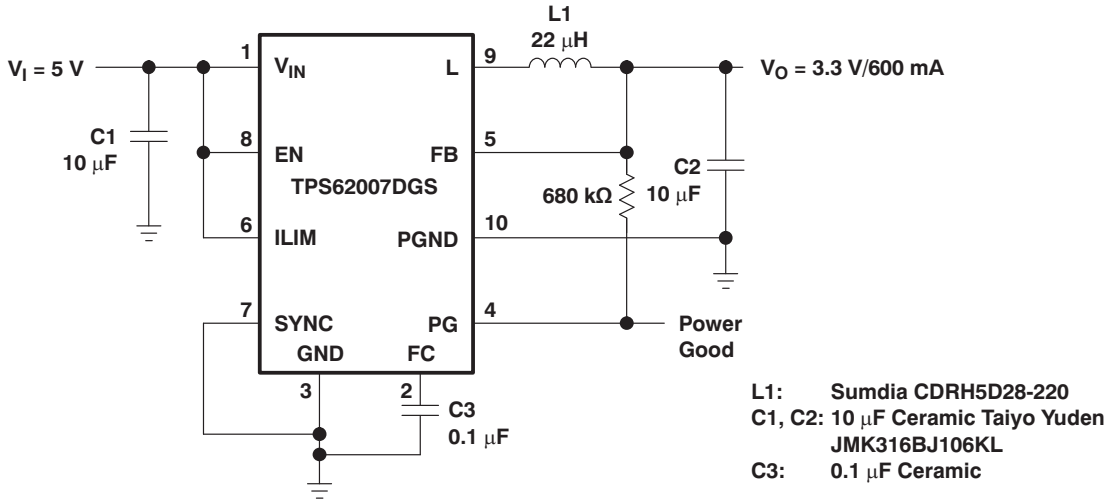


Figure 14. Standard 5-V to 3.3-V/600-mA Conversion; High Efficiency

9.3.2 Single Li-ion to 2.5-V/600-mA Using Ceramic Capacitors Only

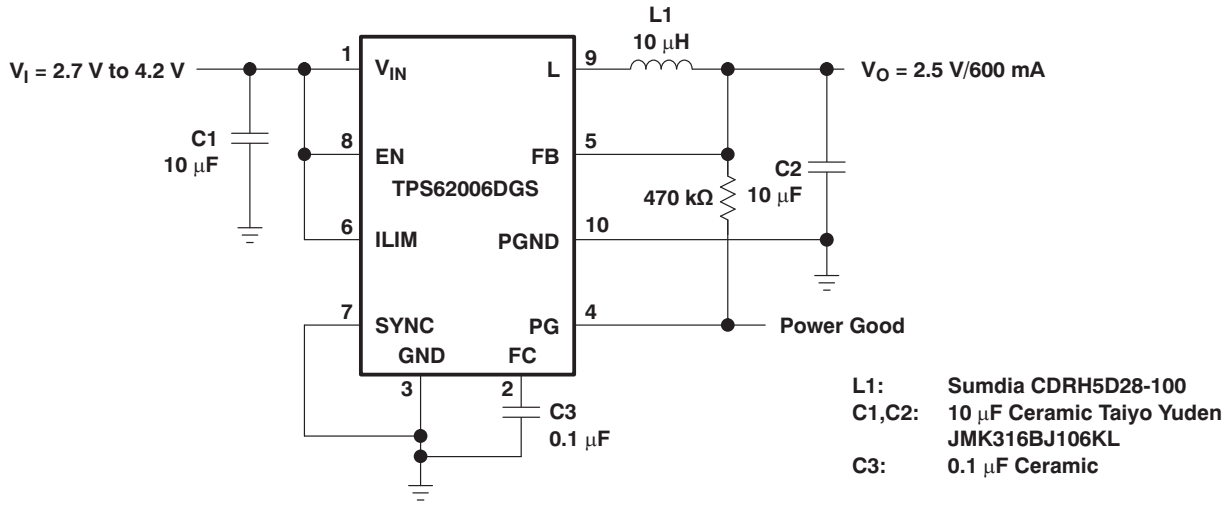
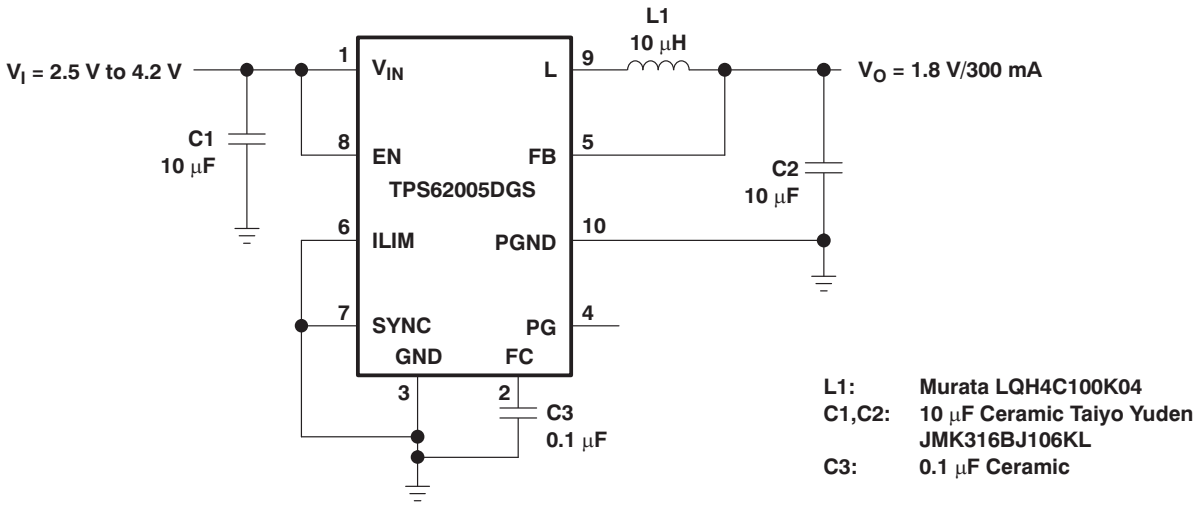


Figure 15. Single Li-ion to 2.5-V/600-mA Using Ceramic Capacitors Only

System Examples (continued)

9.3.3 Single Li-ion to 1.8 V/300 mA; Smallest Solution Size



NOTE: For low noise operation connect SYNC to V_{IN}

Figure 16. Single Li-ion to 1.8 V/300 mA; Smallest Solution Size

9.3.4 Dual Cell NiMH or NiCd to 1.2 V/200 mA; Smallest Solution Size

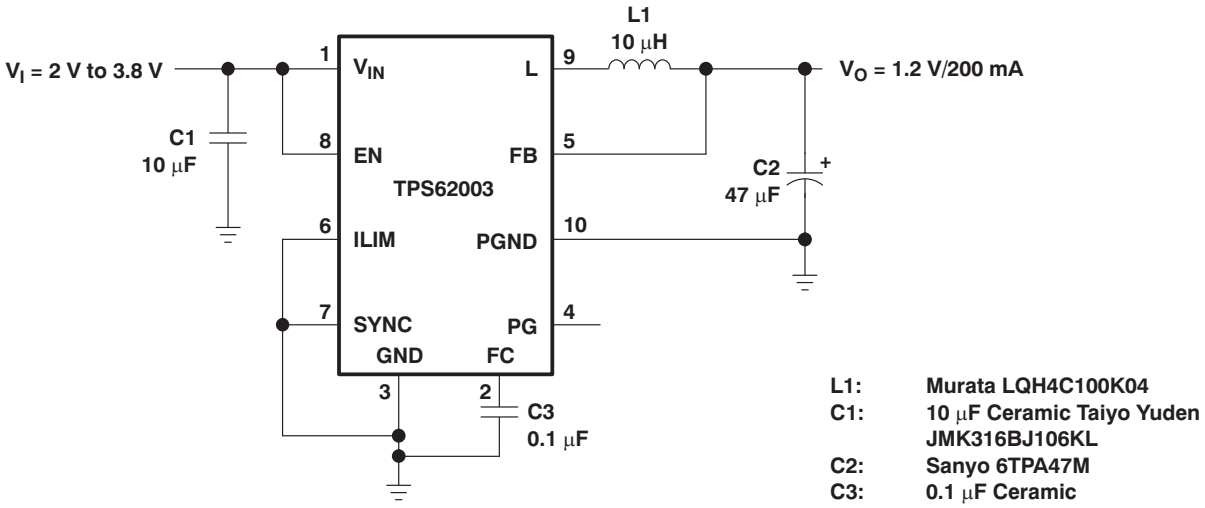
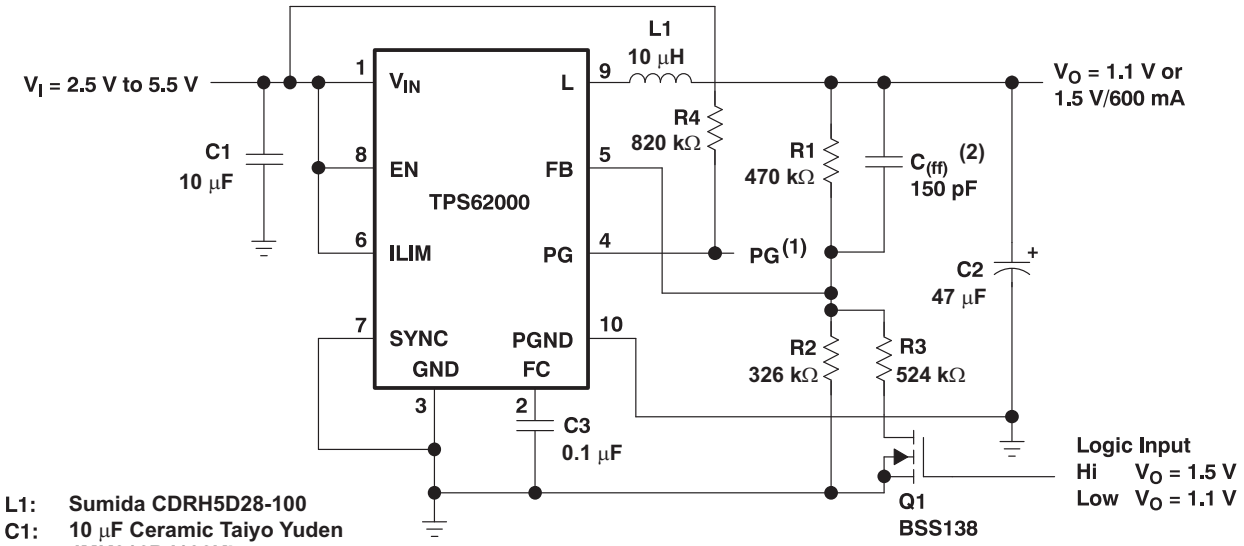


Figure 17. Dual Cell NiMH or NiCd to 1.2 V/200 mA; Smallest Solution Size

System Examples (continued)

9.3.5 Dynamic Output Voltage Programming As Used in Low Power DSP Applications



(1) Use a small R-C filter to filter wrong reset signals during output voltage transitions.

(2) A large value is used for C(ff) to compensate for the parasitic capacitance introduced into the regulation loop by Q1.

Figure 18. Dynamic Output Voltage Programming As Used in Low Power DSP Applications

10 Power Supply Recommendations

The TPS6200x device family has no special requirements for its input power supply. The input power supply's output current needs to be rated according to the supply voltage, output voltage and output current of the TPS6200x.

11 Layout

11.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design especially at high peak currents and switching frequencies. If the layout is not carefully done, the regulator might show stability problems as well as EMI problems.

Therefore, use wide and short traces for the main current paths as indicted in bold in Figure 19. The input capacitor should be placed as close as possible to the IC pins as well as the inductor and output capacitor. Place the bypass capacitor, C3, as close as possible to the FC pin. The analog ground, GND, and the power ground, PGND, need to be separated. Use a common ground node as shown in Figure 19 to minimize the effects of ground noise.

11.2 Layout Example

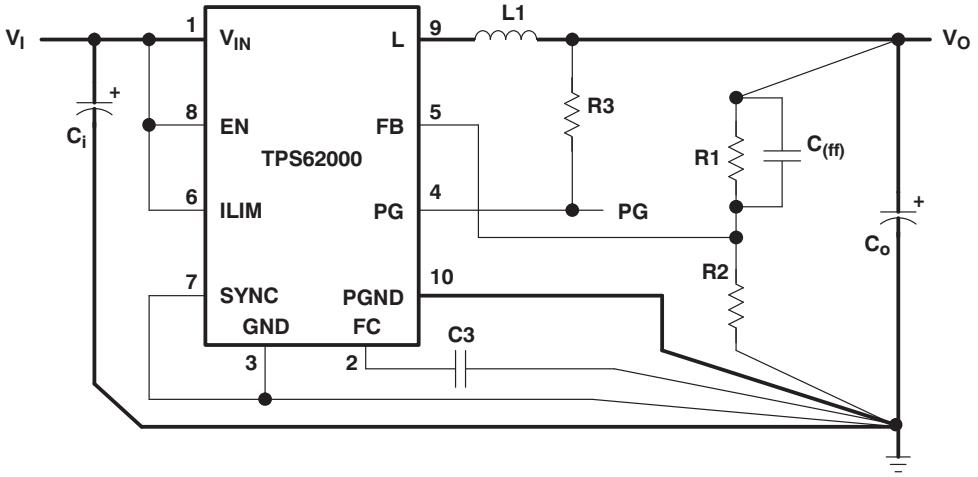


Figure 19. Layout Diagram

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS62000	Click here	Click here	Click here	Click here	Click here
TPS62001	Click here	Click here	Click here	Click here	Click here
TPS62002	Click here	Click here	Click here	Click here	Click here
TPS62003	Click here	Click here	Click here	Click here	Click here
TPS62004	Click here	Click here	Click here	Click here	Click here
TPS62005	Click here	Click here	Click here	Click here	Click here
TPS62006	Click here	Click here	Click here	Click here	Click here
TPS62007	Click here	Click here	Click here	Click here	Click here
TPS62008	Click here	Click here	Click here	Click here	Click here

12.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS62000DGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AIH	Samples
TPS62000DGSG4	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AIH	Samples
TPS62000DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AIH	Samples
TPS62000DGSRG4	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AIH	Samples
TPS62002DGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AIJ	Samples
TPS62002DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AIJ	Samples
TPS62003DGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AIK	Samples
TPS62003DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AIK	Samples
TPS62003DGSRG4	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AIK	Samples
TPS62004DGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AIL	Samples
TPS62004DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AIL	Samples
TPS62005DGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AIM	Samples
TPS62005DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AIM	Samples
TPS62006DGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AIN	Samples
TPS62006DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AIN	Samples
TPS62007DGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AIO	Samples
TPS62007DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU | NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AIO	Samples
TPS62007DGSRG4	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AIO	Samples
TPS62008DGS	ACTIVE	VSSOP	DGS	10	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AJI	Samples
TPS62008DGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	AJI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

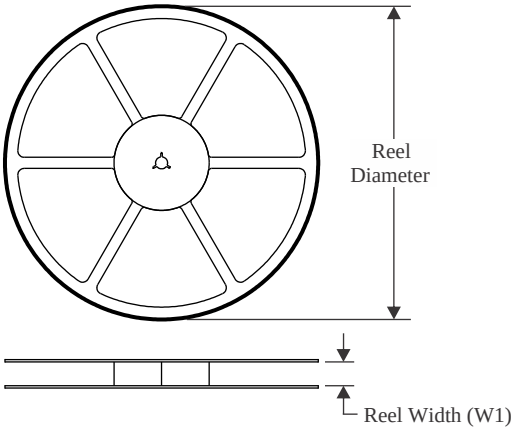
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPS62000 :

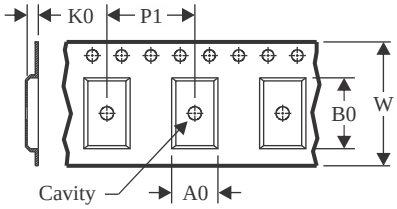
NOTE: Qualified Version Definitions:

TAPE AND REEL INFORMATION

REEL DIMENSIONS

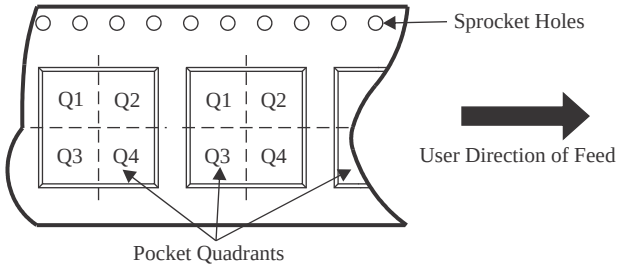


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

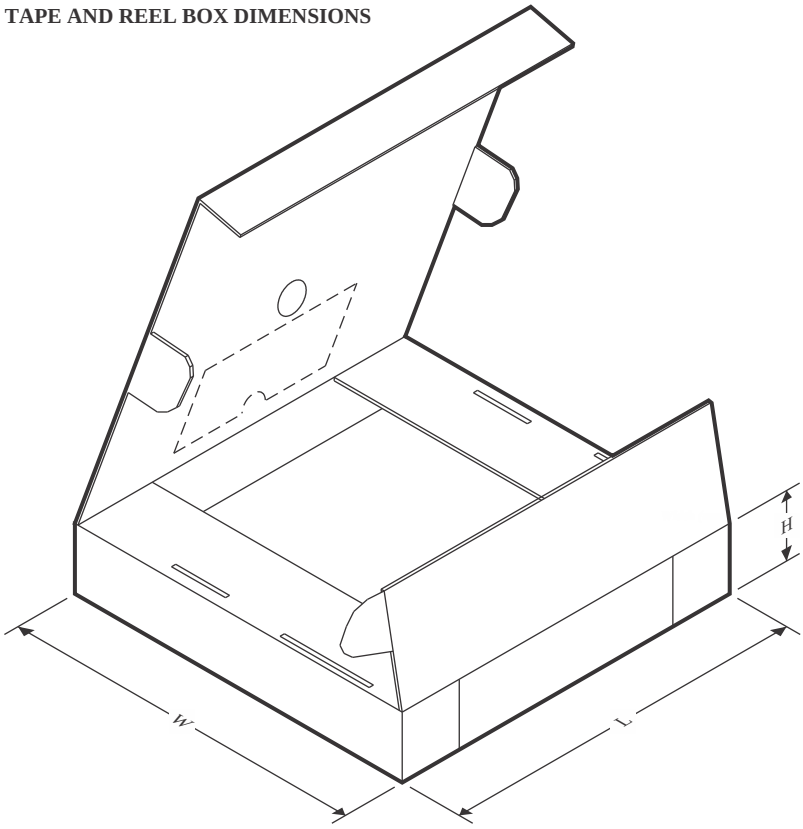
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS62000DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS62002DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS62003DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS62004DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS62005DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS62006DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS62007DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS62008DGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

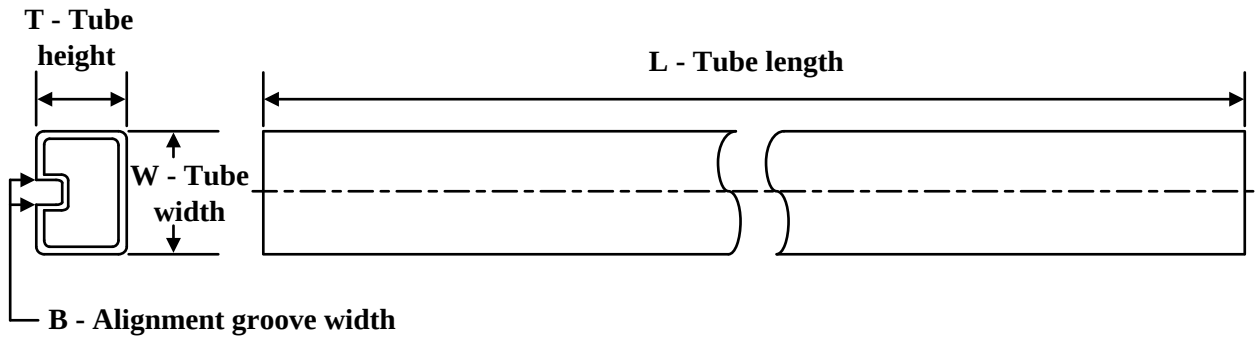
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS62000DGSR	VSSOP	DGS	10	2500	350.0	350.0	43.0
TPS62002DGSR	VSSOP	DGS	10	2500	350.0	350.0	43.0
TPS62003DGSR	VSSOP	DGS	10	2500	350.0	350.0	43.0
TPS62004DGSR	VSSOP	DGS	10	2500	350.0	350.0	43.0
TPS62005DGSR	VSSOP	DGS	10	2500	350.0	350.0	43.0
TPS62006DGSR	VSSOP	DGS	10	2500	350.0	350.0	43.0
TPS62007DGSR	VSSOP	DGS	10	2500	350.0	350.0	43.0
TPS62008DGSR	VSSOP	DGS	10	2500	350.0	350.0	43.0

TUBE



*All dimensions are nominal

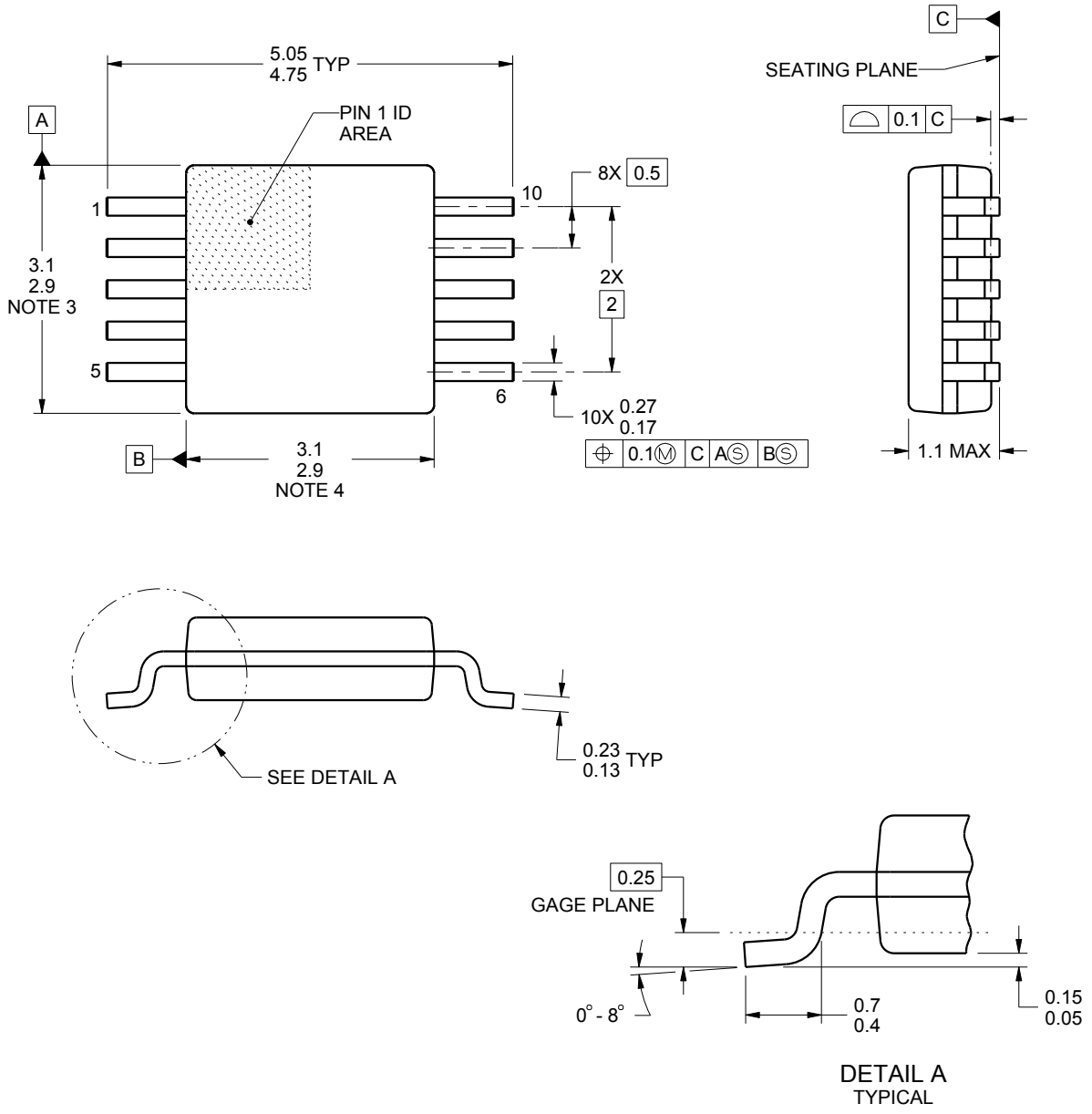
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS62000DGS	DGS	VSSOP	10	80	331.47	6.55	3000	2.88
TPS62000DGSG4	DGS	VSSOP	10	80	331.47	6.55	3000	2.88
TPS62002DGS	DGS	VSSOP	10	80	331.47	6.55	3000	2.88
TPS62003DGS	DGS	VSSOP	10	80	331.47	6.55	3000	2.88
TPS62004DGS	DGS	VSSOP	10	80	331.47	6.55	3000	2.88
TPS62005DGS	DGS	VSSOP	10	80	331.47	6.55	3000	2.88
TPS62006DGS	DGS	VSSOP	10	80	331.47	6.55	3000	2.88
TPS62007DGS	DGS	VSSOP	10	80	331.47	6.55	3000	2.88
TPS62008DGS	DGS	VSSOP	10	80	331.47	6.55	3000	2.88

PACKAGE OUTLINE

DGS0010A

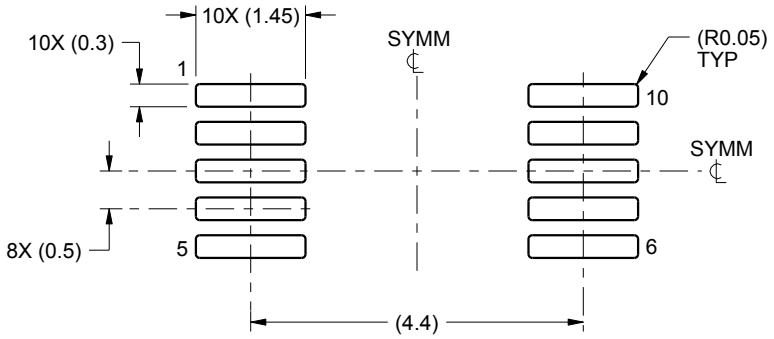
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

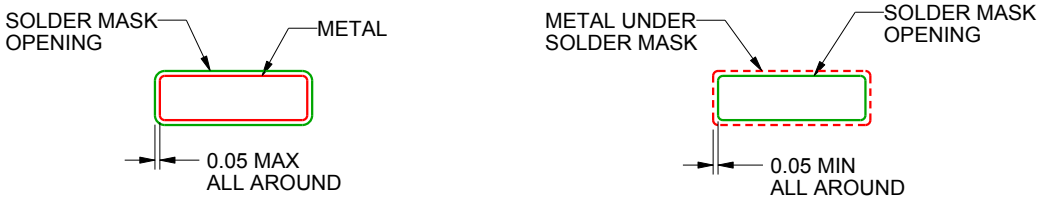


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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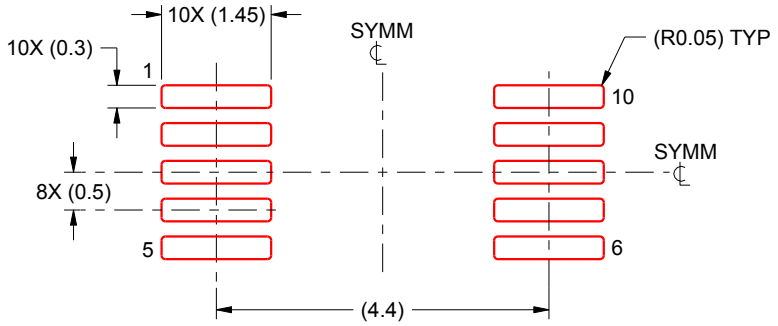
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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