TPS65142 集成 WLED 背光驱动器的 LCD 偏置电源

1 特性

- 集成偏置和背光电源
- 输入偏置电压范围：2.3V 至 6V
  - 高达 16.5V 的升压转换器，开关电流为 1.8A
  - 1.2MHz/650kHz 可选开关频率
  - 内部补偿
  - 上电时内部软启动
  - 复位功能（$\overline{XAO}$ 信号）
  - 经过稳压的 VGH
  - 经过稳压的 VGL
  - 栅极电压整形
  - LCD 放电功能
- 150mA 单位增益 VCOM 缓冲器
- 4.5V 至 24V 白色发光二极管 (WLED) 背光输入范围
  - 集成 1.5A/40V 金属氧化物半导体场效应晶体管 (MOSFET)
  - 升压输出跟踪 WLED 电压
  - 内部补偿
  - 外部电流设置输入
  - 6 条 25mA 灌电流通道
  - 优于 3% 的电流匹配度
  - 高达 1000:1 的脉宽调制 (PWM) 调光范围
- 过压保护
- 热关断
- 欠压锁定
- 32 引脚 6mm x 3mm 四方扁平无引线 (QFN) 封装

2 应用

- 笔记本电脑 TFT-LCD 显示器
- 平板电脑 TFT-LCD 显示器

3 说明

TPS65142 提供了一套针对笔记本电脑 TFT-LCD 显示器内的偏置电源和 WLED 背光的紧凑型解决方案。该器件 配有 升压转换器、正电荷泵稳压器和负电荷泵稳压器，用于为源级驱动器和栅极驱动器供电。150mA 单位增益高速缓冲器用于驱动 VCOM 电源层。栅极电压整形和 LCD 放电功能用于改善图像质量。复位功能可在上电时对 TCON 进行正确复位。TPS65142 还提供了一套完整的解决方案来驱动多达 6 个 PWM 调光比率为 1000:1 的 WLED 链。

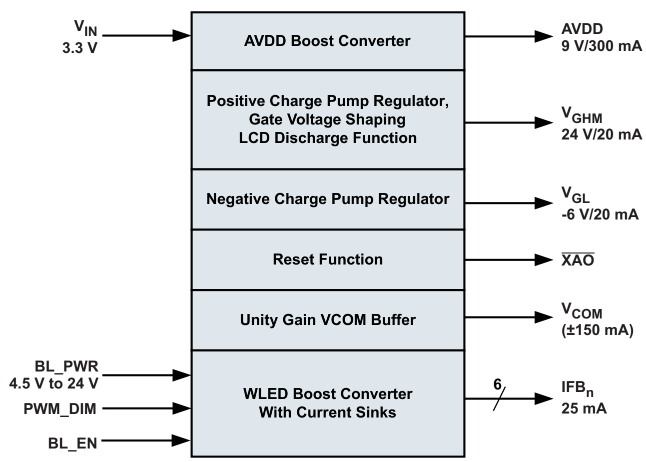
全部 功能 均集成在紧凑型 6 x 3mm^2 薄型 QFN 封装内。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS65142	WQFN (32)	6.00mm x 3.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

简化框图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (November 2012) to Revision B — **Page**

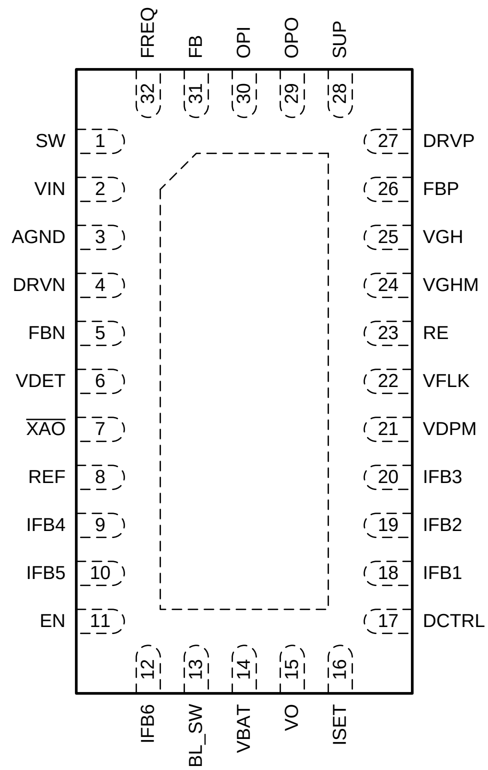
- 已添加 *ESD 额定值表，特性 描述，应用和实施，电源相关建议，器件和文档支持以及机械、封装和可订购信息* 1
- Deleted the *Ordering Information* table 4
- 已添加 *Timing Requirements* table. 8
- 已添加 sentence to the *Power Up Sequence* section: "To ensure proper start-up..." 21
- 已更改 图 32 21

Changes from Original (July 2011) to Revision A — **Page**

- Deleted COMP pin from ABSOLUTE MAXIMUM RATINGS 4
- 已更改 $I_{(IFB\_MAX)}$ TEST CONDITION IFB from 450 mV to 500 mV 8
- 已更改 $I_{(IFB\_MAX)}$ min from 25 mA to 28 mA 8
- 已更改 D_{max} min from 85% to 89% 8
- 已更改 V_{REF} from 3.15 V to 3.12 V in Negative Charge Pump section 16
- 已更改 BL_PWR from 4.5V to 25V to 4.5V to 24V in 图 33 22

5 Pin Configuration and Functions

**WQFN Package
32-Pin (RTG)
Top View**



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	3		Analog ground
BL_SW	13		The backlight boost converter switching node
DCTRL	17	I	Backlight PWM dimming control input
DRVN	4	O	Voltage driver of the negative charge pump
DRVP	27		Voltage driver of positive charge pump
EN	11	I	Backlight enable input
FB	31	I	AVDD Boost converter feedback pin
FBN	5	I	Negative charge pump feedback pin
FBP	26	I	Positive charge pump feedback pin
FREQ	32	I	AVDD boost converter switching frequency selection: 1.2MHz when $V_{(FREQ)} = V_{IN}$ and 650 kHz when $V_{(FREQ)}$ = ground
IFB1	18	I	Channel 1 of the WLED backlight current sink
IFB2	19	I	Channel 2 of the WLED backlight current sink
IFB3	20	I	Channel 3 of the WLED backlight current sink
IFB4	9	I	Channel 4 of the WLED backlight current sink
IFB5	10	I	Channel 5 of the WLED backlight current sink
IFB6	12	I	Channel 6 of the WLED backlight current sink
ISET	16	I	WLED current sink level programming input
OPI	30	I	Input voltage of VCOM Buffer

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
OPO	29	O	Output voltage of VCOM Buffer
PGND	ePAD		Exposed pad that serves as the power ground for both boost converters
RE	23		Sets the slope for the gate shaping function. Pin for external Resistor
REF	8	O	Reference voltage for the negative charge pump
SUP	28	I	Supply pin of the gate shaping and operational amplifier blocks. Connected as well to the overvoltage protection comparator. This pin needs to be connected to the output of the AVDD boost converter.
SW	1		Switch pin of the AVDD boost converter
VBAT	14	I	Input of the backlight boost converter
VDET	6	I	Reset IC threshold pin (Voltage divider)
VDPM	21	O	Sets the delay to enable VGHM Output. Pin for external capacitor. Floating if no delay needed
VFLK	22	I	Charge/discharge signal for VGHM
VGH	25	I	Input for positive Charge Pump
VGHM	24	O	Output for gate-high modulation
VIN	2	I	Input supply pin
VO	15	O	The output of the backlight boost converter
$\overline{XAO}$	7	O	Reset IC output pulling down $\overline{XAO}$ pin when active.

6 Specifications

6.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Voltage	Input voltage range	–0.3	6.5	V
	FB, FREQ, VDPM, VFLK, VDET, FBN, $\overline{XAO}$	–0.3	6.5	V
	SW, OPI, OPO, SUP, DRVP, DRVN, EN, DCTRL, IFB1 to IFB6	–0.3	20	V
	REF, FBP and ISET	–0.3	3.6	V
	VGH, VGHM, RE	–0.3	35	V
	VBAT	–0.3	24	V
	BL_SW and VO	–0.3	40	V
Continuous power dissipation		See the Thermal Information Table		
Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process..

6.3 Recommended Operating Conditions

		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range	2.3		6	V
V_S	AVDD Boost output voltage range(1)			16.5	V
V_{GH}	Positive charge pump output voltage range			32	V
V_{BAT}	Battery voltage range	4.5		24	V
V_O	WLED boost converter output voltage			38	V
V_{GL}	Negative charge pump output voltage range	–14			V
L_1	Inductor for the AVDD boost converter(2)	4.7		10	µH
L_2	Inductor for the WLED boost converter	4.7		10	µH
C_{IN}	Input decoupling capacitor	1			µF
C_{O1}	Output decoupling capacitor of the AVDD boost converter		20		µF
C_{O2}	Output decoupling capacitor of the WLED boost converter	2.2		10	µF
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

(1) Maximum output voltage is limited by the overvoltage protection and not the maximum power switch rating
(2) Refer to application section for further information.

6.4 Thermal Information

THERMAL METRIC(1)		WQFN	UNITS
		RTG (32 PINS)	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	35.4	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	19.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	5.6	
ψ_{JT}	Junction-to-top characterization parameter	0.2	
ψ_{JB}	Junction-to-board characterization parameter	5.4	
$R_{\theta JCbot}$	Junction-to-case (bottom) thermal resistance	1.7	

(1) 有关传统和新热指标的更多信息，请参见《半导体和 IC 封装热指标》应用报告，SPRA953。

6.5 Electrical Characteristics

V_{IN} = 3.3 V, V_S = 9V, V_{GH} = 20 V, V_{BAT} = 10.8V, I_{ISET} = 15µA, V_{IFBx} = 0.5V, EN = V_{IN}, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
$I_{Q(IN)}$	Operating quiescent current into VIN	Device not switching		0.17	0.5	mA
$I_{Q(VGH)}$	Operating quiescent current into VGH	V_{GH} = 20 V, VFLK not oscillating		22	40	µA
$I_{Q(SUP)}$	Operating quiescent current into SUP	Device not switching. V_S = 9 V, EN = high		2.8		mA
		Device not switching. V_S = 9 V, EN = GND		2.5		
$I_{SD(VIN)}$	Shutdown current into VIN	V_{IN} = 1.8 V, V_S = GND		20	33	µA
$I_{SD(VGH)}$	Shutdown current into VGH	V_{IN} = 1.8 V, V_{GH} = 32 V		30	50	µA
$I_{SD(SUP)}$	Shutdown current into SUP	V_{IN} = 1.8 V, V_S = 16.5 V		3	5	µA
$I_{Q(BAT)}$	VBAT pin quiescent current	WLED boost regulator switching, no load			0.2	mA
$I_{SD(BAT)}$	VBAT pin shutdown current	EN = GND			18	µA
$I_{Q(VO)}$	VO pin quiescent current	V_O = 35 V			75	µA
UVLO	VIN under voltage lockout threshold	V_{IN} falling	1.9		2.1	V
		V_{IN} rising			2.2	
	VBAT under voltage lockout threshold	V_{BAT} rising			4.45	V
		V_{BAT} falling	3.9			
	UVLO voltage of WLED control circuit			2.2	2.5	V

Electrical Characteristics (接下页)

V_{IN} = 3.3 V, V_S = 9V, V_{GH} = 20 V, V_{BAT} = 10.8V, I_{ISET} = 15µA, V_{IFBx} = 0.5V, EN = V_{IN}, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LOGIC SIGNALS FREQ, VFLK, EN, DCTRL						
V_{IH}	Logic high input voltage	V_{IN} = 2.5 V to 6 V	2			V
V_{IL}	Logic low input voltage	V_{IN} = 2.5 V to 6 V			0.5	V
I_{LKG}	Input leakage current of VFLK pin	VFLK = 6 V, FREQ = GND			0.1	µA
R_{PD}	Pull-down resistance for EN and DCTRL pins	EN = DCTRL = 3.3 V	400	800	1600	kΩ
AVDD BOOST CONVERTER						
V_S	Output voltage boost(1)		7		16.5	V
V_{OVP}	Overvoltage protection	VS rising	16.9	18	19	V
V_{FB}	Feedback regulation voltage	T_A = –40°C to 85°C	1.226	1.24	1.254	V
		T_A = 25°C	1.23	1.24	1.25	
I_{FB}	Feedback input bias current	V_{FB} = 1.240 V			0.1	µA
$r_{DS(ON)}$	N-channel MOSFET on-resistance	V_{IN} = V_{GS} = 5 V, I_{SW} = current limit		0.13	0.38	Ω
		V_{IN} = V_{GS} = 3.3 V, I_{SW} = current limit		0.15	0.44	
$I_{Lkg(SW)}$	AVDD Boost converter SW leakage current	V_{IN} = 1.8 V, V_{SW} = 17 V, Device not switching			30	µA
I_{LIM}	N-Channel MOSFET current limit	VIN = 2.5 V to 6 V	1.8	2.5	3.2	A
		VIN = 2.3 V to 2.5 V	1.5			A
f_{BOOST}	Switching frequency	FREQ = high	0.9	1.2	1.5	MHz
		FREQ = low	470	625	780	kHz
T_{SS}	Softstart time	FREQ = high, L_1 = 6.8 µH, C_{O1} = 2 0µF and 10 mA load current		2		ms
	Line regulation	V_{IN} = 2.5 V … 6 V, I_{OUT} = 10 mA		0.008		%/V
	Load regulation	I_{OUT} = 0 mA …500 mA		0.15		%/A
VGH REGULATOR						
f_{SWP}	Switching frequency			0.5 x f_{BOOST}		MHz
V_{FBP}	Reference voltage of feedback	T_A = –40°C to 85°C	1.210	1.240	1.270	V
		T_A = 25°C	1.221	1.240	1.259	
I_{FBP}	Feedback input bias current	V_{FBP} = 1.240 V			0.1	µA
$r_{DS(ON)P1}$	DRVP $R_{DS(ON)}$ (PMOS)	V_S = 9 V, $I_{(DRVP)}$ = 40 mA		8	20	Ω
$r_{DS(ON)N1}$	DRVP $R_{DS(ON)}$ (NMOS)	V_S = 9 V, $I_{(DRVP)}$ = –40 mA		3	10	Ω
VGL REGULATOR						
f_{SWN}	Switching frequency			0.5 x f_{BOOST}		MHz
V_{REF}	Reference voltage		3.05	3.12	3.18	V
V_{FBN}	Reference voltage of feedback		–48	0	48	mV
I_{FBN}	Feedback input bias current	V_{FBN} = 0 V			0.1	µA
$r_{DS(ON)P2}$	DRVN $R_{DS(ON)}$ (PMOS)	V_S = 9 V, $I_{(DRVN)}$ = 40 mA		8	20	Ω
$r_{DS(ON)N2}$	DRVN $R_{DS(ON)}$ (NMOS)	V_S = 9 V, $I_{(DRVN)}$ = –40 mA		3	10	Ω
GATE VOLTAGE SHAPING VGHM						
$I_{(DPM)}$	Capacitor charge current VDPM pin		17	20	23	µA
$r_{DS(ON)M1}$	VGH to VGHM $r_{DS(ON)}$ (M1 PMOS)	VFLK = low, $I_{(VGHM)}$ = 20 mA		13	25	Ω
$r_{DS(ON)M2}$	VGHM to RE $r_{DS(ON)}$ (M2 PMOS)	VFLK = high, $I_{(VGHM)}$ = 20 mA, VGHM = 7.5 V		13	25	Ω

(1) Maximum output voltage limited by the overvoltage protection and not the maximum power switch rating

Electrical Characteristics (接下页)

V_{IN} = 3.3 V, V_S = 9V, V_{GH} = 20 V, V_{BAT} = 10.8V, I_{ISET} = 15µA, V_{IFBx} = 0.5V, EN = V_{IN}, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESET						
$V_{IN(DET)}$	VIN voltage range for reset detection		1.6		6	V
$V_{(DET)}$	Reset IC threshold	Falling	1.074	1.1	1.126	V
$V_{(DET\_HYS)}$	Reset IC threshold hysteresis			65		mV
$I_{(DET\_B)}$	Reset IC input bias current	$V_{(DET)}$ = 1.1 V			0.1	µA
I_{XAO}	Reset sink current capability(2)	$V_{(XAO\_ON)}$ = 0.5 V	1			mA
$I_{LKG(XAO)}$	Reset leakage current	$V_{(XAO)}$ = V_{IN} = 3.3 V			2	µA
VCOM BUFFER						
V_{SUP}	SUP input supply range(3)		7		16.5	V
I_B	Input bias current	V_{CM} = $V_{(OPI)}$ = V_{SUP}/2 = 4.5 V	–1		1	µA
V_{CM}	Common Mode Input Voltage Range	V_{OFFSET} = 10 mV, $I_{(OPO)}$ = 10 mA	2		V_S – 2	V
CMRR	Common Mode Rejection Ratio(4)	V_{CM} = $V_{(OPI)}$ = $V_{(SUP)}$/2 = 4.5 V, 1 MHz		66		dB
A_{VOL}	Open Loop Gain(4)	V_{CM} = $V_{(OPI)}$ = $V_{(SUP)}$/2 = 4.5 V, no load		90		dB
V_{OL}	Output Voltage Swing Low	$I_{(OPO)}$ = 10 mA		0.10	0.25	V
V_{OH}	Output Voltage Swing High	$I_{(OPO)}$ = 10 mA	V_S – 0.8	V_S – 0.65		V
I_{SC}	Short Circuit Current	Source ($V_{(OPI)}$ = 4.5V, $V_{(OPO)}$ = GND)	150			mA
		Sink ($V_{(OPI)}$ = 4.5 V, $V_{(OPO)}$ = 9 V)	150			
I_O	Output Current	Source ($V_{(OPI)}$ = 4.5 V, $V_{(OFFSET)}$ = 15 mV)		150		mA
		Sink ($V_{(OPI)}$ = 4.5 V, $V_{(OFFSET)}$ = 15 mV)		140		
PSRR	Power Supply Rejection Ratio(4)			40		dB
SR	Slew Rate(4)	A_V = 1, $V_{(OPI)}$ = 2 V_{PP}		40		V/µs
BW	–3 dB Bandwidth(4)	A_V = 1, $V_{(OPI)}$ = 60 mV_{PP}		50		MHz

(2) External pull-up resistor to be chosen so that the current flowing into $\overline{XAO}$ Pin (/XAO = 0 V) when active is below $I_{(XAO)\ MIN}$ = 1 mA.
(3) Maximum output voltage limited by the Overvoltage Protection and not the maximum Power Switch rating.
(4) Typical values are for reference only

Electrical Characteristics (接下页)

V_{IN} = 3.3 V, V_S = 9V, V_{GH} = 20 V, V_{BAT} = 10.8V, I_{ISET} = 15µA, V_{IFBx} = 0.5V, EN = V_{IN}, T_A = –40°C to 85°C, typical values are at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
WLED CURRENT REGULATION						
$V_{(ISET)}$	ISET pin voltage		1.204	1.229	1.253	V
$K_{(ISET)}$	Current multiple I_{OUT}/ISET (5)	ISET current = 20 µA		1000		
I_{FB}	Current accuracy (5)	ISET current = 20 µA	19.4	20	20.6	mA
K_m	$(I_{max}–I_{min})/I_{AVG}$	ISET current = 20 µA		1%	2.5%	
I_{LKG}	IFB pin leakage current	IFB voltage = 20 V on all pins			3	µA
$I_{(IFB\_MAX)}$	Current sink max output current	IFB = 500 mV	28			mA
WLED BOOST OUTPUT REGULATION						
$V_{(IFB\_L)}$	V_O dial up threshold	Measured on $V_{(IFB)\ min}$		400		mV
$V_{(IFB\_H)}$	V_O dial down threshold	Measured on $V_{(IFB)\ min}$		700		mV
$V_{(reg\_L)}$	Minimum V_O regulation voltage				16	V
$V_{O(step)}$	V_O stepping voltage			100	150	mV
WLED BOOST REGULATOR POWER SWITCH						
$R_{(PWM\_SW)}$	PWM FET on-resistance			0.2	0.45	Ω
$I_{(LN\_NFET)}$	PWM FET leakage current	$V_{(BL\_SW)}$ = 35 V, T_A = 25°C			1	µA
WLED OSCILLATOR						
f_S	Oscillator frequency		0.9	1.0	1.2	MHz
D_{max}	Maximum duty cycle of WLED Boost	IFB = 0 V	89%	94%		
D_{min}	Minimum duty cycle of WLED Boost				7%	
CURRENT LIMIT, OVER VOLTAGE AND SHORT CIRCUIT PROTECTIONS						
I_{LIM}	N-Channel MOSFET current limit	D = D_{MAX}	1.5		3	A
V_{OVP}	VO overvoltage threshold	Measured on the VO pin	38	39	40	V
$V_{OVP(IFB)}$	IFB overvoltage threshold	Measured on the IFBx pin	15	17	20	V
V_{SC}	Short circuit detection threshold	V_{BAT} –V_O, V_O ramp down		1.7	2.5	V
$V_{SC(dly)}$	Short circuit detection delay during start up			32		ms
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown	Temperature rising		150		°C
T_{SDHYS}	Thermal shutdown hysteresis			14		°C

(5) Tested at T_A = 25°C to 85°.

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
t_d	Rising edge delay between V_{BAT} and V_{IN}, measured at their respective rising edge UVLO threshold voltages (see 图 32). (1)	0			s

(1) This means that the voltage on the VBAT pin must exceed its UVLO threshold before the voltage on the VIN pin rises above its UVLO threshold.

6.7 Typical Characteristics

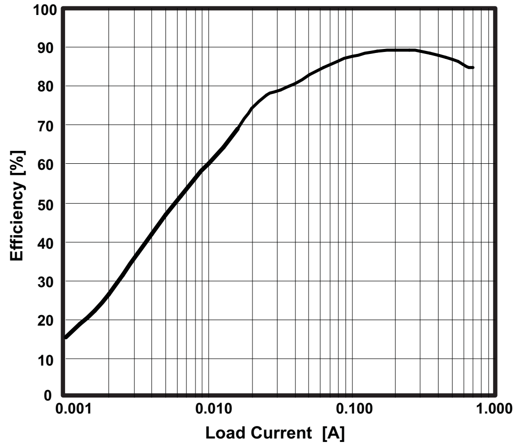


图 1. Boost Converter Efficiency vs Output Current

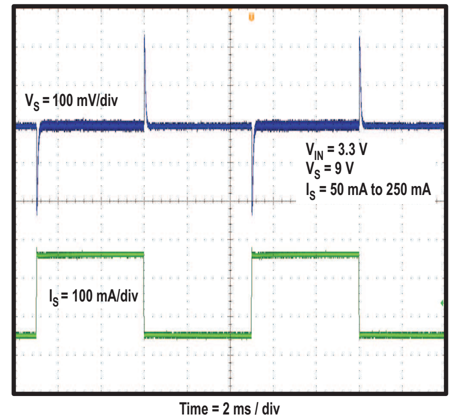


图 2. Boost Converter Load Transient Response

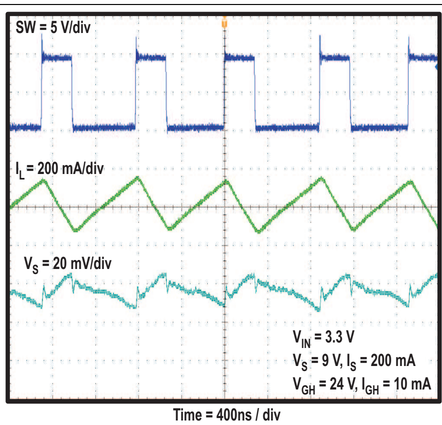


图 3. Boost Converter Continuous Conduction Mode

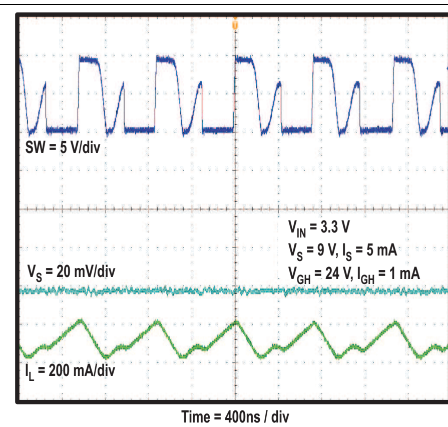


图 4. Boost Converter Discontinuous Conduction Mode

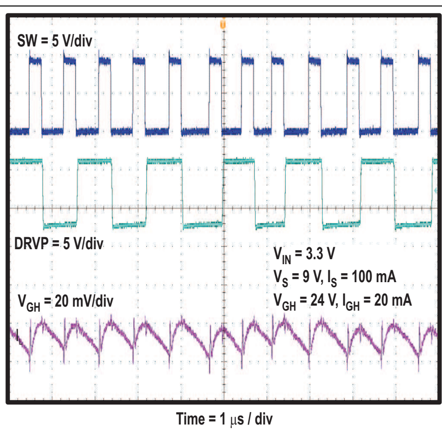


图 5. Positive Charge Pump Output Voltage Ripple

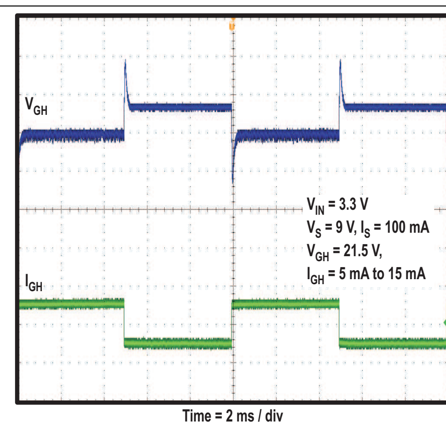


图 6. Positive Charge Pump Load Transient Response

Typical Characteristics (接下页)

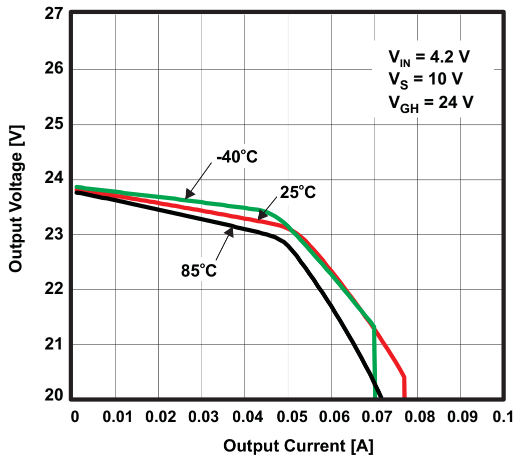


图 7. Positive Charge Pump Voltage vs Load Current

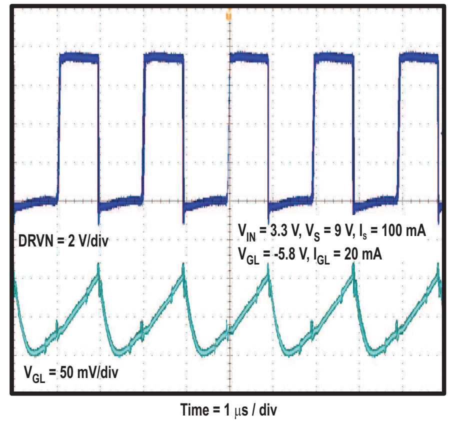


图 8. Negative Charge Pump Output Voltage Ripple

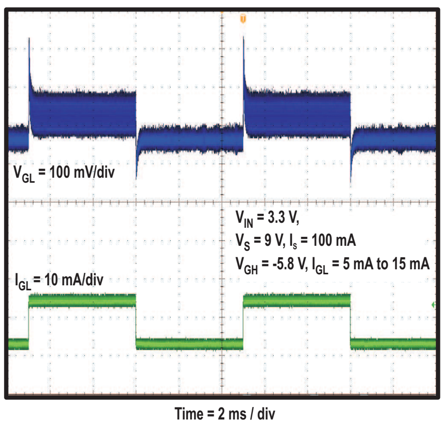


图 9. Negative Charge Pump Load Transient Response

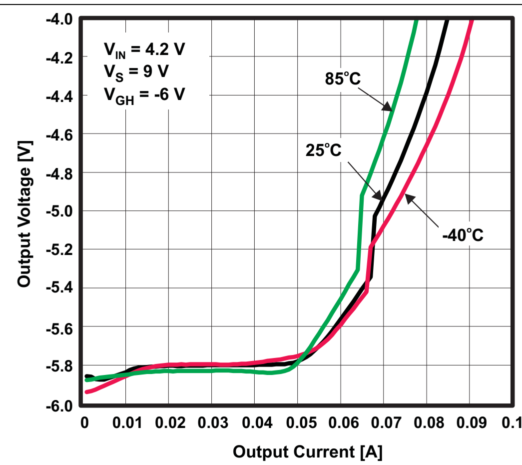


图 10. Negative Charge Pump Voltage vs Load Current

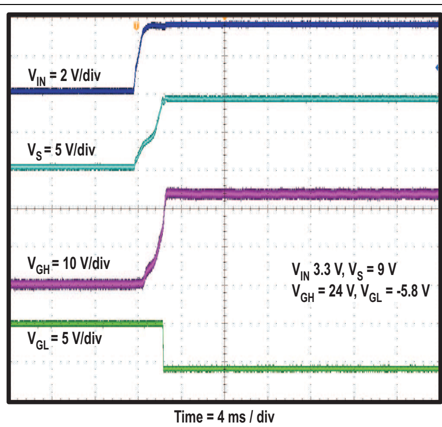


图 11. Power On Sequence

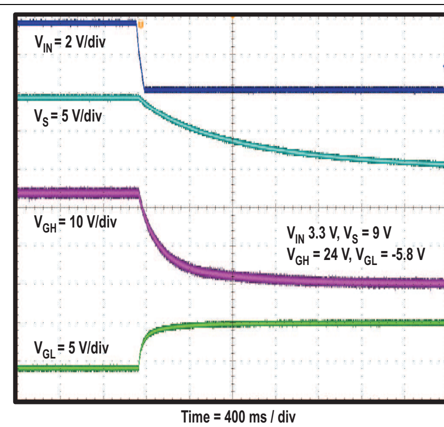


图 12. Power Off Sequence

Typical Characteristics (接下页)

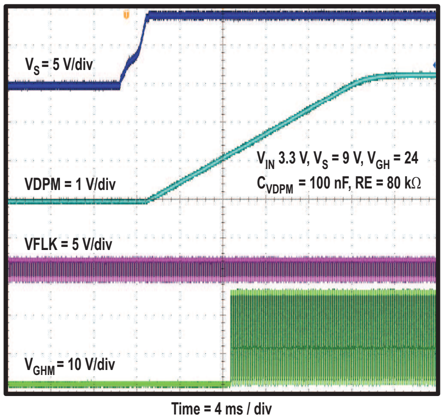


图 13. Power-On Sequence of VGHM

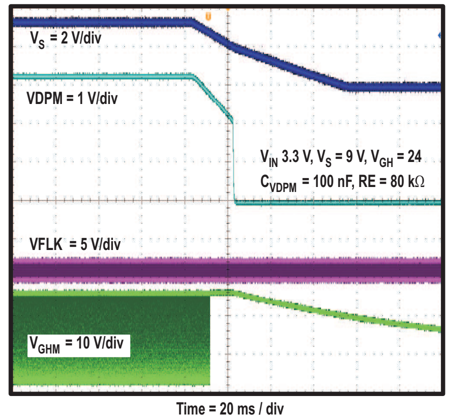


图 14. Power-Off Sequence of VGHM

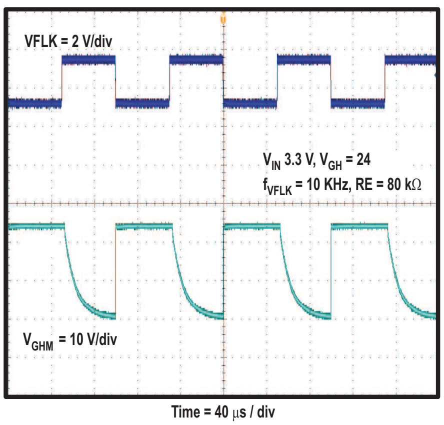


图 15. Gate Voltage Shaping

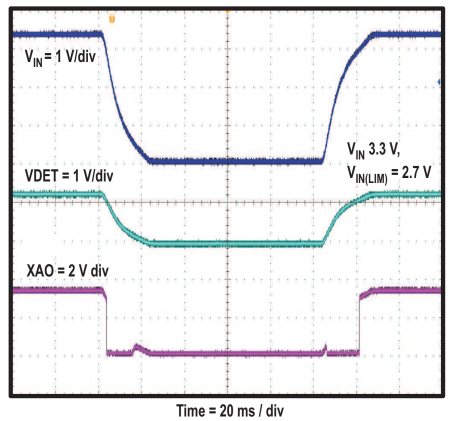


图 16. $\overline{XAO}$ Signal

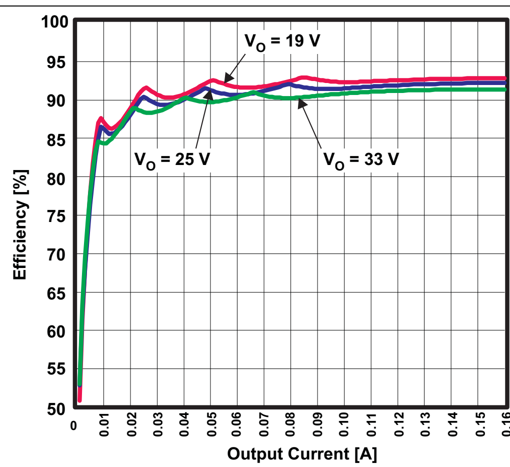


图 17. WLED Driver Efficiency vs Output Current

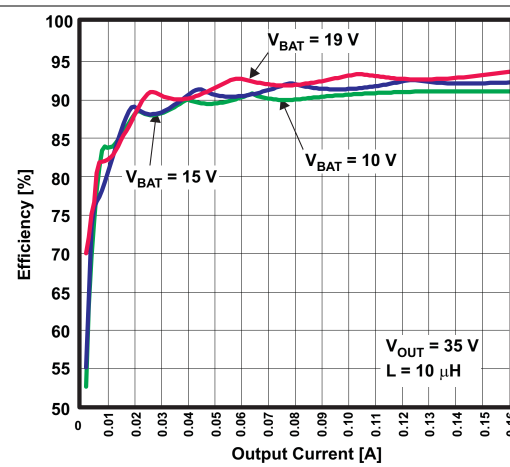


图 18. WLED Driver Efficiency vs Output Current

Typical Characteristics (接下页)

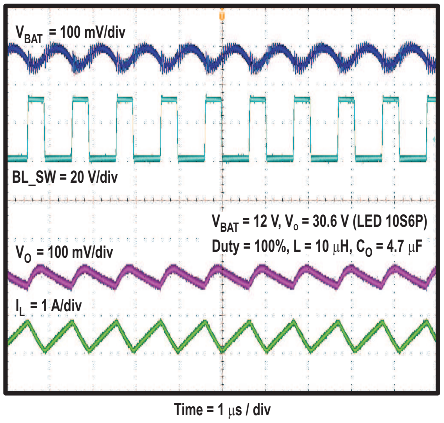


图 19. WLED Driver Switching Waveforms

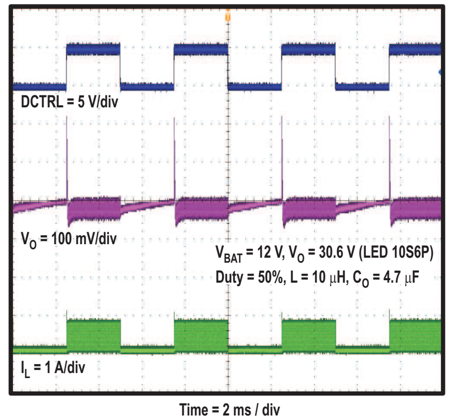


图 20. WLED Driver Output Ripple at PWM Dimming

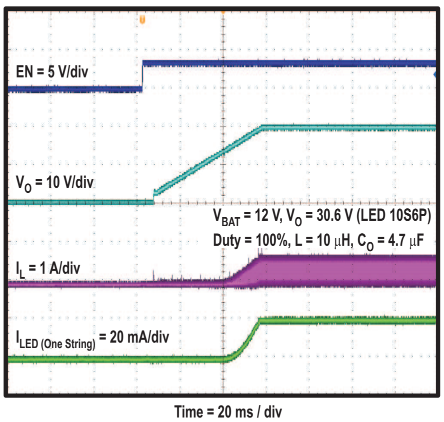


图 21. WLED Driver Power-On Sequence

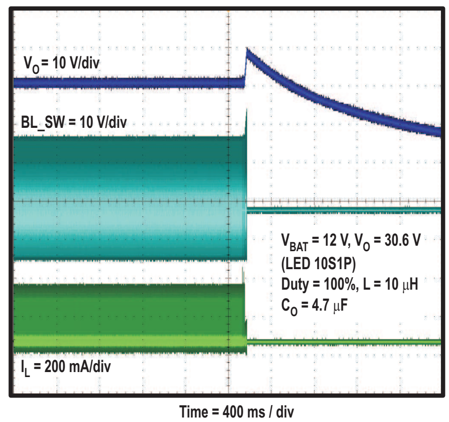


图 22. WLED Driver Open WLED Protection

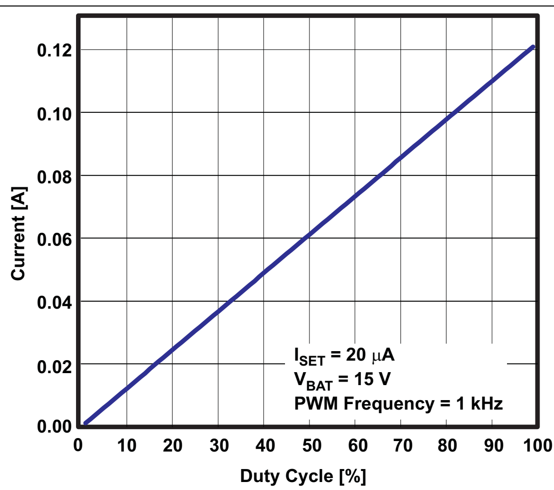


图 23. WLED Driver PWM Dimming Linearity 100 Hz

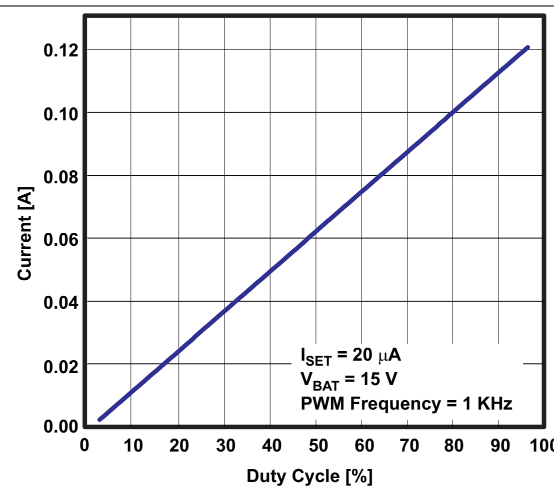


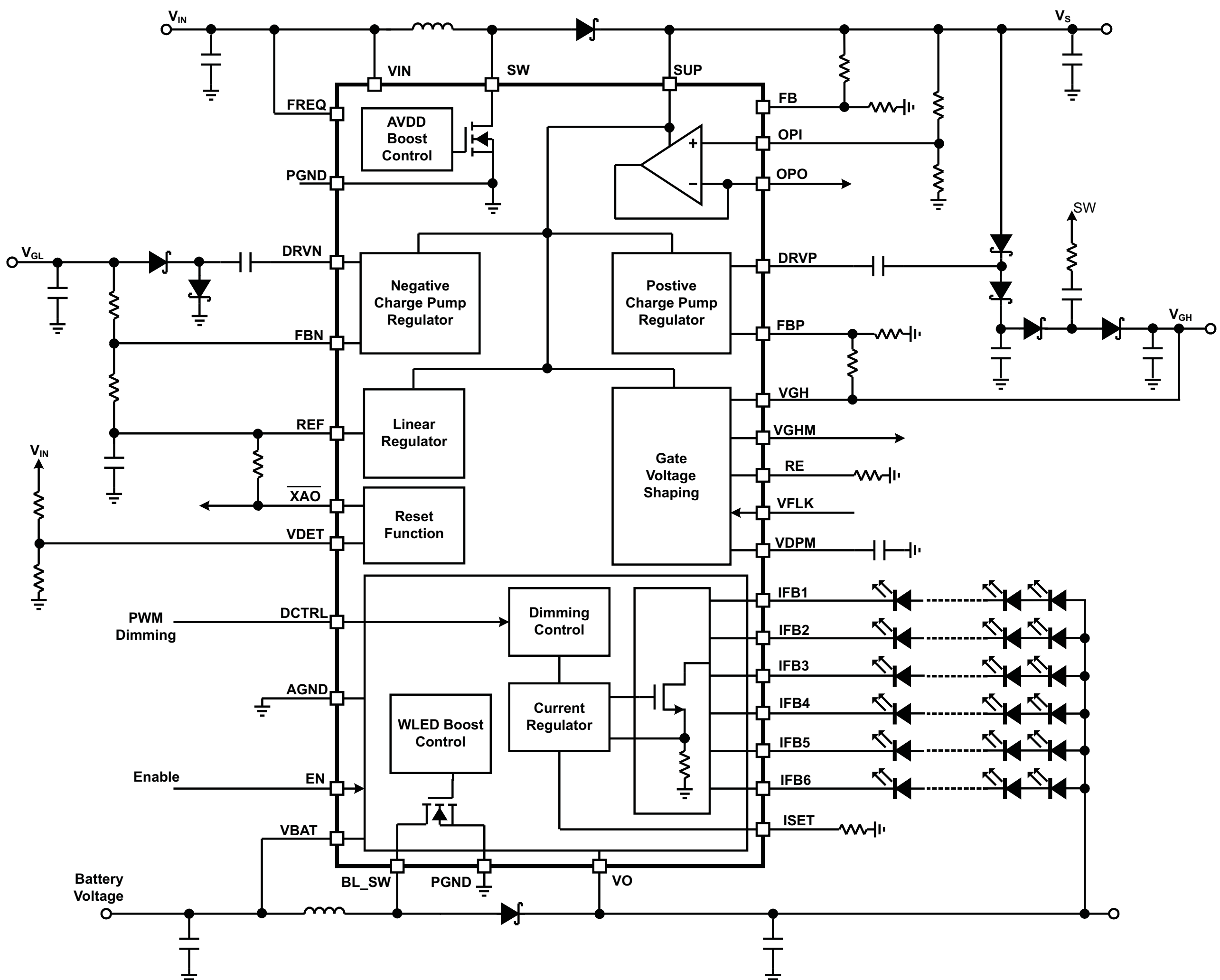
图 24. WLED Driver PWM Dimming Linearity 1 kHz

7 Detailed Description

7.1 Overview

The TPS65142 offers a compact and complete solution to the bias power and the WLED backlight in note-pc TFT-LCD panels. The device features an AVDD boost regulator, a positive charge pump regulator, and a negative charge pump regulator to power the source drivers and the gate drivers. A 150-mA unity-gain high-speed buffer is provided to drive the VCOM plane. Gate voltage shaping and the LCD discharge function are offered to improve the image quality. A reset function allows a proper reset of the TCON at power on or the gate driver ICs during power off. The TPS65142 also includes the complete solution to drive up to 6 chains of WLEDs with 1000:1 ratio PWM dimming.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 AVDD Boost Regulator

The AVDD boost regulator is designed for output voltages up to 16.5 V with a switch peak current limit of 1.8 A minimum. The device, which operates in a current-mode scheme with quasi-constant frequency, is internally compensated to minimize the pin and component counts. The switching frequency is selectable between 650 kHz and 1.2 MHz and the minimum input voltage is 2.3 V.

During the on-time, the current rises in the inductor. When the current reaches a threshold value set by the internal GM amplifier, the power transistor is turned off. The polarity of the inductor voltage changes and forward biases the Schottky diode, which lets the current flow towards the output of the boost regulator. The off-time is fixed for a certain input voltage V_{IN} and output voltage V_S, and therefore maintains the same frequency when varying these parameters. However, for different output loads, the frequency changes slightly due to the voltage drop across the $r_{DS(on)}$ of the power transistor which will have an effect on the voltage across the inductor and thus on t_{ON} (t_{OFF} remains fixed).

The fixed off-time maintains a quasi-fixed frequency that provides better stability for the system over a wide range of input and output voltages than conventional boost converters. The TPS65142 topology has also the benefits of providing very good load and line regulations, and excellent line and load transient responses.

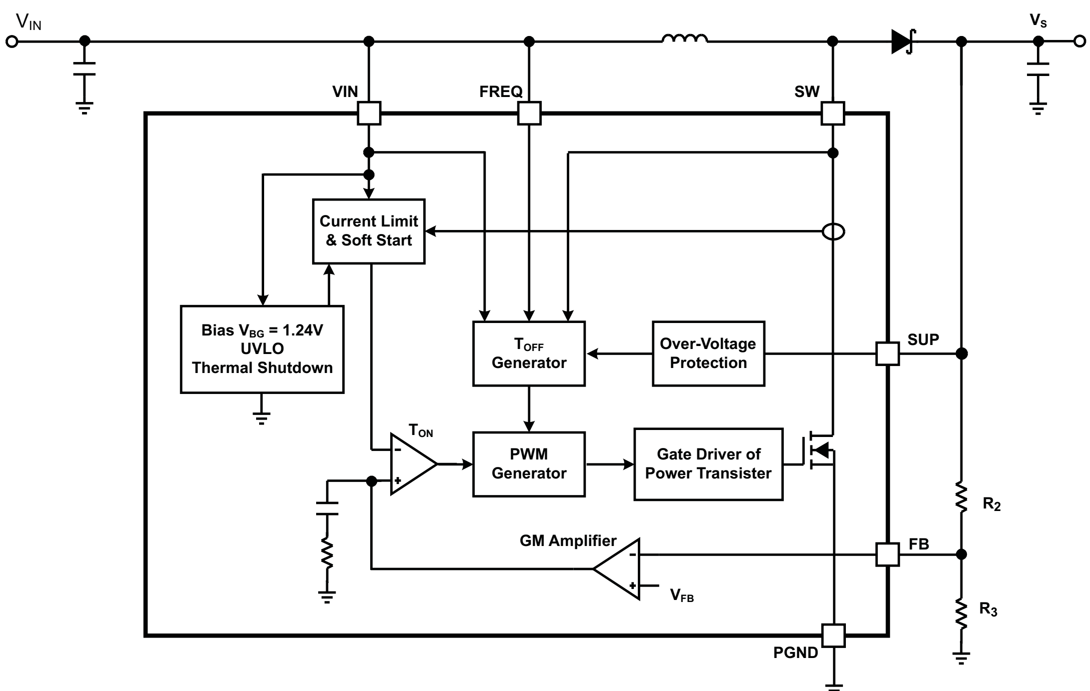


图 25. Boost Converter Block Diagram

7.3.1.1 Setting the Output Voltage

The output voltage is set by an external resistor divider. Typically, a minimum current of 50 µA flowing through the feedback divider is enough to cover the noise fluctuation. If 70 µA is chosen for higher noise immunity, the resistors shown in 图 25 are then calculated as:

$$R_3 = \frac{V_{FB}}{70\ \mu A} \approx 18.2\ k\Omega \qquad R_2 = R_3 \times \left(\frac{V_S}{V_{FB}} - 1\right) \tag{1}$$

where V_{FBP} = 1.240 V

7.3.1.2 Soft-Start (AVDD Boost Converter)

The AVDD boost converter has an internal digital soft-start to prevent high inrush current during start-up. The typical soft-start time is 2 ms.

Feature Description (接下页)

7.3.1.3 Frequency Select Pin (FREQ)

The digital frequency-select pin FREQ allows to set the switching frequency of the device to 650 kHz (FREQ = low) or 1.2 MHz (FREQ = high). Higher switching frequency improves load transient response but reduces slightly the efficiency. The other benefit of a higher switching frequency is the lower output voltage ripple. Usually, it is recommended to use 1.2-MHz switching frequency unless light load efficiency is a major concern.

7.3.1.4 Overvoltage Protection

The AVDD boost converter has an integrated over-voltage protection to prevent the power switch from exceeding the absolute maximum switch voltage rating at pin SW in case the feedback (FB) pin is floating or shorted to GND. In such an event, the output voltage rises and is monitored with the overvoltage protection comparator over the SUP pin. As soon as the comparator trips at typically 18 V, the boost converter turns the N-Channel MOSFET switch off. The output voltage falls below the overvoltage threshold and the converter continues to operate. In order to detect overvoltage, the SUP pin must to be connected to the output voltage of the boost converter V_S.

7.3.2 Regulated Positive Charge Pump

The positive charge pump sets the voltage applied on the VGH input pin, up to 32 V in tripler mode configuration. The charge pump block regulates the VGH voltage by adjusting the drive current I_{DRVP}. Typically, a minimum current of 50 µA flowing through the feedback divider is usually enough to cover the noise fluctuation. If 70 µA is chosen for higher noise immunity, the resistors of the divider used to set the V_{GH} voltage are calculated as (refer to 图 26):

$$R_8 = \frac{V_{FBP}}{70\ \mu A} \approx 18.2\ k\Omega \qquad R_7 = R_8 \times \left(\frac{V_{GH}}{V_{FBP}} - 1\right) \tag{2}$$

where V_{FBP} = 1.240 V

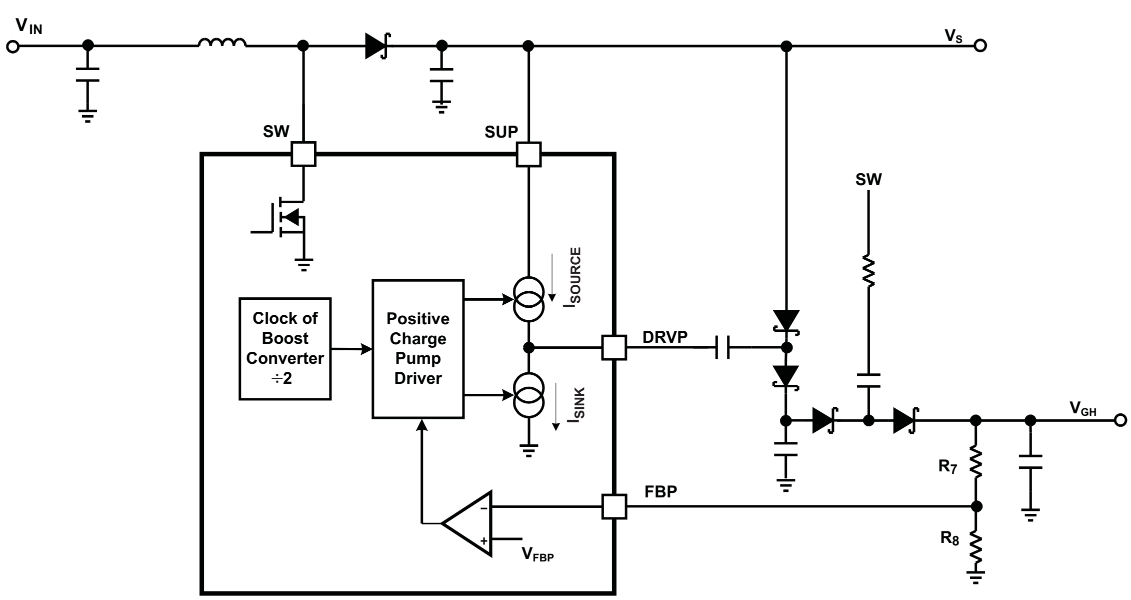


图 26. Block Diagram of the Positive Charge Pump Regulator

Feature Description (接下页)

7.3.3 Negative Charge Pump

图 27 shows the block diagram of the negative charge pump. The negative charge pump needs to generate a voltage of –6 V to –7 V with a negative inverter or –12 V to –13 V with a negative doubler. The reference voltage from the REF pin is 3.15 V. The bias to the REF block comes from the SUP pin. The error amplifier is referenced to the ground. The V_{GL} can be set with the following equation:

$$V_{GL} = -\frac{R_4}{R_5} \times V_{REF} \quad (3)$$

where V_{REF} = 3.12 V

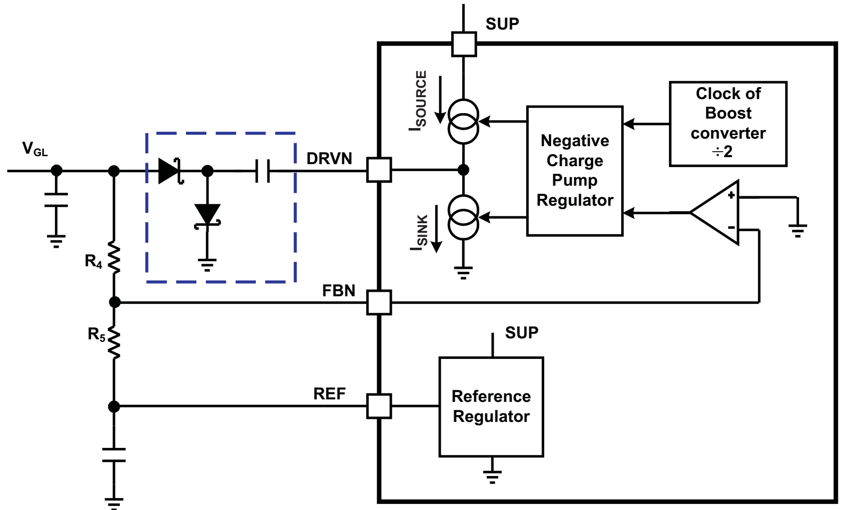


图 27. Block Diagram of the Negative Charge Pump Regulator with a Negative Inverter Configuration

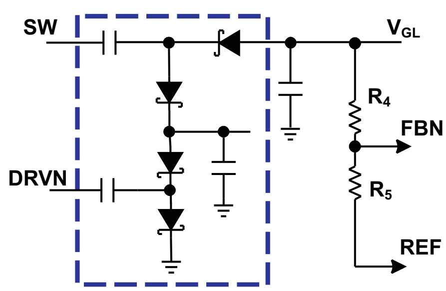


图 28. Negative Doubler Configuration for the Negative Charge Pump Regulator

7.3.4 Gate Voltage Shaping

The VGHM output is controlled by the VFLK logic input and the VDPM voltage level.

The VDPM pin allows the user to set a delay before the Gate Voltage Shaping starts. The voltage of the VDPM pin is zero volt at power on. When the output voltage of the AVDD boost converter rises above a power-good threshold, a power-good signal enables a 20-µA current source that charges the capacitor connected between the VDPM pin and the ground. When the VDPM-pin voltage rises to 1.24 V, the Gate Voltage Shaping is enabled.

The VFLK input controls the M1 and the M2 transistors, as shown in 图 29, after the Gate Voltage Shaping is enabled:

When VFLK = “low”, M1 is turned on so VGHM is connected to the VGH input.

Feature Description (接下页)

When VFLK = “high”, M2 is turned on so VGHM voltage is discharged through M2 and the resistor connected to the RE pin.

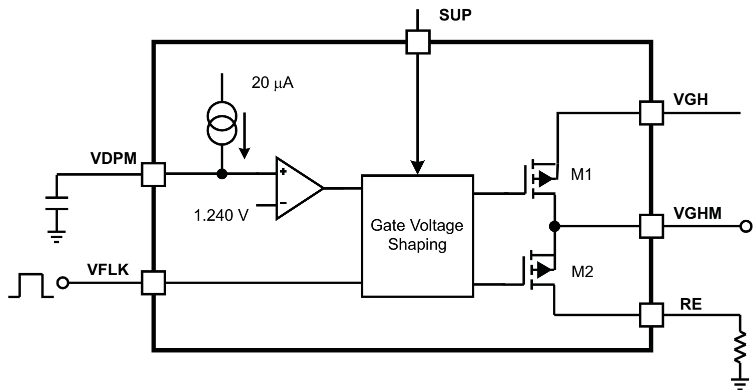


图 29. Block Diagram of the Gate Voltage Shaping Function

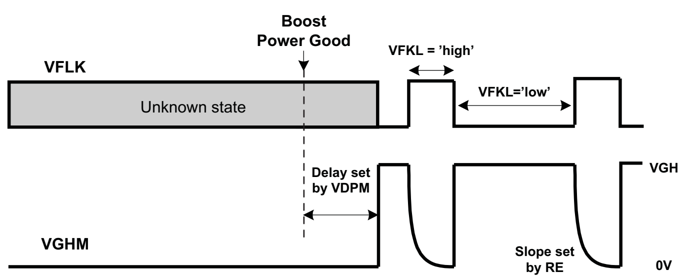


图 30. Gate Voltage Shaping Timing

7.3.5 VCOM Buffer

The VCOM Buffer power supply pin is the SUP pin connected to the AVDD boost converter V_S. To achieve good performance and minimize the output noise, a 1-µF ceramic bypass capacitor is required directly from the SUP pin to ground. The buffer is not designed to drive high capacitive loads; therefore, it is recommended to connect a series resistor at the output to provide stable operation when driving a high capacitive load. With a 3.3-Ω series resistor, a capacitive load of 10 nF can be driven, which is usually sufficient for typical LCD applications.

7.3.6 Reset

The device has an integrated reset function with an open-drain output capable of sinking 1 mA. The reset function monitors the voltage applied to its sense input $V_{(DET)}$. As soon as the voltage on $V_{(DET)}$ falls below the threshold voltage, $V_{(DET)}$, of typically 1.1 V, the reset function asserts its reset signal by pulling $\overline{XAO}$ low. Typically, a minimum current of 50 µA flowing through the feedback divider is enough to cover the noise fluctuation. Therefore, to select R_{12} and R_{13} (see 图 33), one has to set the input voltage limit ($V_{IN(LIM)}$) at which the reset function will pull $\overline{XAO}$ to low state. $V_{IN(LIM)}$ must be higher than the UVLO threshold. If 70 µA is chosen,

$$R_{13} = \frac{V_{(DET)}}{70\ \mu A} \approx 18.2\ k\Omega \qquad R_{12} = R_{13} \times \left(\frac{V_{IN(LIM)}}{V_{(DET)}} - 1 \right) \tag{4}$$

where V_{DET} = 1.1 V.

The $\overline{XAO}$ output is also controlled by the UVLO function. When the input voltage is below the UVLO threshold, $\overline{XAO}$ output is forced low until the input voltage is lower than 1.6 V. The $\overline{XAO}$ output is in an unknown state when the input voltage is below the 1.6 V threshold.

Feature Description (接下页)

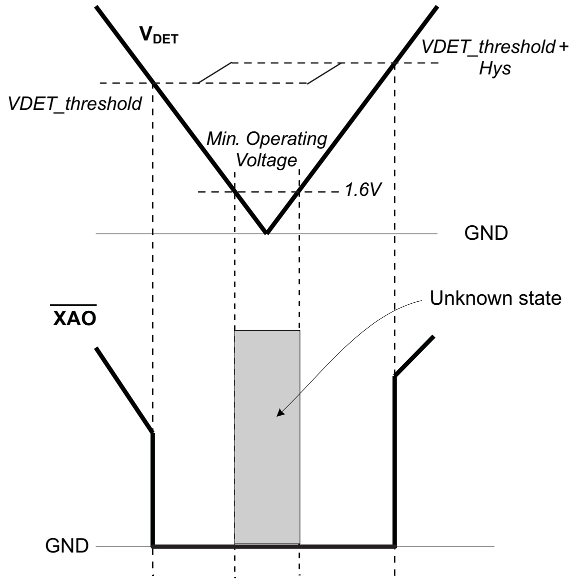


图 31. Voltage Detection and $\overline{XAO}$ Pin

When the input voltage VIN rises, once the voltage on VDET pin exceeds its threshold voltage plus the hysteresis, the $\overline{XAO}$ signal will go high.

The reset function is operational for $V_{IN} \geq 1.6$ V.

The reset function is configured as a standard open-drain and requires a pull-up resistor. The resistor $R_{(XAO)}$ (R_{14} in 图 33), which must be connected between the $\overline{XAO}$ pin output and a positive voltage V_X greater than 2 V – 'high' logic level can be chosen as follows:

$$R_{14} > \frac{V_X}{1\ mA} \quad \text{and} \quad R_{14} < \frac{V_X - 2\ V}{2\ \mu A} \tag{5}$$

7.3.7 Under-voltage Lockout (UVLO)

The TPS65142 monitors both VIN and VBAT inputs for under-voltage lockout. When the VIN input in under its UVLO threshold, the whole IC is disabled to avoid mis-operation. When the VIN input rises above its UVLO threshold, all functions are enabled except the WLED driver. The WLED driver, including the WLED boost converter and the current sinks, will be enabled when the VBAT input is also higher than its UVLO threshold.

7.3.8 Thermal Shutdown

A thermal shutdown is implemented to prevent damages because of excessive heat and power dissipation. Typically the thermal shutdown threshold for the junction temperature is 150°C. When the thermal shutdown is triggered the device stops switching until the junction temperature falls below typically 136°C. Then the device starts switching again.

7.3.9 WLED Boost Regulator

The WLED boost regulator is a current-mode PWM regulator with internal loop compensation. The internal compensation ensures a stable output over the full input and output voltage range. The WLED boost regulator switches at fixed 1 MHz. The output voltage of the boost regulator is automatically set by the TPS65142 to minimize the voltage drop across the current-sink IFBx pins. The lowest IFB-pin voltage to regulated to 400 mV. When the output voltage is too close to the input, the WLED boost regulator may not be able to regulate the output due to the limitation of the minimum duty cycle. In that case, the user needs to increase the number of WLED in series or to include series ballast resistors to provide enough headroom for the boost converter to operate. The WLED boost regulator cannot regulate its output to a voltage below 15 V.

Feature Description (接下页)

7.3.10 Current Sinks

The six current sink regulators can each provide a maximum of 25 mA. The IFB current must be programmed to the highest WLED current expected using an ISET-pin resistor with the following equation:

$$I_{(FB)} = K_{(ISET)} \frac{V_{(ISET)}}{R_{(ISET)}} \quad (6)$$

where

$K_{(ISET)}$ = Current multiple (1000 typical)
$V_{(ISET)}$ = ISET pin voltage (1.229 V typical)
$R_{(ISET)}$ = ISET-pin resistor value

The TPS65142 has built-in precise current sink regulators. The current matching error among 6 current sinks is below 2.5%. This means the differential values between the maximum and minimum currents of the six current sinks divided by the average current of the six is less than 2.5%.

7.3.11 Unused IFB Pins

If the application requires less than 6 WLED strings, one can easily disable unused IFBx pins by simply leaving the unused IFB pin open or shorting it to ground. If the IFB pin is open, the boost output voltage ramps up to V_O overvoltage threshold during start up. The IC then detects the zero current string and removes it from the feedback loop. If the IFB pin is shorted to ground, the IC detects the short immediately after WLED driver is enable, and the boost output voltage does not go up to V_O overvoltage threshold. Instead, it ramps to the regulation voltage after the soft start.

7.3.12 PWM Dimming

The WLED brightness is controlled by the PWM signal on the DCTRL pin. The frequency and duty cycle of the DCTRL signal is replicated on the IFB pin current. Keep the dimming frequency in the range of 100 Hz to 1 kHz to avoid screen flickering and to maintain dimming linearity. Screen flickering may occur if the dimming frequency is below the range. The minimum achievable duty cycle increases with the dimming frequency. For example, while a 0.1% dimming duty cycle, giving a 1000:1 dimming range, is achievable at 100 Hz dimming frequency, only 1% duty cycle, giving a 100:1 dimming range, is achievable with a 1-kHz dimming frequency, and 5% dimming duty cycle is achievable with 5 kHz dimming frequency. The device can work at high dimming frequency such as 20 kHz, but then only 15% duty cycle can be achieved. The TPS65142 is designed to minimize the AC ripple on the output capacitor during PWM dimming. Careful passive component selection is also critical to minimize AC ripple on the output capacitor.

7.3.13 Enabling the WLED Driver

The WLED driver (including the WLED boost converter and the six current sinks) is enabled when all following four conditions are satisfied:

1. the VBAT input voltage is higher than its under-voltage-lockout (UVLO) threshold;
2. the REF regulator output is higher than its power-good threshold;
3. the output voltage V_O is within 2 V of the input voltage V_{BAT};
4. and the enable input from the EN pin is high.

Pulling the EN pin low shuts down the WLED driver.

7.3.14 Soft-Start of WLED Boost Regulator

Once the above four conditions are satisfied, the WLED boost converter begins the internal soft-start. The soft-start function gradually ramps up the reference voltage of the error amplifier to prevent the output-voltage over shoot and inrush current from the VBAT input.

7.3.15 Protection of WLED Driver

The TPS65142 has multiple protection mechanisms to secure the safe operation of the WLED driver.

Feature Description (接下页)

7.3.15.1 Current Limit Protection

The WLED boost regulator switching MOSFET has a pulse-by-pulse over-current limit of 1.5 A (minimum value). The PWM switch turns off when the inductor current reaches this current threshold and remains off until the beginning of the next switching cycle. This protects the device and external components under over-load conditions. When there is sustained overcurrent condition for more than 16 ms (under 100% dimming duty cycle), the IC turns off and requires VBAT POR or the EN pin toggling to restart.

Under severe over load and/or short-circuit conditions, the VO pin can be pulled below the input (VBAT pin voltage). Under this condition, the current can flow directly from the input to the output through the inductor and the Schottky diode. Turning off the PWM switch alone does not limit current anymore. In this case, the TPS65142 relies on the fuse at the input to protect the whole system. When the TPS65142 detects the output voltage to be 1 V (short-circuit detection threshold) below the input voltage, it shuts down the WLED driver. The IC restarts after input power-on reset (VBAT POR) or EN pin logic toggling.

7.3.15.2 Open WLED String Protection

If one of the WLED strings is open, the boost output rises to its over-voltage threshold (39 V typically). The IC detects the open WLED string by sensing no current in the corresponding IFBx pin. As a result, the IC removes the open IFBx pin from the voltage feedback loop. The output voltage drops and is regulated to the voltage for the remaining connected WLED strings. The IFBx current of the connected WLED string remains in regulation during the whole transition.

The IC shuts down if it detects that all of the WLED strings are open.

7.3.15.3 Overvoltage Protection

If the overvoltage threshold is reached, but the current sensed on the IFBx pin is below the regulation target, the IC regulates the boost output at the overvoltage threshold. This operation could occur when the WLED is turned on under cold temperature, and the forward voltages of the WLEDs exceed the over-voltage threshold. Maintaining the WLED current allows the WLED to warm up and their forward voltages to drop below the overvoltage threshold.

If any IFBx pin voltage exceeds IFB overvoltage threshold (17 V typical), the IC turns off the corresponding current sink and removes this IFB pin from VO regulation loop. The remaining IFBx pins' current regulation is not affected. This condition often occurs when there are several shorted WLEDs in one string. WLED mismatch typically does not create such large voltage difference among WLED strings.

7.3.16 Power Up/Down Sequence

The power up and power down sequences are shown in 图 32.

The operation of the bias converters are gated by the UVLO of the VIN voltage. The start-up of the WLED boost converter is gated by the UVLO of the VBAT input, the power good of the REF output, the (VBAT – 2 V) and VO comparator output, and the EN input. The REF output is powered by the output of the AVDD boost converter through the SUP pin; and hence, the WLED boost converter will not start before the AVDD boost converter.

7.3.16.1 Power Up Sequence

The power up sequence of the bias portion is as following. When the VIN rises above the ULVO threshold, and the internal device enable signal is asserted. The AVDD boost converter begins the soft-start, the REF regulator starts to rise, the VCOM buffer is enabled, and both charge pumps begins to operate. When the REF output reaches its regulation voltage, a VREF power good signal is asserted for the WLED section. The AVDD boost converter continues the soft start until its output voltage reaches the AVDD power good threshold when an AVDD power good signal is asserted. The AVDD power good signal enables the 20-µA current to the VDPM pin to start the gate voltage shaping delay timer. The delay is programmed by the external capacitor connected to the VDPM pin and should be long enough to ensure that both charge pumps are ready before the delay ends. Once the delay ends, the gate voltage shaping (VGHM) output is enabled to be controlled by the VFLK input.

The power up sequence of the WLED driver section is as following. When the four conditions for the Enabling the WLED Driver section are satisfied, the WLED boost converter begins the soft start, together with the start of the current sinks. When any of the four conditions is not satisfied, the WLED boost converter will stop switching.

Feature Description (接下页)

To ensure proper start-up of the TPS65142 device, it is recommended to apply V_{BAT} before V_{IN} (see *Timing Requirements* and 图 32).

7.3.16.2 Power Down Sequence and LCD Discharge Function

The power down sequence of the bias section is as following. When the input voltage V_{IN} falls below a predefined threshold set by $V_{(DET\_THRESHOLD)}$, $\overline{XAO}$ is driven low and the VGHM output is driven to V_{GH}. (Note that when V_{IN} falls below the UVLO threshold, all IC functions are disabled except $\overline{XAO}$ and VGHM outputs). Since VGHM is connected to VGH, it tracks the output of the positive charge pump as it decays. This feature, together with $\overline{XAO}$, can be used to discharge the panel by turning on all the pixel TFTs and discharging them into the gradually decaying VGHM voltage. VHGM is held low during power-up.

The REF regulator will be disabled when V_{IN} falls below the UVLO threshold, hence, the WLED boost converter as well.

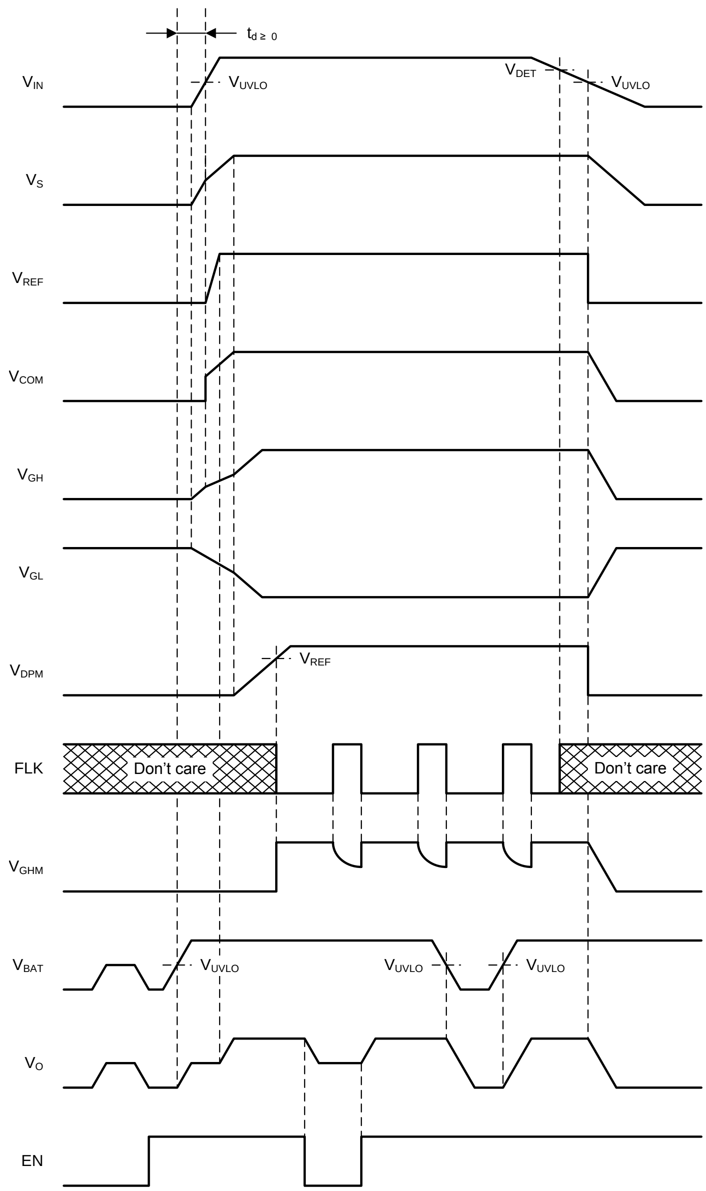


图 32. Power Up/Down Sequence

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Typical Application

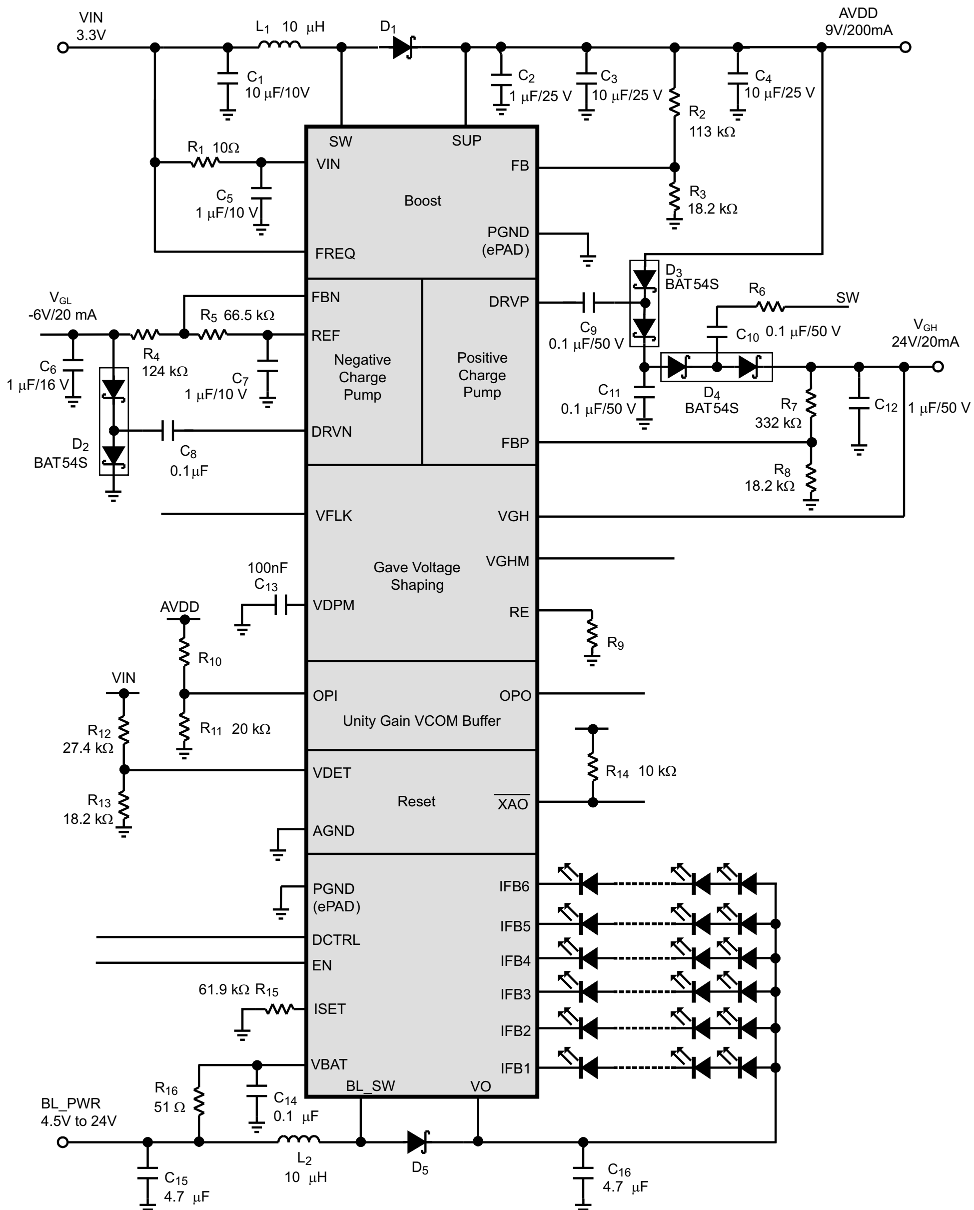


图 33. Typical Application Circuit

9 器件和文档支持

9.1 社区资源

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TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

9.2 商标

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9.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

9.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

10 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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	产品		应用
数字音频	www.ti.com.cn/audio	通信与电信	www.ti.com.cn/telecom
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数据转换器	www.ti.com.cn/dataconverters	消费电子	www.ti.com/consumer-apps
DLP® 产品	www.dlp.com	能源	www.ti.com/energy
DSP - 数字信号处理器	www.ti.com.cn/dsp	工业应用	www.ti.com.cn/industrial
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接口	www.ti.com.cn/interface	安防应用	www.ti.com.cn/security
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RFID 系统	www.ti.com.cn/rfidsys		
OMAP应用处理器	www.ti.com/omap		
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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65142RTGR	ACTIVE	WQFN	RTG	32	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TS65142	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

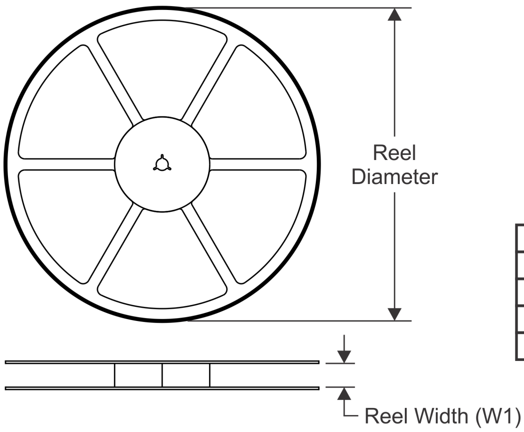
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

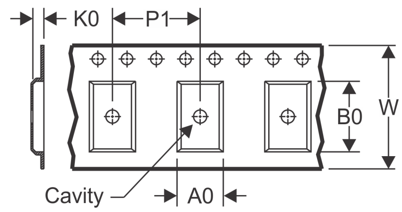
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

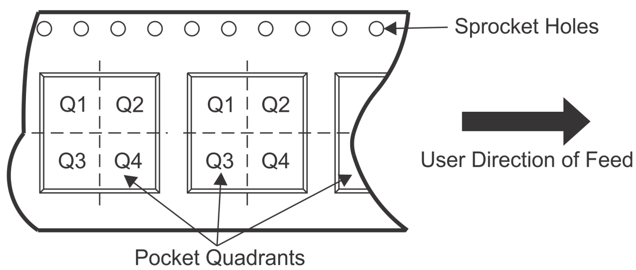
TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

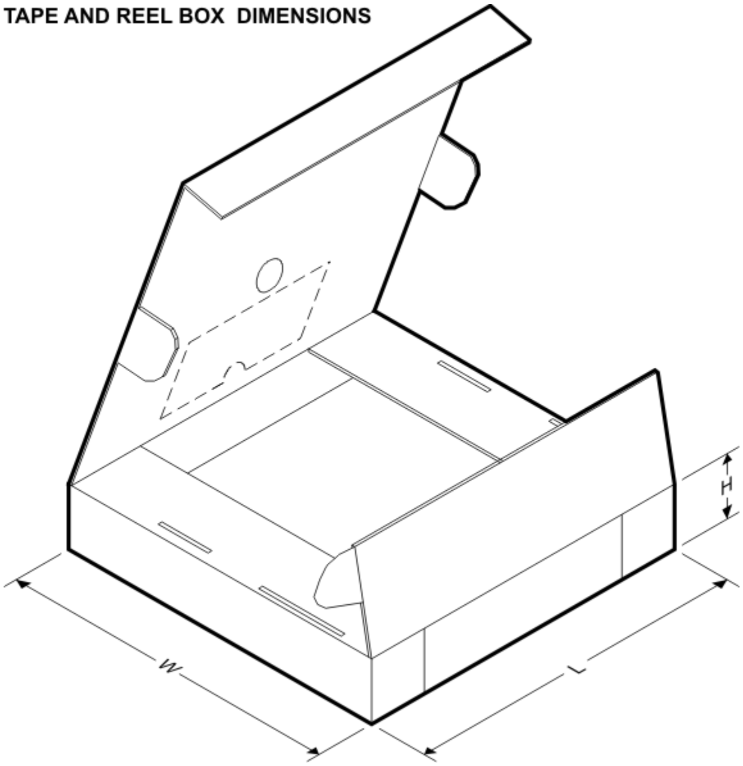
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65142RTGR	WQFN	RTG	32	3000	330.0	16.4	3.3	6.3	1.0	8.0	16.0	Q1

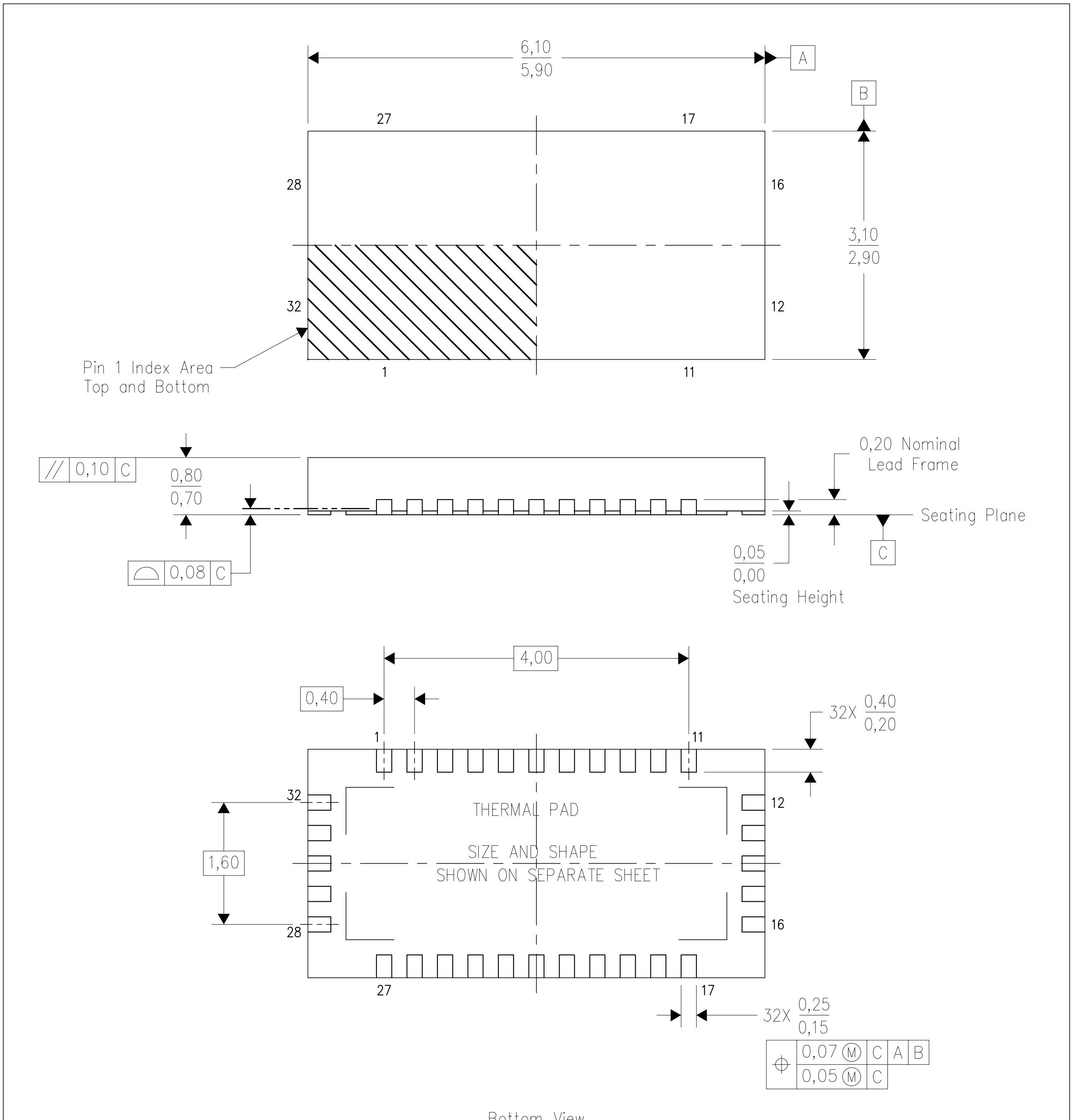
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65142RTGR	WQFN	RTG	32	3000	367.0	367.0	38.0

RTG (R–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



4210467/B 05/2011

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Reference JEDEC MO–220.

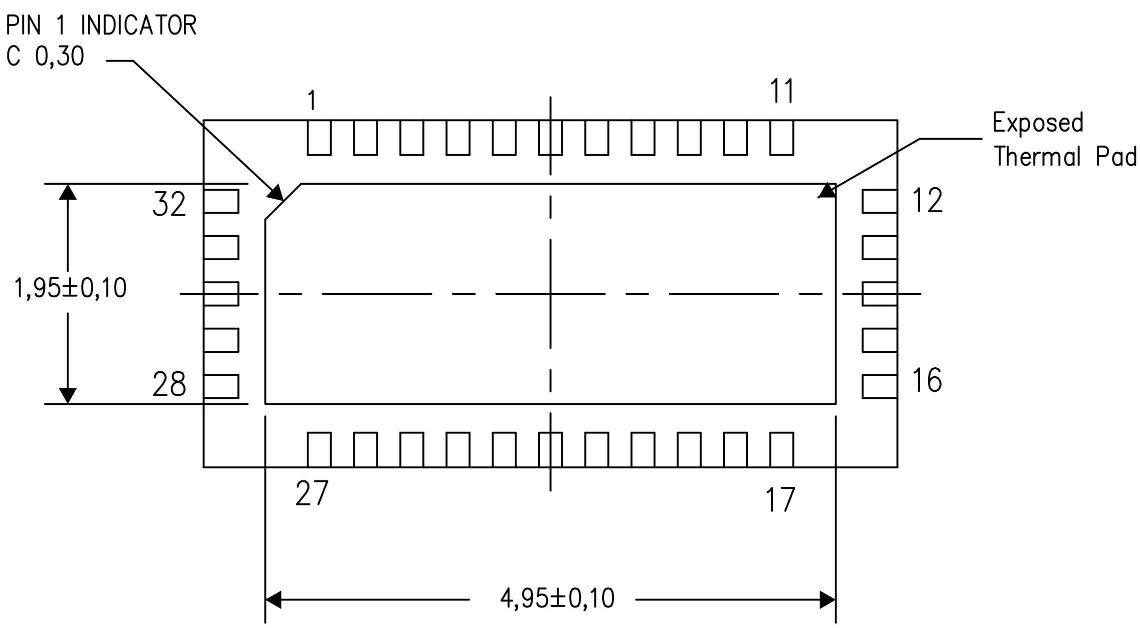
RTG (R-PWQFN-N32) PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



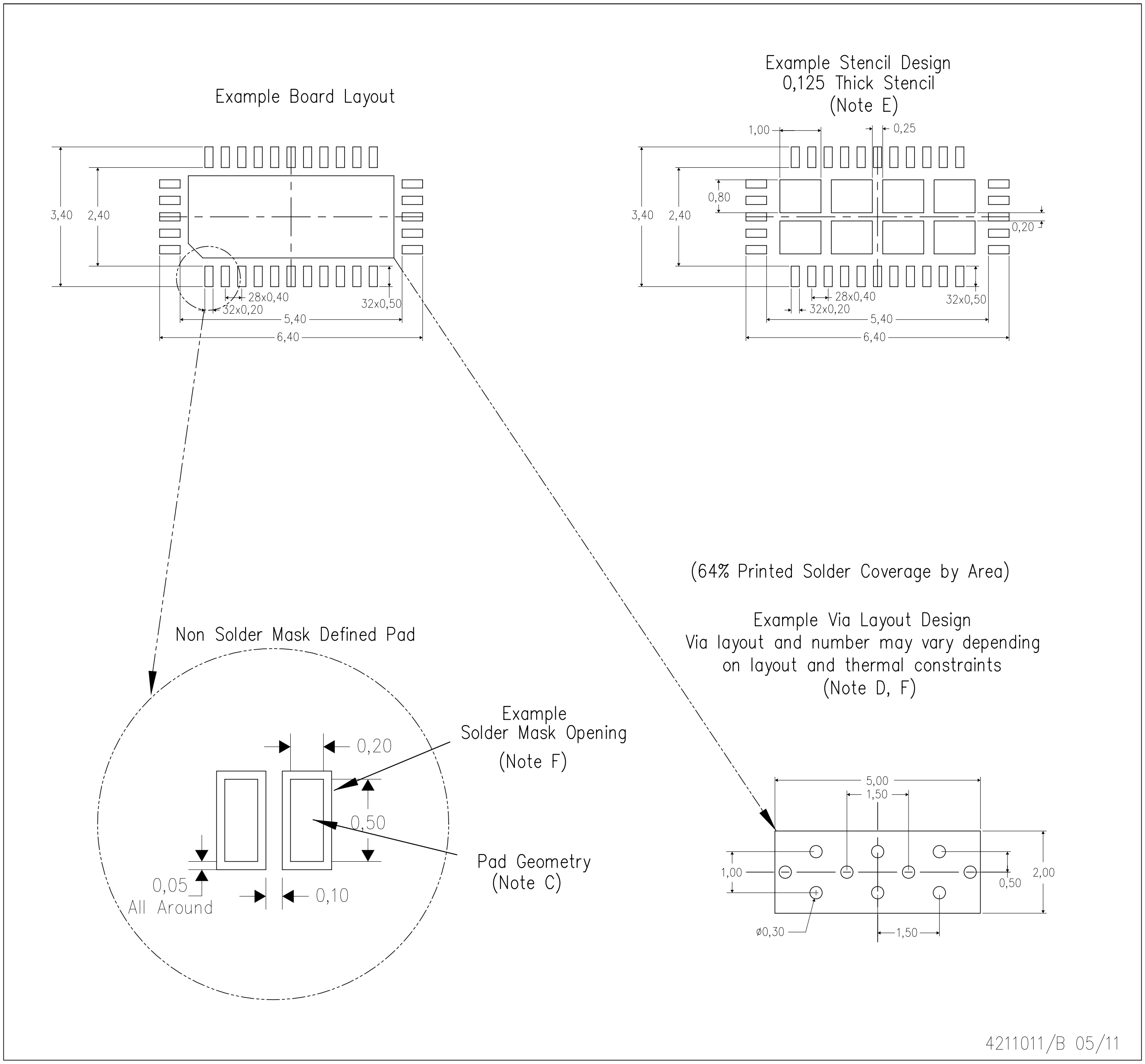
Bottom View

Exposed Thermal Pad Dimensions

4210534-2/D 12/13

NOTE: All linear dimensions are in millimeters

RTG (R–PWQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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