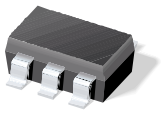


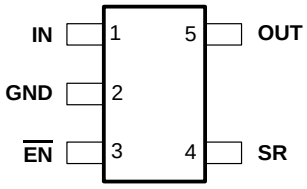
SLVS382A – JUNE 2001 – REVISED JULY 2001

# 150-mA LOW-NOISE LDO WITH IN-RUSH CURRENT CONTROL FOR USB APPLICATION

## FEATURES

- **150-mA Low-Dropout Regulator**
- **Available in 2.5 V, 3.3 V**
- **Programmable Slew Rate Control**
- **Output Noise Typically 56 $\mu V_{RMS}$**
- **Only 17 μA Quiescent Current at 150 mA**
- **1 μA Quiescent Current in Standby Mode**
- **Dropout Voltage Typically 150 mV at 150 mA (TPS78833)**
- **Over Current Limitation**
- **–40°C to 125°C Operating Junction Temperature Range**
- **5-Pin SOT-23 (DBV) Package**

**DBV PACKAGE**
**(TOP VIEW)**



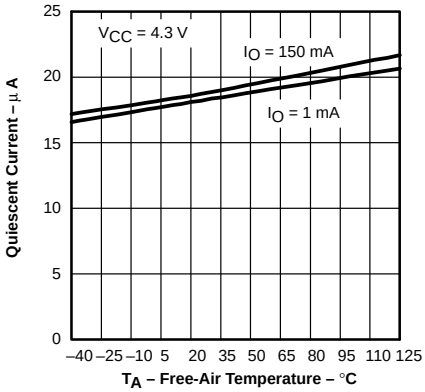

## DESCRIPTION

The TPS78825 and TPS78833 are very small (SOT-23) package, low-noise LDOs that regulate the output voltage to 2.5 V and 3.3 V with input voltage ranging from 2.7 V to an absolute maximum of 13.5 V. These devices output 150 mA with a peak current of 350 mA (typ). The TPS788xx family uses the SR pin to program the output voltage slew rate to control the in-rush current. This is specifically used in the USB application where large load capacitance is present at start-up. The TPS788xx devices use only 17 μA of quiescent current and exhibit only 56 $\mu V_{RMS}$ of output voltage noise using a 10 μF output capacitor.

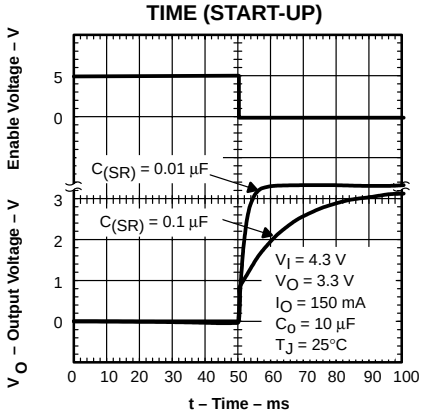
The usual PNP pass transistor has been replaced by a PMOS pass element. Because the PMOS pass element behaves as a low-value resistor, the dropout voltage is very low, typically 150 mV at 150 mA of load current, and is directly proportional to the load current.

The TPS788xx also features a logic-enabled sleep mode to shut down the regulator, reducing quiescent current to 1 μA typical at $T_J$ = 25°C.

**QUIESCENT CURRENT**
**vs**
**FREE-AIR TEMPERATURE**




**OUTPUT VOLTAGE, ENABLE VOLTAGE**
**vs**
**TIME (START-UP)**

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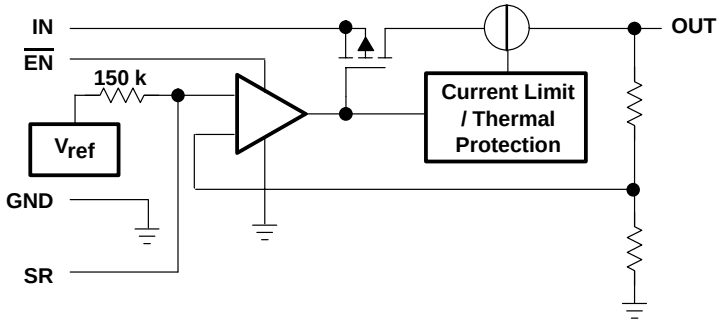
**AVAILABLE OPTIONS**

| $T_J$ | VOLTAGE | PACKAGE | PART NUMBER | | SYMBOL |
|---|---|---|---|---|---|
| –40°C to 125°C | 2.5 V | SOT-23 (DBV) | TPS78825DBVT† | TPS78825DBVR‡ | PGZI |
| | 3.3 V | | TPS78833DBVT | TPS78833DBVR | PGTI |

† The DBVT indicates tape and reel of 250 parts.
‡ The DBVR indicates tape and reel of 3000 parts.

## functional block diagram




## Terminal Functions

| TERMINAL NAME | TERMINAL NO. | I/O | DESCRIPTION |
|---|---|---|---|
| $\overline{EN}$ | 3 | I | Active low enable |
| GND | 2 | | Regulator ground |
| IN | 1 | I | The IN terminal is the input to the device. |
| OUT | 5 | O | The OUT terminal is the regulated output of the device. |
| SR | 4 | I | The SR terminal is used to control the in-rush current. |

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)§

Input voltage range (see Note 1) . . . . . –0.3 V to 13.5 V
Voltage range at EN . . . . . –0.3 V to $V_I$ + 0.3 V
Voltage on OUT . . . . . 7 V
Peak output current . . . . . Internally limited
ESD rating, HBM . . . . . 2 kV
Continuous total power dissipation . . . . . See Dissipation Rating Table
Operating virtual junction temperature range, $T_J$ . . . . . –40°C to 150°C
Operating ambient temperature range, $T_A$ . . . . . –40°C to 85°C
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

§ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to network ground terminal.

**DISSIPATION RATING TABLE**

| BOARD | PACKAGE | $R_{\theta JC}$ | $R_{\theta JA}$ | DERATING FACTOR ABOVE $T_A$ = 25°C | $T_A \le 25°C$ POWER RATING | $T_A$ = 70°C POWER RATING | $T_A$ = 85°C POWER RATING |
|---|---|---|---|---|---|---|---|
| Low K¶ | DBV | 65.8°C/W | 259°C/W | 3.9 mW/°C | 386 mW | 212 mW | 154 mW |
| High K# | DBV | 65.8°C/W | 180°C/W | 5.6 mW/°C | 555 mW | 305 mW | 222 mW |

¶ The JEDEC Low K (1s) board design used to derive this data was a 3 inch x 3 inch, two layer board with 2 ounce copper traces on top of the board.
# The JEDEC High K (2s2p) board design used to derive this data was a 3 inch x 3 inch, multilayer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.

## electrical characteristics over recommended operating free-air temperature range $\overline{EN}$ = 0, $T_J$ = –40 to 125 °C, $V_I = V_{O(typ)} + 1$ V, $I_O$ = 1 mA, $C_o$ = 4.7 µF, $C_{(SR)}$ = 0.01 µF (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_I$ Input voltage (see Note 2) | | | | 2.7 | | 10 | V |
| $I_O$ Continuous output current (see Note 3) | | | | 0 | | 150 | mA |
| $T_J$ Operating junction temperature | | | | –40 | | 125 | °C |
| Output voltage | TPS78825 | $T_J$ = 25°C | | | 2.5 | | V |
| | | 10 µA< $I_O$ < 150 mA, 3.5 V < $V_I$ < 10 V | | 2.425 | | 2.575 | |
| | TPS78833 | $T_J$ = 25°C | | | 3.3 | | |
| | | 10 µA< $I_O$ < 150 mA, 3.8 V < $V_I$ < 10 V | | 3.201 | | 3.399 | |
| Quiescent current (GND current) | | 10 µA< $I_O$ < 450 mA, $T_J$ = 25°C | | | 17 | | µA |
| | | 10 µA< $I_O$ < 150 mA | | | | 28 | |
| Load regulation | | 10 µA< $I_O$ < 200 mA, $T_J$ = 25°C | | | 12 | | mV |
| Output voltage line regulation ($\Delta V_O/V_O$) (see Note 5) | | $V_O$ + 1 V < $V_I$ ≤ 10 V, $T_J$ = 25°C | | | 0.04 | | %/V |
| | | $V_O$ + 1 V < $V_I$ ≤ 10 V | | | | 0.1 | |
| Output noise voltage (TPS78833) | | BW = 200 Hz to 100 kHz, $I_O$ = 150 mA, $T_J$ = 25°C, $C_o$ = 10 µF, $C_{(SR)}$ = 0.47 µF | | | 56 | | $\mu V_{RMS}$ |
| Time, start-up (TPS78833) | | $R_L$ = 22 Ω, $C_o$ = 10 µF, $T_J$ = 25°C | $C_{(byp)}$ = 0.01 µF | | 10 | | ms |
| | | | $C_{(byp)}$ = 0.1 µF | | 50 | | |
| | | | $C_{(byp)}$ = 0.47 µF | | 300 | | |
| Output current limit | | $V_O$ = 0 V (see Note 4) | | | 350 | 750 | mA |
| Standby current | | EN = 0 V, 2.7 V < $V_I$ < 10 V | | | 1 | 2 | µA |
| High level enable input voltage | | 2.7 V < $V_I$ < 10 V | | 1.7 | | | V |
| Low level enable input voltage | | 2.7 V < $V_I$ < 10 V | | | | 0.9 | V |
| Input current (EN) | | EN = 0 | | –1 | | 1 | µA |
| Power supply ripple rejection | TPS78833 | f = 1 kHz, $T_J$ = 25°C, $C_o$ = 10 µF | $C_{(SL)}$ = 0.01 µF, $I_O$ = 150 mA, | | 70 | | dB |
| Dropout voltage (see Note 6) | TPS78833 | $I_O$ = 150 mA, $T_J$ = 25°C | | | 150 | | mV |
| | | $I_O$ = 150 mA | | | | 300 | |

NOTES: 2. To calculate the minimum input voltage for your maximum output current, use the following formula:
$V_I(min) = V_O(max) + V_{DO}$ (max load)

3. Continuous output current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

4. The minimum IN operating voltage is 2.7 V or $V_{O(typ)}$ + 1 V, whichever is greater. The maximum IN voltage is 5.5 V. The maximum output current is 200 mA.

5. If $V_O \le 2.5$ V then $V_{Imin}$ = 2.7 V, $V_{Imax}$ = 5.5 V:

$$\text{Line regulation (mV)} = (\%/V) \times \frac{V_O\left(V_{Imax} - 2.7\ V\right)}{100} \times 1000$$

If $V_O$ > 2.5 V then $V_{Imin} = V_O$ + 1 V, $V_{Imax}$ = 5.5 V.

6. IN voltage equals $V_O(typ)$ – 100 mV

## TYPICAL CHARACTERISTICS

**OUTPUT VOLTAGE vs LOAD CURRENT**

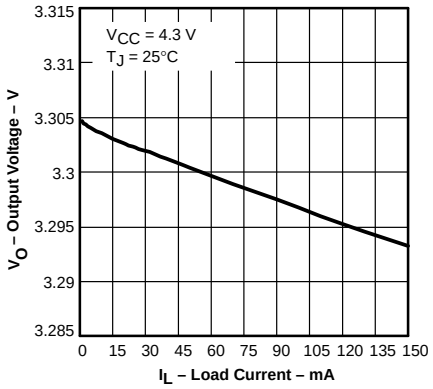



Figure 1

**OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE**

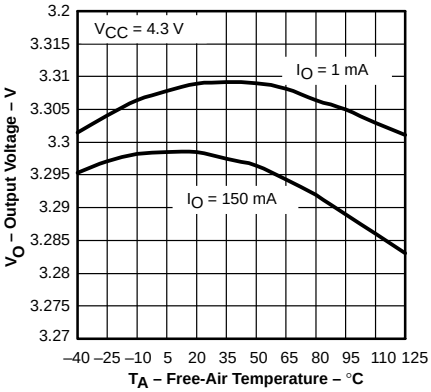



Figure 2

**QUIESCENT CURRENT vs FREE-AIR TEMPERATURE**

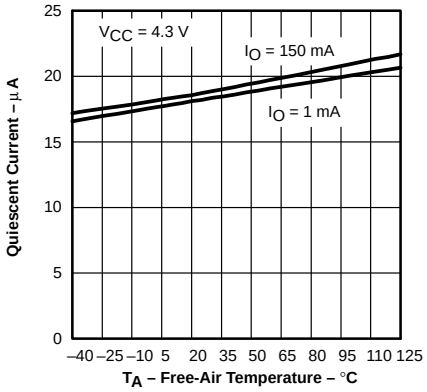



Figure 3

**OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY**

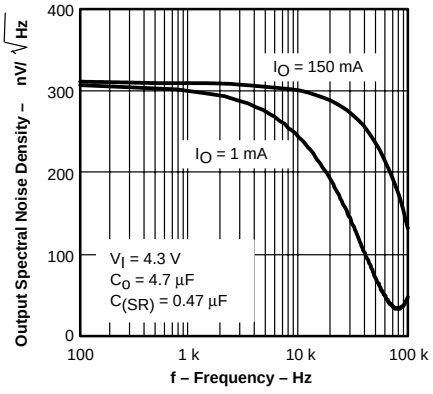



Figure 4

**ROOT MEAN SQUARED OUTPUT NOISE vs SLEW RATE CAPACITANCE**

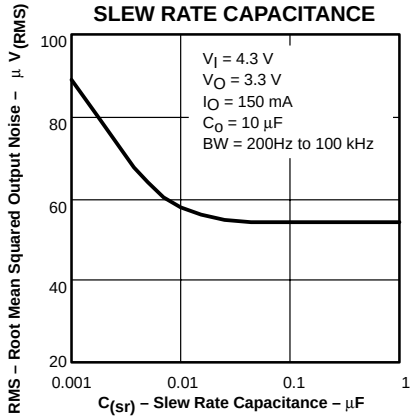



Figure 5

**OUTPUT IMPEDANCE vs FREQUENCY**

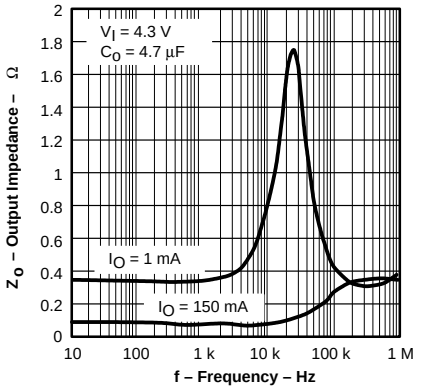



Figure 6

**DROPOUT VOLTAGE vs FREE-AIR TEMPERATURE**

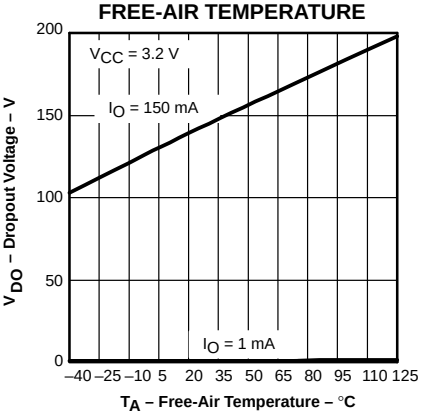



Figure 7

**RIPPLE REJECTION vs FREQUENCY**

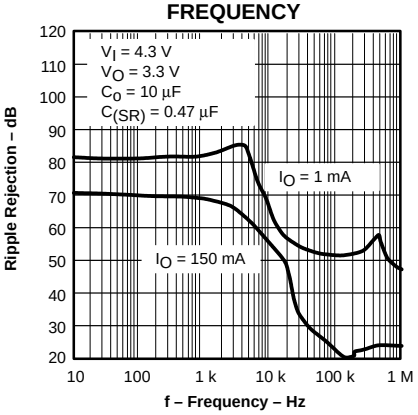



Figure 8

**OUTPUT VOLTAGE, ENABLE VOLTAGE vs TIME (START-UP)**

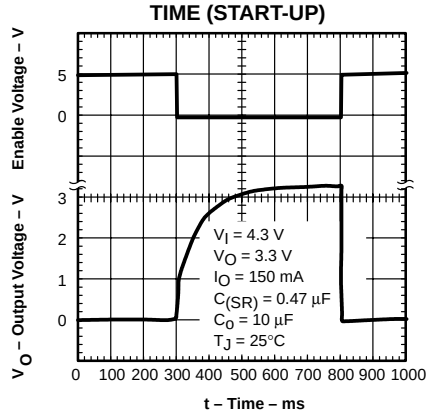



Figure 9

## TYPICAL CHARACTERISTICS

**OUTPUT VOLTAGE, ENABLE VOLTAGE vs TIME (START-UP)**

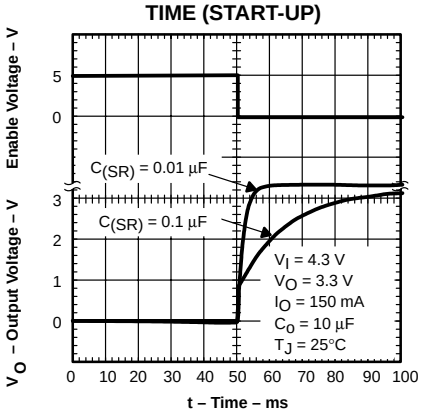



Figure 10

**LINE TRANSIENT RESPONSE**

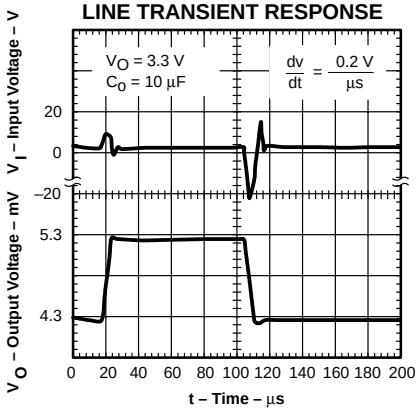



Figure 11

**LOAD TRANSIENT RESPONSE**

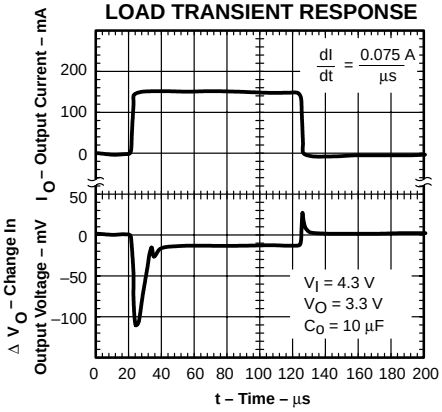



Figure 12

**TYPICAL REGIONS OF STABILITY EQUIVALENT SERIES RESISTANCE (ESR) vs OUTPUT CURRENT**

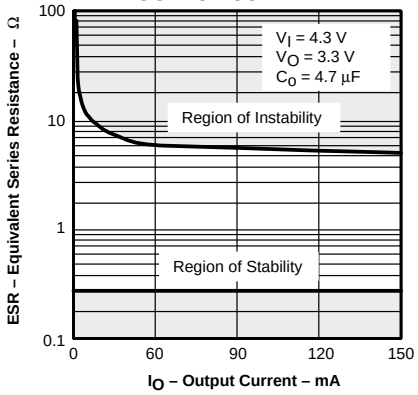



Figure 13

**TYPICAL REGIONS OF STABILITY EQUIVALENT SERIES RESISTANCE (ESR) vs OUTPUT CURRENT**

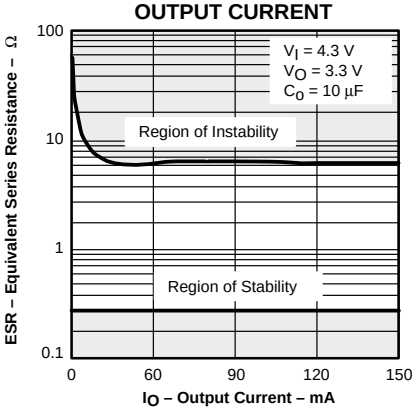



Figure 14

## APPLICATION INFORMATION

The TPS788xx family of low-dropout (LDO) regulators has been optimized for use in battery-operated equipment. It features extremely low dropout voltages, low output noise, low quiescent current (17 μA typically), and enable inputs to reduce supply currents to 1 μA when the regulator is turned off. A typical application circuit is shown in Figure 15.

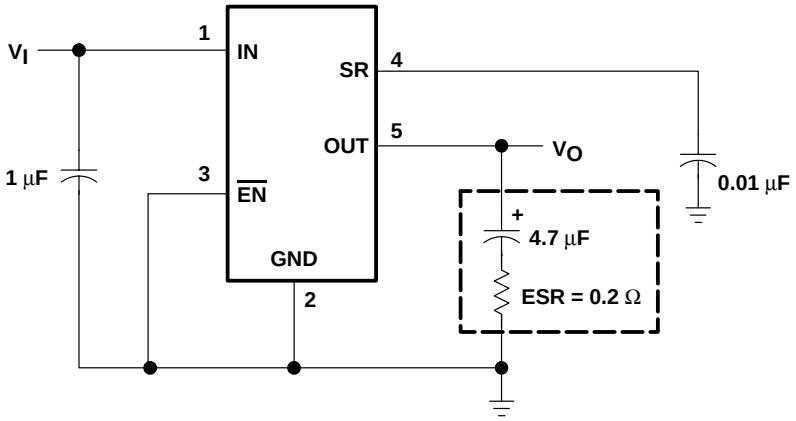



**Figure 15. Typical Application Circuit**

### external capacitor requirements

Although not required, a 0.047-μF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS788xx, is recommended to improve transient response and noise rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like all low dropout regulators, the TPS788xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 4.7 μF. The ESR (equivalent series resistance) of the capacitor should be between 0.2 Ω and 10 Ω. to ensure stability. Capacitor values larger than 4.7 μF are acceptable, and allow the use of smaller ESR values. Capacitances less than 4.7 μF are not recommended because they require careful selection of ESR to ensure stability. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Most of the commercially available 4.7 μF surface-mount solid tantalum capacitors, including devices from Sprague, Kemet, and Nichico, meet the ESR requirements stated above. Multilayer ceramic capacitors may have very small equivalent series resistances and may thus require the addition of a low value series resistor to ensure stability.

**CAPACITOR SELECTION**

| PART NO. | MFR. | VALUE | MAX ESR† | SIZE (H × L × W)† |
|---|---|---|---|---|
| T494B475K016AS | Kemet | 4.7 μF | 1.5 Ω | 1.9 × 3.5 × 2.8 |
| 195D106x0016x2T | Sprague | 10 μF | 1.5 Ω | 1.3 × 7.0 × 2.7 |
| 695D106x003562T | Sprague | 10 μF | 1.3 Ω | 2.5 × 7.6 × 2.5 |
| TPSC475K035R0600 | AVX | 4.7 μF | 0.6 Ω | 2.6 × 6.0 × 3.2 |

† Size is in mm. The ESR maximum resistance is in Ohms at 100 kHz and $T_A$ = 25°C. Contact the manufacturer for the minimum ESR values.

## APPLICATION INFORMATION

### external capacitor requirements (continued)

The external bypass capacitor, used in conjunction with an internal resistor to form a low-pass filter, should be a low ESR ceramic capacitor. For example, the TPS78833 exhibits only 56 $\mu V_{RMS}$ of output voltage noise using a 0.01 μF ceramic bypass capacitor and a 10-μF ceramic output capacitor. Note that the output will start up slower as the bypass capacitance increases due to the RC time constant at the bypass pin that is created by the internal 150-kΩ resistor and external capacitor.

### power dissipation and junction temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, $P_D$, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}}$$

Where:

$T_J max$ is the maximum allowable junction temperature.

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, see the dissipation rating table.

$T_A$ is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = \left(V_I - V_O\right) \times I_O$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

### regulator protection

The TPS788xx PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS788xx features internal current limiting and thermal protection. During normal operation, the TPS78833 limits output current to approximately 350 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds approximately 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below approximately 140°C, regulator operation resumes.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS78825DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | PGZI | Samples |
| TPS78825DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | PGZI | Samples |
| TPS78833DBVR | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | PGTI | Samples |
| TPS78833DBVT | ACTIVE | SOT-23 | DBV | 5 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | 0 to 70 | PGTI | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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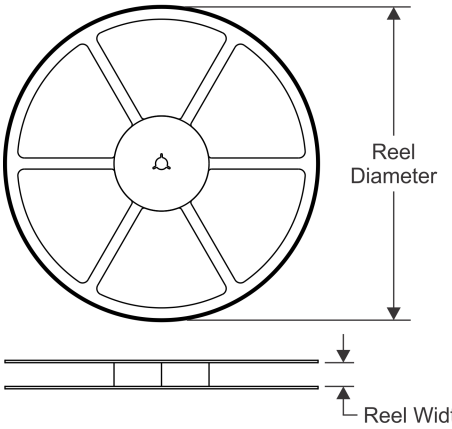
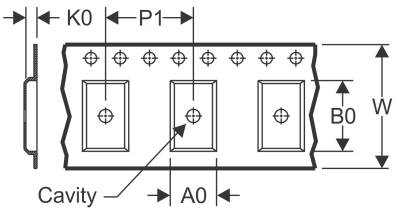
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

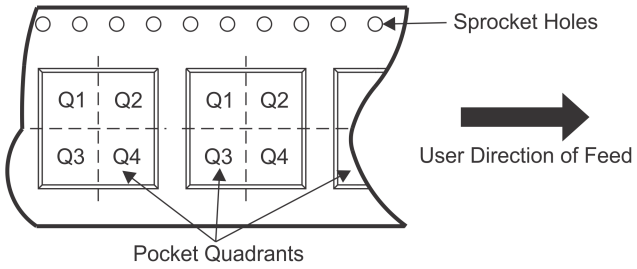



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

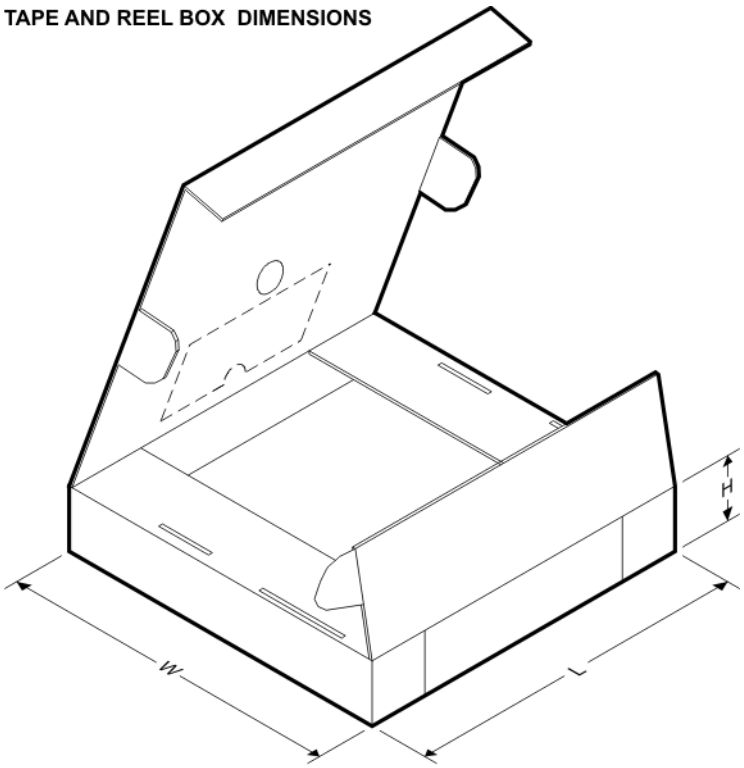
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TPS78825DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS78825DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 9.0 | 3.15 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS78833DBVR | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| TPS78833DBVT | SOT-23 | DBV | 5 | 250 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TPS78825DBVR | SOT-23 | DBV | 5 | 3000 | 182.0 | 182.0 | 20.0 |
| TPS78825DBVT | SOT-23 | DBV | 5 | 250 | 182.0 | 182.0 | 20.0 |
| TPS78833DBVR | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| TPS78833DBVT | SOT-23 | DBV | 5 | 250 | 210.0 | 185.0 | 35.0 |

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