TPS7A7002 具有使能端的极低输入、极低压降 3A 稳压器

1 特性

- 输入电压低至 1.425V
- 2A 时，最大压降 380mV
- 3A 时，最大压降 600mV
- 从 0.5V 开始的可调输出
- 保护：电流限制和热关断
- 启用引脚
- 关断模式下的接地电流为 1μA
- 完整工业温度范围
- 采用小外型尺寸集成电路 (SOIC)-8，完全 RoHS 标准兼容封装

2 应用

- 电信和网卡
- 主板和外设卡
- 工业应用
- 无线基础设施
- 机顶盒
- 医疗设备
- 笔记本电脑
- 电池供电系统

3 说明

TPS7A7002 是一款高性能、正电压、低压降 (LDO) 稳压器，针对 要求 在高达 3A 的电流下拥有超低输入电压和超低压降的应用而设计。该器件支持低至 1.425V 的单输入电压，输出电压最低可通过编程设置为 0.5V。输出电压可使用外部分压器进行设置。

TPS7A7002 具有 超低压降，非常 适用于 V_{OUT} 与 V_{IN} 极为接近的应用。此外， TPS7A7002 还有使能引脚以便在关断模式下进一步减少功率耗散。TPS7A7002 在线路、负载和温度变化时提供出色的稳压功能。

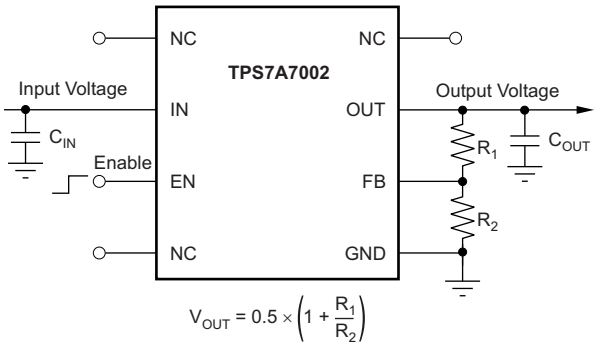
TPS7A7002 提供 8 引脚小型 PowerPAD™封装选项。

器件信息(1)

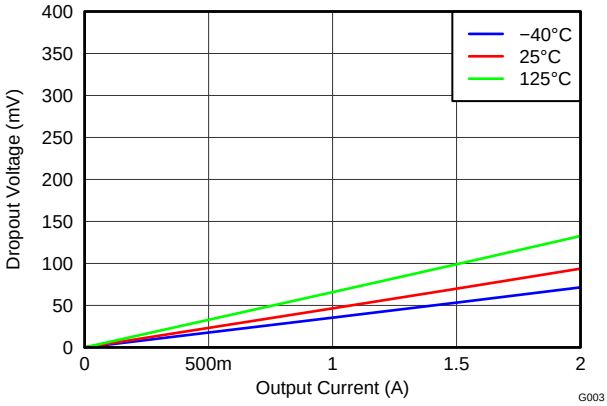
器件型号	封装	封装尺寸（标称值）
TPS7A7002	SO PowerPAD (8)	3.90mm x 4.89mm

(1) 要了解所有可用封装，请参见数据表末尾的封装选项附录。

典型应用



压降与输出电流间的关系
(V_{OUT} = 3.3V)



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision C (July 2015) to Revision D — **Page**

- Changed OUT pin description text from "TI recommends using at least a 4.7-μF ceramic capacitor, and up to 10 μF for a good transient response." to " A 4.7-μF or larger capacitor of any type is required for stability." for clarity ... 3
- Changed "operating free-air" to "junction" in *Absolute Maximum Ratings* table condition line ... 4
- Added rows for enable pin voltage, input capacitor, output capacitor, and feedforward capacitance to *Recommended Operating Conditions* table ... 4
- Added min value of 0 to output current in *Recommended Operating Conditions* table ... 4
- Changed note (1) in *Electrical Characteristics* table; deleted initial reference to R_1 and updated R_2 resistor range ... 5
- Changed *Output Capacitor (OUT)* section; reworded for clarity ... 9

Changes from Revision B (November 2013) to Revision C — **Page**

- 已添加 *ESD 额定值*表，*特性 描述*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分。 ... 1

Changes from Revision A (September 2013) to Revision B — **Page**

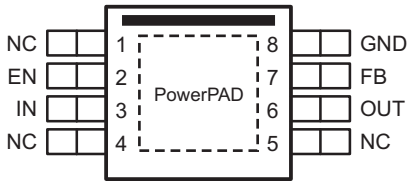
- 将数据表状态从产品预览改为生产数据 ... 1
- Added pin 1 identifier (black bar) to pinout diagram ... 3

Changes from Original (May 2013) to Revision A — **Page**

- Changed product preview data sheet ... 7

5 Pin Configuration and Functions

DDA Package
8-Pin SO PowerPAD
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	2	I	Enable input. Pulling this pin to less than 0.5 V turns the regulator off. Connect to V_{IN} if not being used.
FB	7	I	This pin is the output voltage feedback input through voltage dividers. See Table 2 for more details.
GND	8	—	Ground pin
IN	3	I	Input pin. Although it is not required for stability, TI recommends connecting a 1-μF to 10-μF capacitor with low equivalent series resistance (ESR) across this pin and GND.
NC	1, 4, 5	—	Not internally connected. The NC pins are not connected to any electrical node. TI recommends connecting the NC pins to large-area planes.
OUT	6	O	Regulated output pin. A 4.7-μF or larger capacitor of any type is required for stability.
PowerPAD	—	—	TI strongly recommends connecting the thermal pad to a large-area ground plane. If an electrically floating, dedicated thermal plane is available, the thermal pad can also be connected to it.

6 Specifications

6.1 Absolute Maximum Ratings

over junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	IN	–0.3	7	V
	EN, FB, OUT	–0.3	V_{IN} + 0.3(2)	
Current	OUT	Internally limited		A
Temperature	Operating virtual junction, T_J	–55	150	°C
	Storage temperature, T_{stg}	–55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The absolute maximum rating is V_{IN} + 0.3 V or 7 V, whichever is smaller.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	1.425		6.5	V
V_{EN}	Enable pin voltage	0		V_{IN}	V
C_{IN}	Input capacitor	1		10	µF
C_{OUT}	Output capacitor(1)(2)	4.7	10	200	µF
C_{FB}	Feedforward capacitance	0		100	nF
I_{OUT}	Output current	0		3	A
T_J	Junction temperature	–40		125	°C

(1) See Figure 1 and Figure 2 for additional output capacitor ESR requirements.
(2) For output capacitors larger than 47 µF, a feedforward capacitor of at least 220 pF must be used.

6.4 Thermal Information

THERMAL METRIC(1)		TPS7A7002 DDA (SO PowerPAD) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	46.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	29.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

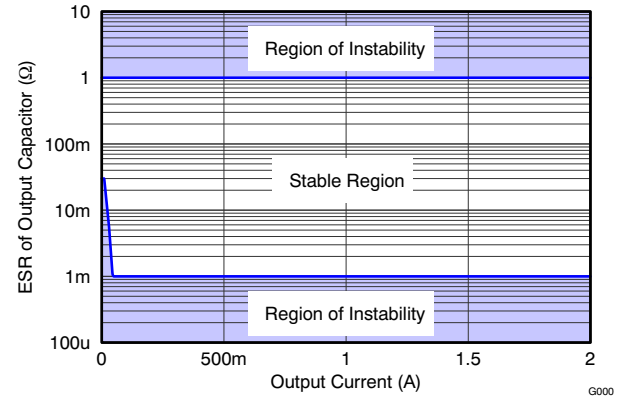
Over the full operating temperature range (see *Recommended Operating Conditions*), V_{EN} = 1.1 V, V_{FB} = V_{OUT}(1), 1.425 V ≤ V_{IN} ≤ 6.5 V, 10 µA ≤ I_{OUT} ≤ 3 A, C_{OUT} = 10 µF (unless otherwise noted). Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE						
I_{GND}	GND pin current	V_{IN} = 3.3 V, 50-Ω load resistor between OUT and GND			3	mA
	Shutdown GND pin current	V_{IN} = 6.5 V, V_{EN} = 0 V			5	µA
OUTPUT VOLTAGE						
V_{OUT}	Output voltage accuracy(2)(3)	V_{IN} = V_{OUT} + 0.5 V(4), I_{OUT} = 10 mA	–2%		2%	
		V_{IN} = 1.8 V, I_{OUT} = 0.8 A, 0°C ≤ T_J = T_A ≤ 85°C	–2%		2%	
		I_{OUT} = 10 mA	–3%		3%	
$\Delta V_{O(\Delta VI)}$	Line regulation	I_{OUT} = 10 mA		0.2	0.4	%/V
$\Delta V_{O(\Delta IO)}$	Load regulation(3)	10 mA ≤ I_{OUT} ≤ 3 A		0.25	0.75	%/A
V_{DO}	Dropout voltage (5)	I_{OUT} = 1 A, 0.5 V ≤ V_{OUT} ≤ 5 V			200	mV
		I_{OUT} = 2 A, 0.5 V ≤ V_{OUT} ≤ 5 V			380	
		I_{OUT} = 3 A, 0.5 V ≤ V_{OUT} ≤ 4.8 V			600	
I_{CL}	Output current limit	V_{IN} = 1.425 V, V_{OUT} = 0.9 × $V_{OUT(NOM)}$	3.36			A
FEEDBACK						
V_{REF}	Reference voltage accuracy	V_{IN} = 3.3 V, I_{OUT} = 10 mA	0.49	0.5	0.51	V
I_{FB}	FB pin current	V_{FB} = 0.5 V			1	µA
ENABLE						
I_{EN}	EN pin current	V_{EN} = 0 V, V_{IN} = 3.3 V			0.2	µA
$V_{EN(LO)}$	EN pin input low (disable)	V_{IN} = 3.3 V	0		0.5	V
$V_{EN(HI)}$	EN pin input high (enable)	V_{IN} = 3.3 V	1.1		V_{IN}	V
TEMPERATURE						
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		160		°C
		Reset, temperature decreasing		140		

(1) When setting V_{OUT} to a value other than 0.5 V, connect R_2 to the FB pin using 27-kΩ ≤ R_2 ≤ 33-kΩ resistors. See Figure 7 for details of R_1 and R_2.
(2) Accuracy does not include error on feedback resistors R_1 and R_2.
(3) TPS7A7002 is not tested at V_{OUT} = 0.5 V, 2.3 V ≤ V_{IN} ≤ 6.5 V, and 500 mA ≤ I_{OUT} ≤ 3 A because the power dissipation is higher than the maximum rating of the package. Also, this accuracy specification does not apply to any application condition that exceeds the power dissipation limit of the package.
(4) V_{IN} = V_{OUT} + 0.5 V or 1.425 V, whichever is greater.
(5) V_{DO} = V_{IN} – V_{OUT} with V_{FB} = GND configuration.

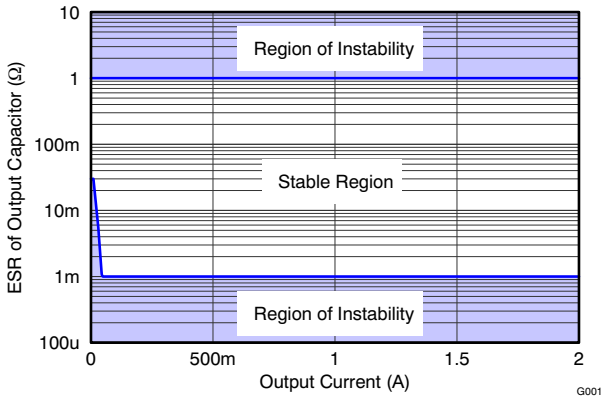
6.6 Typical Characteristics

for all fixed voltage versions and an adjustable version at T_J = 25°C, V_{EN} = V_{IN}, C_{IN} = 10 µF, C_{OUT} = 10 µF, and using the component values in Table 2 (unless otherwise noted)



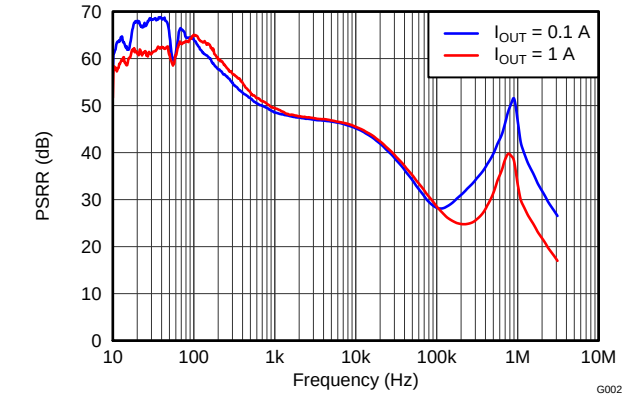
C_{OUT} = 10 µF

Figure 1. Stability Curve



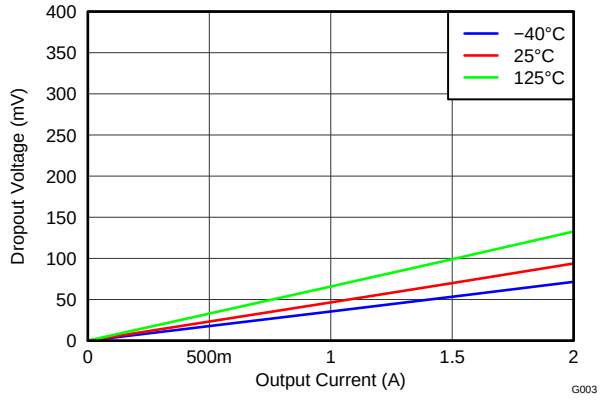
C_{OUT} = 100 µF

Figure 2. Stability Curve



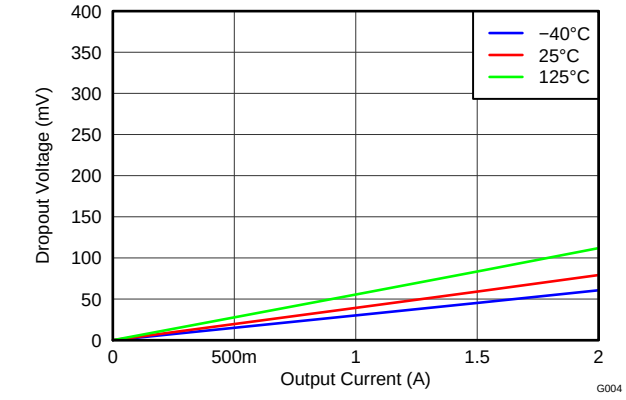
V_{IN} = 5 V, V_{OUT} = 3.3 V

Figure 3. Power-Supply Ripple Rejection vs Frequency



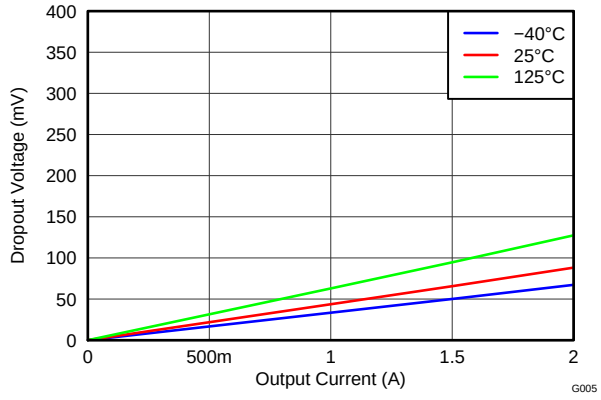
V_{OUT} = 3.3 V

Figure 4. Dropout Voltage vs Output Current



V_{OUT} = 1.6 V

Figure 5. Dropout Voltage vs Output Current



V_{OUT} = 1.4 V

Figure 6. Dropout Voltage vs Output Current

7 Detailed Description

7.1 Overview

The TPS7A7002 offers a high current supply with very-low dropout voltage. The TPS7A7002 is designed to minimize the required component count for a simple, small-size, and low-cost solution.

7.2 Functional Block Diagram

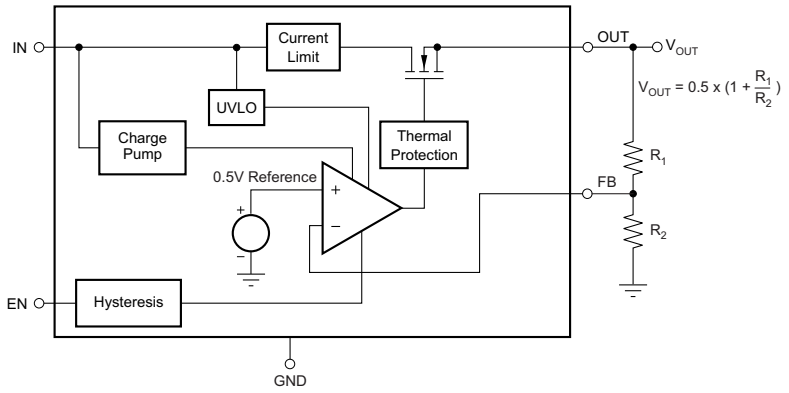


Figure 7. Adjustable Output Voltage Version

7.3 Feature Description

7.3.1 Internal Current Limit

The TPS7A7002 internal current limit helps protect the regulator during fault conditions. During a current limit condition, the output sources a fixed amount of current largely independent of output voltage. For reliable operation, do not operate the device in a current limit state for an extended period of time.

Powering on the device with the enable pin, or increasing the input voltage above the minimum operating voltage while a low-impedance short exists on the output of the device, may result in a sequence of high-current pulses from the input to the output of the device. The energy consumed by the device is minimal during these events; therefore, there is no failure risk. Additional input capacitance helps to mitigate the load transient requirement of the upstream supply during these events.

7.3.2 Enable (EN)

The enable pin (EN) is an active-high logic input. When it is logic low, the device turns off, and the consumption current is less than 1 µA. When it is logic high, the device turns on. The EN pin must be connected to a logic high or logic low level.

When the enable function is not required, connect EN to IN.

7.4 Device Functional Modes

Table 1 provides a quick comparison between the normal, dropout, and disabled modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	EN	I_{OUT}	T_J
Normal	$V_{IN} > V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$
Dropout	$V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(HI)}$	$I_{OUT} < I_{CL}$	$T_J < T_{SD}$
Disabled	—	$V_{EN} < V_{EN(LO)}$	—	$T_J > T_{SD}$

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)} + V_{DO}$).
- The enable voltage has previously exceeded the enable rising threshold voltage and not yet decreased below the enable falling threshold.
- The output current is less than the current limit ($I_{OUT} < I_{CL}$).
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD}$).

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. During this mode, the transient performance of the device becomes significantly degraded because the pass device is in a triode state and no longer controls the current through the LDO. Line or load transients in dropout can result in large output-voltage deviations.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7A7002 offers a high current supply with very-low dropout voltage, and it is designed to minimize the required component count for a simple, small-size, and low-cost solution. This section discusses the implementation of the TPS7A7002 LDO.

8.1.1 Input Capacitor (IN)

An input capacitor is not required for stability; however, TI recommends connecting a 1-µF to 10-µF low equivalent series resistance (ESR) capacitor across IN and GND as close as possible to the device.

8.1.2 Output Capacitor (OUT)

The TPS7A7002 is stable with standard ceramic capacitors with capacitance values from 4.7 µF to 47 µF without a feedforward capacitor. For output capacitors from 47 µF to 200 µF, a feedforward capacitor of at least 220 pF must be used. The TPS7A7002 is evaluated using an X5R-type, 10-µF ceramic capacitor. X5R- and X7R-type capacitors are recommended because of minimal variation in value and ESR over temperature. Maximum ESR must be less than 1 Ω.

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude, but increases duration of the transient response.

8.1.3 Feedback Resistors (FB)

The voltage on the FB pin sets the output voltage and is determined by the values of R1 and R2. Use Equation 1 to calculate the values of R_1 and R_2 for any voltage.

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) \quad (1)$$

Table 2 shows the recommended resistor values for the best performance of the TPS7A7002. If the values in Table 2 are not used, keep the value of R_2 from 27 kΩ to 33 kΩ. In Table 2, E96 series resistors are used. For the actual design, pay attention to any resistor error factors.

Table 2. Sample Resistor Values for Common Output Voltages

V_{OUT}	R_1 (kΩ)	R_2 (kΩ)
1	30.1	30.1
1.2	42.2	30.1
1.5	60.4	30.1
1.8	78.7	30.1
2.5	121	30.1
3	150	30.1
3.3	169	30.1
5	274	30.1

8.2 Typical Application

This section describes the implementation of the TPS7A7002, using the feedback pin to configure the output voltage and regulate a 2-A load at 1.4 V using a 1.6-V input voltage, operating in a temperature range of 25°C to 85°C. Figure 8 shows the schematic for this typical application circuit.

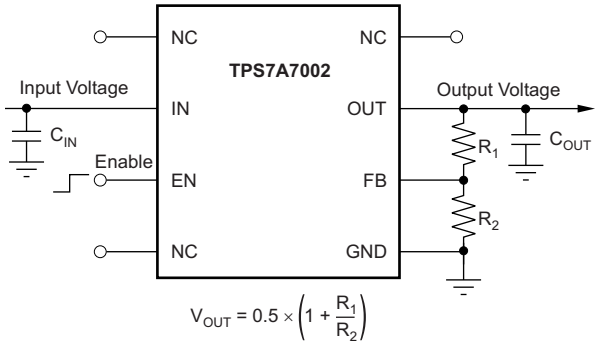


Figure 8. Typical Application Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 3 as the input parameters.

Table 3. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	1.6 V ±3%
Output voltage	1.4 V ±3%
Maximum output current	2 A
Ambient temperature	25°C ≤ T_A ≤ 75°C

8.2.2 Detailed Design Procedure

At I_{OUT} = 2 A, the TPS7A7002 has a maximum dropout of less than 150 mV over temperature, as seen in Figure 9; thus, a 200-mV headroom is sufficient for operation over both input and output voltage accuracy.

To achieve 1.2 V on the output, choose the correct feedback resistors. The *Feedback Resistors (FB)* section suggests keeping the value of R_2 in the range of 27 kΩ to 33 kΩ, so select R_2 to be 30.1 kΩ, a standard resistor in the E96 series. Using Equation 1 to achieve a 1.4-V output, determine the size for R_1 using Equation 2.

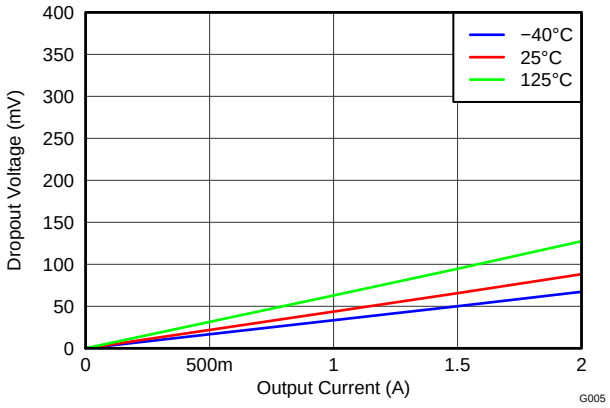
$$R_1 = ((2 \times V_{OUT}) - 1) \times R_2 \quad (2)$$

Given that R_2 = 30.1 kΩ and V_{OUT} = 1.4 V, R_1 = 54.2 kΩ. The closest resistor in the E96 series is 53.6 kΩ, giving an output voltage within the output design requirements.

With a headroom voltage of 200 mV and a 2-A maximum load, the internal power dissipation is 400 mW, and corresponds to a 18.56°C junction temperature rise for the DDA package.

With a 75°C maximum ambient temperature as per design constraints, the junction temperature is at 93.56°C, and satisfies the recommended operating junction temperature range.

8.2.3 Application Curve



V_{OUT} = 1.4 V

Figure 9. Dropout Voltage vs Output Current

9 Power Supply Recommendations

These devices are designed to operate from an input voltage supply range from 1.425 V to 6.5 V. The input voltage range provides adequate headroom for the device to have a regulated output. This input supply is well regulated and stable. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

For best performance, place all circuit components on the same side of the circuit board, and place the external components as close to the device as practically possible. The use of vias and long traces is strongly discouraged because of parasitics that might affect performance; follow these guidelines to minimize parasitics. Also, embed a ground reference plane to maintain accuracy of the output voltage and shield noise. Make sure that this plane is connected to the PowerPAD in order to help spread (or sink) heat from the device; be aware that NC pins might be connected to this plane. The recommended layout is shown in Figure 10.

10.2 Layout Example

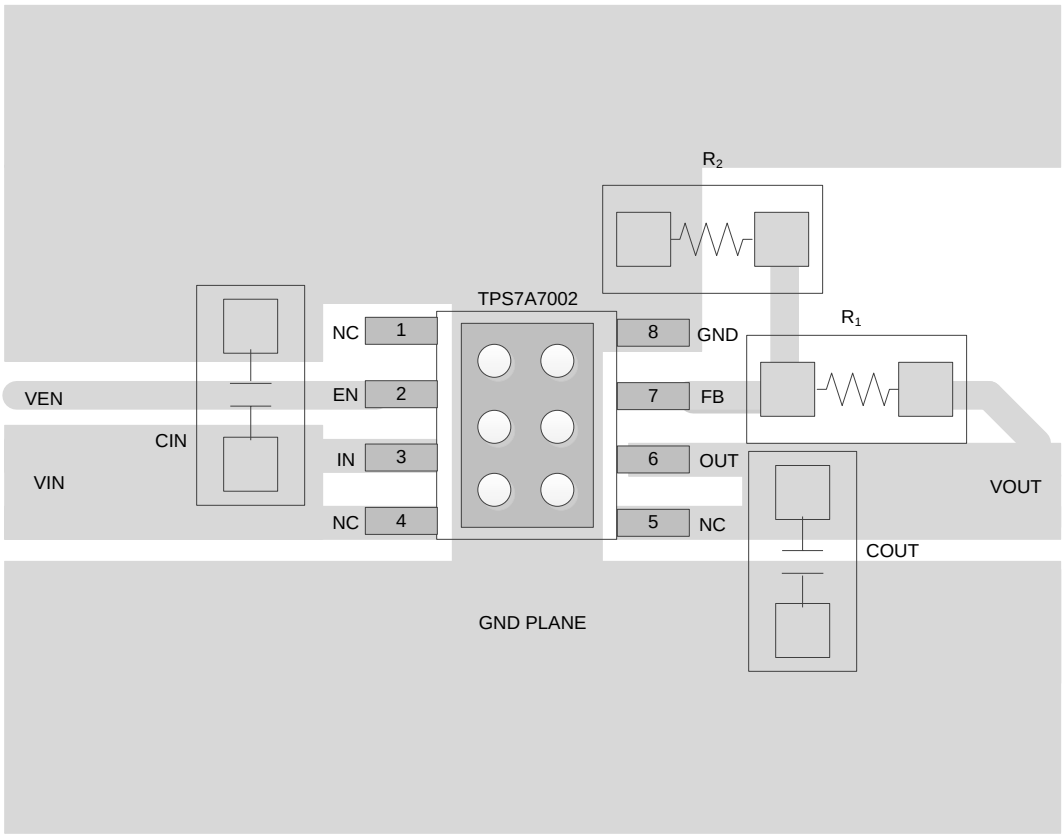


Figure 10. Layout Recommendation

10.3 Thermal Consideration

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is re-enabled.

The internal protection circuitry of the TPS7A7002 is designed to protect against overload conditions. The protection circuitry is not intended to replace proper heat sinking. Continuously running the TPS7A7002 into thermal shutdown degrades device reliability.

10.4 Power Dissipation

Power dissipation (P_D) of the device depends on the input voltage and load conditions, and is calculated using Equation 3.

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{3}$$

In order to minimize power dissipation and achieve greater efficiency, use the lowest possible input voltage necessary to achieve the required output voltage regulation

On the SOIC (DDA) package, the primary conduction path for heat is through the exposed pad to the PCB. The pad can either be connected to ground or left floating; however, attach the pad to an appropriate amount of copper PCB area to prevent the device from overheating. The maximum junction-to-ambient thermal resistance depends on the maximum ambient temperature, maximum device junction temperature, and power dissipation of the device, and is calculated using Equation 4:

$$R_{\theta JA} = \left(\frac{+125°C - T_A}{P_D} \right) \tag{4}$$

11 器件和文档支持

11.1 器件支持

11.1.1 器件命名规则

产品(1)	说明
TPS7A7002**yyyz**	YYY 为封装标识符。 Z 为封装数量。

(1) 要获得最新的封装和订货信息，请参阅本文档末尾的封装选项附录，或者访问器件产品文件夹，此文件夹位于www.ti.com内。

11.2 文档支持

11.2.1 相关文档

相关文档如下：

- *TI LDO 应用手册的主题索引*
- *半导体和集成电路 (IC) 封装热度量*

11.3 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

11.4 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 商标

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A7002DDA	ACTIVE	SO PowerPAD	DDA	8	75	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	SJA	Samples
TPS7A7002DDAR	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	SJA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

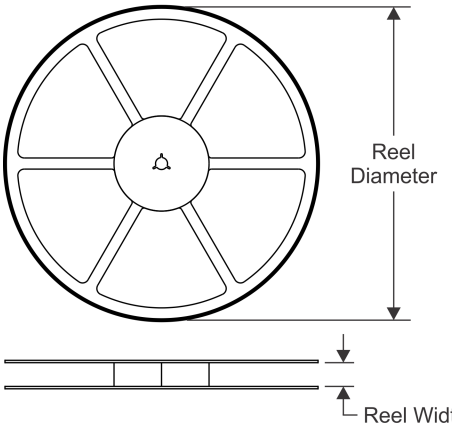
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

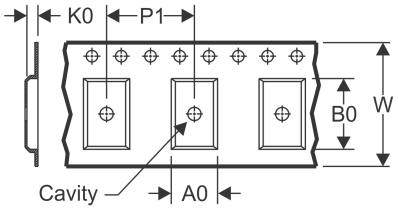
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

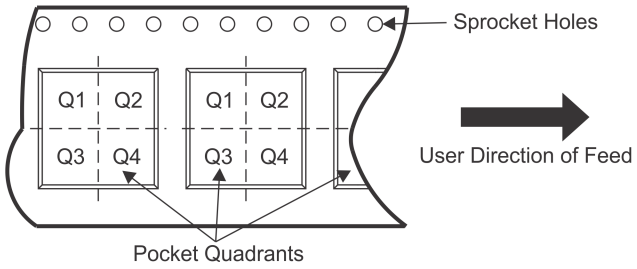


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

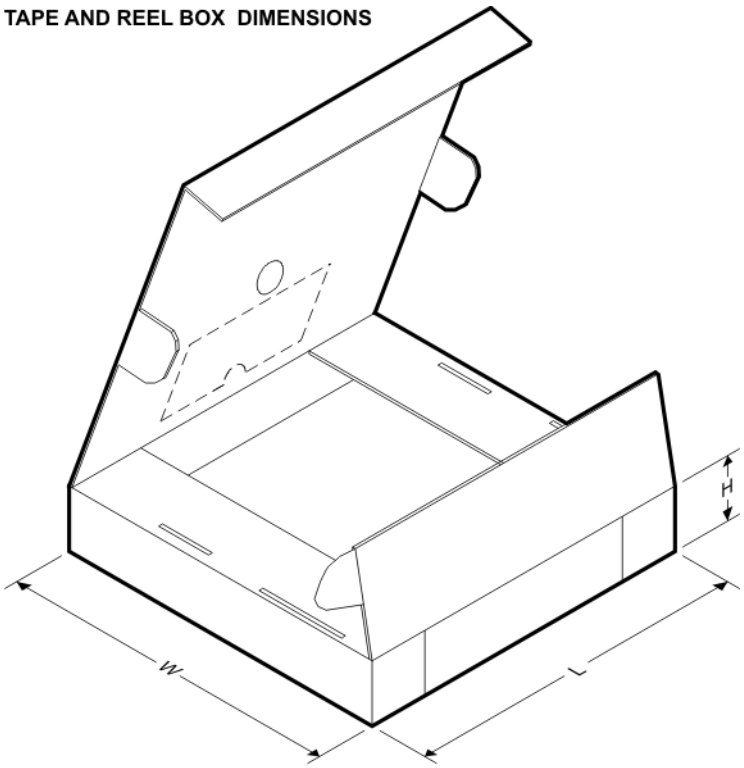
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A7002DDAR	SO Power PAD	DDA	8	2500	330.0	12.8	6.4	5.2	2.1	8.0	12.0	Q1

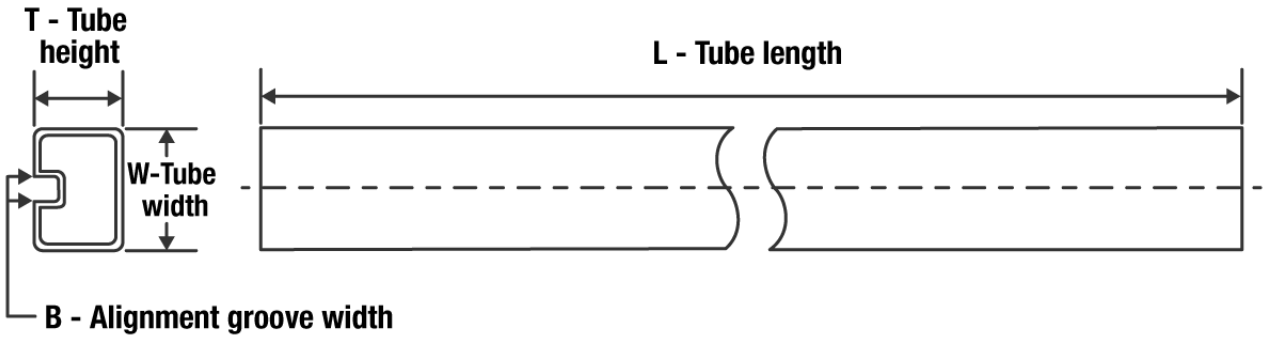
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A7002DDAR	SO PowerPAD	DDA	8	2500	366.0	364.0	50.0

TUBE

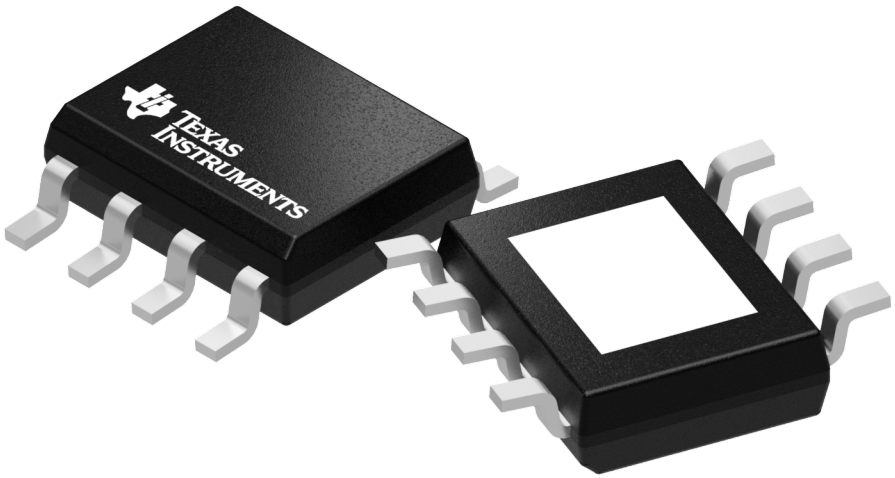


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS7A7002DDA	DDA	HSOIC	8	75	517	7.87	635	4.25

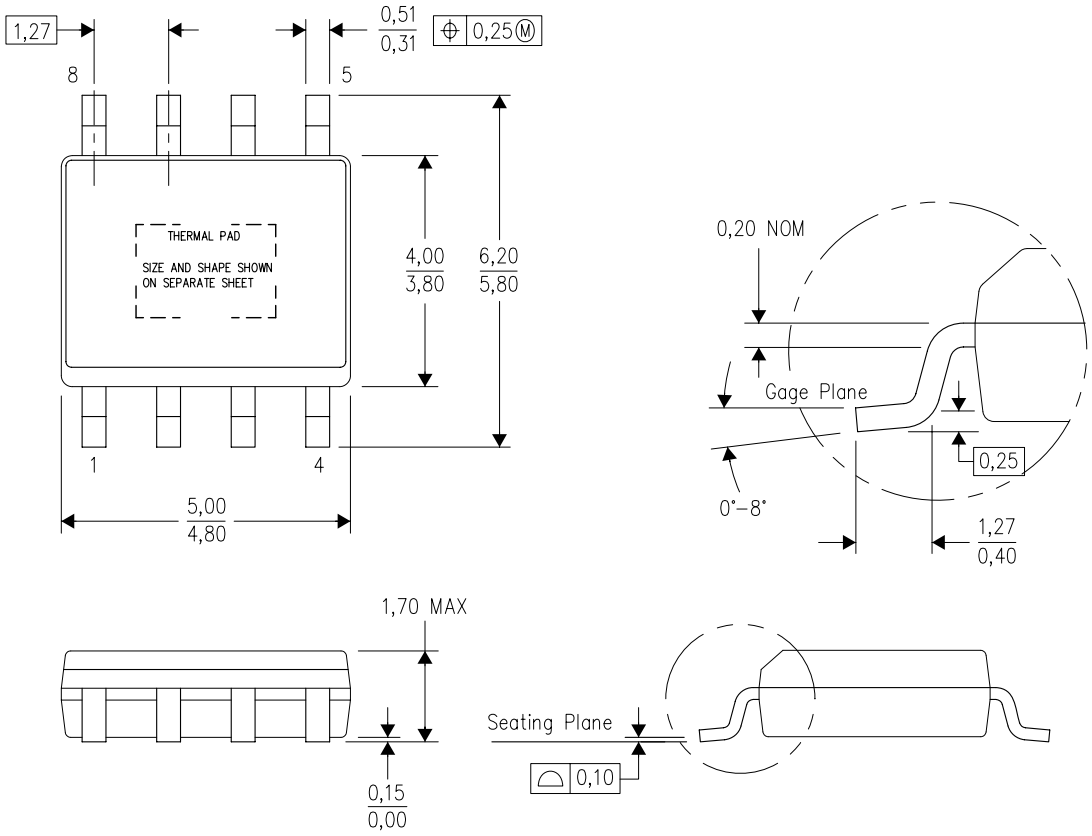
DDA 8 PowerPAD™ SOIC - 1.7 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

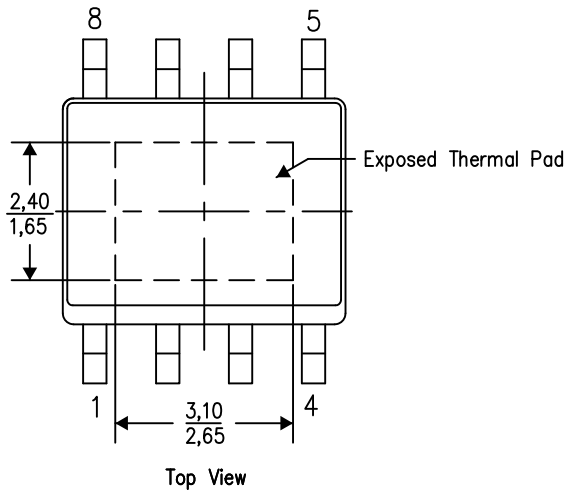
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



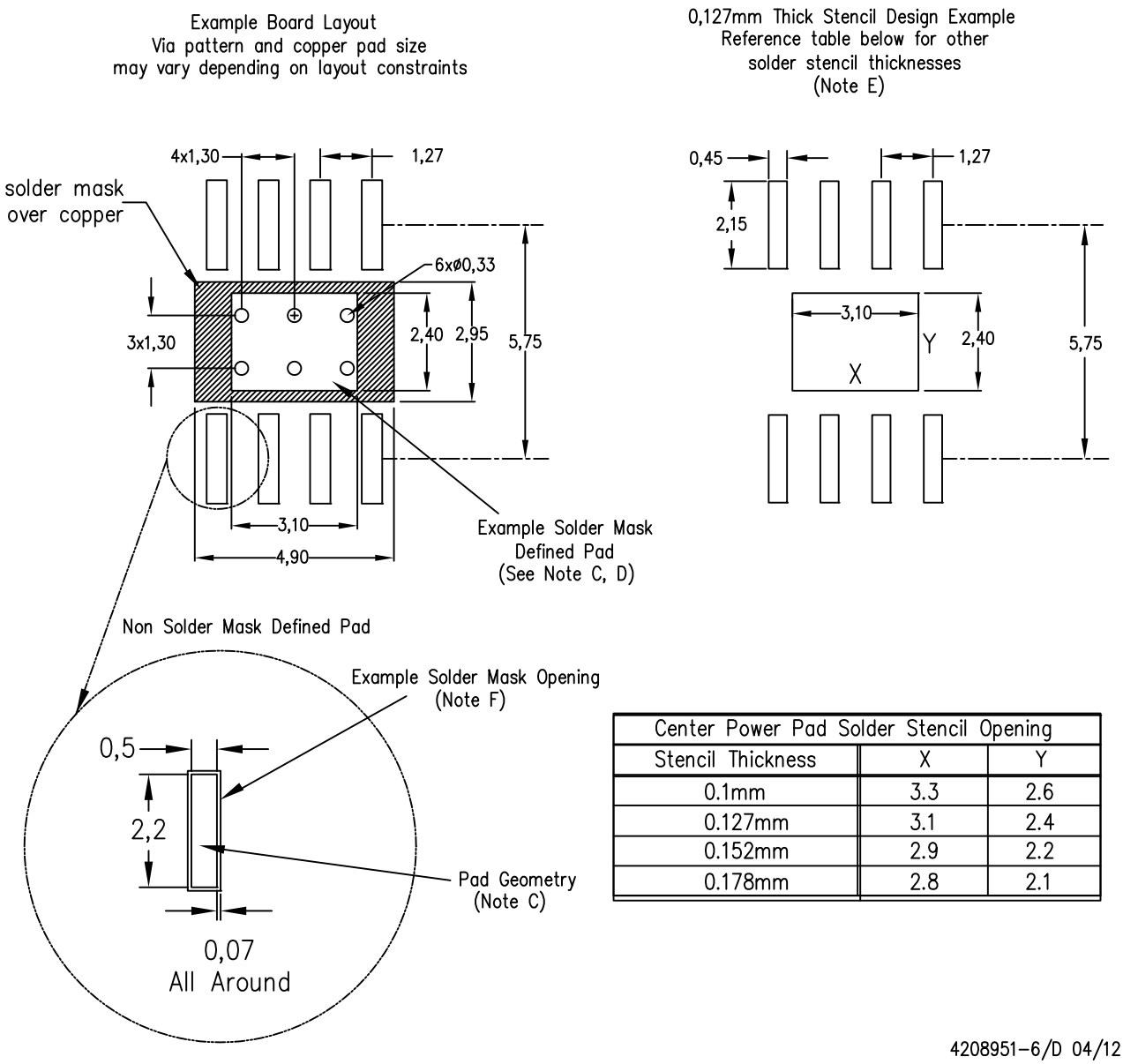
Exposed Thermal Pad Dimensions

4206322–6/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.3	2.6
0.127mm	3.1	2.4
0.152mm	2.9	2.2
0.178mm	2.8	2.1

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

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