TPS7H1201-HT 1.5V 至 7V 输入、超低压差 (LDO) 稳压器

1 特性

- 较宽的输入电压范围：1.5V 至 7V
- 电流共享/并联工作可提供较高 的输出电流
- 与陶瓷输出电容一起工作时保持稳定
- 线路、负载和温度范围内的精度为 ±4.2%
- 可编程软启动
- 电源正常输出
- LDO 电压：
  0.5A (210°C)、V_{OUT} = 6.8V 时为 100mV（最大值）
- 低噪声：
  V_{IN} = 2.1V、V_{OUT} = 1.8V、电流为 0.5A 时为 20.26 μVRMS
- 电源抑制比 (PSRR)：1kHz 频率下超过 45dB
- 负载/线路瞬态响应
- 请参见工具和软件 (Tools & Software) 选项卡

2 应用

- 射频 5V 组件压控振荡器、接收器、模数转换器、放大器
- 时钟分配
- 洁净模拟电源需求
- 支持恶劣环境中的 应用
- 可用于极限温度范围，即 –55°C 至 210°C(1)
- TI 的高温产品采用高度优化的硅（裸片）解决方案，通过改进设计和制造工艺，最大限度提升在更大温度范围内的性能

3 说明

TPS7H1201-HT 是一款采用 PMOS 导通元件配置的 LDO 线性稳压器。此器件可在 1.5V 至 7V 的宽输入电压范围内运行，同时提供出色的 PSRR。

TPS7H1201-HT 通过 极宽的调节范围实现了精确的可编程折返电流限值功能。为了满足 FPGA、DSP 或微控制器的复杂电源要求，TPS7H1201-HT 提供使能导通和关断功能、可编程软启动、电流共享功能以及电源正常开漏输出。

TPS7H1201-HT 采用 16 引脚耐热增强型陶瓷扁平封装 (CFP) 和 KGD（裸片）封装。

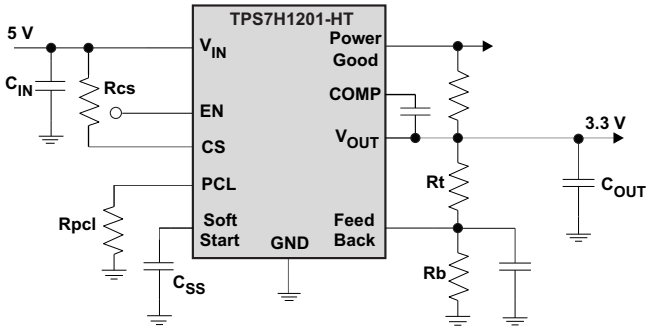
器件信息(2)

器件型号	封装	封装尺寸（标称值）
TPS7H1201-HT	CFP (16)	11.00mm x 9.60mm

(1) 支持定制温度范围

(2) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用电路



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision I (January 2016) to Revision J — **Page**

- Changed output voltage MAX from V_{IN} : to 7.5 V in *Absolute Maximum Ratings* table ... 6
- Deleted peak output current spec in *Absolute Maximum Ratings* table ... 6
- Added rise time specifications for EN and VIN signals in *Recommended Operating Conditions* table ... 6
- Added test conditions to V_{ILEN} and V_{IHEN} in the *Electrical Characteristics* table ... 7
- 已添加 *接收文档更新通知* 部分添加到*器件和文档支持*部分 ... 26
- 已添加 *器件命名规则* 部分添加到*器件支持*部分（以前位于 *机械、封装和可订购信息* 部分） ... 26
- 已更改 *相关文档*部分列出的文档 ... 26

Changes from Revision H (December 2014) to Revision I — **Page**

- 已删除数据表中的部件编号 ... 1
- Corrected the thermal values for $R_{\theta JB}$ ... 6
- Removed the ψ_{JT} thermal metric ... 6

Changes from Revision G (January 2014) to Revision H — **Page**

- 已添加 *ESD 额定值*表，*特性 说明*部分、*器件功能模式*、*应用和实施*部分、*电源相关建议*部分、*布局*部分、*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1

Changes from Revision F (December 2013) to Revision G — **Page**

- Added Bare Die Information ... 4

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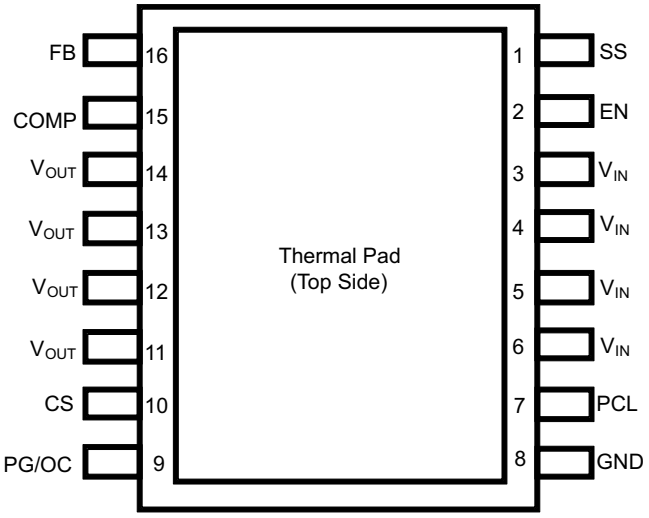
5 Pin Configuration and Functions

HKS Package
16-Pin CFP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
SS	1	O	Soft-start terminal. Connecting an external capacitor slows down the output voltage ramp rate after enable event. The soft-start terminal can be used to disable the device as described in the *Soft Start* section.
EN	2	I	Enable terminal. Driving this terminal to logic high enables the device; driving the terminal to logic low disables the device. V_{IN} voltage must be greater than 3.5 V when using the EN pin. For V_{IN} < 3.5 V, enable terminal cannot be used to disable the device. TI recommends to connect the enable terminal to V_{IN}.
V_{IN}	3	I	Unregulated supply voltage. TI recommends to connect an input capacitor as a good analog circuit practice.
	4		
	5		
	6		
PCL	7	O	Programmable current limit. A resistor to GND sets the overcurrent limit activation point. The range of resistor that can be used on the PCL terminal to GND is 47 kΩ to 160 kΩ.
GND	8	—	Ground/thermal pad. (1)
PG/OC	9	O	Power Good terminal. PG is an open-drain output to indicate the output voltage reaches 90% of target. PG terminal is also used as indicator when an overcurrent condition is activated. PG pin should have a pull-up resistor to the V_{OUT} pin.
CS	10	O	Current sense terminal. Resistor connected from CS to V_{IN}. CS terminal indicates voltage proportional to output current.
V_{OUT}	11	O	Regulated output.
	12		
	13		
	14		
COMP	15	I	Internal compensation point for error amplifier.
FB	16	I	The output voltage feedback input through voltage dividers. See *Adjustable Output Voltage (Feedback Circuit)* section.

(1) Thermal pad must be connected to GND.

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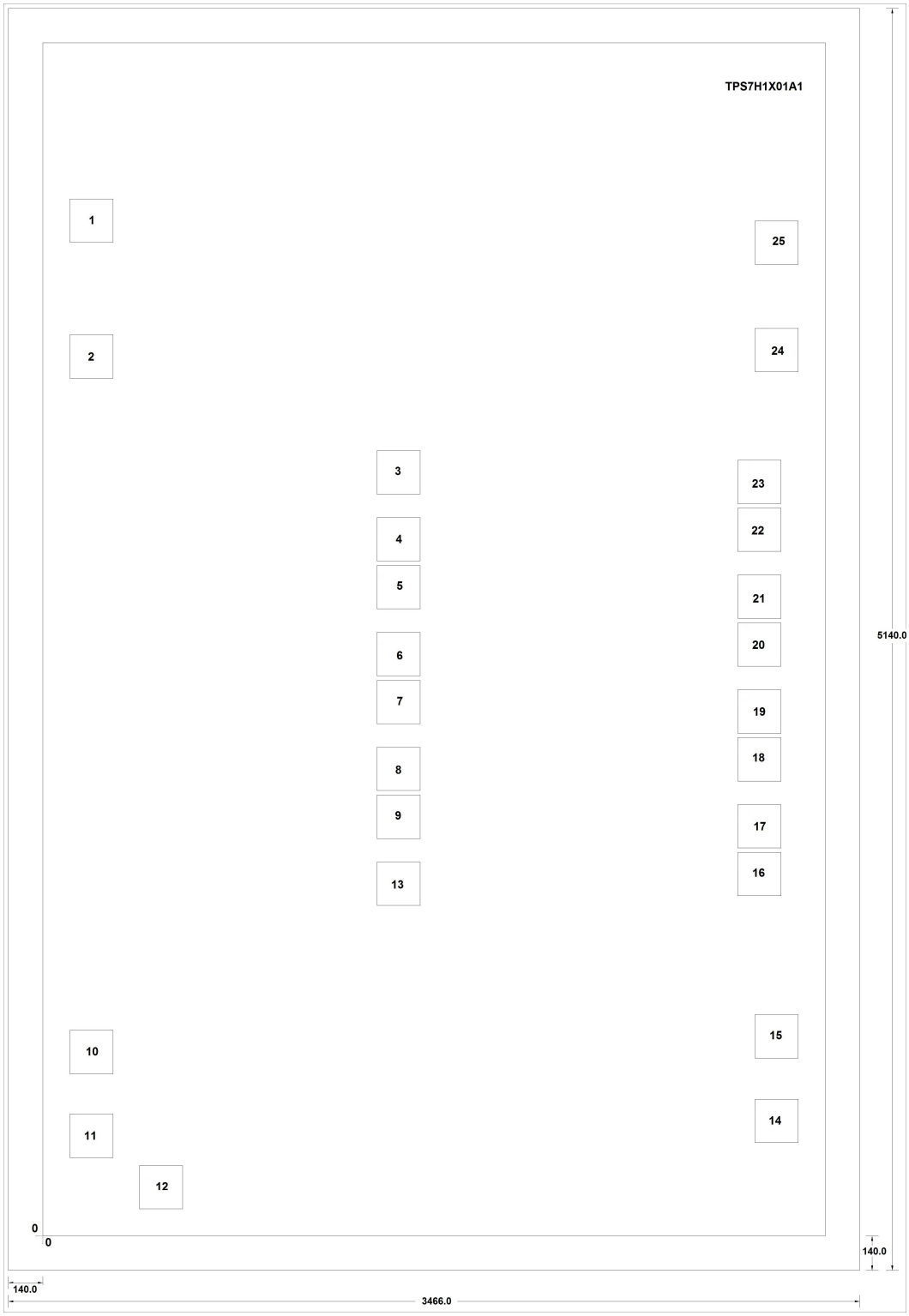
Bare Die Information

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
15 mils	Silicon with backgrind	Ground	AlCu	30 kA



NOTE: All dimensions are in microns.

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Bond Pad Coordinates in Microns

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
SS	1	109.89	4046.805	287.19	4224.105
EN	2	109.89	3493.35	287.19	3670.65
VIN	3	1359.99	3021.345	1537.29	3198.645
VIN	4	1359.99	2749.005	1537.29	2926.305
VIN	5	1359.99	2553.705	1537.29	2731.005
VIN	6	1359.99	2281.365	1537.29	2458.665
VIN	7	1359.99	2086.065	1537.29	2263.365
VIN	8	1359.99	1813.725	1537.29	1991.025
VIN	9	1359.99	1618.425	1537.29	1795.725
PCL	10	109.89	660.285	287.19	837.585
GND	11	109.89	319.455	287.19	496.755
N/C	12	392.58	109.935	569.88	287.235
VIN	13	1359.99	1346.085	1537.29	1523.385
PG/OC	14	2898.945	379.62	3076.245	556.92
CS	15	2898.945	724.32	3076.245	901.62
VOUT	16	2829.105	1384.695	3006.405	1561.995
VOUT	17	2829.105	1579.815	3006.405	1757.115
VOUT	18	2829.105	1852.335	3006.405	2029.635
VOUT	19	2829.105	2047.455	3006.405	2224.755
VOUT	20	2829.105	2319.975	3006.405	2497.275
VOUT	21	2829.105	2515.095	3006.405	2692.395
VOUT	22	2829.105	2787.615	3006.405	2964.915
VOUT	23	2829.105	2982.735	3006.405	3160.035
COMP	24	2898.945	3519.72	3076.245	3697.02
FB	25	2898.945	3956.535	3076.245	4133.835

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	V_{IN}, PG	–0.3	7.5	V
	FB, COMP, PCL, CS, EN	–0.3	V_{IN} + 0.3	V
Output voltage	V_{OUT}, SS	–0.3	7.5	V
PG terminal sink current		0.001	5	mA
Maximum operating junction temperature, T_J		–55	220	°C
Storage temperature, T_{stg}		–55	220	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_J	Operating junction temperature	–55		210	°C
t_R EN	Rise time (10% to 90%) for EN signal	100			µs
t_R VIN	Rise time (10% to 90%) for VIN = EN	1			ms

6.4 Thermal Information

THERMAL METRIC(1)(2)		TPS7H1201-HT HKS (CFP)(3) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	75.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	64.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	53.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) Maximum power dissipation may be limited by overcurrent protection.
(2) Test board conditions:
  (a) 2.5 inches × 2.5 inches, 4 layers, thickness: 0.062 inch
  (b) 2-oz. copper traces located on the top of the PCB
  (c) 2-oz. copper ground planes on the 2 internal layers and bottom layer
  (d) 48 (0.010-inch) thermal vias located under the device package
(3) Power rating at a specific ambient temperature T_A should be determined with a junction temperature below 220°C. This is the point where distortion starts to substantially increase. Thermal management of the PCB should strive to keep the junction temperature at or below 220°C for best performance and long-term reliability.

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6.5 Electrical Characteristics

1.5 V ≤ V_{IN} ≤ 7 V, $V_{OUT(target)}$ = V_{IN} – 0.3 V, I_{OUT} = 10 mA, V_{EN} = 1.1 V, C_{OUT} = 22 µF, PG terminal pulled up to V_{IN} with 50 kΩ, over operating temperature range (T_J = –55°C to 210°C), unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range			1.5		7	V
V_{FB}	Feedback terminal voltage	1.5 V ≤ V_{IN} ≤ 7 V	T_J = 125°C	0.593	0.605	0.617	V
			T_J = 210°C	0.580	0.605	0.630	
V_{OUT}	Output voltage range			0.8		V_{IN} – 0.2	V
	Output voltage accuracy	I_{OUT} ≤ 0.5 A, 1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 6.8 V(1)	T_J = 125°C	–2%		2%	
			T_J = 210°C	–4.2%		4.2%	
ΔV_{OUT}% / ΔV_{IN}	Line regulation	1.5 V ≤ V_{IN} ≤ 7 V		–0.07	0.01	0.07	%/V
ΔV_{OUT}% / ΔI_{OUT}	Load regulation	0.8 V ≤ V_{OUT} ≤ 6.8 V, 0 ≤ I_{Load} ≤ 0.5 A			0.0125		%/A
ΔV_O	DC input line regulation	1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 0.8 V, I_{OUT} = 10 mA, T_J = –55°C(2)			0.5	3	mV
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 0.8 V, I_{OUT} = 10 mA, T_J = 25°C(2)			0.2	0.6	
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 0.8 V, I_{OUT} = 10 mA, T_J = 125°C(2)			0.2	1	
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 0.8 V, I_{OUT} = 10 mA, T_J = 210°C(2)			0.84	3	
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 1.2 V, I_{OUT} = 10 mA, T_J = –55°C(2)			0.5	3	
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 1.2 V, I_{OUT} = 10 mA, T_J = 25°C(2)			0.2	0.6	
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 1.2 V, I_{OUT} = 10 mA, T_J = 125°C(2)			0.2	1	
		1.5 V ≤ V_{IN} ≤ 7 V, V_{OUT} = 1.2 V, I_{OUT} = 10 mA, T_J = 210°C(2)			0.84	3	
ΔV_O	DC output load regulation	V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 0.5 A, T_J = –55°C(2)			0.05		mV
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 0.5 A, T_J = 25°C(2)			0.05		
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 0.5 A, T_J = 125°C(2)			0.07		
		V_{OUT} = 0.8 V, 0 ≤ I_{Load} ≤ 0.5 A, T_J = 210°C(2)			0.51		
		V_{OUT} = 6.8 V, 0 ≤ I_{Load} ≤ 0.5 A, T_J = –55°C(2)			0.10		
		V_{OUT} = 6.8 V, 0 ≤ I_{Load} ≤ 0.5 A, T_J = 25°C(2)			0.04		
		V_{OUT} = 6.8 V, 0 ≤ I_{Load} ≤ 0.5 A, T_J = 125°C(2)			0.05		
		V_{OUT} = 6.8 V, 0 ≤ I_{Load} ≤ 0.5 A, T_J = 210°C(2)			0.47		
V_{DO}	Dropout voltage	I_{OUT} = 0.5 A, V_{OUT} = 6.8 V, V_{IN} = V_{OUT} + 0.1 V			55.5	100	mV
I_{CL}	Programmable output current limit range	V_{IN} = 1.5 V, V_{OUT} = 1.2 V, PCL resistance = 47 kΩ		500		700	mA
		V_{IN} = 1.5 V, V_{OUT} = 1.2 V , PCL resistance varies		200		700	
V_{CS}	Operating voltage range at CS			0.3		V_{IN}	V
CSR	Current sense ratio	I_{LOAD} / $I_{CS,}$ V_{IN} = 2.3 V, V_{OUT} = 1.9 V			47394		
I_{GND}	GND terminal current	V_{IN} = 1.5 V, V_{OUT} = 1.2 V, I_{OUT} = 0.5 A			13	20	mA
I_Q	Quiescent current (no load)	V_{IN} = V_{OUT} + 0.5 V, I_{OUT} = 0 A			12	17	mA
I_{SHDN}	Shutdown current	V_{EN} < 0.5 V, 0.8 V ≤ V_{IN} ≤ 7 V			15	4500	µA
I_{SNS}, I_{FB}	FB/SNS terminal current	V_{IN} = 7 V, V_{OUT} = 6.8 V			1	10	nA
I_{EN}	EN terminal input current	V_{IN} = 7 V, V_{EN} = 7 V			6.75	610	nA
V_{ILEN}	EN terminal input low (disable)	3.5 V < V_{IN} < 7 V			0.30 × V_{IN}		V

(1) Based upon using 0.1% resistors.
(2) Line and load regulations done under pulse condition for T < 10 ms.

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Electrical Characteristics (continued)

1.5 V ≤ V_{IN} ≤ 7 V, $V_{OUT(target)}$ = V_{IN} – 0.3 V, I_{OUT} = 10 mA, V_{EN} = 1.1 V, C_{OUT} = 22 µF, PG terminal pulled up to V_{IN} with 50 kΩ, over operating temperature range (T_J = –55°C to 210°C), unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IHEN}	EN terminal input high (enable)	3.5 V < V_{IN} < 7 V			0.75 × V_{IN}		V
Eprop Dly	Enable terminal propagation delay	V_{IN} = 2.2 V, EN rise to I_{OUT} rise			650	1000	µs
T_{EN}	Enable terminal turn-on delay	V_{IN} = 2.2 V, V_{OUT} = 1.8 V, I_{LOAD} = 0.5 A, C_{OUT} = 220 µF, C_{SS} = 2 nF			1.4	1.6	ms
V_{THPG}	PG threshold on	No load,V_{OUT} = 1.2 V and V_{OUT} = 6.8 V		84%	90%		
$V_{THPGHYS}$	PG hysteresis	1.5 V ≤ V_{IN} ≤ 7 V			2%		
V_{OLPG}	PG terminal output low	I_{PG} = 0 mA to –1 mA			73	300	mV
I_{LKGPG}	PG terminal leakage current	V_{OUT} > V_{THPG}, V_{PG} = 7 V			0.02	20	µA
I_{SS}	SS terminal current	V_{IN} = 1.5 V to 7 V			2.5	6.3	µA
I_{SSdisb}	SS terminal disable current	V_{IN} = 1.5 V to 7 V			5	13	µA
V_{SS}	SS terminal voltage (device enabled)	V_{IN} = 1.5 V to 7 V				1.2	V
PSRR	Power-supply rejection ratio	V_{IN} = 2.5 V, V_{OUT} = 1.8 V, C_{OUT} = 220 µF	1 kHz		45		dB
			100 kHz		20		
V_N	Output noise voltage	BW = 10 Hz to 100 kHz, I_{OUT} = 500 mA, V_{IN} = 2 V, V_{OUT} = 1.8 V			20.26		$µV_{RMS}$
T_J	Operating junction temperature			–55		210	°C

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6.6 Typical Characteristics

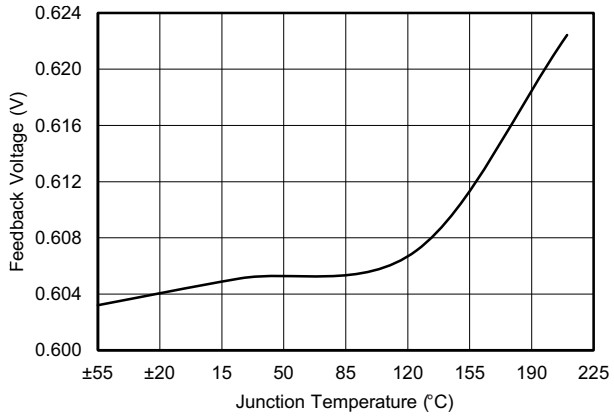

Figure 1. Feedback Voltage vs Temperature

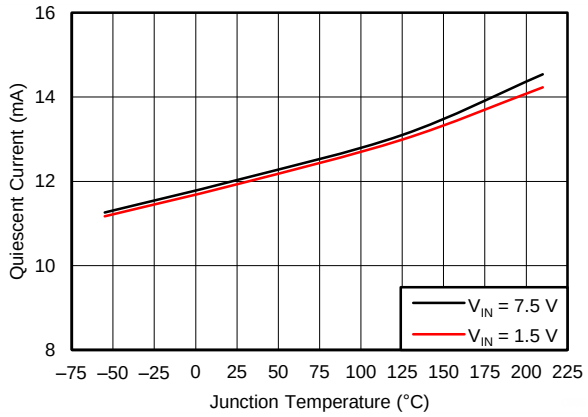

Figure 2. Quiescent Current vs Temperature

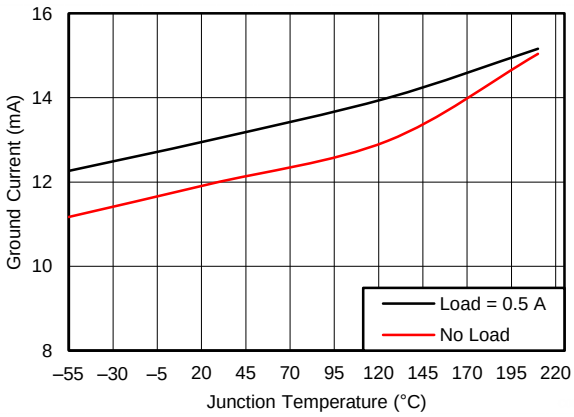

Figure 3. Ground Current vs Temperature

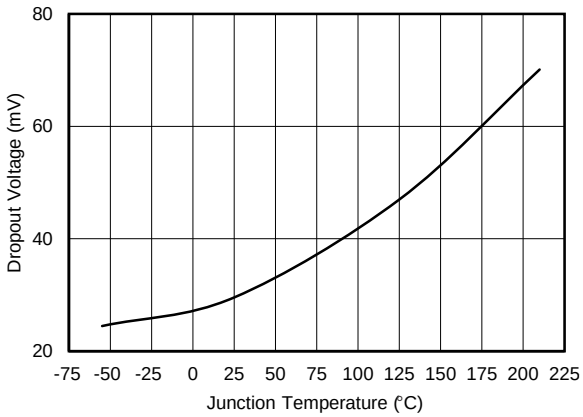

Figure 4. Dropout Voltage vs Temperature

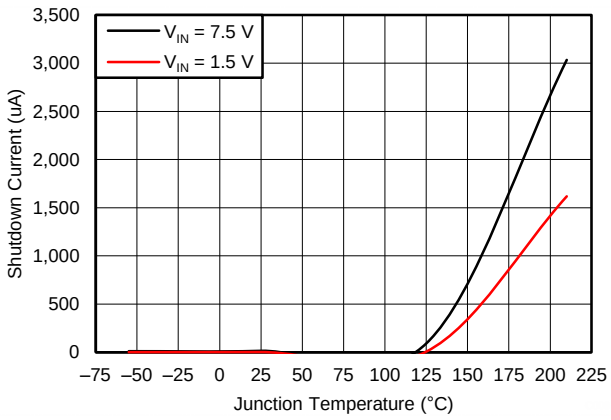

Figure 5. Shutdown Current vs Temperature

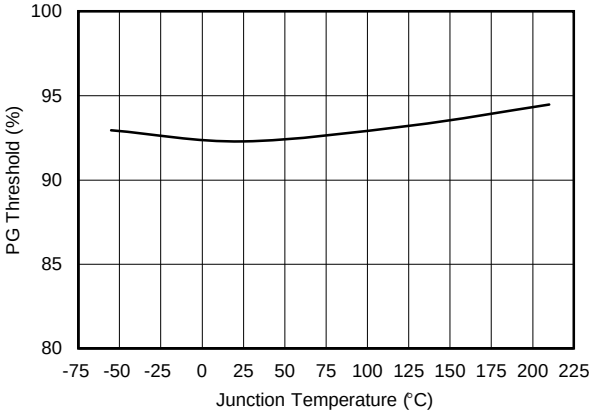

Figure 6. PG Threshold vs Temperature

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Typical Characteristics (continued)

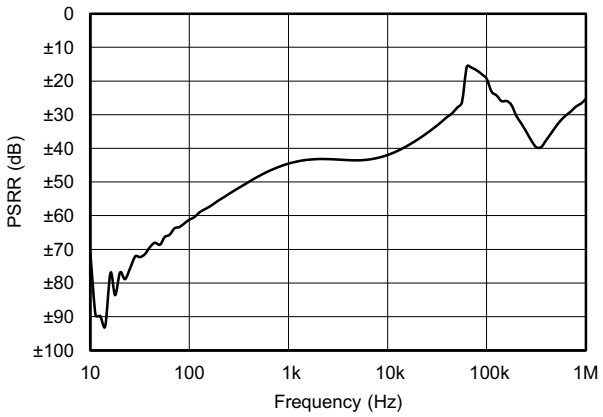

Figure 7. Power Supply Ripple Rejection vs Frequency, I_{OUT} = 250 mA

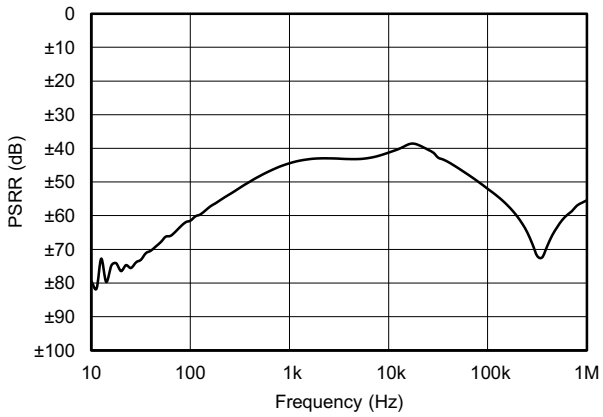

Figure 8. Power Supply Ripple Rejection vs Frequency, I_{OUT} = No Load

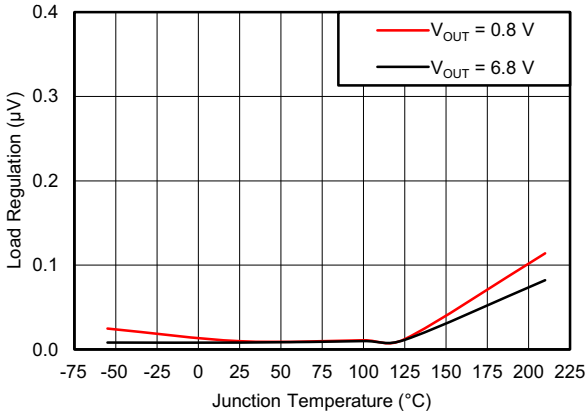

Figure 9. Load Regulation vs Temperature

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7 Detailed Description

7.1 Overview

The TPS7H1201-HT is a 0.5-A, 1.5- to 7-V LDO linear regulator that uses PMOS pass element configuration.

It uses TI's proprietary process to achieve low noise, high PSRR combined with high thermal performance in a 16-terminal ceramic flatpack package (HKS) or KGD (bare die) package.

A number of features are incorporated in the design to provide high reliability and system flexibility. Overload protection is incorporated in the design to make it viable for harsh environments.

A resistor connected from the PCL terminal to ground sets the current limit activation point. When current limit activation point is reached, output voltage drops while output load current is maintained at current limit point.

The device also has a current sense monitoring feature. A resistor connected from the CS terminal to VIN indicates voltage proportional to the output load current. *PCL* provides a detailed description of this feature.

To provide system flexibility for demanding current needs, the LDO can be configured in parallel operation as indicated in Figure 24. *Current Sharing* provides detailed parallel operation information.

An enable feature is incorporated in the design allowing the user to enable or disable the LDO. Power Good, an open-drain connection, indicates the status of the output voltage. These provide the customers' system flexibility in monitoring and controlling the LDO operation. When using the Enable function, V_{IN} voltage must be > 3.5 V. For V_{IN} from 1.5 to 7 V, TPS7H1201-HT can be disabled using the SS terminal as described in *Enable/Disable*.

7.2 Functional Block Diagram

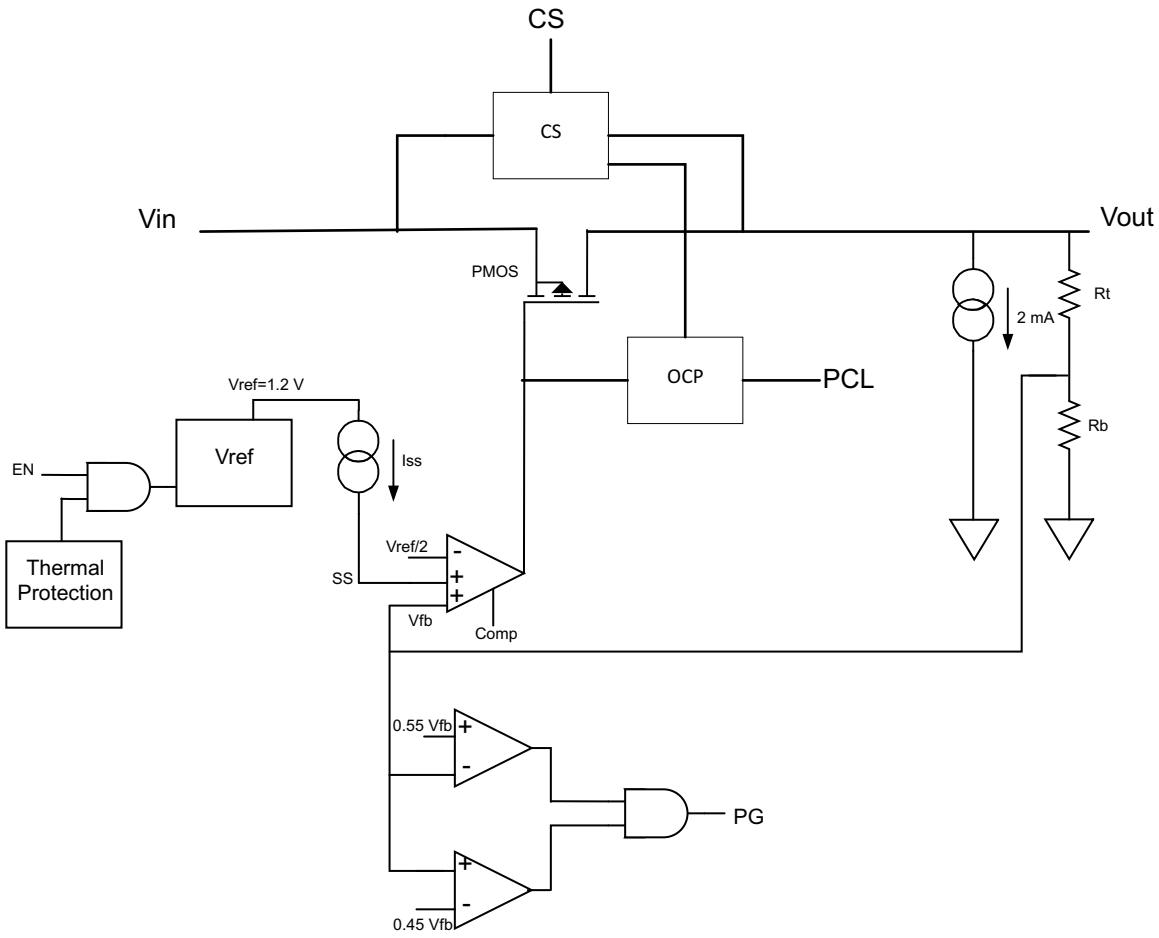

Figure 10. Block Diagram

7.3 Feature Description

7.3.1 Soft Start

Connecting a capacitor from the SS terminal to GND (C_{SS}) slows down the output voltage ramp rate. The soft-start capacitor charges up to 1.2 V.

$$C_{SS} = \frac{t_{SS} \bullet I_{SS}}{V_{FB}} \quad (1)$$

where

- t_{ss} = Soft-start time
- I_{ss} = 2.5 µA
- $V_{FB} = V_{REF} / 2 = 0.605$ V

7.3.2 Power Good (PG)

Power Good terminal (9) is an open-drain connection and can be used to sequence multiple LDOs. Figure 11 shows typical connection for V_{IN} > 3.5 V. The PG terminal will be pulled low until the output voltage reaches 90% of its maximum level. At that point, the PG pin will be pulled up. Since the PG pin is open drain, it can be pulled up to any voltage as long as it does not exceed the absolute max of 7.5 V listed in the table.

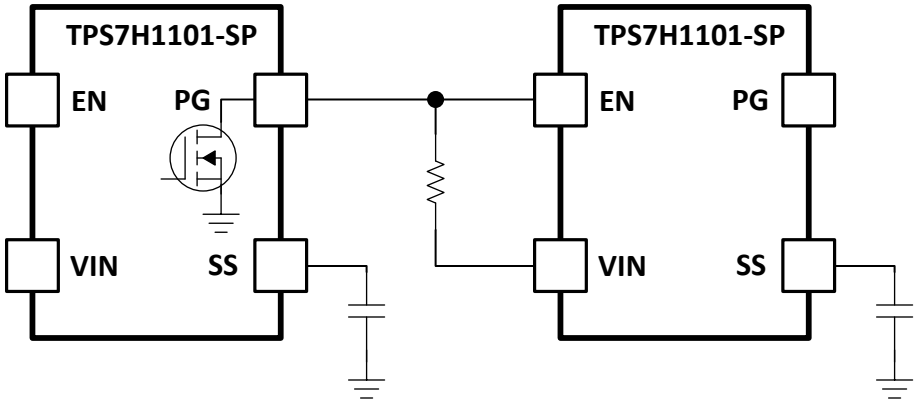

Figure 11. Sequencing LDOs with Power Good

NOTE

For PSpice models, WEBENCH, and mini-POL reference design, see the *Tools & Software* tab.

1. PSpice average model (stability – bode plot)
2. PSpice transient model (switching waveforms)
3. WEBENCH design tool (www.ti.com/product/TPS7H1201-HT/toolssoftware)

7.4 Device Functional Modes

7.4.1 Enable/Disable

For V_{IN} from 1.5 V to 7 V, TPS7H1201-HT can be disabled using the SS terminal. The minimum soft-start pulldown current is 10 µA, with soft start to ground voltage of 400 mV or lower. External voltage applied to the SS terminal must be limited to 1.2-V maximum. Removing the logic-low condition on soft start enables the device allowing the soft-start capacitor to get charged by the internal current source. Alternatively, for V_{IN} > 3.5 V, the device can be disabled by pulling the enable terminal to logic low. In all other cases, the enable terminal should be connected to VIN.

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Device Functional Modes (continued)

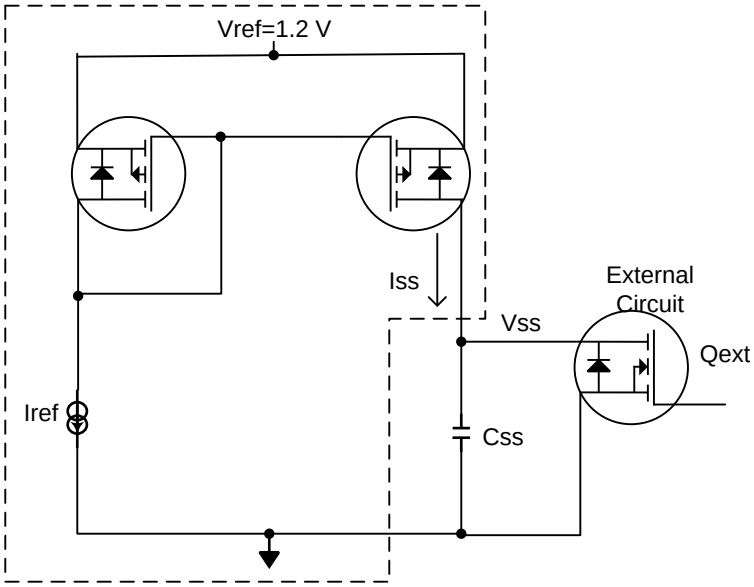

Figure 12. Enable/Disable

The circuit shown in Figure 12 highlights the SS terminal 1 along with block diagram of internal circuitry. Circuitry in dashed outline is internal to the IC composed of PMOSFET current mirror. The PMOS current mirror sources current from the positive supply and external circuitry composed of Qext is used to sink current from SS terminal 1. As highlighted in the table, typical ISS = 2.5 μA and max ISS = 3.5 μA for TPS7H1101-SP. If ISS current is exceeded, such as sinking higher current in excess of max ISS, this disables the LDO. See the table for the external sink current from SS terminal necessary to disable the IC. Exceeding maximum external sink current does not damage the device.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7H1201-HT LDO linear regulator is targeted to harsh environment applications. This regulator has various features such as low dropout, soft start, output current foldback, high-side current sensing (where sensing voltage at CS pin provides voltage proportional to output current), and current sharing.

8.1.1 Stability

Conventional Bode plots are a standard approach in assessing stability as shown in Figure 13. This approach requires that we have a single feedback path where an AC signal is injected across a resistor (typically 50 Ω) and measurements are taken on either side of the resistor. From this, loop gain and phase plots can be generated. Crossover frequency, f_C, is defined as the frequency where the magnitude of the loop gain is unity and phase margin is evaluated at the crossover frequency f_C.

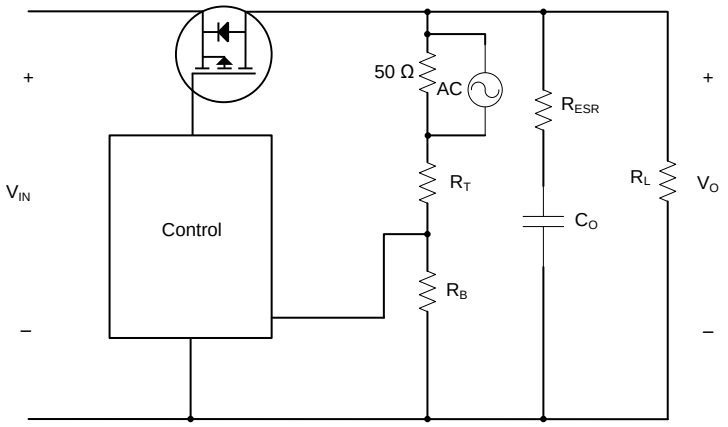

Figure 13. Conventional Bode Plot

However, there are conditions where the feedback loop is not accessible or there may be multiple feedback paths, as with the TPS7H1101-SP. When there are multiple feedback loops the conventional bode plot approach will not be representative of the device's true response. The TPS7H1101-SP uses a conventional feedback loop in addition to an inner fast loop that injects current into the error amplifier, which in turn greatly improves the transient response of the device. The Bode plot method can still be used to understand the behavior of the main loop, but this will show a lower crossover frequency and thus imply a slower transient response than the actual performance of the device. Fortunately, accurate and quantitative stability metrics can still be assessed from output impedance measurements and simulations.

There are multiple ways output impedance can be measured. One approach is to inject a small current at the output of the regulator and compare it to the resulting voltage response. The variation in the phase of the output impedance across frequency can be related to the phase margin through the group delay.

Group delay, T_g, is the rate of change of phase with respect to frequency as shown in Equation 2. Most SPICE simulation packages can plot this parameter and certain frequency analyzers boast software that supports a direct measurement. Using this software, phase margin can be extracted from the group delay plot. The phase margin and crossover frequency reported from these measurements will include the effects of both feedback loops.

$$T_g = \frac{d\phi}{d\omega} \tag{2}$$

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Application Information (continued)

The stability of the device can be qualitatively validated by applying a step load to the output and observing the response. The SPICE models for the device can be found in *Tools & Software* on the product page. To simulate impedance measurements, the transient model should be used. For a more detailed explanation of this approach and how to use the model to simulate the output impedance and group delay, please see reference (1).

8.2 Typical Application

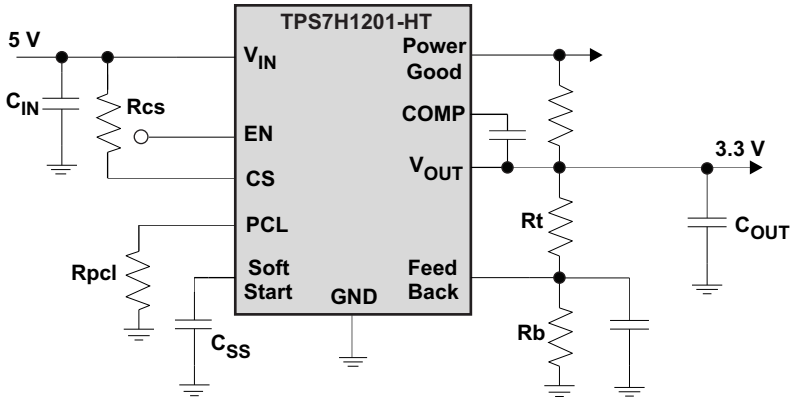

Figure 14. Typical Application Circuit

8.2.1 Design Requirements

Table 1 shows the design parameters.

Table 1. Design Parameters

PARAMETER	VALUE
Input voltage	1.5 V to 7 V
Output voltage	User programmable
Output current	3-A max

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8.2.2 Detailed Design Procedure

8.2.2.1 Adjustable Output Voltage (Feedback Circuit)

The output voltage of the TPS7H1201-HT can be set to a user-programmable level between 0.8 and 6.8 V. Achieve this by using a resistor divider connected between V_{OUT}, FB, and GND terminals. R_{TOP} connected between V_{OUT} and V_{FB}, and R_{BOTTOM} connected between V_{FB} and GND.

Use Equation 3 to determine V_{OUT}.

$$V_{OUT} = \frac{(R_{TOP} + R_{BOTTOM}) \bullet V_{FB}}{R_{BOTTOM}} \quad (3)$$

where

- V_{FB} = 0.605 V

Table 2. Resistor Values for Typical Voltages

V_{OUT}	Standard 1% Resistors		Standard 0.1% Resistors	
	R_{TOP}	R_{BOTTOM}	R_{TOP}	R_{BOTTOM}
0.8 V	10.7 kΩ	33.2 kΩ	10.7 kΩ	33.2 kΩ
1 V	13.7 kΩ	21 kΩ	12.6 kΩ	19.3 kΩ
1.2 V	11.3 kΩ	11.5 kΩ	11.8 kΩ	12 kΩ
1.5 V	15.8 kΩ	10.7 kΩ	18.2 kΩ	12.3 kΩ
1.8 V	23.2 kΩ	11.8 kΩ	32 kΩ	16.2 kΩ
2.5 V	10.7 kΩ	3.4 kΩ	37.9 kΩ	12.1 kΩ
3.3 V	51.1 kΩ	11.5 kΩ	10.2 kΩ	2.29 kΩ
4 V	13.3 kΩ	2.37 kΩ	31.2 kΩ	5.56 kΩ
5 V	11.5 kΩ	1.58 kΩ	16.2 kΩ	2.23 kΩ
5.5 V	17.4 kΩ	2.15 kΩ	89.8 kΩ	11.1 kΩ
6 V	90.9 kΩ	10.2 kΩ	10.7 kΩ	1.2 kΩ
6.5 V	26.7 kΩ	2.74 kΩ	15.2 kΩ	1.56 kΩ
6.6 V	11.3 kΩ	1.15 kΩ	22.1 kΩ	2.23 kΩ
6.7 V	39.2 kΩ	3.92 kΩ	13.8 kΩ	1.37 kΩ

8.2.2.2 PCL

PCL resistor, R_{pcl}, sets the overcurrent limit activation point and can be calculated per Equation 4.

$$R_{pcl} = (CSR \times V_{ref}) / (I_{CL} - 0.0403) \quad (4)$$

where

- V_{ref} = 0.605 V
- I_{CL} = Programmable current limit (A)
- Current sense ratio (CSR) is the ratio of output load current to I_{CS}. The typical value of the CSR is 47394.

Figure 15 shows the output load current (I_{OUT}) versus PCL terminal current (I_{CL})

A suitable resistor R_{pcl} must be chosen to ensure the CS terminal is within its operating range of 0.3 V to V_{IN}.

The maximum PCL is 700 mA. The range of resistor that can be used on the PCL terminal to GND is 47 kΩ to 160 kΩ.

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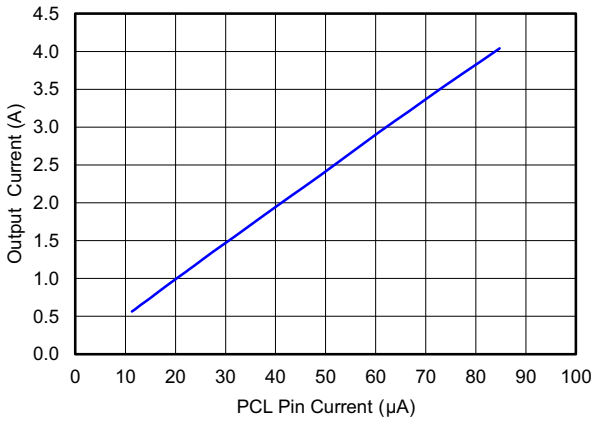

V_{IN} = 2.3 V V_{OUT} = 1.8 V y = 47394x + 0.0403

Figure 15. I_{OUT} (A) vs I_{PCL} (µA)

8.2.2.3 High-Side Current Sense

Figure 16 shows the cascode NMOS current mirror. V_{cs} must be in the range as specified in the *Electrical Characteristics* table. The following example shows the typical calculation of R_{cs}.

$$I_{CS} = \frac{I_{LOAD} + I_{offset}}{CSR} \quad (5)$$

$$R_{CS} = \frac{V_{IN} - V_{CS}}{I_{CS}} \quad (6)$$

where

- I_{LOAD} is the output load current.
- CSR is the current sense ratio.

When V_{IN} = 2.3 V, select V_{CS} = 2.05 V, I_{LOAD} = 3 A, CSR = 47394, and I_{offset} = 0.1899 A, then I_{CS} = 67.306 µA and R_{CS} = 3.714 kΩ.

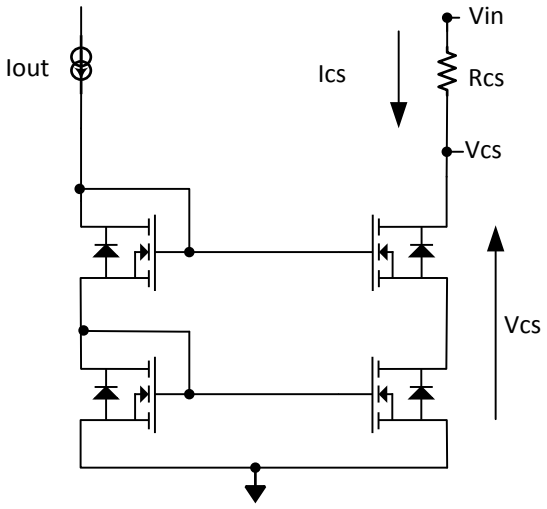

Figure 16. Cascode NMOS Current Mirror

For TPS7H1201-HT, Figure 17 shows the typical curve V_{CS} vs I_{OUT} for V_{IN} = 2.28 V and R_{CS} = 3.65 kΩ. A resistor connected from the CS terminal to V_{IN} indicates voltage proportional to the output current.

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Monitoring current in the CS terminal (I_{CS} vs I_{OUT}) indicates the current sense ratio between the main PMOSFET and the current sense MOSFET as shown in .

Figure 19 shows I_{OUT} vs I_{CS} when the voltage on CS terminal is varied from 0.3 V to 7 V.

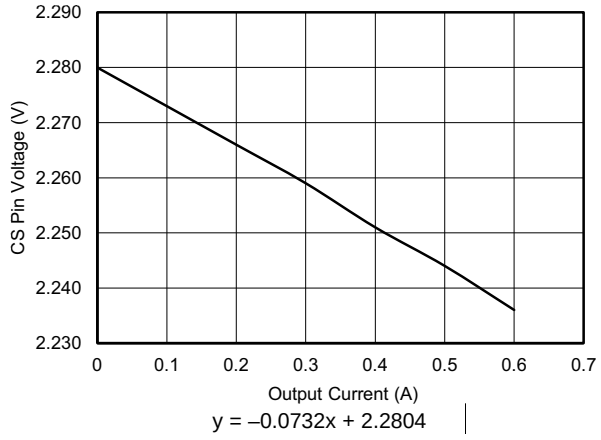


Figure 17. V_{CS} (V) vs I_{OUT} (A)

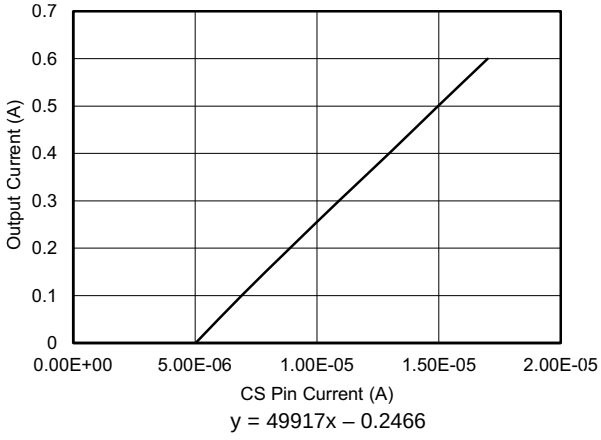
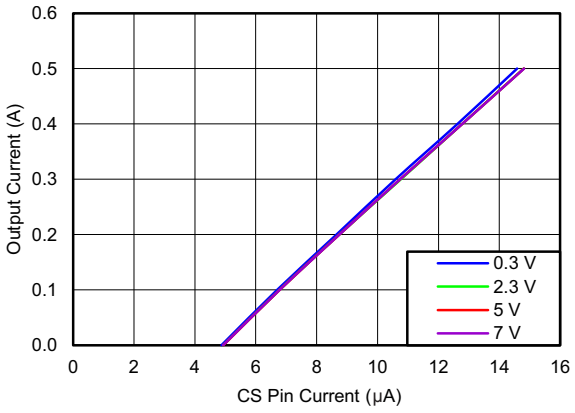


Figure 18. I_{OUT} (A) vs I_{CS} (A)



V_{IN} = 2.3 V

V_{OUT} = 1.8 V

Figure 19. I_{OUT} (A) vs I_{CS} (A)

8.2.2.4 Current Foldback

1. The TPS7H1201-HT has a current foldback feature which can be enabled when the CS terminal is held high. Shorting CS low disables the foldback current limit. If the foldback current limit is disabled, then the LDO will begin regulating again as soon as the current falls below the clamp threshold.
2. With foldback current limit enabled, when current limit trip point is activated,
   a. Output voltage drops low.
   b. Output current folds back to approximately 50% of the current limit trip point.

   This results in minimizing the power loss under fault conditions. Monitoring the voltage at the CS terminal indicates voltage proportional to the output current.

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8.2.2.5 Transient Response

Figure 20, Figure 21, and Figure 22 indicate the transient response behavior of the TPS7H1201-HT.

Channel 1: Output voltage overshoot/undershoot

Channel 2: Step load in current

Channel 3: Input voltage

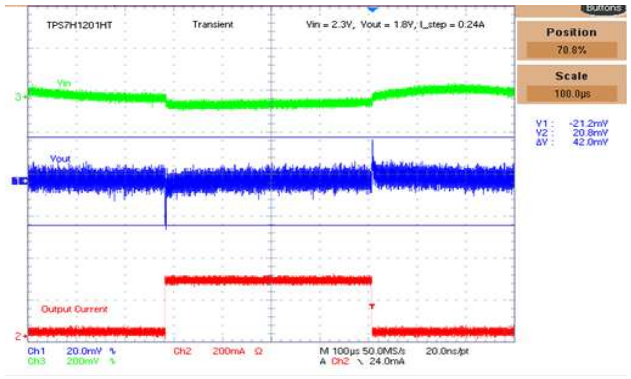

Figure 20. Load Transient Response: Step Load 0 A to 250 µA, V_{IN} = 2.3 V, V_{OUT} = 1.8 V

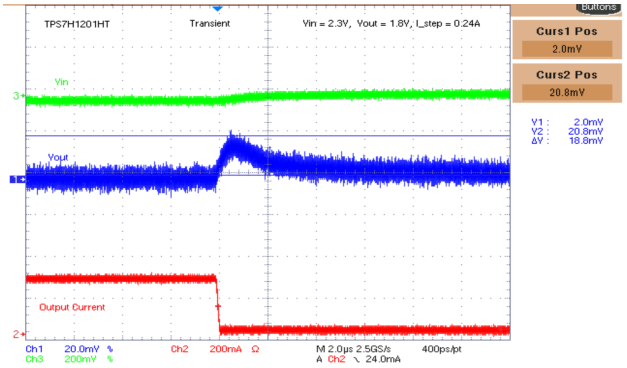

Figure 21. Expanded View Overshoot

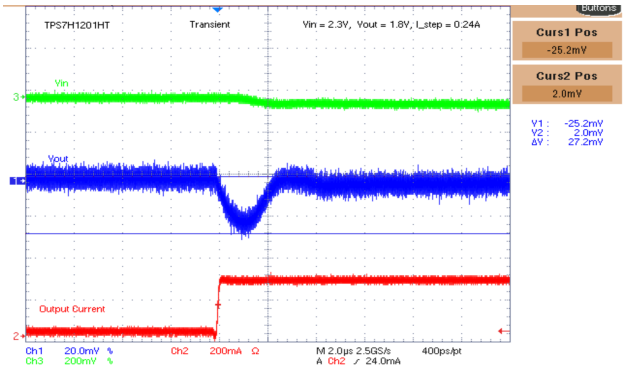

Figure 22. Expanded View Undershoot

8.2.2.6 Current Sharing

For demanding load requirements, multiple LDOs can be paralleled as indicated in Figure 24. In parallel mode, the CS terminal of LDO1 must be connected to the PCL terminal of LDO2 via a series resistor R_{CL}, and CS terminal of LDO2 must be connected to PCL terminal of LDO1 via series resistor R_{CL}. The typical value of R_{CL} in parallel operation is 3.75 kΩ for current limit > 6 A. In parallel configuration, R_{CL} (resistor from PCL to GND) and R_{CS} (resistor from CS terminal to V_{IN}) must be left open (unpopulated). The R_{CL} value must be selected so that the operating condition of the CS terminal is maintained, as specified in the *Electrical Characteristics* table. The current from PCL through RCL of LDO1 is determined by the output load current of LDO2 divided by the CSR. Hence, the voltage at CS terminal of the LDO1 is 0.605 V – ((output load current of LDO2 + 0.2458) / CSR × R_{CL}).

Alternately, it can also provide twice the output current to meet system needs. When using two LDOs in parallel operation for higher output load current, use POL TPS50601-SP as an input source.

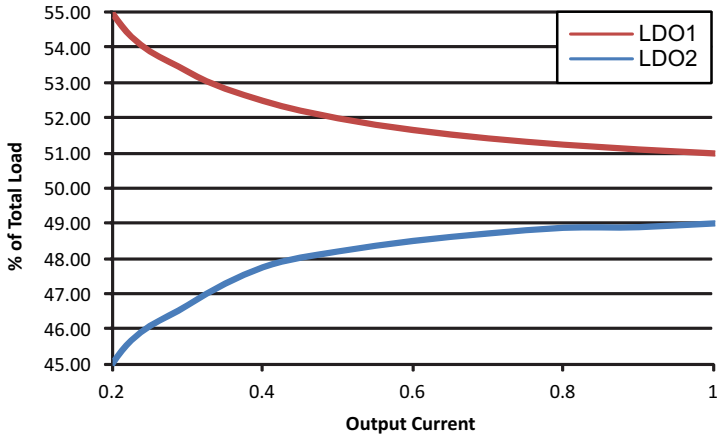

Figure 23. LDO Current Share

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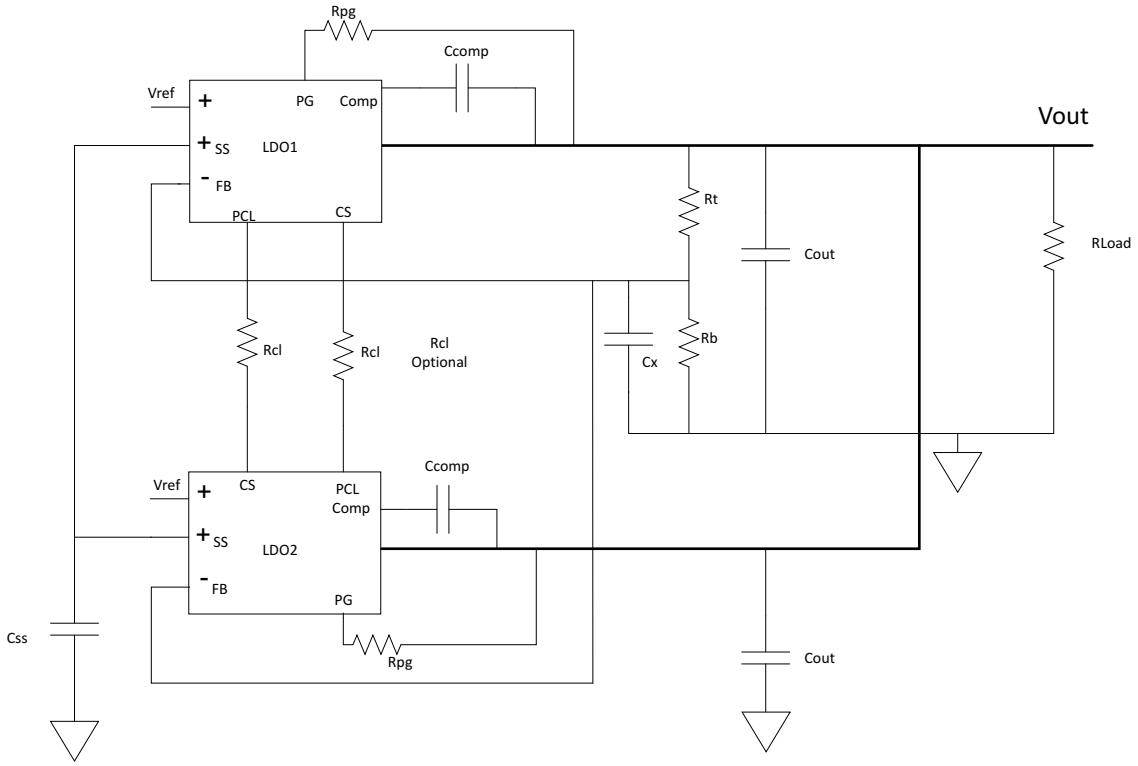

Figure 24. Block Diagram (Parallel Operation)

8.2.2.7 Compensation

Figure 25 shows a generic block diagram for TPS7H1201-HT LDO with external compensation components. LDO incorporates nested loops, thus providing the high gain necessary to meet design performance.

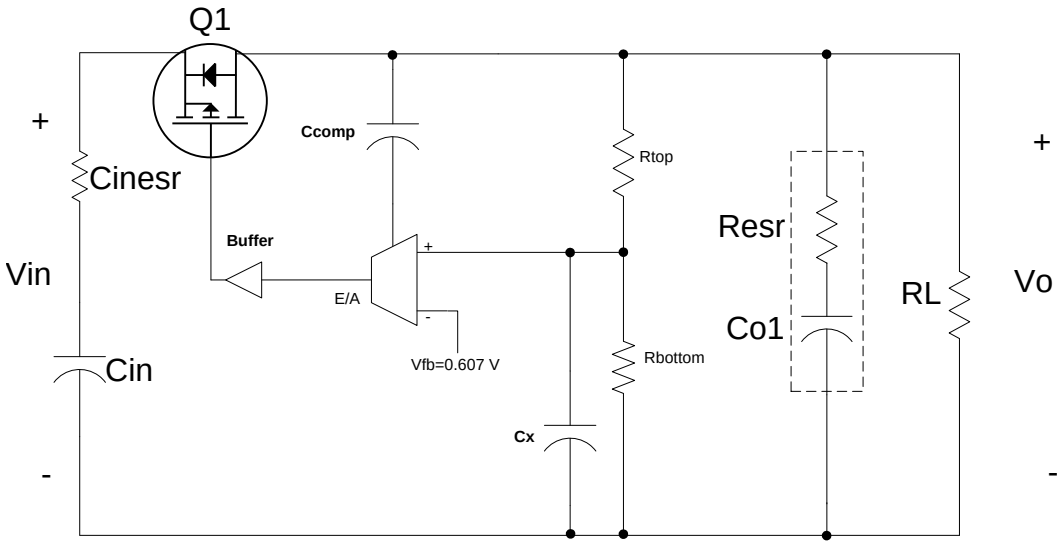

Figure 25. TPS7H1201-HT Compensation

Resistor divider composed of R_{top} and R_{bottom} determine the output voltage set points as indicated by Equation 3.

Output capacitor C_{OUT} introduces a pole and a zero as shown in the following.

$$F_{p\_co} = \frac{1}{2 \bullet \pi \bullet C_o \bullet R_L} \quad (7)$$

$$F_{z\_co} = \frac{1}{2 \bullet \pi \bullet C_o \bullet C_{esr}} \quad (8)$$

The TPS7H1101-SP was designed so that the ESR of the output capacitor will not have a strong influence on the response of the LDO. However, an optional capacitor, C_x, can be added in parallel with the bottom feedback resistor to introduce a pole to cancel F_{z_co}. Equation 9 shows how to calculate the location of the pole introduced by C_x. To cancel the zero directly, F_p should be equal to F_{z_co}.

$$F_p = \frac{1}{2 \bullet \pi \bullet C_x \bullet R_{bottom}} \quad (9)$$

C_x is calculated to be 1000 pF for C_o = 220 µF, C_{esr} = 45 mΩ, and R_{bottom} = 10 kΩ.

Internal compensation in the LDO cancels the output capacitor pole introduced by C_{OUT} and R_L.

C_{comp} introduces a dominant pole at low frequency. TI recommends that a C_{comp} value of 10 nF.

8.2.2.8 Output Noise

Output noise is measured using an HP3495A. , , Figure 26, and Figure 27 show noise of the TPS7H1201-HT in µV/√Hz vs frequency.

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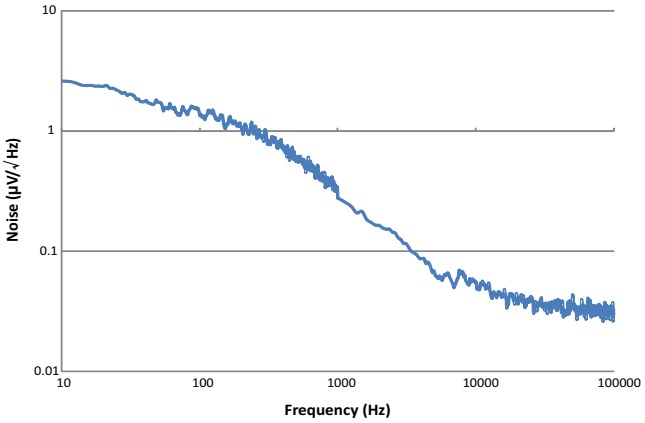
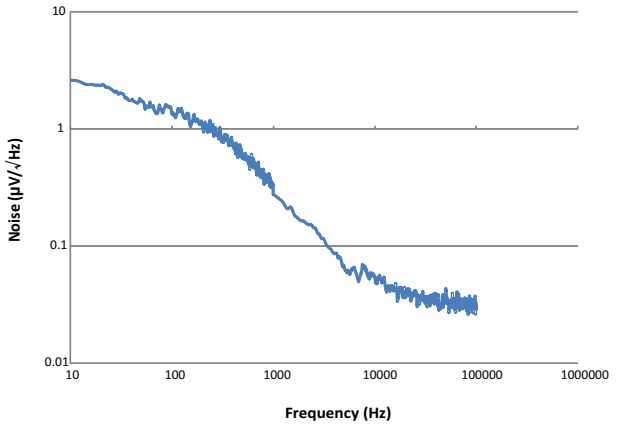


V_{IN} = 2.1 V V_{OUT} = 1.8 V at I_{LOAD} = 0.5 A
C_{IN} = 220 µF C_{LOAD} = 220 µF

Figure 26. RMS Noise (10 Hz to 100 kHz) = 20.26 µVrms



V_{IN} = 7 V V_{OUT} = 6.7 V at I_{LOAD} = 0.5 A
C_{IN} = 220 µF C_{LOAD} = 220 µF

Figure 27. RMS Noise (10 Hz to 100 kHz) = 31 µVrms

8.2.2.9 Capacitors

TPS7H1201-HT requires the use of a combination of tantalum and ceramic capacitors to achieve good volume to capacitance ratio. Table 3 highlights some of the capacitors used in the device. TI recommends to follow proper derating guidelines as recommended by the capacitor manufacturer based upon output voltage and operating temperature.

Note that polymer-based tantalum capacitors must be derated to at least 60% of rated voltage, whereas manganese oxide (MnO_2) based tantalum capacitors should be derated to 33% of rated voltage depending upon the operating temperature.

TI recommends to use a tantalum capacitor along with a 0.1-µF ceramic capacitor. The device is stable for input and output tantalum capacitor values of 10 to 220 µF with the ESR range of 10 mΩ to 2 Ω. However, the dynamic performance of the device varies based on load conditions and the capacitor values used.

TI recommends a minimum output capacitor of 22 µF with ESR of 1 Ω or less to prevent oscillations. X7R dielectrics are preferred. See Table 3 for various capacitor recommendations.

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Table 3. TPS7H1201-HT Capacitors

CAPACITOR PART NUMBER	CAPACITOR DETAILS (CAPACITOR, VOLTAGE, ESR)	TYPE	VENDOR
T493X107K016CH612A(1)	100 µF, 16 V, 100 mΩ	Tantalum - MnO2	Kemet
T493X226M025AH6x20(1)	22 µF, 25 V, 35 mΩ	Tantalum - MnO2	Kemet
T525D476M016ATE035(1)	47 µF, 10 V, 35 mΩ	Tantalum - Polymer	Kemet
T540D476M016AH6520(1)	47 µF, 16 V, 20 mΩ	Tantalum - Polymer	Kemet
T525D107M010ATE025(1)	100 µF, 10 V, 25 mΩ	Tantalum - Polymer	Kemet
T541X337M010AH6720(1)	330 µF, 10 V, 6 mΩ	Tantalum - Polymer	Kemet
T525D227M010ATE025(1)	220 µF, 10 V, 25 mΩ	Tantalum - Polymer	Kemet
T495X107K016ATE100(1)	100 µF, 16 V, 100 mΩ	Tantalum - MnO2	Kemet
CWR29FK227JTHC(1)	220 µF, 10 V, 180 mΩ	Tantalum - MnO2	AVX
THJE107K016AJH	100 µF, 16 V, 58 mΩ	Tantalum	AVX
THJE227K010AJH	220 µF, 10 V, 40 mΩ	Tantalum	AVX
SMX33C336KAN360	33 µF, 25 V	Stacked ceramic	AVX
SR2225X7R335K1P5#M123	3.3 µF, 25 V, 10 mΩ	Ceramic	Presidio Components Inc

(1) Operating temperature is –55°C to 125°C.

8.2.3 Application Curves

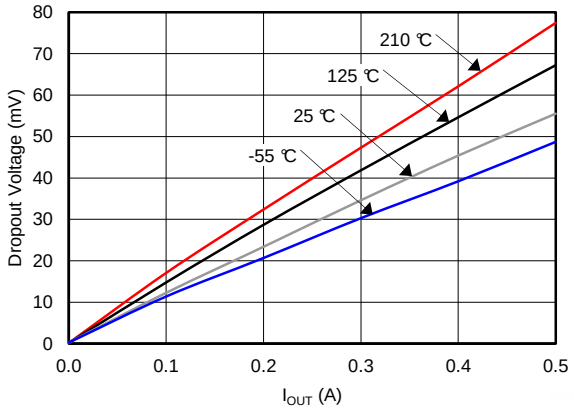

Figure 28. VDO vs I_{OUT}

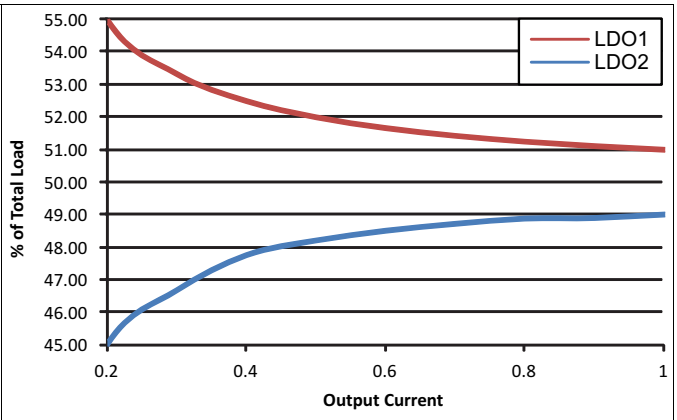

Figure 29. LDO Current Share

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9 Power Supply Recommendations

This device is designed to operate with an input voltage supply up to 7 V. The minimum input voltage should provide adequate headroom greater than the dropout voltage for the device to have a regulated output. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

- For best performance, all traces should be as short as possible, and no longer than 5 cm.
- Use wide traces for IN, Out and GND to minimize the parasitic electrical effects.
- Place the output capacitors (COUT) as close as possible to the OUT pin of the device.

10.2 Layout Example

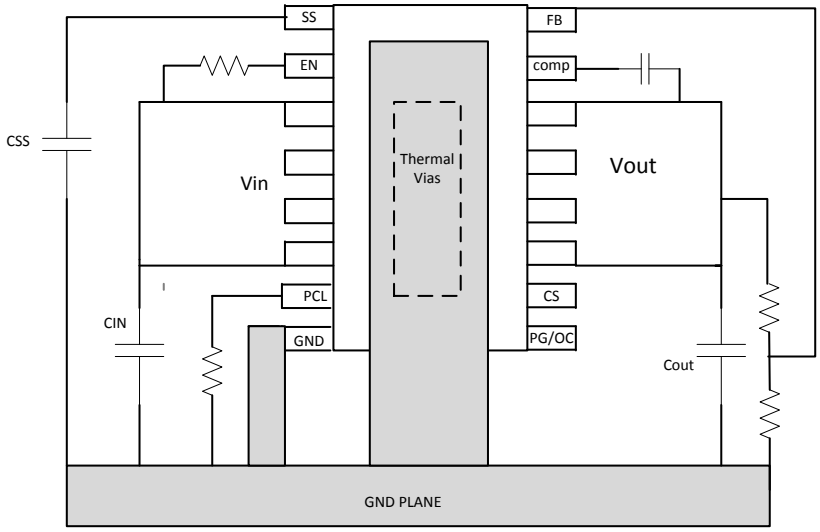

Figure 30. PCB Layout Example

11 器件和文档支持

11.1 器件支持

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11.1.2 器件命名规则

KGD 已知的合格芯片

11.2 文档支持

11.2.1 相关文档

(1) *固定稳压器的稳定性评估 - Tom Boehler、Paul Ho，AEi 系统*

11.3 接收文档更新通知

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11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参见左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7H1201SHKS	ACTIVE	CFP	HKS	16	15	RoHS & Green	NIAU	N / A for Pkg Type	-55 to 210	TPS7H1201SHKS	Samples
TPS7H1201SKGD1	ACTIVE	XCEPT	KGD	0	70	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 210		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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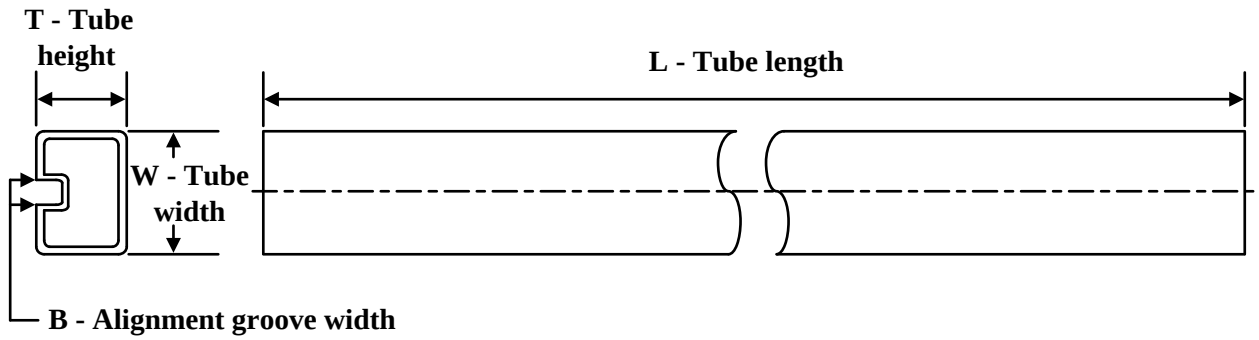
TUBE



*All dimensions are nominal

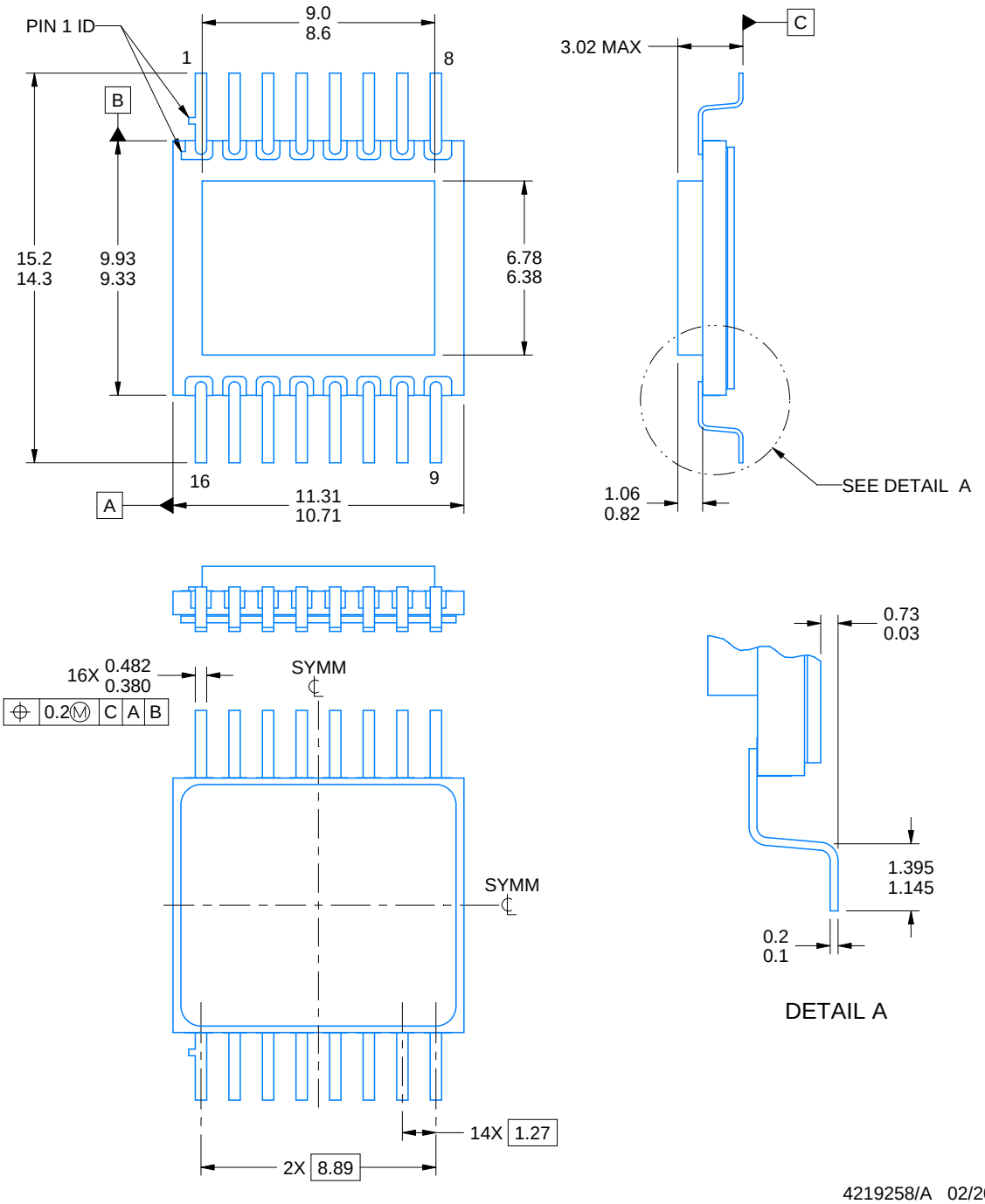
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS7H1201SHKS	HKS	CFP	16	15	506.98	26.16	6220	NA

HKS0016A

PACKAGE OUTLINE

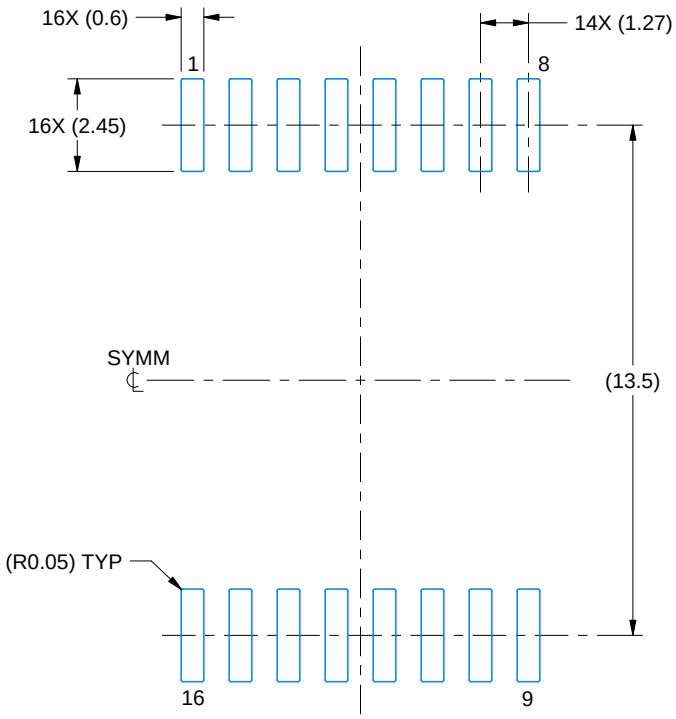
CFP - 3.02 mm max height

CERAMIC FLATPACK

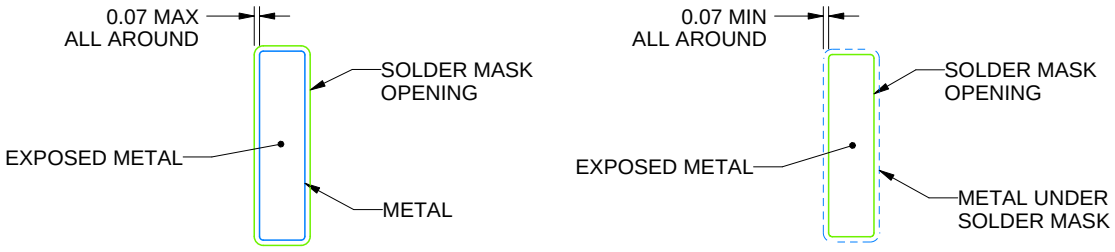


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid. The lid and heat slug are connected to pin 8.
4. The leads are gold plated.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 5X



NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4219258/A 02/2017

NOTES: (continued)

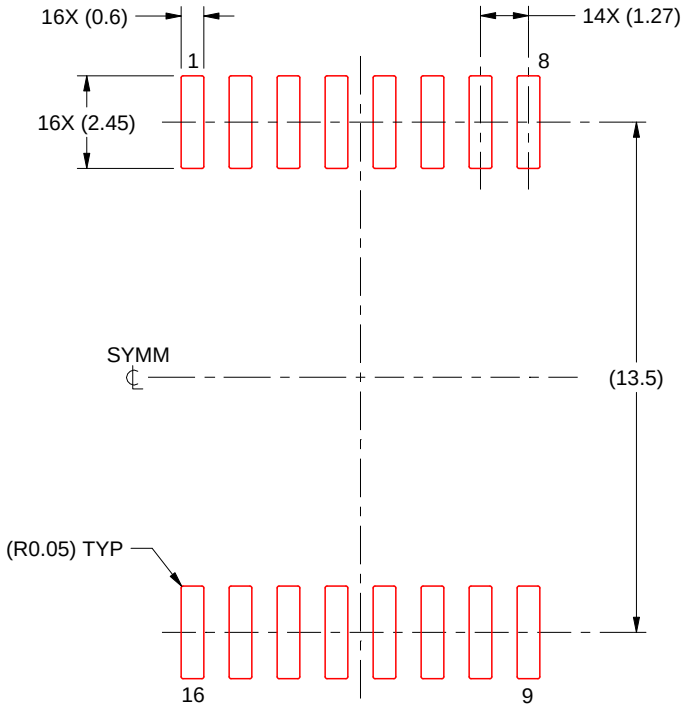
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

HKS0016A

CFP - 3.02 mm max height

CERAMIC FLATPACK



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 5X

4219258/A 02/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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