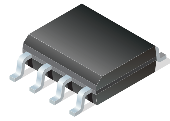


具有数字基准控制的非隔离、相位可调光、降压功率因数控制器 (PFC) 发光二极管 (LED) 驱动器

查询样品: TPS92075

特性

- 取自 **PFC** 的受控基准
- 集成数字相位角解码器
- 数字 **50/60Hz** 同步
- 相位对称均衡
- 恒定 **LED** 电流运行
- 快速启动
- 由模拟基准控制实现的调光
- 平滑调光转换
- 过压保护
- 反馈短路保护
- 前缘和后缘调光器兼容性
- 低物料清单 **(BOM)** 成本和小型印刷电路板 **(PCB)** 封装尺寸
- 正在申请专利的数字架构
- 可提供 **8** 引脚小外形尺寸集成电路 **(SOIC)** 封装。将于近期提供 **6** 引脚薄型小外形晶体管封装 **(TSOT)** 封装。

应用范围

- 灯泡替换
- 大面积照明
- 亮度可调节和亮度不可调节的 **LED** 灯

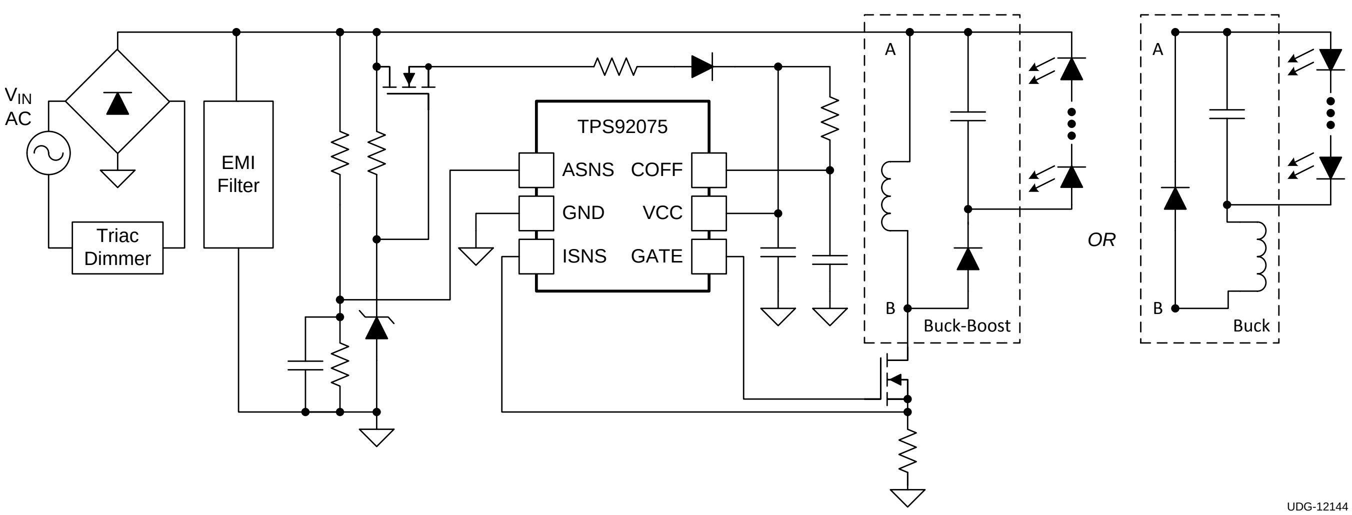
说明

TPS92075 是一款内置有相位调光解码器的混合功率因数控制器 (PFC)。 此器件使用一个内部、低功耗数字控制器来分析线周期以实现整形和对称。 功率转换器级生成一个模拟电流基准并用它来调节输出电流。 此器件使用控制算法来操纵此模拟基准。 这些算法优化了调光器的兼容性、功率因数和总谐波失真 (THD)。

通过使用一个恒定关闭时间控制，这个解决方案实现了低组件数量、高效率并自然提供了开关频率的变化。 这个变化创建了一个仿真展频效应，从而简化了转换器电磁干扰 (EMI) 签名并可使用一个更小的输出滤波器。

TPS92075 还包含一些标准特性：电流限制、过压保护、热关断和 VCC 欠压闭锁，所有这些都采用仅有 6 引脚的封装。

简化的应用图



English Data Sheet: SLUSB88

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

TEMPERATURE RANGE (T_J)	PACKAGE(2)	PINS	ORDERABLE DEVICE NUMBER	TRANSPORT MEDIUM	QUANTITY
–40 to 125°C	SOIC	8	TPS92075D	Rail	95
			TPS92075DR	Tape and Reel	2500
–40 to 125°C	TSOT(3)	6	TPS92075DDC	Tape and Mini-Reel	1000
			TPS92075DDCR	Tape and Reel	3000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) TSOT package is Product Preview only. Release date TBA.

ABSOLUTE MAXIMUM RATINGS[(1)]

All voltages are with respect to GND, –40°C < T_J = T_A < 125°C, all currents are positive into and negative out of the specified terminal (unless otherwise noted)

		VALUE MIN	VALUE MAX	UNIT
Input voltage range	VCC	–0.3	22	V
	ASNS, COFF	–0.3	6.0	
Bias and ISNS	I_Q bias current (non-switching)		2.5	mA
	ISNS[(2)] to Ground	–0.3	2.5	V
Gate	GATE - continuous	–0.3	18	V
	GATE - 100 ns	–2.5	20.5	V
Continuous power dissipation		Internally Limited		
Electrostatic discharge	Human Body Model (HBM)		2	kV
	Field Induced Charged Device Model (FICDM)		750	V
Operating junction temperature, T_J[(3)]			160	°C
Storage temperature range, T_{stg}		–65	150	°C
Lead temperature, soldering, 10s			260	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) ISNS can sustain –2 V for 100 ns without damage.
(3) Maximum junction temperature is internally limited.

THERMAL INFORMATION

THERMAL METRIC[(1)]		TPS92075 SOIC (D) 8 PINS	TPS92075 TSOT (DDC) 6 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance[(2)]	112.3	165.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[(3)]	58.4	28.8	
θ_{JB}	Junction-to-board thermal resistance[(4)]	52.5	24.6	
ψ_{JT}	Junction-to-top characterization parameter[(5)]	12.5	0.3	
ψ_{JB}	Junction-to-board characterization parameter[(6)]	51.9	23.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[(7)]	NA	NA	

(1) 有关传统和新的热 度量的更多信息，请参阅*IC 封装热度量*应用报告， SPRA953。
(2) 在 JESD51-2a 描述的环境中，按照 JESD51-7 的指定，在一个 JEDEC 标准高 K 电路板上进行仿真，从而获得自然 对流条件下的结至环境热阻。
(3) 通过在封装顶部模拟一个冷板测试来获得结至芯片外壳（顶部）的热阻。 不存在特定的 JEDEC 标准测试，但 可在 ANSI SEMI 标准 G30-88 中能找到内容接近的说明。
(4) 按照 JESD51-8 中的说明，通过 在配有用于控制 PCB 温度的环形冷板夹具的环境中进行仿真，以获得结板热阻。
(5) 结至顶部特征参数， ψ_{JT}，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中 描述的程序从仿真数据中 提取出该参数以便获得 θ_{JA}。
(6) 结至电路板特征参数， ψ_{JB}，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中 描述的程序从仿真数据中 提取出该参数以便获得 θ_{JA} 。
(7) 通过在外露（电源）焊盘上进行冷板测试仿真来获得 结至芯片外壳（底部）热阻。 不存在特定的 JEDEC 标准 测试，但可在 ANSI SEMI 标准 G30-88 中能找到内容接近的说明。

RECOMMENDED OPERATING CONDITIONS(1)

Unless otherwise noted, all voltages are with respect to GND, –40°C < T_J = T_A < 125°C.

		MIN	TYP	MAX	UNIT
Supply input voltage range	VCC		11	18	V
Operating junction temperature		–40		125	°C

(1) Operating Ratings are conditions under which operation of the device is specified and do not imply assured performance limits. For specified performance limits and associated test conditions, see the Electrical Characteristics table.

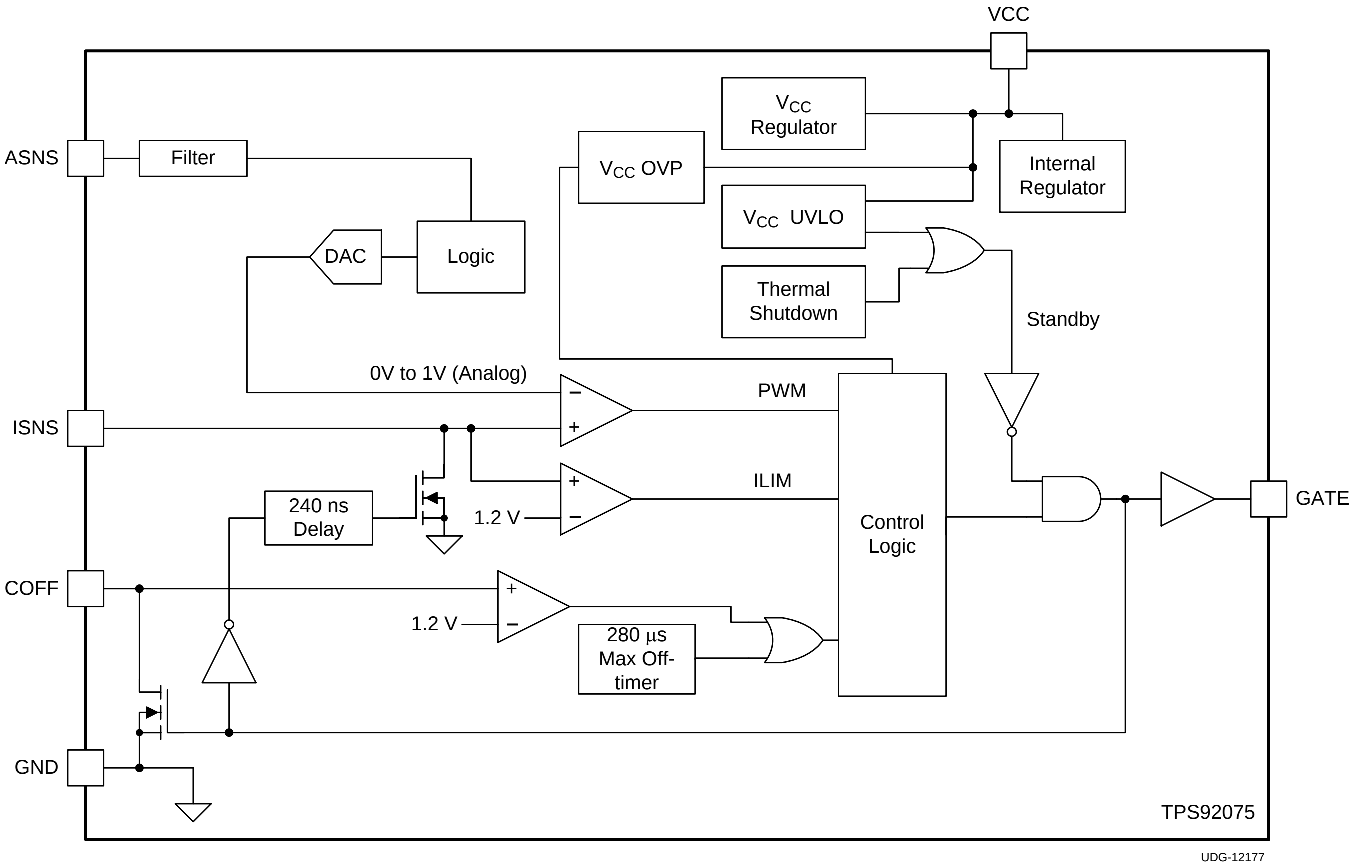
ELECTRICAL CHARACTERISTICS

Unless otherwise specified –40°C ≤ T_J = T_A ≤ 125°C, V_{CC} = 14 V, C_{VCC} = 10 µF C_{GATE} = 2.2 nF

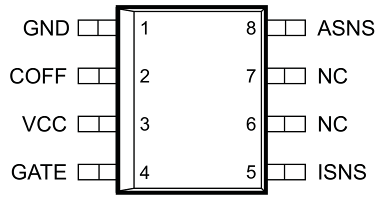
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE INPUT (VCC)						
I_Q	V_{CC} quiescent current	Not switching		1.3	2.5	mA
I_{Q_SD}	V_{CC} low power mode current	V_{CC} < $V_{CC(UVLO)}$		120	250	µA
V_{VCC}	Input range	V_{CC} ≤ $V_{CC(OVP)}$			18	V
$V_{CC(OVP)}$	Overvoltage protection threshold	V_{CC} > $V_{CC(OVP)}$	18.0		20.0	V
$V_{CC(UVLO)}$	V_{CC} UVLO threshold	V_{CC} rising		9.8	10.5	V
		V_{CC} falling	5.75	6.40		V
$V_{CC(HYS)}$	V_{CC} UVLO hysteresis			3.3		V
ANGLE DEMODULATION						
$ASNS_{TH-Hi}$	Angle detect rising threshold		0.9	1.0	1.1	V
$ASNS_{TH-Low}$	Angle detect falling threshold		0.465	0.500	0.540	V
OFF-TIME CONTROL						
V_{COFF}	OFF capacitor threshold		1.14	1.20	1.285	V
R_{COFF}	OFF capacitor pull-down resistance			33	60	Ω
$t_{OFF-max}$	Maximum off-time			280		µs
GATE DRIVER OUTPUT (GATE)						
$R_{GATE(H)}$	Gate sourcing resistance			3	8	Ω
$R_{GATE(L)}$	Gate sinking resistance			3	8	Ω
CURRENT SENSE						
V_{ISNS}	Average ISNS limit threshold	DAC: 63/127	445	500	555	mV
V_{CL}	Current Limit			1.2		V
t_{ISNS}	Leading edge blanking			240		ns
	Current limit reset delay			280		µs
	ISNS limit to GATE delay			33		ns
t_{COFF_DLY}	OFF capacitor limit to GATE delay			33		ns
THERMAL SHUTDOWN						
T_{SD}	Thermal limit threshold			160		°C
T_{HYS}	Thermal limit hysteresis			20		°C

DEVICE INFORMATION

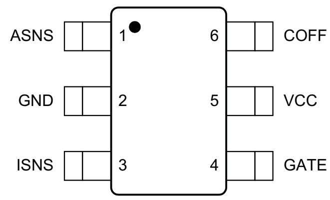
FUNCTIONAL BLOCK DIAGRAM



SOIC (D) PACKAGE
8 PINS
(TOP VIEW)



TSOT (DDC) PACKAGE
6 PINS
(TOP VIEW)



PIN DESCRIPTIONS

NAME	PIN NUMBERS		I/O	DESCRIPTION
	SIOC (D)	TSOT (DDC)		
ASNS	8	1	I	The phase of the TRIAC is detected through this pin and is then fed to the digital decoder. Sensing thresholds are 1V rising and 0.5V falling – nominal.
COFF	2	6	I	Used to set the converter constant off-time. A current and capacitor connected from the output to this pin sets the constant off-time of the switching controller.
GATE	4	4	O	Power MOSFET driver pin. This output provides the gate drive for the power switching MOSFET.
GND	1	2	—	Circuit ground connection
ISNS	5	3	I	LED current sense pin. Connect a resistor from main switching MOSFET source to GND to set the maximum switching cycle LED current. Connect ISNS to the switching FET source.
VCC	3	5	—	Input voltage pin. This pin provides the power for the internal control circuitry and gate driver. V_{CC} undervoltage lockout has been implemented with a wide range: 10V rising, 6V falling to ensure operation with start-up methods that allow elimination of the linear pass device. This includes using a coupled inductor with resistive start-up.

TYPICAL CHARACTERISTICS

Unless otherwise stated, –40°C ≤ T_A = T_J ≤ 125°C, V_{CC} = 14 V, C_{VCC} = 10 µF C_{GATE} = 2.2 nF

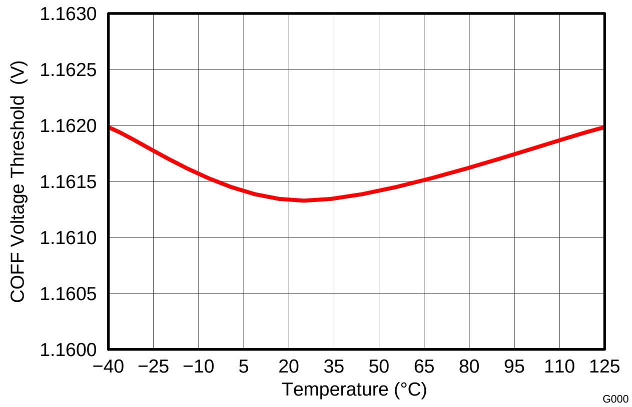


Figure 1. COFF Threshold Voltage vs Temperature

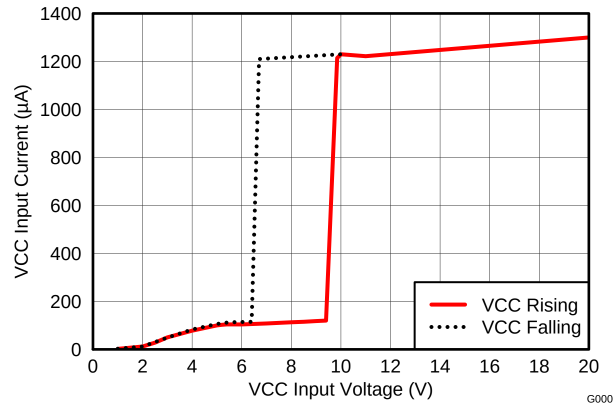


Figure 2. VCC Input Current vs Vcc Input Voltage

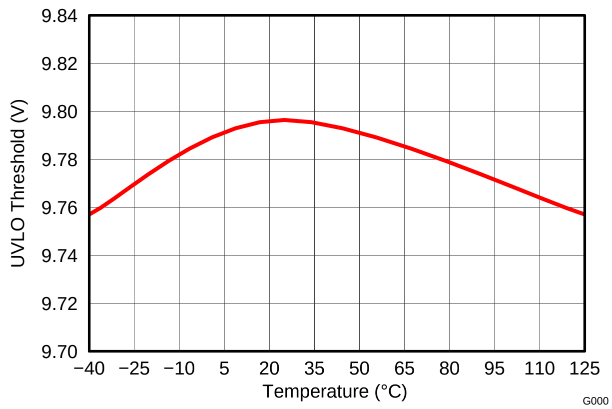


Figure 3. Input Voltage (UVLO Rising) vs Junction Temperature

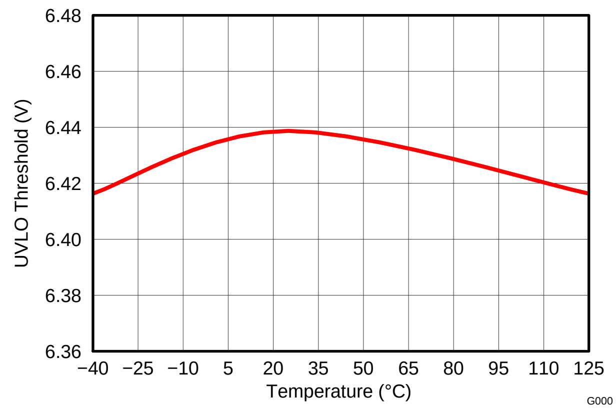


Figure 4. Input Voltage (UVLO Falling) vs Junction Temperature

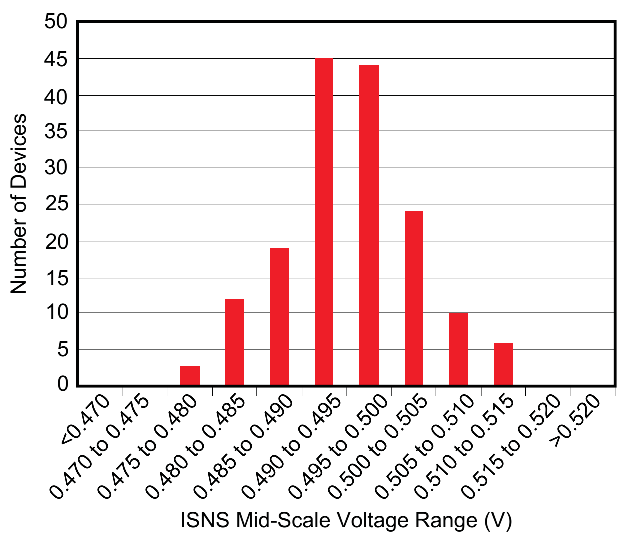


Figure 5. ISNS 0.5V Threshold Distribution

APPLICATION INFORMATION

The TPS92075 is an AC-DC power factor correction (PFC) controller for phase-cut dimmer-compatible, LED lighting applications. A hysteretic, peak current, constant off-time approach implements the conversion.

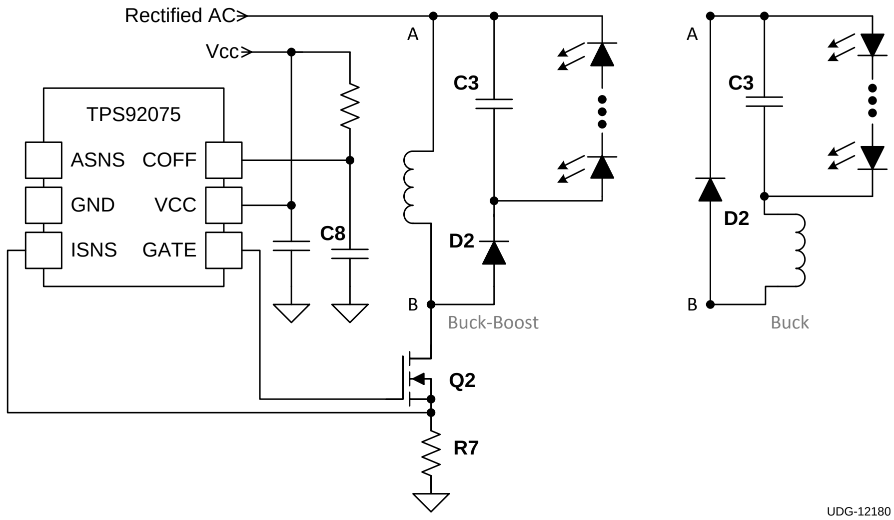


Figure 6. Simplified TPS92075 Schematic

The TPS92075 controls the inductor current by controlling two features: (A) The peak inductor current, and (B) The cycle off-time. The following items summarize the basics of the switch operation in this hysteretic controller.

- The main switch Q2 turns on and current ramps in the inductor.
- The Q2 current flows through the sense resistor R7. The R7 voltage is compared to a reference voltage at ISNS. The Q2 on-time ends when the voltage on R7 is equal to a controlled reference voltage and the inductor current has reached its set peak current level for that switching cycle.
- Q2 is turned off and a constant off-time timer begins. Voltage begins ramping on C8.
- The next cycle begins when the voltage on C8 reaches 1.2V. This ends the constant off-time and discharges C8.
- Capacitor C3 eliminates most of the ripple current seen in the LEDs.

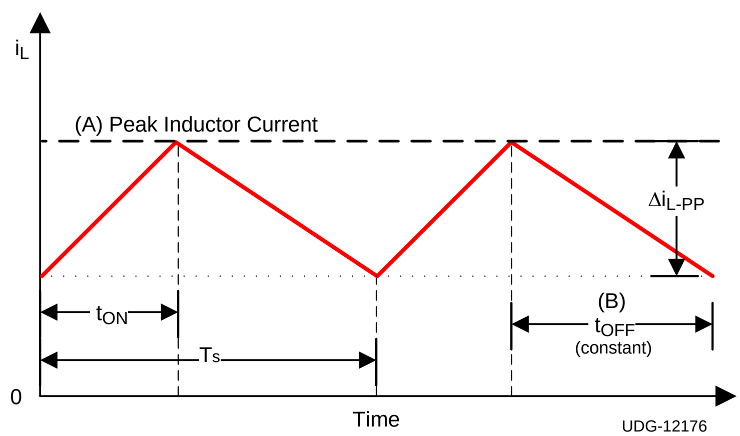


Figure 7. Controlled Reference Derived Power Factor Correction

The TPS92075 incorporates a patent-pending control methodology to generate the reference for the conversion stage. The controlled reference used for the comparison of the ISNS signal may be DC or another shape depending on the mode of operation. Each mode controls the peak current level using a different methodology.

Initial Start-Up

The TPS92075 is designed to achieve instant turn-on using an external linear regulator circuit. The start-up sequence is internally controlled by a V_{CC} under-voltage lockout (UVLO) circuit. Sufficient headroom has been incorporated to support the use of an auxiliary winding with start-up linear, resistive or coupled capacitor start-up methods.

VCC Bias Supply

The TPS92075 can be configured to use a linear regulator with or without the use of an auxiliary winding. Using a linear regulator to provide V_{CC} incurs more losses than an auxiliary winding, but has several advantages:

- allows the use of inexpensive off-the-shelf inductors as the main magnetic
- speeds start-up time under deep dimming conditions
- can reduce the size of the required VCC capacitor
- the extra current draw when dimming can improve dimming compatibility

Another consideration when selecting a bias method involves the OVP configuration. Because the feature is enabled via the VCC pin, an auxiliary winding provides the simplest implementation of output over-voltage protection.

A typical start-up sequence begins with V_{CC} input voltage below the UVLO threshold and the device operating in low-power, shut-down mode. The V_{CC} input voltage increases to the UVLO threshold of 9.8V typical. At this point all of the device features are enabled. The device loads the initial start-up value as the output reference and switching begins. The device operates until the V_{CC} level falls below the $V_{CC(UVLO)}$ falling threshold. (6.4V typical) When V_{CC} is below this threshold, the device enters low-power shut-down mode.

Angle Sense Operation

The ASNS (angle sense) pin is the only input to the digital controller. The time between the rising edge and the falling edge of the signal determines converter functions. The pin incorporates internal analog and digital filtering so that any transition that remains beyond the threshold for more than approximately 150 µs will cause the device to record a change-of-state.

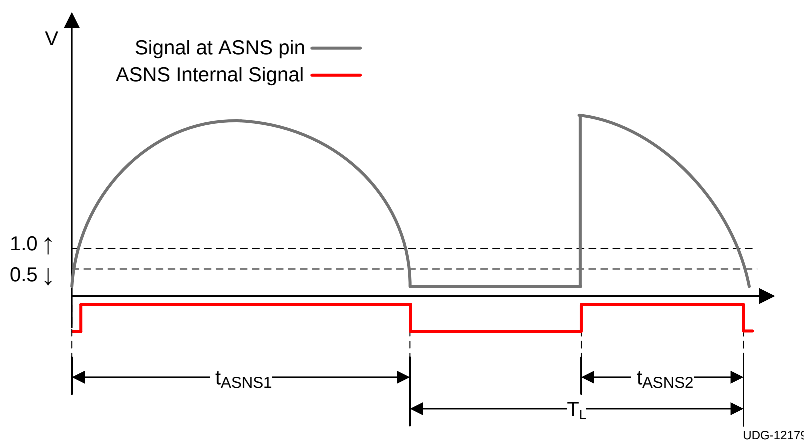


Figure 8. Angle Sense Operation

Controller

Basic Operation and Modes

The controller continuously monitors the line cycle period and the present conduction angle length to determine the state of operation and configure other control features. Control algorithms use a normalized line period of 256 samples from ASNS fall to ASNS fall and a normalized converter reference control of 127 levels over a range of 0V to 1V .

The four main controller states are:

- Start-up
- Non-Dimming
- Dimming
- ASNS signal lost

With the exception of start-up, the controller can enter any of the states at any time as conditions demand.

The two primary modes of controlling the converter reference are:

- DC mode
- Ramp mode

During active dimming, a DC control reference increases or decreases depending on the input AC duty cycle derived from the ASNS signal. The relationship follows the algorithm: (ASNS Length + Fixed Offset) = Output Set point. When the conduction angle is long enough, the converter reference is changed to a triangular ramp to achieve a high power factor. The ramp is generated gradually over several cycles ensuring the implementation is undetectable. The controller maintains the ramp between the rising and falling ASNS signals.

The controller also sets DC reference levels during start-up and when the ASNS signal is lost. Active states in the controller and controlled ranges are shown in Table 1.

Table 1. Control States and Controlled Reference Values

MODE	LINE DUTY CYCLE	CONTROLLED REFERENCE VALUE (value / 127) X 1V = reference
Start-up	Any	50
Non-Dimming	> 70%, typical average	55
	> 70%, typical ramp range	22 to 127
Dimming	≤ 70%	35 to 63
No ASNS	Any	42

Initial Start-up

Line Synchronization

When the device reaches the turn-on UVLO threshold, the output current reference resets to 0.393V (50/127) and switching begins. The controller samples the line for approximately 80 ms (t_1 to t_2 , Figure 9) to determine the line frequency and establish the present state of operation. After determining the line frequency, the controller uses the information to calibrate the internal oscillator. The controller supports line frequencies from 45Hz to 65Hz. After determining frequency and duty cycle, the controller enters the appropriate control state.

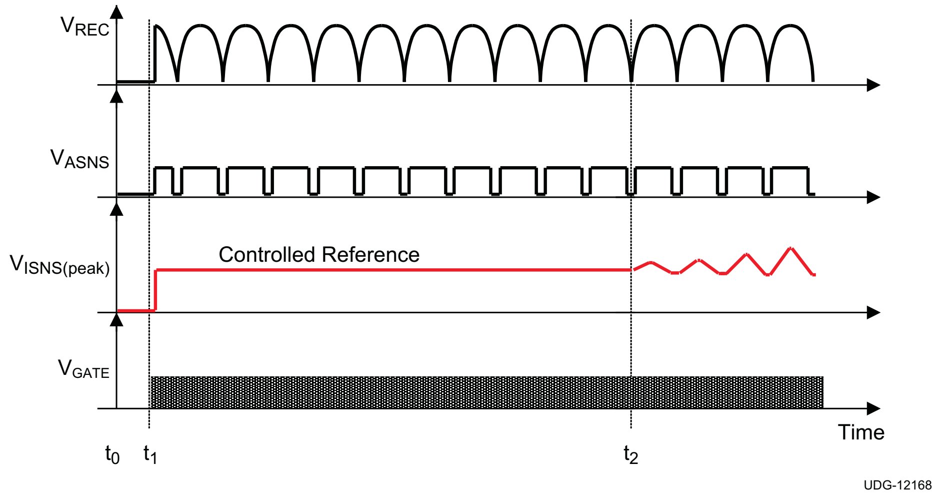


Figure 9. Line Synchronization

Non-Dimming Ramp Mode

When the conduction angle is greater than 70%, the controller begins to create a triangular ramp that is synchronized to the line and is centered between rising and falling edges of the ASNS signal as shown in Figure 10. The triangular shape is much easier to generate than a sine wave while maintaining a high power factor and low THD. The edges of the ramp do not decrease completely to zero to ensure compatibility with TRIAC dimmers that can provide conduction angles approaching 100%.

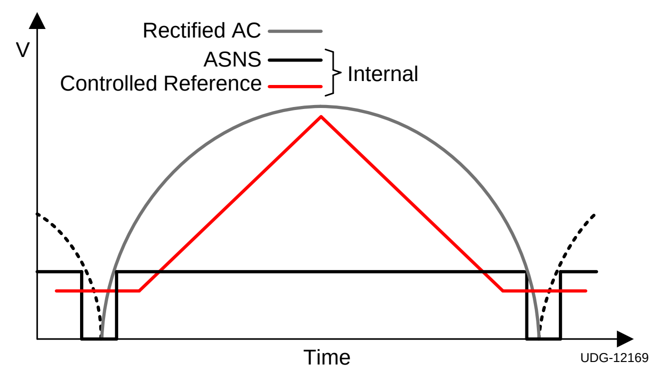


Figure 10. Controlled Reference Output, Non-dimming

When changing between dimming mode and non-dimming mode, the ramp is created over 127 line cycles (see Figure 11) or approximately 1 second (t_2 to t_3 ≈ 1 second). Because the output level before and after the change is very similar and the change very gradual, it is impossible for the user to perceive a change in output level. The ramp morphs from a DC level to a ramp using a method that further ensures transparency to the user. Ramp transition occurs during construction and deconstruction of the ramp and is reversed if the conduction angle changes sufficiently during the change process. A hysteresis in angle length is also built in to the change-to-ramp-mode and change-from-ramp-mode transition.

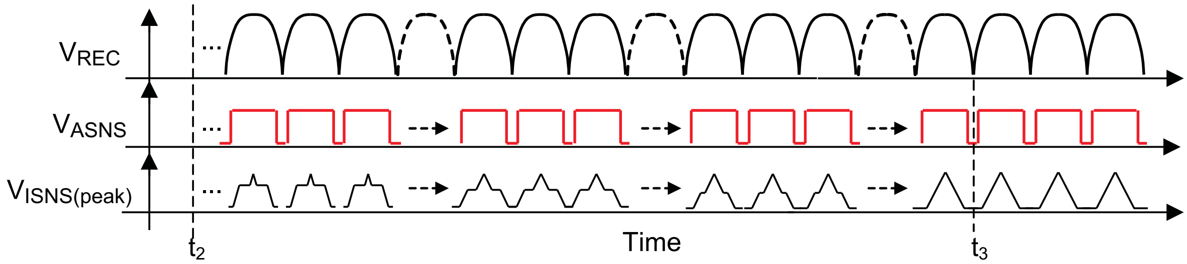


Figure 11. Transition Stages of the Controlled Reference

Dimming Mode

When the conduction angle is reduced below the 70% threshold the output is controlled with a DC reference level based on: (angle sense rise to fall length count) / 2 + 35, ≤ 63. The control level clamps at both the high and low end of the range to increase TRIAC dimmer compatibility. Rather than adding passive (heat generating) hold current or implementing other means to draw sufficient current from the TRIAC dimmer to maintain optimal operation, the TPS92075 implements a translation that shifts output demand higher, lower in the dimming range. The effect is that more current is drawn at low angles, eliminating the need for hold circuitry. A net reduction in light output occurs because of the energy transfer relation. As the phase-dimmer conduction decreases, the time during which the converter can provide output power during each cycle decreases, and a reduction in light output follows.

Triac Asymmetry Balancing

Triacs are two silicon-controlled rectifiers (SCRs) configured so that one device conducts current in the positive AC cycle and the other device conducts current in the negative AC cycle. It is common for the devices to have different trigger levels and this leads to differences in conduction angle for each of the positive and negative AC cycles. The amount of variation between each cycle varies greatly between dimmer brands, makes and models. In all single stage TRIAC compatible dimming solutions, the ability of the converter to provide output power depends on the length of the conduction time. If the output current demand remains constant during each cycle and if there is a difference in TRIAC conduction angles, the result is a difference in light output for each cycle.

The TPS92075 incorporates a balancing algorithm to reduce the difference in LED current (and light output) between cycles that have a conduction angle difference greater than 20%.

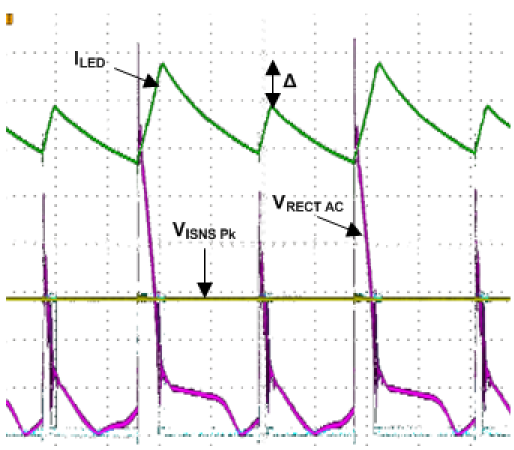


Figure 12. LED current variation, Constant Reference

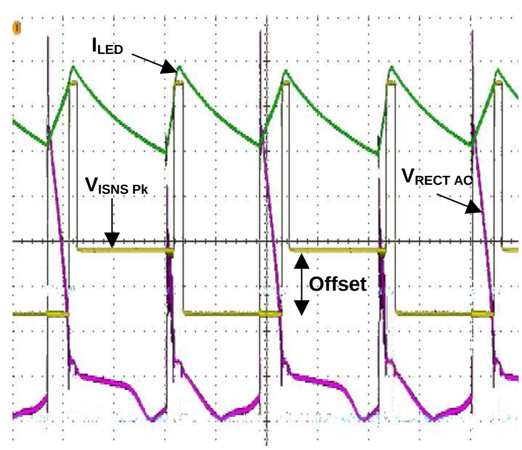


Figure 13. LED current variation, TPS92075 with Balancing

When the difference in conduction becomes greater than 20%, the controller begins to adjust the controller reference line-cycle by line-cycle to balance the energy provided to the LEDs. In this example the difference in conduction angles is 800 µs and flicker was visible with the constant reference (Figure 12). With the TPS92075 balancing feature the peaks in the LED current have been equalized and flicker cannot be seen (Figure 13).

Lossless or 'Active' Hold

When used in the buck configuration, the converter enters a drop-out condition each cycle as the input AC line drops below the LED stack voltage. When this occurs, a resonance in the input filter can be excited causing a ring in the input current at the end of the conduction cycle. This can lead to output flicker if not controlled. One method of eliminating this is to modify the control method to send the energy that would otherwise affect the ringing to the output. To do this, the controller increases the output set-point at the end of each cycle after the ASNS fall (< 0.5 V) signal is received. The increse in set point can be seen in Figure 14.

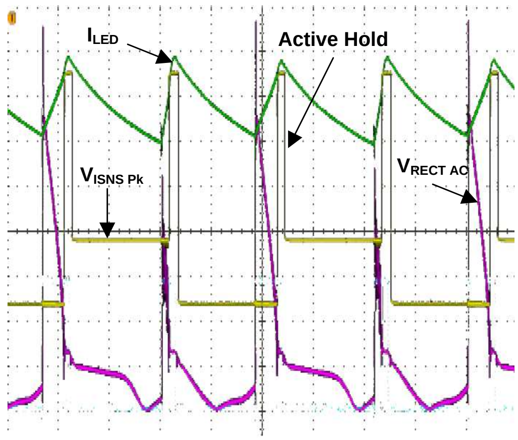


Figure 14. TPS92075 Reference Control - Active Hold

Another benefit of the active hold is that a low impedance path is created to the LED stack. This ensures the current demand is as high as possible for as long as possible before the converter fully enters drop-out.

Active Hold, ASNS, and Buck-Boost Topology

When using the converter in a buck-boost configuration attention must be given to the configuration of the ASNS signal to ensure there is some added delay in the signal crossing the 0.5V threshold. Because the converter can continue to provide energy to the output below the LED stack voltage, it is best to configure the ASNS signal to fall when the rectified AC signal is as close to zero as possible.

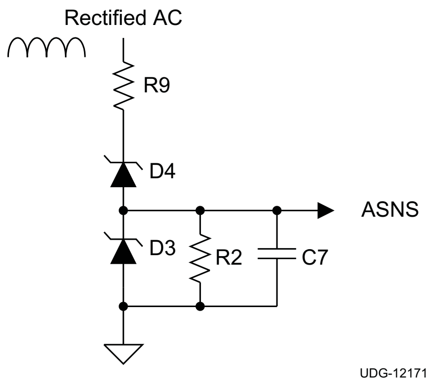


Figure 15. Buck-Boost Angle Sense Circuit

This can be implemented by adding an additional zener and capacitor on the ASNS pin. Capacitance between 2200 pF and 4700 pF provides a good balance between allowing the ASNS signal to fall below 0.5V and extending the ASNS time. The D4 zener allows the ASNS signal to be widened further. This component can be the same type of zener selected for the input voltage linear supply, in many prototyping examples a 15V zener diode is used. The buck-boost configuration tends to provide greater dimmer compatibility because of its ability to continue to draw power below the LED stack. This increases the time the converter can provide output current and increases the light output at a given dimmer setting. A higher light output for a given dimmer setting is an important control technique which increases the probability that the design will remain flicker-free over its lifetime and range of installations. This trade-off between dimming ratio, dimmer compatibility and component count make the components a desirable addition.

Loss of Angle Sense

When using a dimmer that can control the phase angle to very short conduction times (< 250 µs), the ASNS signal may become so narrow that the controller cannot determine its length. When this occurs the controller simply sets the reference to a default value 0.33V (42/127) and waits for the ASNS signal to return.

A simplified version of the TPS92075 circuit can be implemented by grounding the ASNS signal if minimum component count and size are essential design criteria. In this configuration balancing, ramp mode and active hold are not implemented. The output is controlled with a default, static reference of 0.394V (50/127). If used in conjunction with an on-time clamp, good dimming and power factors (>0.9) can still be achieved.

Thermal Shutdown

The TPS92075 includes thermal shutdown protection. If the die temperature reaches approximately 160°C the device stops switching (GATE pin low). When the die temperature cools to approximately 140°C, the device resumes normal operation.

If thermal fold back is desired at levels below the IC thermal shut down, application circuits have been created to implement this feature. The simplest of these is the addition of a thermistor in the off-time circuitry.

Thermal Foldback

To implement thermal foldback, adjust the resistance of an existing circuit resistor with the use of an NTC (negative temperature coefficient) thermistor.

For example, a resistor combination creating a dominant effect when the thermistor reaches the desired temperature and resistance can be incorporated by paralleling a thermistor and another resistor with R10 (Figure 17). This circuit option creates a shorter on-time as the temperature increases, reducing the output current. The use of a thermistor in these types of circuit implementations is simple and saves costly added circuitry and additional device pins.

Overvoltage Protection (OVP)

The implementation of overvoltage protection is simple and built-in if using a two-coil magnetic (coupled inductor) to derive V_{CC}. If the LED string is opened the auxiliary V_{CC} rises and reaches the $V_{CC(OVP)}$ trip point. This action disables and grounds the gate pin, preventing the converter from switching. The converter remains disabled until V_{CC} drops 0.5V after a 1 second time-out. If an inductor is used, implement other discrete circuits to disable the converter.

Output Bulk Capacitor

The required output bulk capacitor, C_{BULK}, stores energy during the input voltage zero crossing interval and limits twice the line frequency ripple component flowing through the LEDs. Equation 1 describes the calculation of the of output capacitor value.

$$C_{BULK} \geq \frac{P_{IN}}{4\pi \times f_L \times R_{LED} \times V_{LED} \times I_{LED(ripple)}}$$

where

- R_{LED} is the dynamic resistance of LED string
- $I_{LED(ripple)}$ is the peak to peak LED ripple current
- and f_L is line frequency (1)

R_{LED} is found by computing the difference in LED forward voltage divided by the difference in LED current for a given LED using the manufacturer's V_F vs. I_F curve. For a rough initial estimate a typical value of 0.25Ω per LED can be used. More detail can be found in Application Note 1656.

In typical applications, the solution size becomes a limiting factor and dictates the maximum dimensions of the bulk capacitor. When selecting an electrolytic capacitor, manufacturer recommended de-rating factors should be applied based on the worst case capacitor ripple current, output voltage and operating temperature to achieve the desired operating lifetime. It should also be a consideration to provide a minimum load at the output of the driver to discharge the capacitor after the power is switched off or during LED open circuit failures.

Design Guidelines

This TPS92075 application design requires the selection of components for the power conversion stage and angle sensing. Output inductor, sense resistor and switching frequency are the key aspects of the power stage design. Another important consideration is the inclusion of an on-time clamp. The combination of the line voltage going to zero each cycle and the hysteretic control method can lead to large increases in current draw at the start and end of each cycle. The components required for the on-time clamp are very inexpensive and return results that make their inclusion a common choice for LED driver designers. This simplified design procedure assumes the use of an on-time clamp in the design.

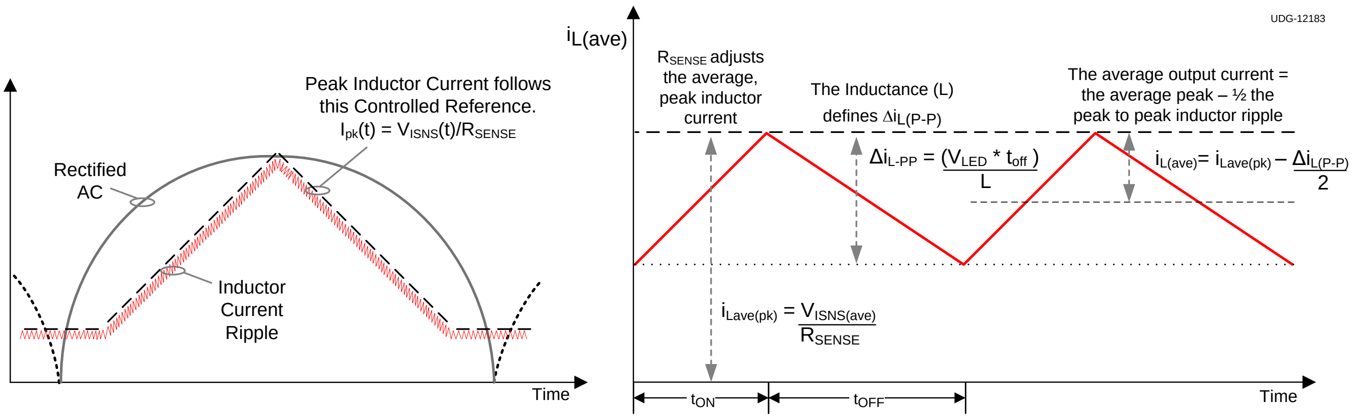


Figure 16. TPS92075 Output Current Control

The mode of operation that determines average continuous output current is non-dimming, during which the reference is a triangular waveform.

The device uses the controller reference every switching cycle to set the peak current through the main switch and sense resistor. The average value of this reference and the inductor ripple current can be used to calculate the average output current. Another consideration is the length of time the converter is providing power to the LEDs. A conversion factor (CF) that accounts for a lower level of power conversion at the ends of each cycle is used to provide a more accurate sense resistor value. The lower level of power conversion in these areas also helps to increase the power factor. For the R_{SENSE} calculation use $V_{ISNS\ (ave)}$ = 0.433V (55/127). The CF calculation involves computing the normalized time length of the angle sense pulse using a formula shown in Equation 3. Simplified design expressions are provided below. For a more comprehensive approach refer to the TPS92075 Design Spreadsheet.

To calculate R_{SENSE}, use Equation 2.

$$R_{SENSE} = \left(\frac{V_{ISNS(ave)}}{I_{LED} + \frac{\Delta i_{L(P-P)}}{2}} \right) \times CF \tag{2}$$

To calculate the conversion factor, use Equation 3.

$$CF = 1 - \left(\frac{\sin^{-1}\left(\frac{V_{LED}}{\sqrt{2} \times V_{RMS}} \right)}{90} \times \frac{3}{2} \right) \tag{3}$$

To calculate inductance ripple, use Equation 4.

$$\Delta i_{L(P-P)} = \left(\frac{V_{LED} \times t_{OFF}}{L} \right) \tag{4}$$

To calculate the constant off-time, use Equation 5

$$t_{OFF} = \left(\ln\left(-\left(\frac{1.2}{V_{VCC}} - 1 \right) \right) \right) \times \left(-C_{TOFF} \times R_{COFF} \right) \tag{5}$$

To calculate the average switching frequency, use Equation 6.

$$f_{SW} = \left(\frac{1}{t_{OFF} + \left(t_{OFF} \times CF \right)} \right) \tag{6}$$

On-Time Clamp

The use of an on-time clamp (Figure 17) provides a soft-start and soft-stop action to the conversion each line cycle. It also adds a means to control the energy in these conversion areas to optimize dimming performance. For example, cutting the energy conversion in these areas in half maintains strong current pull through these critical TRIAC regions, but is not high enough to excite circuit resonances.

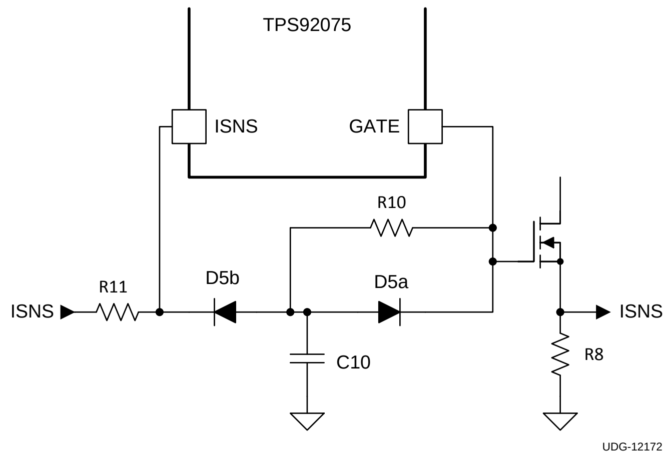


Figure 17. On-time Clamp Circuitry

The circuit uses the gate drive output to generate a ramp. The ramp increases at a rate to reach the current sense trip point at the desired maximum conduction time. The gate signal, resistor R10 and capacitor C10 create the ramp. Diode D5b resets the ramp for each switching cycle. Resistor R11 provides an impedance so this signal can override ISNS.

In the regions at the start and end of a line cycle the current sense reference is controlled to 0.173V (22/127). To select an R-C to reach this point in the desired time use Equation 7. A good starting estimate for the maximum on-time clamp is ~t_{OFF}/2 . For example, choosing 33 nF as the value of capacitor C10, and assuming $V_{GATE} \approx V_{CC}$, R10 ($R_{ton(max)}$) is calculated in Equation 7.

$$R_{ton(max)} = \frac{t_{OFF}}{2 \times \left[\ln\left(-\left(\frac{0.173}{V_{GATE}} - 1 \right) \right) \right] \times -C_{ton(max)}} \tag{7}$$

Angle Sense Circuitry and Minimum ASNS Signal Length

If implementing a buck converter, select the divider so the falling 0.5V ASNS threshold is reached when the rectified AC voltage is at the LED stack voltage. For example, if the LED stack is 20V and the top resistor is 400 kΩ, the bottom resistor should be 10.25 kΩ to provide a falling ASNS signal at 0.5V when the rectified AC reaches 20V. A 20V ASNS falling signal will mean a 40V ASNS rising threshold because of the 2:1 hysteresis. This will provide an ASNS signal length of ~7.4 ms, adequate to activate the ramp mode when not connected to a dimmer. This buck configuration and ASNS divider will activate the hold feature each time the rectified AC reaches the LED stack voltage. This method is shown in Figure 18. Regardless of the ASNS connection method used, the divider must ensure an adequate angle sense length (t_{ASNS} > 5.9 ms) when non-dimming to activate the creation of the ramp if this is desired. For example, if a straight resistor divider (Figure 18) is implemented and the design LED stack is more than 42V, the ASNS conduction time may not be adequate to activate the use of the ramp reference.

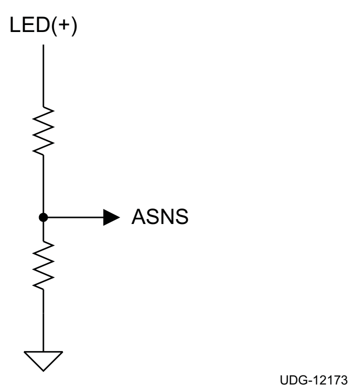


Figure 18. Angle Sense for Low Voltage Buck Applications

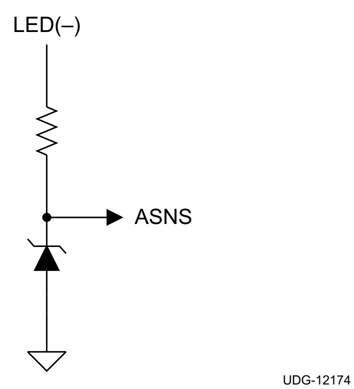


Figure 19. Angle Sense for Buck Applications up to 65V

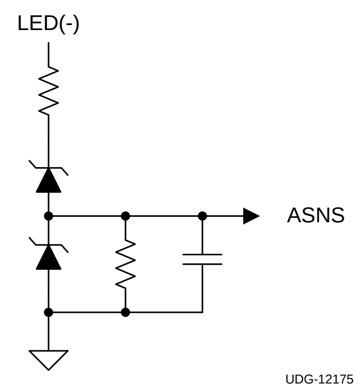


Figure 20. Angle Sense for Buck-Boost Applications

For LED stack voltages between 3V and 65V, use an alternate method that senses from LED(–). Because LED(–) reaches ground each line cycle, the absolute ASNS comparison limits of 0.5V and 1V can be used, providing extra conduction time for the ASNS signal as shown in Figure 19. Beyond a ~65V LED stack, alternate ASNS methods utilizing a bridge tap can be used. For buck-boost applications, implement the circuit shown in Figure 20.

A capacitor on the ASNS pin may be required, depending on operating conditions.

EMI Filtering: AC versus DC side of the rectifier bridge

The TPS92075 requires a minimal amount of EMI filtering to pass conducted and radiated emissions levels to comply with agency requirements. Applications have been tested with the filter on the AC or DC side of the diode bridge and have obtained passing results. The use of an R-C snubber to damp filter resonances and optimize TRIAC compatibility is strongly recommended. The EMI filter design involves optimizing several factors and design considerations, including:

- the use of ‘X’ versus non-X rated filter capacitors
- the use of ceramic versus film capacitors
- component rating requirements when on the AC or DC side of the diode bridge
- filtering on the AC or DC side of the bridge and the effect on the TRIAC firing angle and dimming range
- snubber time constant and position in the design schematic
- filter design choices and audible noise

Application Circuits

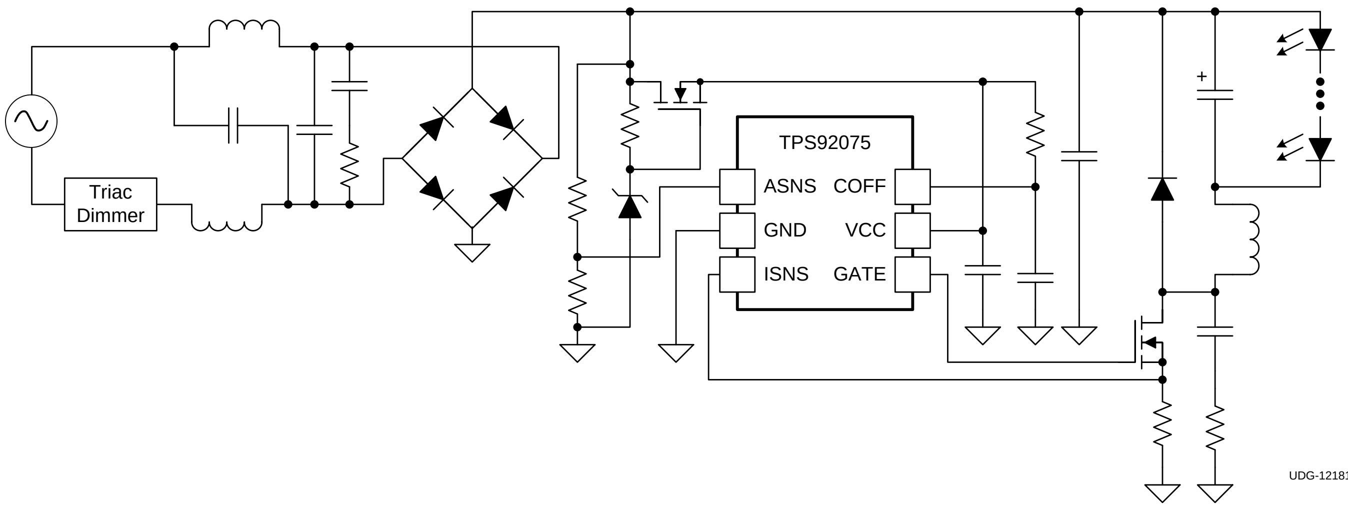


Figure 21. TPS92075 Application Circuit for Buck Topology with AC Side Filter

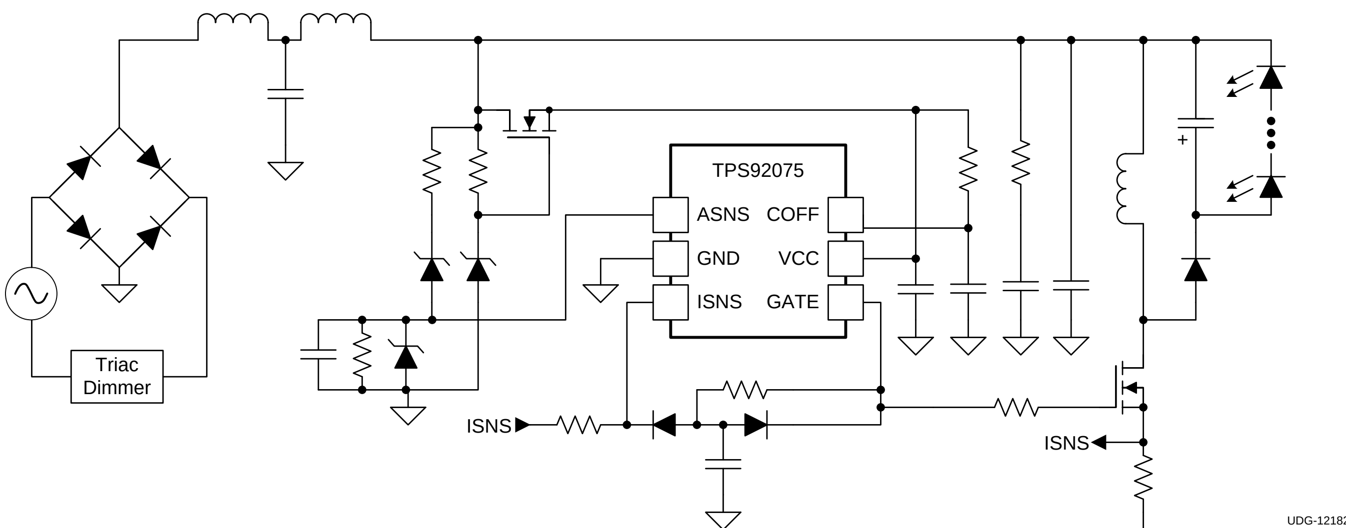


Figure 22. TPS92075 Application Circuit for Buck-Boost Topology with DC Side Filter

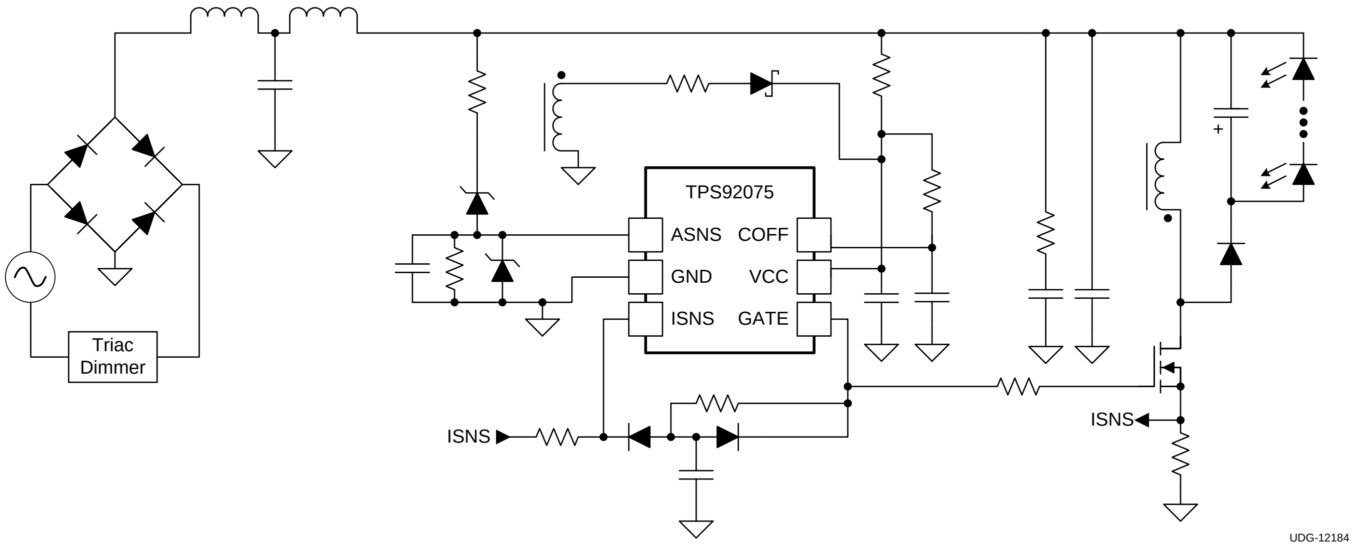


Figure 23. TPS92075 Application Circuit for Buck-Boost with Resistive Start-up and AUX Supply

REVISION HISTORY

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS92075D/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	T92075	Samples
TPS92075DDC/NOPB	ACTIVE	SOT-23-THIN	DDC	6	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SN8B	Samples
TPS92075DDCR/NOPB	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	SN8B	Samples
TPS92075DR/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	T92075	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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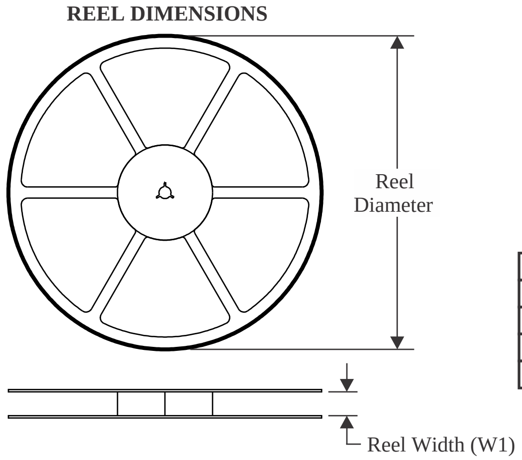
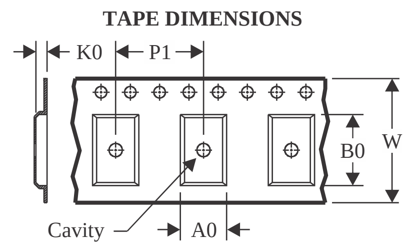
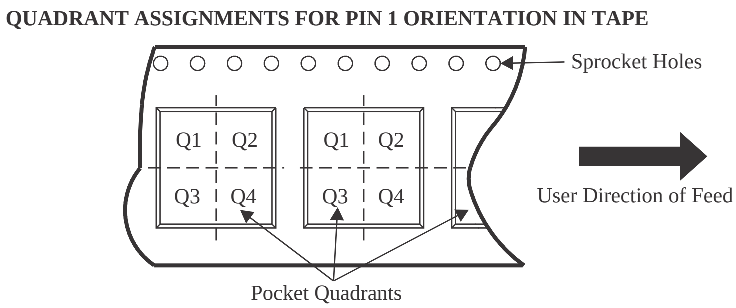
TAPE AND REEL INFORMATION





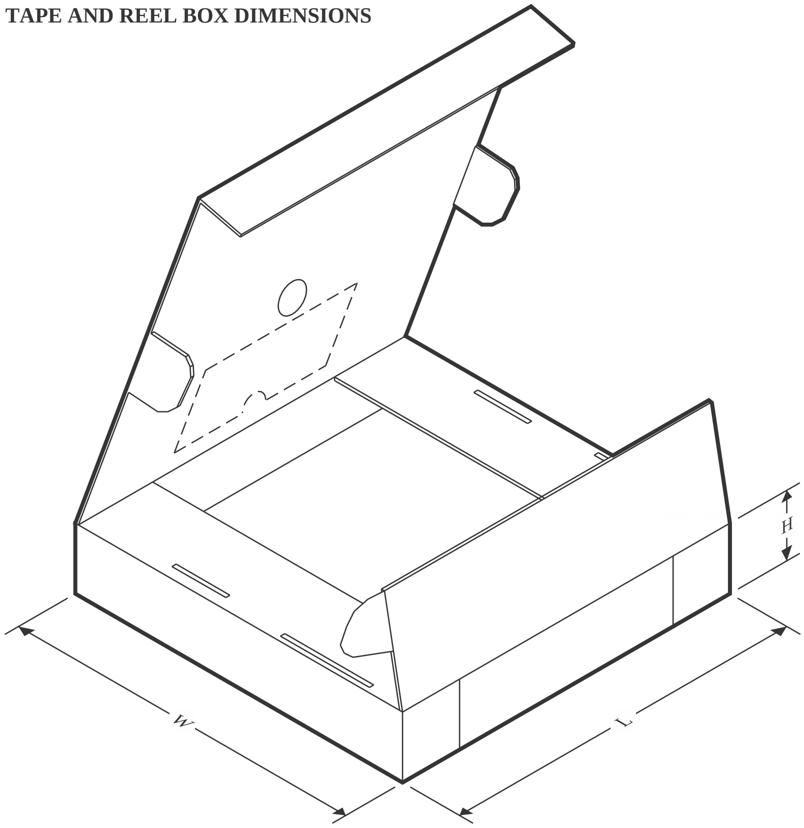
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS92075DDC/NOPB	SOT-23-THIN	DDC	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS92075DDCR/NOPB	SOT-23-THIN	DDC	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS92075DR/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

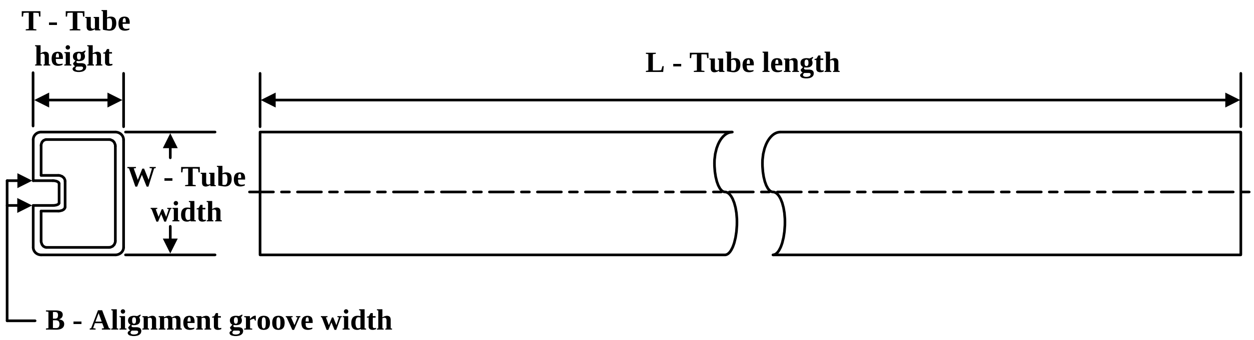
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

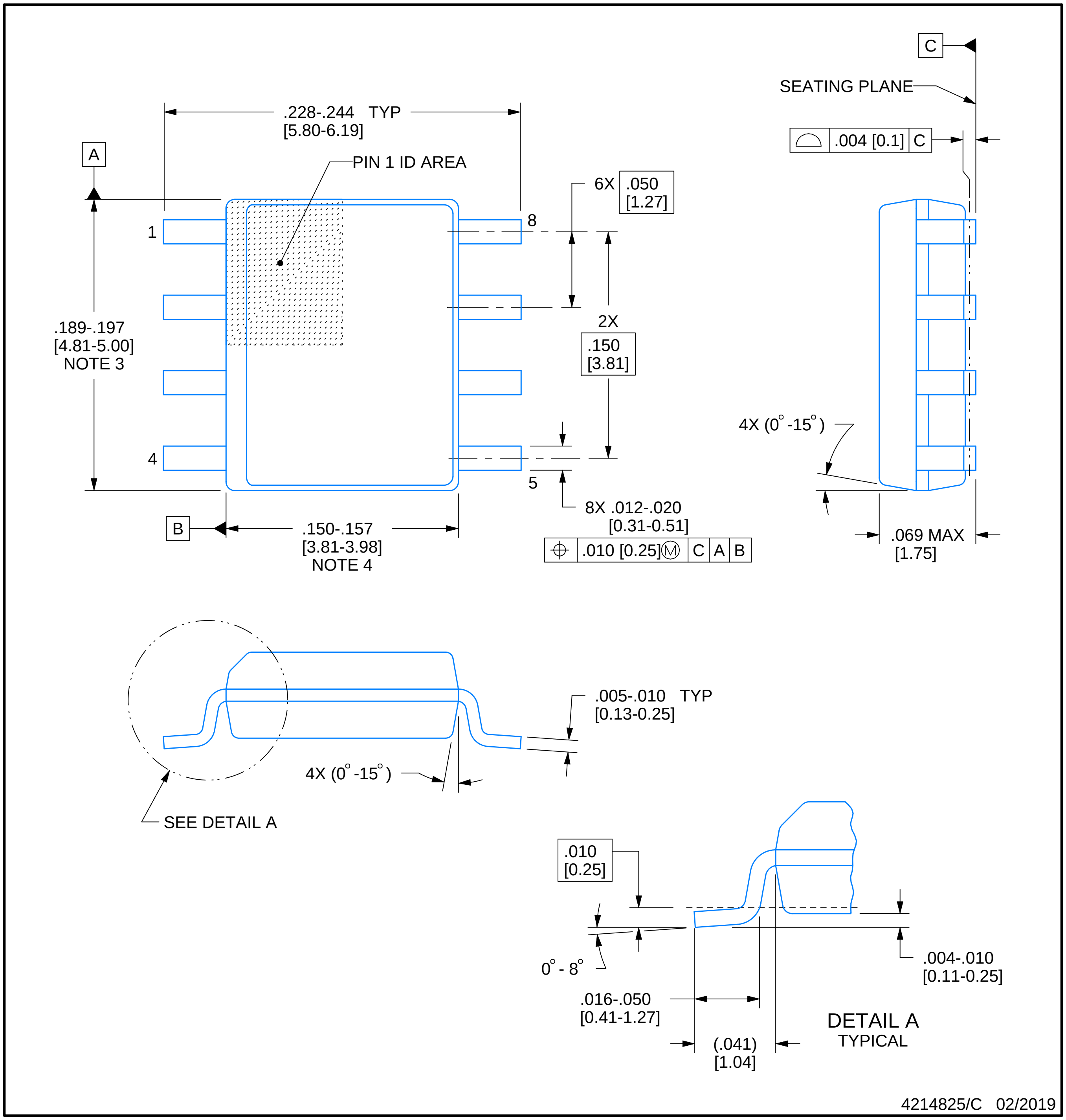
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS92075DDC/NOPB	SOT-23-THIN	DDC	6	1000	208.0	191.0	35.0
TPS92075DDCR/NOPB	SOT-23-THIN	DDC	6	3000	208.0	191.0	35.0
TPS92075DR/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



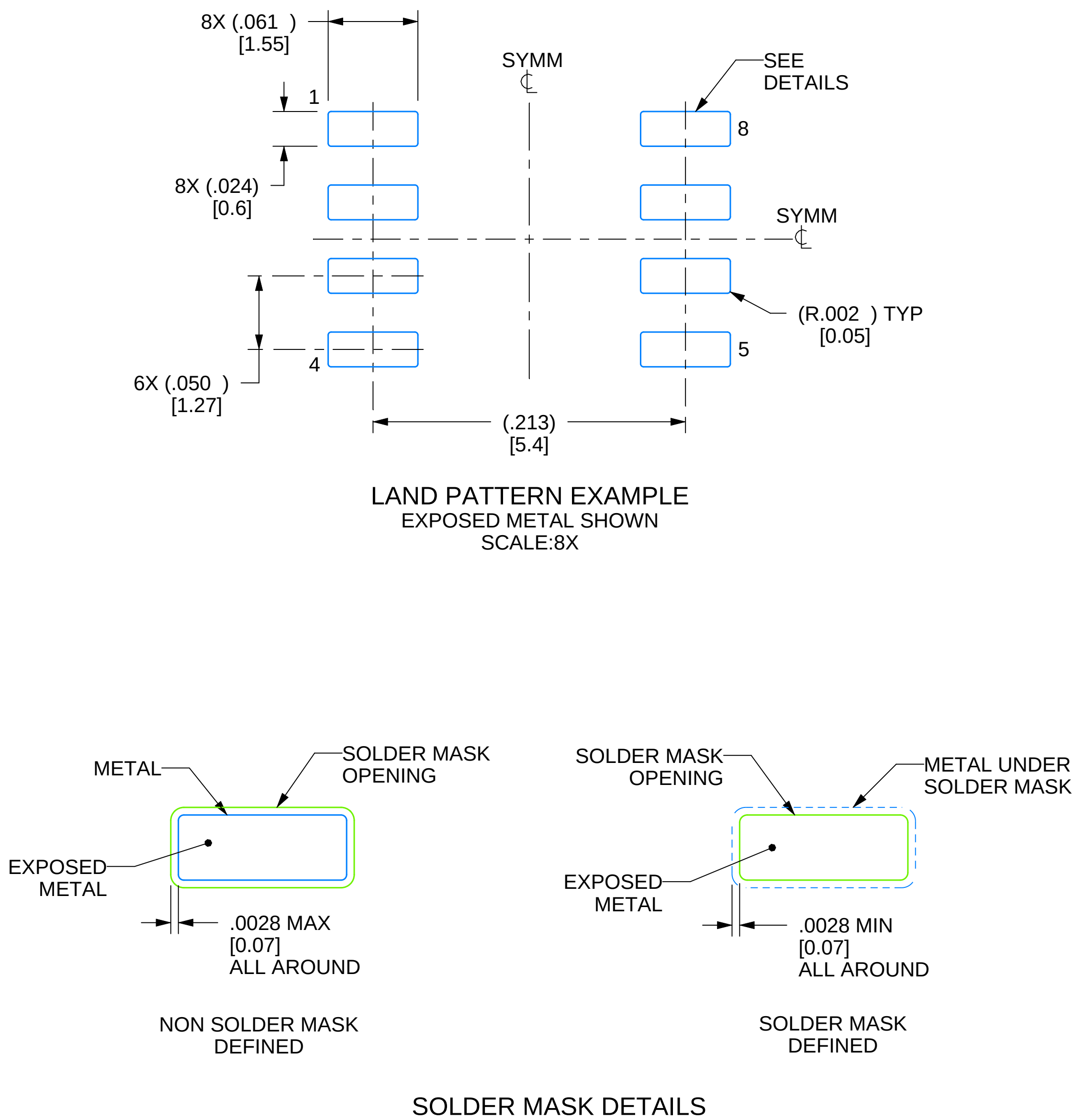
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS92075D/NOPB	D	SOIC	8	95	495	8	4064	3.05



NOTES:

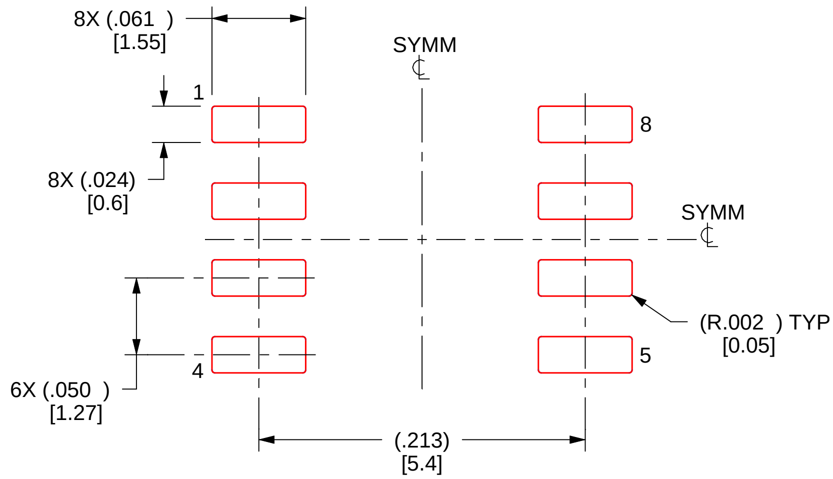
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

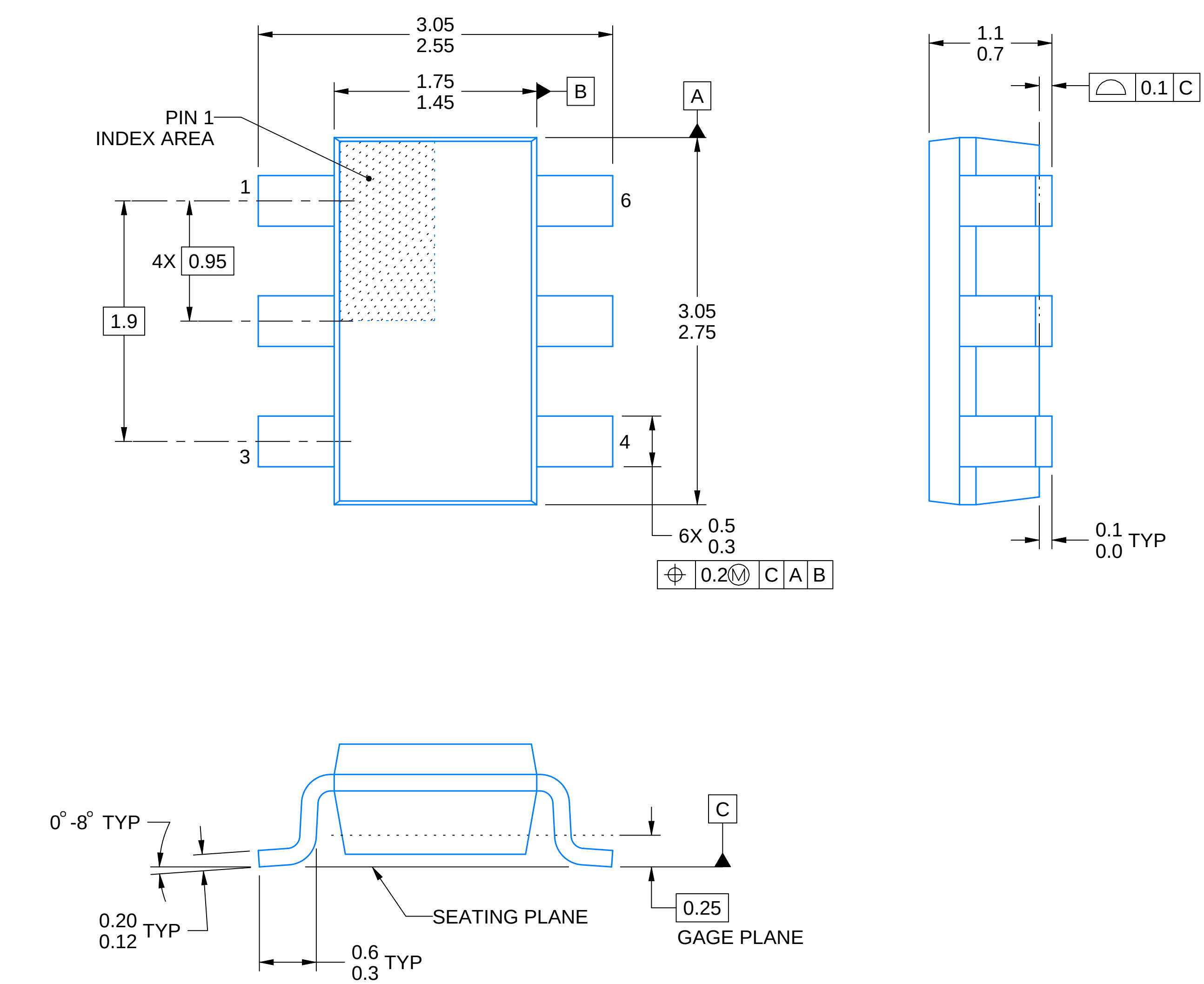
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

SOT-23 - 1.1 max height

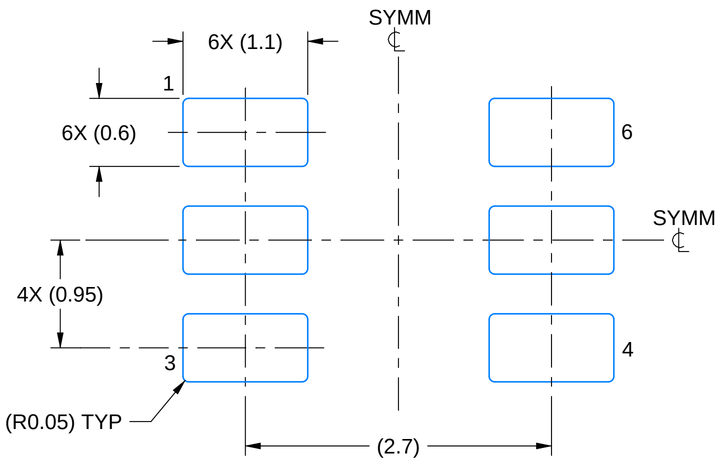
SMALL OUTLINE TRANSISTOR



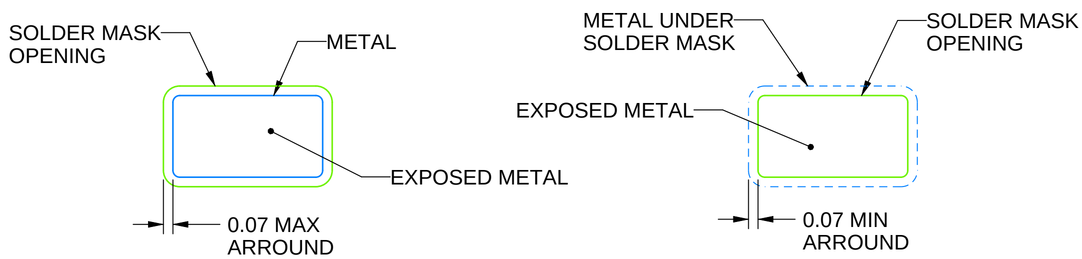
4214841/C 04/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED

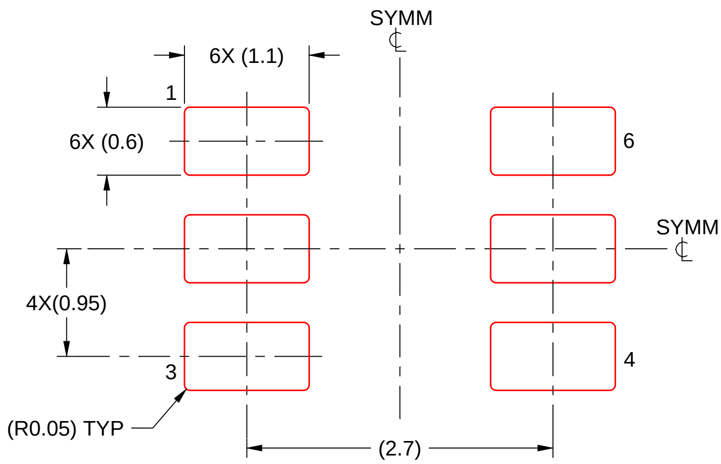
SOLDER MASK
DEFINED

SOLDERMASK DETAILS

4214841/C 04/2022

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214841/C 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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