具有逻辑侧独立电源引脚的 RS-232 收发器

查询样片: **TRS3253E-EP**

特性

- 用于实现与逻辑侧电压低至 **1.8V** 的混合电压系统兼容的 V_L 引脚
- **RIN** 输入和 **DOUT** 输出上的增强型静电放电 **(ESD)** 保护
  - **±8kV IEC 61000-4-2** 空气间隙放电
  - **±8kV IEC 61000-4-2** 接触放电
  - **±15kV** 人体模型
- **300μA** 低电源电流
- 额定 **1000kbps** 数据速率
- 自动断电增强特性

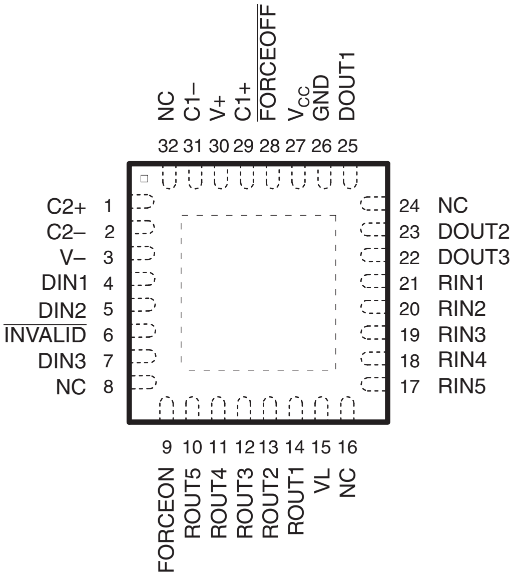
应用范围

- 手持设备
- 掌上电脑 **(PDA)**
- 手机
- 电源供电类设备
- 数据线

支持国防、航空航天、和医疗应用

- 受控基线
- 同一组装和测试场所
- 同一制造场所
- 支持军用（**-55°C** 至 **125°C**）温度范围
- 延长的产品生命周期
- 延长的产品变更通知
- 产品可追溯性

RSM PACKAGE
(TOP VIEW)



NC – No internal connection

说明

TRS3253E 是一款 3 驱动器和 5 接收器 RS-232 接口器件，此器件具有针对混合信号运行的独立电源引脚。 使用 IEC 61000-4-2 空气间隙放电方法，IEC 61000-4-2 接触放电方法和人体模型分别保护全部的 RS-232 输入和输出不受 ±8kV，±8kV 和 ±15kV 电压的影响。

在由一个 3.3V 电源供电时，电荷泵只需 4 个小型 0.1μF 电容器即可运行。 TRS3253E 在保持 RS-232 兼容输出电平的同时，运行数据速率可高达 1000kbps。

TRS3253E 具有一个独特的 V_L 引脚，此引脚可实现混合逻辑电压系统内的运行。 可通过 V_L 引脚对驱动器输入 (DIN) 和接收器输出 (ROUT) 逻辑电平进行设定。 这在与低压微控制器或通用异步收发器 (UART) 对接时免除了对于额外电压电平位移器的需要。 TRS3253E 采用节省空间的四方扁平无引线 (QFN) 封装 (4mm × 4mm RSM)。

English Data Sheet: SLLSEF5

说明（继续）

自动断电增强功能可在 FORCEON 和 $\overline{\text{FORCEOFF}}$ 为高电平时被禁用。 在自动断电增强功能被启用时，此器件在任一接收器或驱动器输入上被施加有效信号时被自动激活。 如果任一接收器输入电压大于 2.7V 或小于 -2.7V，或者介于 -0.3V 至 0.3V 之间的时间少于 30μs，INVALID 为高电平（有效数据）。 如果全部接收器输入电压在 -0.3V 至 0.3V 之间的时间超过 30μs，INVALID 为低电平（无效数据）。 对于接收器输入电平，请参考 Figure 6。

ORDERING INFORMATION[1]

T_J	PACKAGE	ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
–55°C to 125°C	QFN - RSM	TRS3253EMRSMREP	RS53EP	V62/13621-01XE

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

FUNCTION TABLES

Each Driver[1]

INPUTS				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	$\overline{\text{FORCEOFF}}$	TIME ELAPSED SINCE LAST RIN OR DIN TRANSITION		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown plus disabled
H	H	H	X	L	
L	L	H	<30 µs	H	Normal operation with auto-powerdown plus enabled
H	L	H	<30 µs	L	
L	L	H	>30 µs	Z	Powered off by auto-powerdown plus feature
H	L	H	>30 µs	Z	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

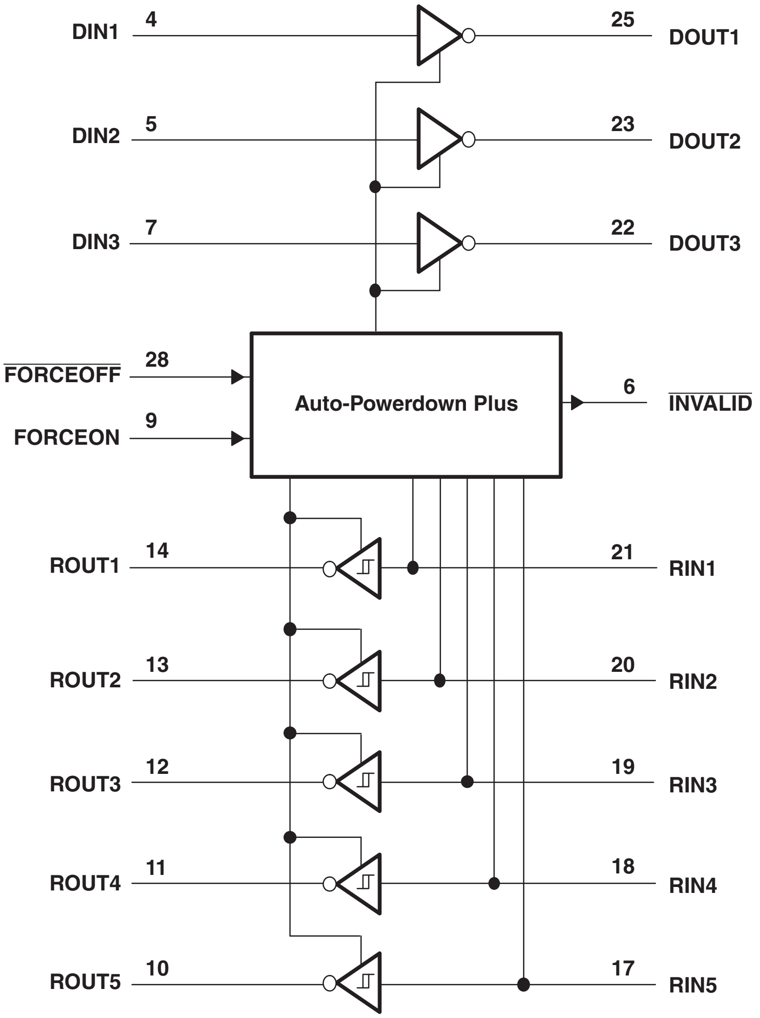
Each Receiver[1]

INPUTS			OUTPUTS	RECEIVER STATUS
RIN1–RIN5	$\overline{\text{FORCEOFF}}$	TIME ELAPSED SINCE LAST RIN OR DIN TRANSITION	ROUT1-ROUT5	
X	L	X	Z	Powered off
L	H	<30 µs	H	Normal operation with auto-powerdown plus disabled/enabled
H	H	<30 µs	L	
Open	H	<30 µs	H	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTIONAL BLOCK DIAGRAM



TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	**RSM**	
C1+, C2+	29, 1	Positive terminal of the voltage-doubler charge-pump capacitor
V+	30	5.5-V supply generated by the charge pump
C1–, C2-	31, 2	Negative terminal of the voltage-doubler charge-pump capacitor
INVALID	6	Invalid Output Pin
V–	3	–5.5-V supply generated by the charge pump
DIN1 DIN2 DIN3	4 5 7	Driver inputs
ROUT5 - ROUT1	10, 11, 12, 13, 14	Receiver outputs. Swing between 0 and V_L.
V_L	15	Logic-level supply. All CMOS inputs and outputs are referenced to this supply.
RIN5-RIN1	17, 18, 19, 20, 21	RS-232 receiver inputs
DOUT3 DOUT2 DOUT1	22 23 25	RS-232 driver outputs
GND	26	Ground
V_{CC}	27	3-V to 5.5-V supply voltage
$\overline{\text{FORCEOFF}}$	28	Powerdown Control input (Refer to Truth Table)
FORCEON	9	Powerdown Control input (Refer to Truth Table)

ABSOLUTE MAXIMUM RATINGS[1]

over junction temperature range (unless otherwise noted)

			MIN	MAX	UNIT
	V_{CC} to GND		–0.3	6	V
	V_L to GND		–0.3	V_{CC} + 0.3	V
	V+ to GND		–0.3	7	V
	V– to GND		0.3	–7	V
	V+ + |V–|[2]			13	V
V_I	Input voltage	DIN, $\overline{\text{FORCEOFF}}$ to GND, FORCEON to GND	–0.3	6	V
		RIN to GND		±25	
V_O	Output voltage	DOUT to GND		±13.2	V
		ROUT	–0.3	V_L + 0.3	
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2) V+ and V– can have maximum magnitudes of 7 V, but their absolute difference cannot exceed 13 V.

THERMAL INFORMATION

THERMAL METRIC[1]		TRS3253E-EP	UNITS
		RSM	
		32 PINS	
θ_{JA}	Junction-to-ambient thermal resistance[2]	37.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance[3]	30.1	
θ_{JB}	Junction-to-board thermal resistance[4]	7.8	
ψ_{JT}	Junction-to-top characterization parameter[5]	0.4	
ψ_{JB}	Junction-to-board characterization parameter[6]	7.6	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance[7]	2.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.

(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).

(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).

(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

				MIN	MAX	UNIT
V_{CC}	Supply voltage			3	5.5	V
V_L	Supply voltage			1.65	V_{CC}	V
	Input logic threshold low	DIN, $\overline{\text{FORCEOFF}}$, FORCEON	V_L = 3 V or 5.5 V		0.8	V
			V_L = 2.3 V		0.6	
			V_L = 1.65 V		0.5	
	Input logic threshold high	DIN, $\overline{\text{FORCEOFF}}$, FORCEON	V_L = 5.5 V	2.4		V
			V_L = 3 V	2.0		
			V_L = 2.7 V	1.4		
			V_L = 1.95 V	1.25		
	Junction temperature			–55	125	°C
	Receiver input voltage			–25	25	V

ELECTRICAL CHARACTERISTICS(1)

over junction temperature range, V_{CC} = V_L = 3 V to 5.5 V, C1–C4 = 0.1 μF (tested at 3.3 V ± 10%), C1 = 0.047 μF, C2–C4 = 0.33 μF (tested at 5 V ± 10%) (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(2)	MAX	UNIT
I_I	Input leakage current	$\overline{\text{FORCEOFF}}$, FORCEON			±0.01	±2.9	μA
I_{CC}	Supply current (T_J = 25°C)	Auto-powerdown plus disabled	No load, $\overline{\text{FORCEOFF}}$ and FORCEON at V_{CC}		0.5	1.11	mA
		Powered off	No load, $\overline{\text{FORCEOFF}}$ at GND		1	10	μA
		Auto-powerdown plus enabled	No load, $\overline{\text{FORCEOFF}}$ at V_{CC}, FORCEON at GND, All RIN are open or grounded		1	10	

(1) Testing supply conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.15 V; C1–C4 = 0.22 μF at V_{CC} = 3.3 V ± 0.3 V; and C1 = 0.047 μF and C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_J = 25°C.

ESD PROTECTION

PARAMETER	TEST CONDITIONS	TYP	UNIT
RIN, DOUT	Human-Body Model	±15	kV
	IEC 61000-4-2 Air-Gap Discharge	±8	
	IEC 61000-4-2 Contact Discharge	±8	

RECEIVER SECTION

Electrical Characteristics

over junction temperature range, V_{CC} = V_L = 3 V to 5.5 V, C1–C4 = 0.1 μF (tested at 3.3 V ± 10%), C1 = 0.047 μF, C2–C4 = 0.33 μF (tested at 5 V ± 10%), T_A = T_{MIN} to T_{MAX} (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
I_{off}	Output leakage current	ROUT, receivers disabled			±0.05	±25	μA
V_{OL}	Output voltage low	I_{OUT} = 1.6 mA				0.4	V
V_{OH}	Output voltage high	I_{OUT} = –1 mA		V_L – 0.6	V_L – 0.1		V
V_{IT-}	Input threshold low	T_J = 25°C	V_L = 5 V	0.8	1.2		V
			V_L = 3.3 V	0.6	1.5		
V_{IT+}	Input threshold high	T_J = 25°C	V_L = 5 V		1.8	2.4	V
			V_L = 3.3 V		1.5	2.4	
V_{hys}	Input hysteresis				0.5		V
	Input resistance	T_J = 25°C		3	5	7	kΩ

(1) Typical values are at V_{CC} = V_L = 3.3 V, T_J = 25°C

Switching Characteristics

over junction temperature range, V_{CC} = V_L = 3 V to 5.5 V, C1–C4 = 0.1 μF (tested at 3.3 V ± 10%), C1 = 0.047 μF, C2–C4 = 0.33 μF (tested at 5 V ± 10%), T_J = T_{MIN} to T_{MAX} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP[1]	UNIT
t_{PHL}	Receiver propagation delay	Receiver input to receiver output, C_L = 150 pF	0.15	μs
t_{PLH}			0.15	
$t_{PHL} - t_{PLH}$	Receiver skew		50	ns
t_{en}	Receiver output enable time	From $\overline{\text{FORCEOFF}}$	200	ns
t_{dis}	Receiver output disable time	From $\overline{\text{FORCEOFF}}$	200	ns

(1) Typical values are at V_{CC} = V_L = 3.3 V, T_J = 25°C.

DRIVER SECTION

Electrical Characteristics

over junction temperature range, $V_{CC} = V_L = 3$ V to 5.5 V, C1–C4 = 0.1 µF (tested at 3.3 V ± 10%), C1 = 0.047 µF, C2–C4 = 0.33 µF (tested at 5 V ± 10%), $T_J = T_{MIN}$ to T_{MAX} (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
V_{OH}	Output voltage swing	All driver outputs loaded with 3 kΩ to ground, V_{CC}= 3.1V to 5.5V	±5	±5.4		V
r_O	Output resistance	V_{CC} = V+ = V– = 0, Driver output = ±2 V	300	10M		Ω
I_{OS}	Output short-circuit current	$V_{T\_OUT} = 0$			±60	mA
I_{OZ}	Output leakage current	V_{T_OUT} = ±12 V, $\overline{\text{FORCEOFF}}$ = GND, V_{CC} = 3 V to 3.6 V			±25	µA
		V_{T_OUT} = ±12 V, $\overline{\text{FORCEOFF}}$ = GND, V_{CC} = 4.5 V to 5.5 V				
	Driver input hysteresis				0.5	V
	Input leakage current	DIN, $\overline{\text{FORCEOFF}}$, FORCEON		±0.01	±2.9	µA

(1) Typical values are at $V_{CC} = V_L = 3.3$ V, $T_J = 25$°C

Timing Requirements

over junction temperature range, $V_{CC} = V_L = 3$ V to 5.5 V, C1–C4 = 0.1 µF (tested at 3.3 V ± 10%), C1 = 0.047 µF, C2–C4 = 0.33 µF (tested at 5 V ± 10%), $T_j = T_{MIN}$ to T_{MAX} (unless otherwise noted)

PARAMETER				MIN	TYP[1]	MAX	UNIT
	Maximum data rate	R_L = 3 kΩ, C_L = 200 pF, One driver switching		1000			kbps
	Time-to-exit powerdown	$\lvert V_{T\_OUT} \rvert$ > 3.7 V			100		µs
$\lvert t_{PHL} - t_{PLH} \rvert$	Driver skew[2]				100		ns
	Transition-region slew rate	V_{CC} = 3.3 V, T_j = 25°C, R_L = 3 kΩ to 7 kΩ, Measured from 3 V to –3 V or –3 V to 3 V	C_L = 150 pF to 1000 pF	15		150	V/µs

(1) Typical values are at $V_{CC} = V_L = 3.3$ V, $T_J = 25$°C.

(2) Driver skew is measured at the driver zero crosspoint.

AUTO-POWERDOWN SECTION

Electrical Characteristics

over recommended ranges of supply voltage and junction temperature (unless otherwise noted) (see Figure 7)

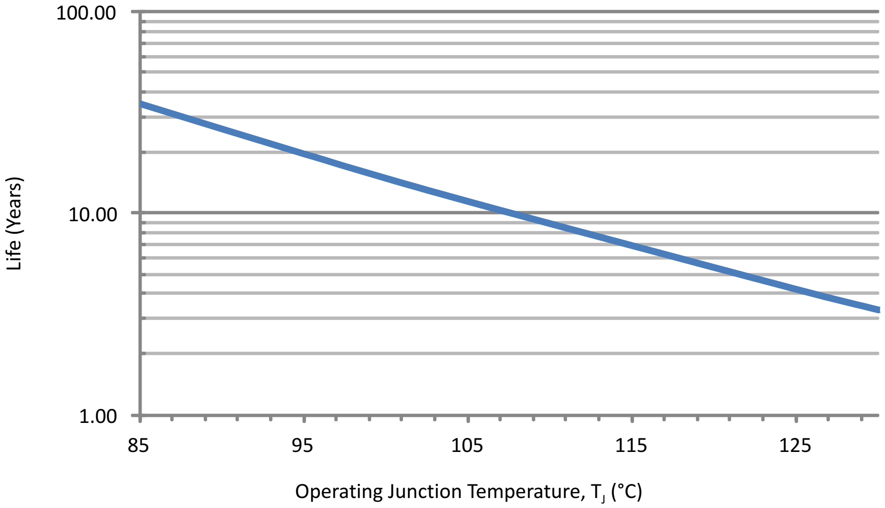
PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$V_{IT+(valid)}$	Receiver input threshold for $\overline{\text{INVALID}}$ high-level output voltage	FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V_L		2.7	V
$V_{IT–(valid)}$	Receiver input threshold for $\overline{\text{INVALID}}$ high-level output voltage	FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V_L	–2.7		V
$V_{T(invalid)}$	Receiver input threshold for $\overline{\text{INVALID}}$ low-level output voltage	FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V_L	–0.3	0.3	V
V_{OH}	$\overline{\text{INVALID}}$ high-level output voltage	I_{OH} = -1 mA, FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V_L	V_L – 0.6		V
V_{OL}	$\overline{\text{INVALID}}$ low-level output voltage	I_{OL} = 1.6 mA, FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V_L		0.4	V

Switching Characteristics

over recommended ranges of supply voltage and junction temperature (unless otherwise noted) (see Figure 7)

PARAMETER		MIN	TYP(1)	MAX	UNIT
t_{valid}	Propagation delay time, low- to high-level output		0.1		µs
$t_{invalid}$	Propagation delay time, high- to low-level output		50		µs
t_{en}	Supply enable time		25		µs
t_{dis}	Receiver or driver edge to auto-powerdown plus		30		µs

(1) All typical values are at $V_{CC} = V_L = 3.3$ V and $T_J = 25°C$.



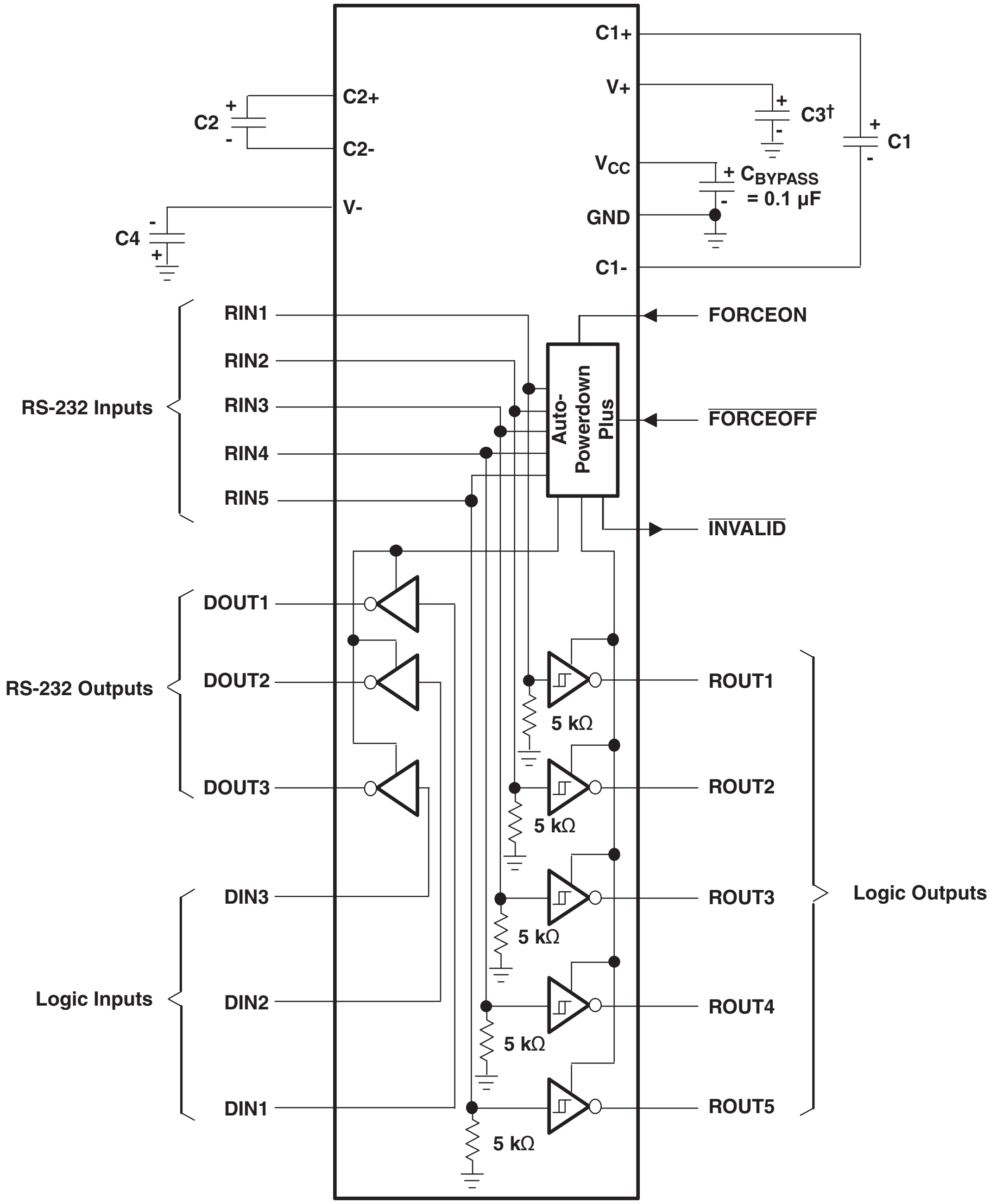
(1) See datasheet for absolute maximum and minimum recommended operating conditions.

(2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

(3) Enhanced plastic product disclaimer applies.

Figure 1. TRS3253E-EP Operating Life Derating Chart

APPLICATION INFORMATION



† C3 can be connected to V_{CC} or GND.

NOTES:
- A. Resistor values shown are nominal.
- B. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they should be connected as shown.

V_{CC} vs CAPACITOR VALUES

V_{CC}	C1	C2, C3, and C4
3.3 V ± 0.3 V	0.1 µF	0.1 µF
5 V ± 0.5 V	0.047 µF	0.33 µF
3 V to 5.5 V	0.1 µF	0.47 µF

Figure 2. Typical Operating Circuit and Capacitor Values

PARAMETER MEASUREMENT INFORMATION

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

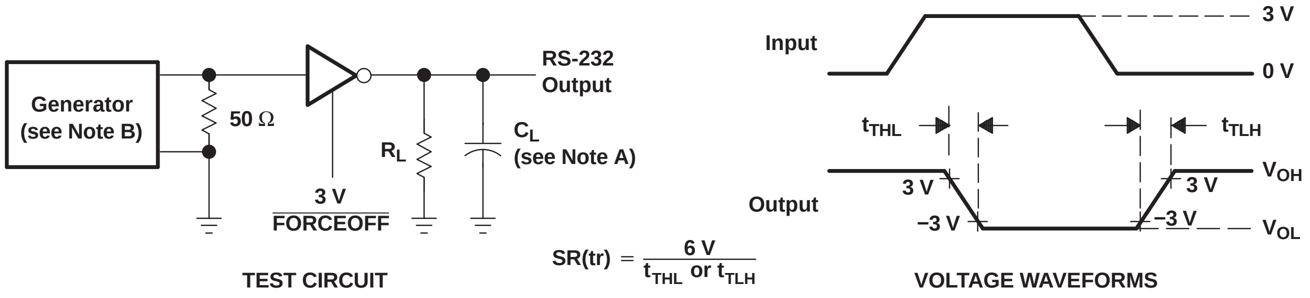


Figure 3. Driver Slew Rate

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 250 kbit/s, Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

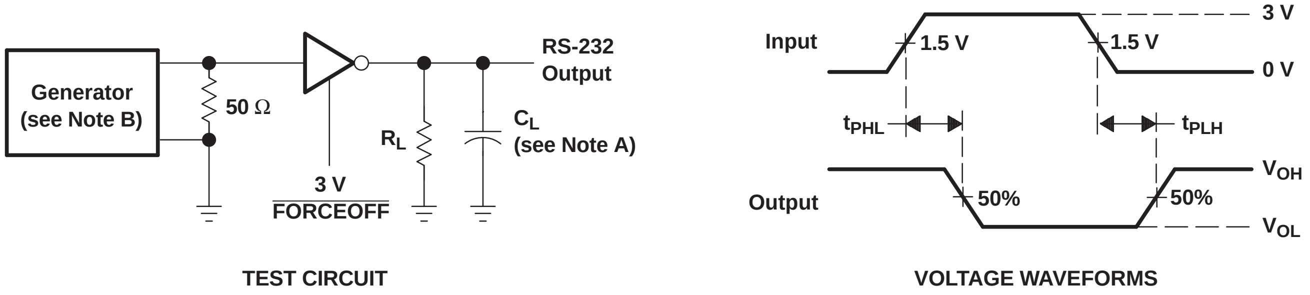


Figure 4. Driver Pulse Skew

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

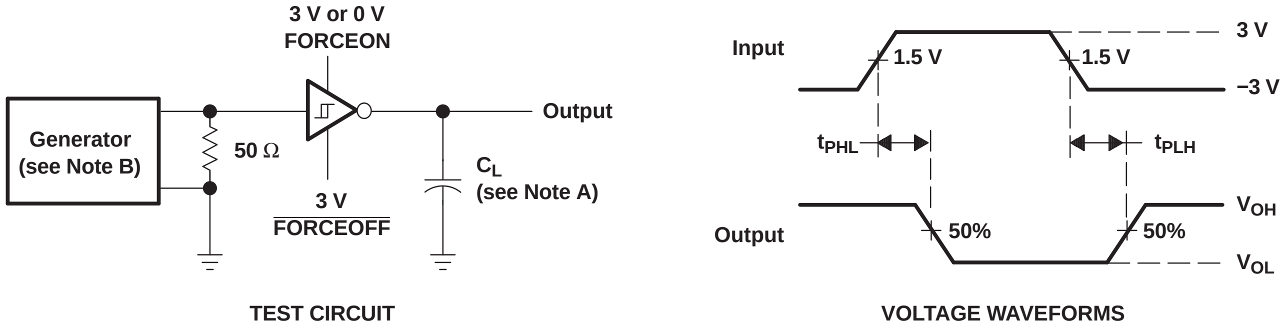


Figure 5. Receiver Propagation Delay Times

A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.

C. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

D. t_{PZL} and t_{PZH} are the same as t_{en}.

PARAMETER MEASUREMENT INFORMATION (continued)

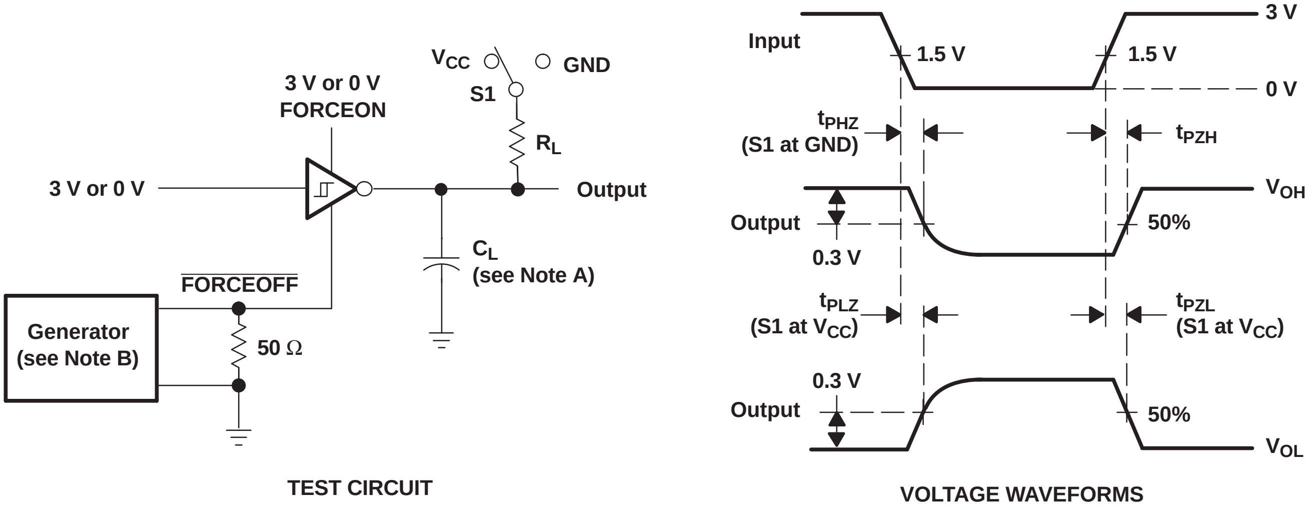
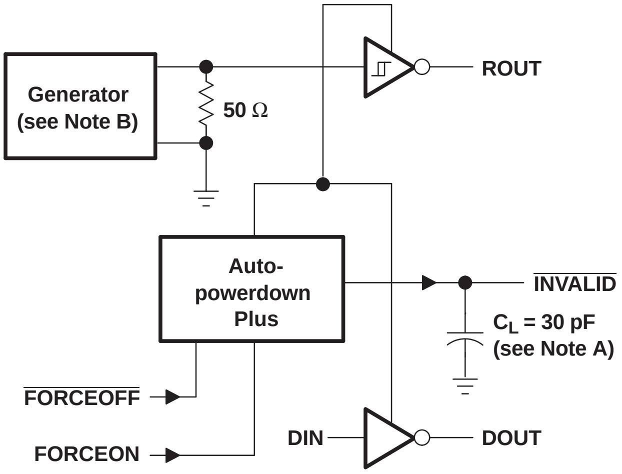
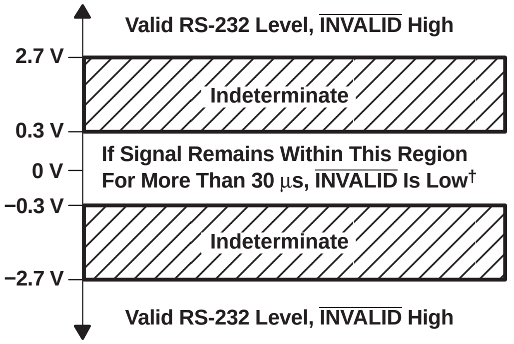


Figure 6. Receiver Enable and Disable Times

PARAMETER MEASUREMENT INFORMATION (continued)

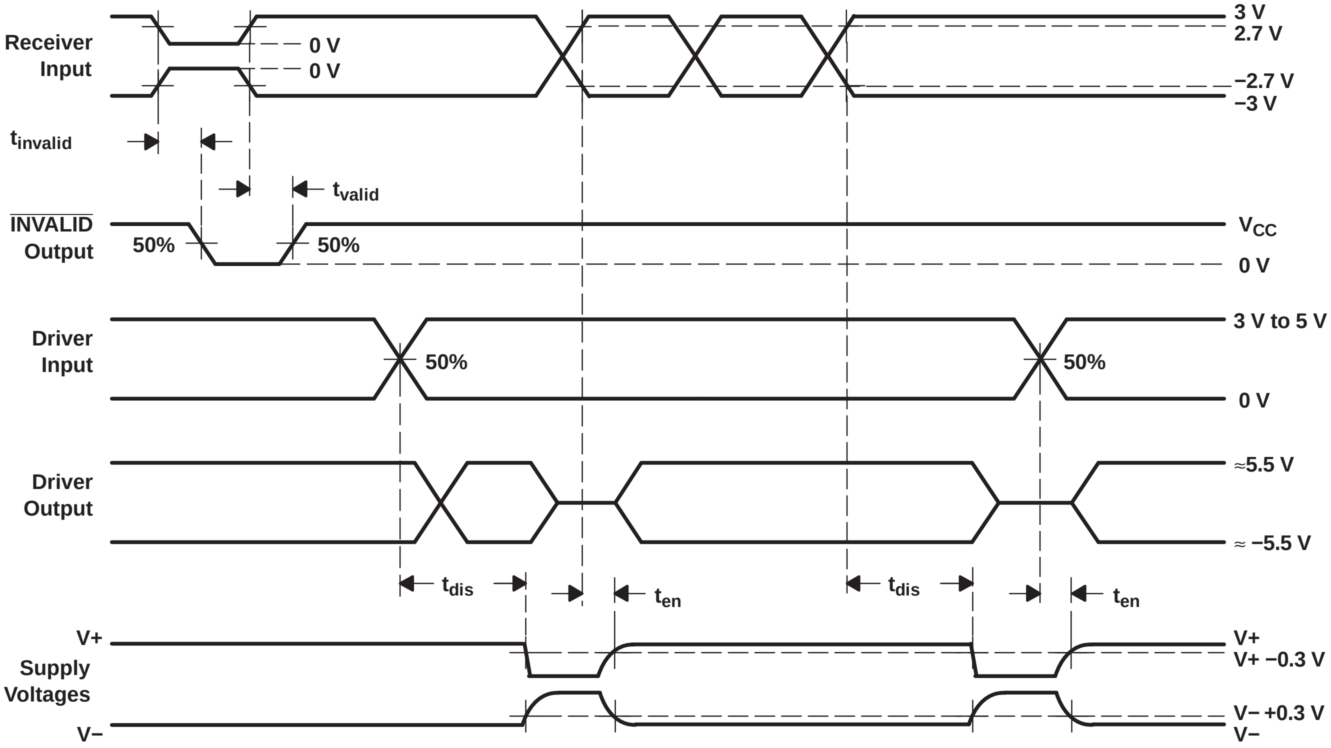


TEST CIRCUIT



† Auto-powerdown plus disables drivers and reduces supply current to 1 µA.

NOTES:
- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 5 kbit/s, Z_O = 50 Ω, 50% duty cycle, t_r ≤ 10 ns, t_f ≤ 10 ns.



Voltage Waveforms and Timing Diagrams

Figure 7. INVALID Propagation-Delay Times and Supply-Enabling Time

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRS3253EMRSMREP	ACTIVE	VQFN	RSM	32	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	RS53EP	Samples
V62/13621-01XE	ACTIVE	VQFN	RSM	32	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-55 to 125	RS53EP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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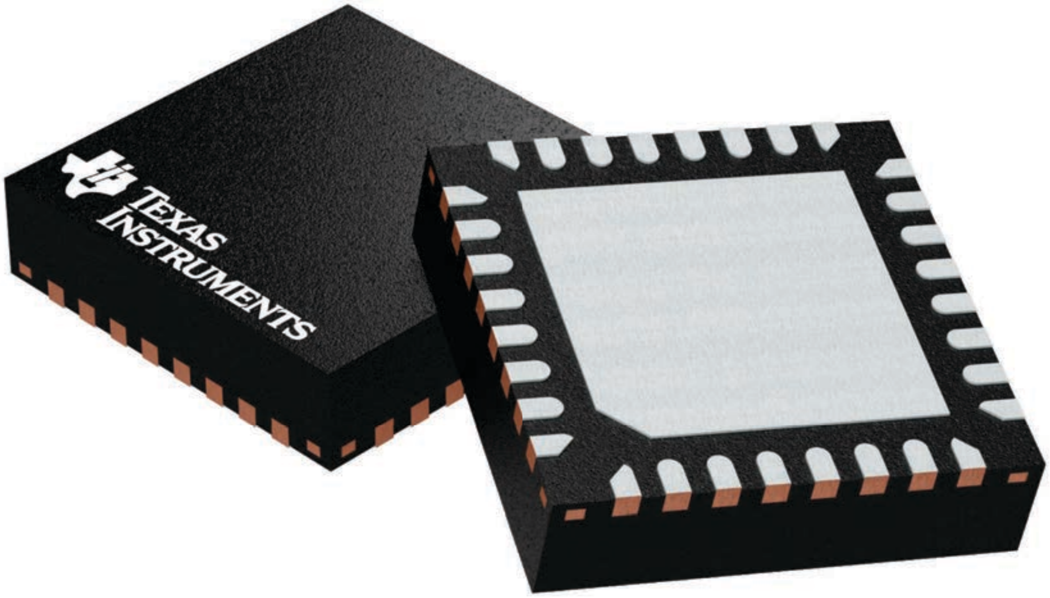
RSM 32

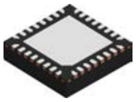
VQFN - 1 mm max height

4 x 4, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

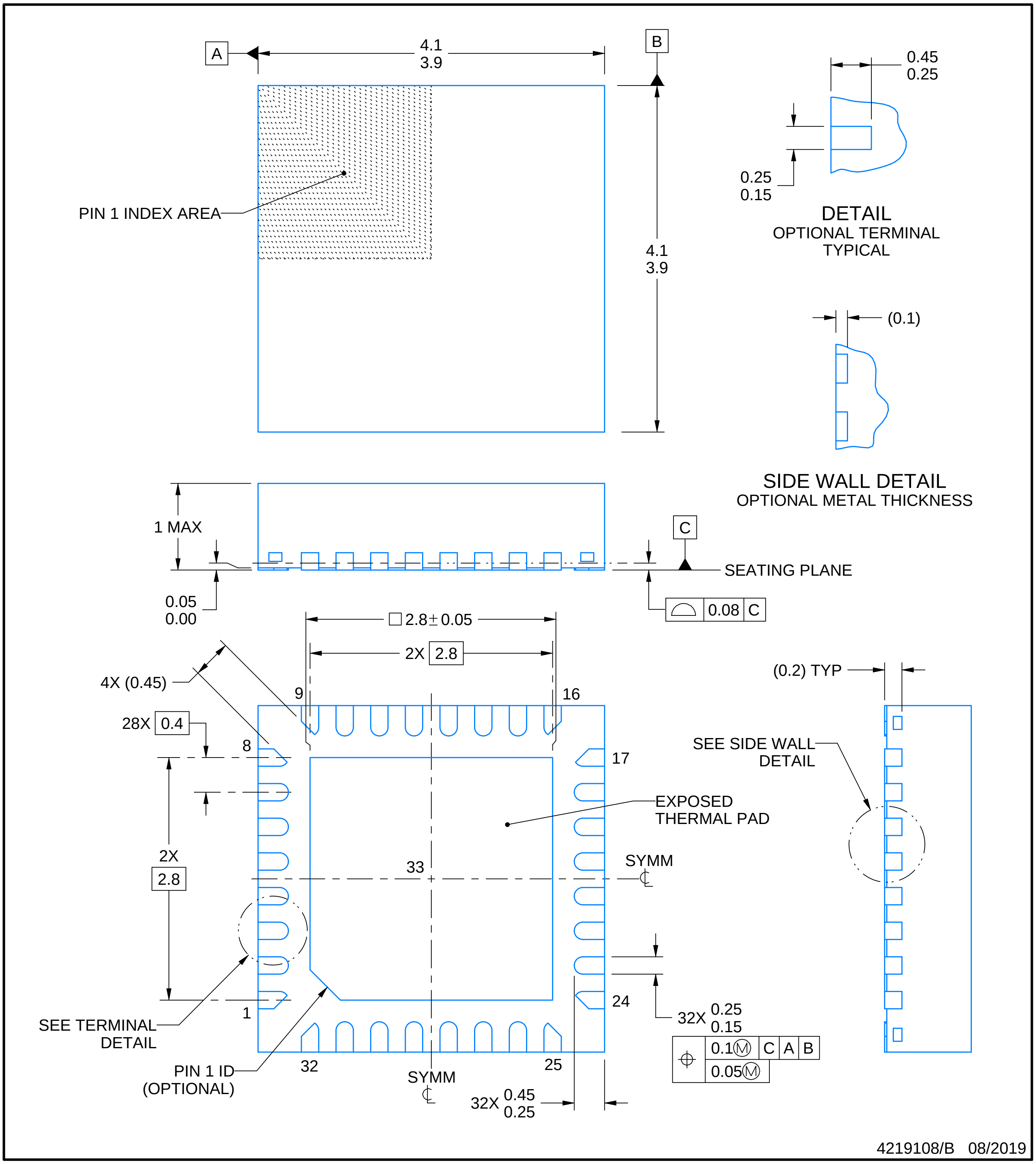




PACKAGE OUTLINE

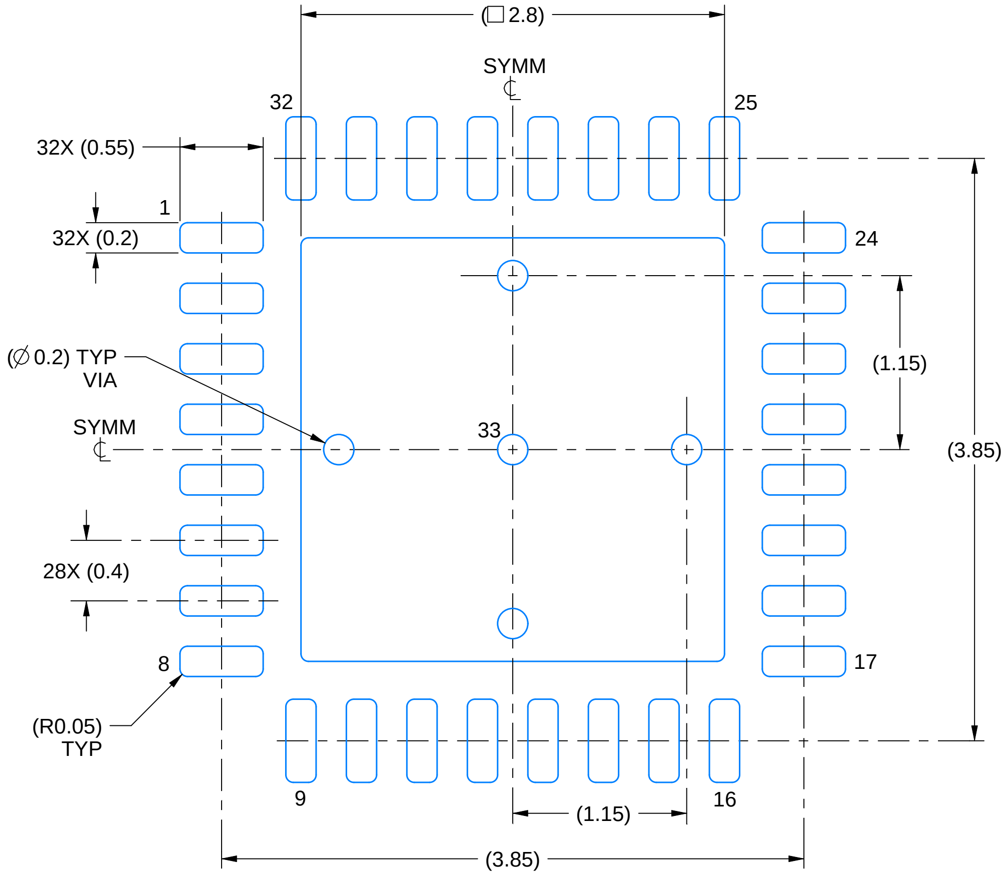
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

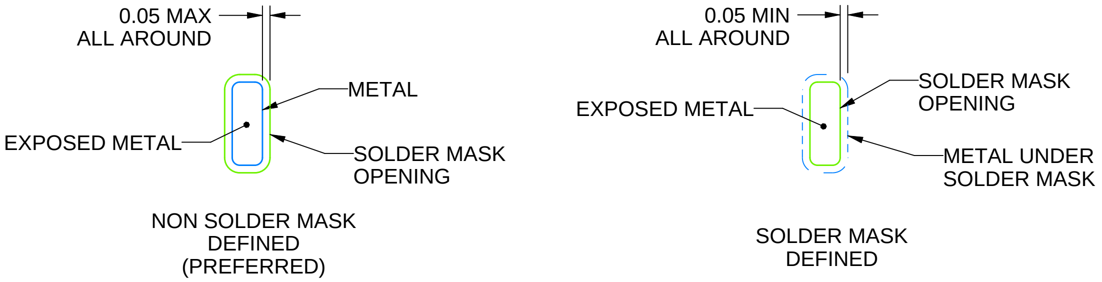


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



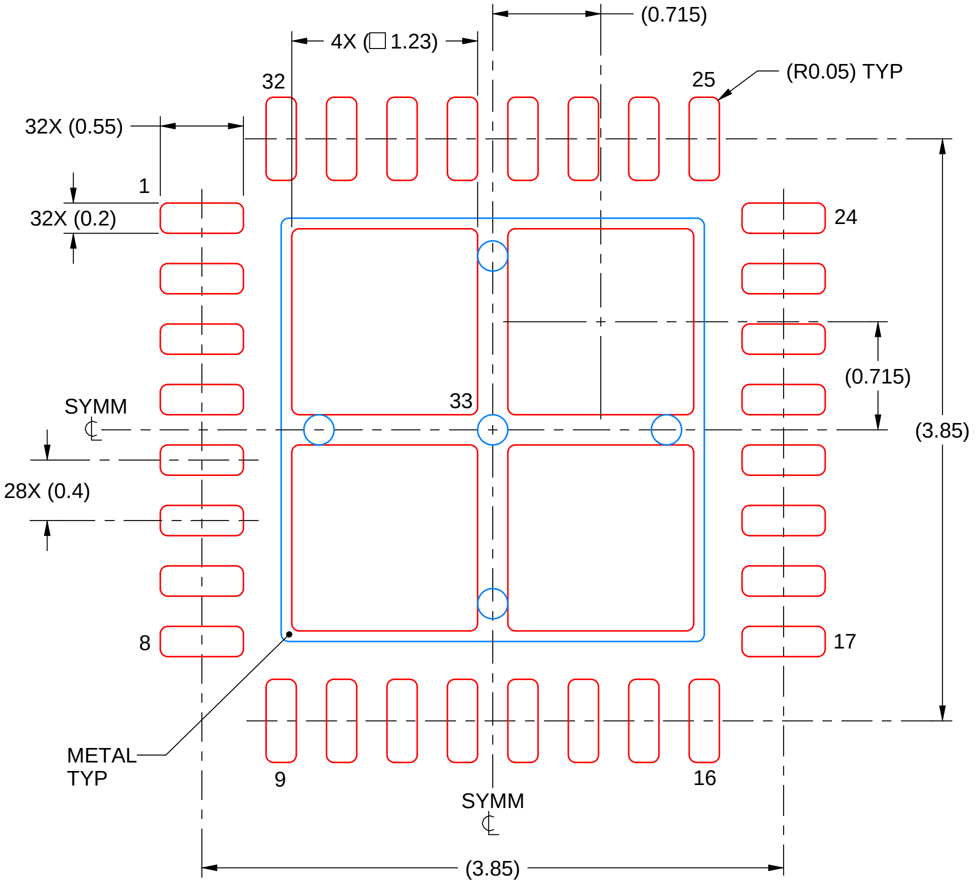
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 33:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

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