

## TS3USBCA4 USB Type-C SBU 多路复用器

### 1 特性

- USB Type-C™用于模拟音频 MIC/AGND、DisplayPort AUX 和其他信号的 4:1 (TS3USBCA420) 和 3:1 (TS3USBCA410) 多路复用器 (MUX)
- 适用于 0 至 3.6V 差分或单端信号的通用多路复用器
- 用于 AGND 连接的 60mΩ 超低电阻  $R_{ON}$ ，可实现低串扰性能
- 低总谐波失真 (THD)
- 高达 500MHz 的高带宽通道
- 支持引脚和 I<sup>2</sup>C 配置
- 支持在 3.3V ±10% 稳压电源或 2.4V 至 5.5V 电池电压下工作
- 工业温度范围：-40°C 至 85°C TS3USBCA420I 和 TS3USBCA410I
- 商业温度范围：0°C 至 70°C TS3USBCA420 和 TS3USBCA410
- 1.8mm x 2.6mm、16 引脚、0.4mm 间距 QFN 封装

### 2 应用

- 平板电脑
- 笔记本电脑
- 台式机
- 游戏控制台
- VR 模块
- 智能手机
- 显示器

### 3 说明

TS3USBCA4 是无源 4:1 (TS3USBCA420) 和 3:1 (TS3USBCA410) 多路复用器，支持将 USB Type-C 连接器端接到不同接口的 SBU1/SBU2 端子上的各种类型的差分或单端信号。这些信号可以是差分 DisplayPort 辅助 (AUX)、模拟音频 MIC 和 AGND、PCIe 差分时钟或任何其他受支持的通用差分或单端信号。

音频路径具有超低导通状态电阻 ( $R_{ON}$ )、低串扰和出色的总谐波失真 (THD) 性能。先断后通功能防止在信号从一个通道传输到另一个通道时产生信号失真。高速路径支持的带宽高达 500MHz，为 DisplayPort AUX、PCIe 时钟和其他类似信号提供充分支持。这些特性再加上低功耗性能，使得这款器件适合于便携式音频应用。

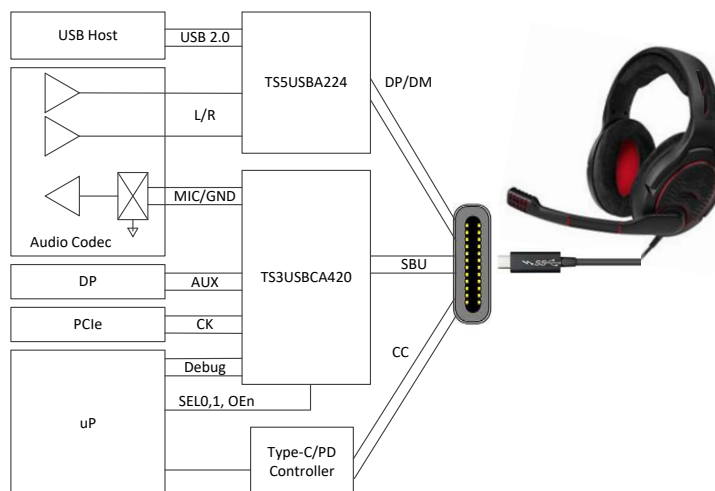
TS3USBCA4 具有 2.4V 至 5.5V 宽电源电压范围，用户可以灵活地选择使用单节电池、3.3V 稳压器或 VBUS 供电。它还提供面向商业和工业温度范围的选项。

器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸 (标称值)
TS3USBCA4	UQFN (16)	1.80mm x 2.60mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



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## 4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

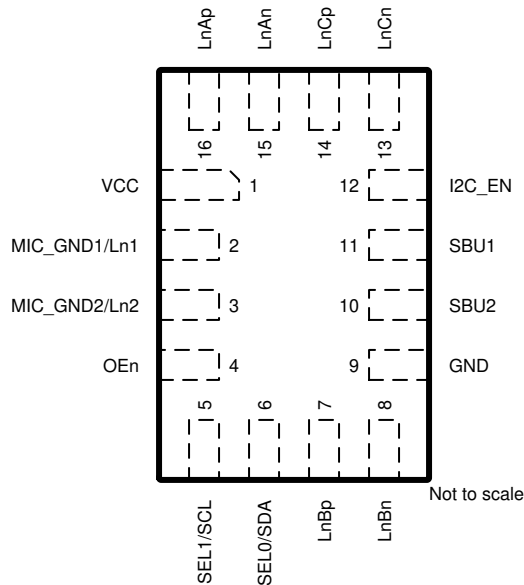
<b>Changes from Revision B (January 2019) to Revision C</b>	<b>Page</b>
• Changed description for LaAp pin From: "as a negative polarity" To "as a positive polarity".	<b>4</b>

<b>Changes from Revision A (August 2018) to Revision B</b>	<b>Page</b>
• Changed the I2C_EN pin Description From: This pin has an internal weak pull-up. To: This pin has an internal weak pull-down.	<b>3</b>

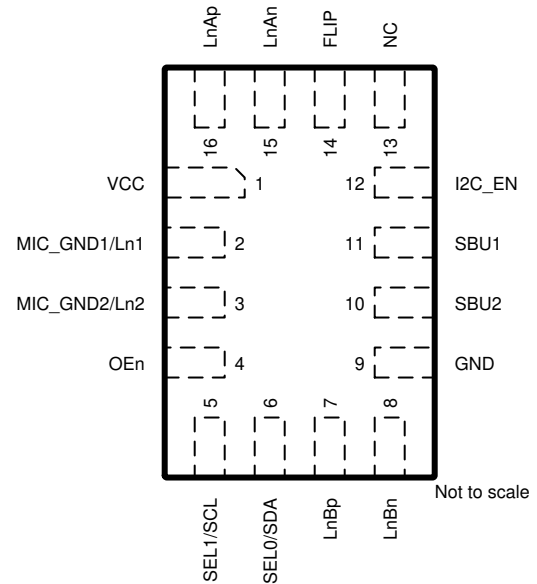
<b>Changes from Original (February 2018) to Revision A</b>	<b>Page</b>
• 将器件从预告信息 更改成了生产数据	<b>1</b>

## 5 Pin Configuration and Functions

UQFN Package for TS3USBCA420  
16-Pin (RSV)  
Top View



UQFN Package for TS3USBCA410  
16-Pin (RSV)  
Top View



### Pin Functions

NAME	PIN		I/O	DESCRIPTION
	TS3USBCA420	TS3USBCA410		
VCC	1	1	P	Power supply. External decoupling capacitors are required close to this pin.
MIC_GND1/Ln1	2	2	I/O, CMOS	Analog audio MIC/AGND signal connection to audio codec. This pin can also function as a general purpose I/O.
MIC_GND2/Ln2	3	3	I/O, CMOS	Analog audio MIC/AGND signal connection to audio codec. This pin can also function as a general purpose I/O.
OEn	4	4	2 Level I	Output Enable: L: Normal Operation H: Standby Mode, I <sup>2</sup> C registers reset (Default) This pin has an internal weak pull-up.
SEL1/SCL	5	5	2 Level I (Failsafe)	In Pin Configuration Mode (I2C_EN = L), this pin functions as SEL1 which is used along with SEL0 pin to select switch configurations (Refer to 表 2). This pin has an internal weak pull-down. In I <sup>2</sup> C Mode (I2C_EN = M or H), this pin functions as SCL pin for I <sup>2</sup> C clock. When used for I <sup>2</sup> C clock, pull it up to V <sub>I2C</sub> with a resistor between 0.62 kΩ and 2.2 kΩ.
SEL0/SDA	6	6	2 Level I/O (Failsafe)	In Pin Configuration Mode (I2C_EN = L), this pin functions as SEL0 which is used along with SEL1 pin to select switch configurations (Refer to 表 2). This pin has an internal weak pull-down. In I <sup>2</sup> C Mode (I2C_EN = M or H), this pin functions as SDA pin for I <sup>2</sup> C data. When used for I <sup>2</sup> C data, pull it up to V <sub>I2C</sub> with a resistor between 0.62 kΩ and 2.2 kΩ.
LnBp	7	7	I/O, CMOS	This pin can be used in single-ended format or as a positive polarity differential pair partner to pin LnBn. It can be used for connection to any generic I/O signals such as for DisplayPort AUX, PCI Express clock, I <sup>2</sup> C, UART, and debug interfaces.
LnBn	8	8	I/O, CMOS	This pin can be used in single-ended format or as a negative polarity differential pair partner to pin LnBp. It can be used for connection to any generic I/O signals such as for DisplayPort AUX, PCI Express clock, I <sup>2</sup> C, UART, and debug interfaces.
GND	9	9	G	Primary ground connection for the TS3USBCA4. Must be connected to system ground.
SBU2	10	10	I/O, CMOS (Failsafe)	This pin should be DC coupled to the SBU2 pin of the Type-C receptacle. This pin has an internal nominally 1.6-MΩ pull-down resistor.
SBU1	11	11	I/O, CMOS (Failsafe)	This pin should be DC coupled to the SBU1 pin of the Type-C receptacle. This pin has an internal nominally 1.6-MΩ pull-down resistor.
I2C_EN	12	12	3 Level I	This pin enables I <sup>2</sup> C Mode and sets I <sup>2</sup> C mode addresses (Refer to 表 5) depending on the pin level defined in 表 1. L: Pin Configuration Mode M: I <sup>2</sup> C Mode enabled with I <sup>2</sup> C address ADDR0 H: I <sup>2</sup> C Mode enabled with I <sup>2</sup> C address ADDR1 This pin has an internal weak pull-down.

### Pin Functions (continued)

NAME	PIN		I/O	DESCRIPTION
	TS3USBCA420	TS3USBCA410		
LnCn	13		I/O, CMOS	This pin can be used in single-ended format or as a negative polarity differential pair partner to pin LnCp. It can be used for connection to any generic I/O signals such as for DisplayPort AUX, PCI Express clock, I <sup>2</sup> C, UART, and debug interfaces.
LnCp	14		I/O, CMOS	This pin can be used in single-ended format or as a positive polarity differential pair partner to pin LnCn. It can be used for connection to any generic I/O signals such as for DisplayPort AUX, PCI Express clock, I <sup>2</sup> C, UART, and debug interfaces.
NC		13		Not connected.
FLIP		14	I/O, CMOS	This pin flips the switches based on type-C plug orientation in pin configuration mode (I2C_EN=L). L: Normal orientation. H: Flipped orientation. This pin has an internal weak pull-down.
LnAn	15	15	I/O, CMOS	This pin can be used in single-ended format or as a negative polarity differential pair partner to pin LnAp. This pin is preferred for connection to DisplayPort AUX. It can also be used for connection to any generic I/O signals such as for PCI Express clock, I <sup>2</sup> C, UART, and debug interfaces.
LnAp	16	16	I/O, CMOS	This pin can be used in single-ended format or as a positive polarity differential pair partner to pin LnAn. This pin is preferred for connection to DisplayPort AUX. It can also be used for connection to any generic I/O signals such as for PCI Express clock, I <sup>2</sup> C, UART, and debug interfaces.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

Over operating free-air temperature range unless otherwise noted.<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply Voltage Range <sup>(2)</sup>	-0.5	6	V
V <sub>IN_DIFF</sub>	Differential Voltage at Differential Inputs	-4	4	V
V <sub>IN_SE</sub>	Input Voltage at Differential Inputs <sup>(2)</sup>	-0.5	6	V
V <sub>IN_CMOS</sub>	Input Voltage at CMOS Inputs other than SBU1/SBU2 Pins <sup>(2)</sup>	-0.5	6	V
V <sub>IN_SBU</sub>	Input Voltage at SBU1/SBU2 Input-output Pins <sup>(2)</sup>	-0.5	6	V
T <sub>J</sub>	Junction Temperature		105	°C
T <sub>STG</sub>	Storage temperature	-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to the GND terminal.

### 6.2 ESD Ratings

	PARAMETER	VALUE	UNIT
V <sub>HBM</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±2000 V
V <sub>CDM</sub>	Electrostatic discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±500 V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

Over operating free-air temperature range unless otherwise noted.

		MIN	NOM	MAX	UNIT
T <sub>A</sub>	Ambient temperature for TS3USBCA410 and TS3USBCA420	0		70	°C
T <sub>A</sub>	Ambient temperature for TS3USBCA410I and TS3USBCA420I	-40		85	°C
V <sub>CC</sub>	Supply voltage	2.4	5.0	5.5	V
V <sub>I2C</sub>	Supply that external resistors on SDA and SCL are pulled up too	1.7		3.6	V
V <sub>I/O_DIFF</sub>	Differential Input-output Voltage	0		1.8	V
V <sub>PSN</sub>	Power supply noise			100	mV

## 6.4 Thermal Information

THERMAL METRIC		TS3USBCA4	
		RSV (R-PUQFN-N16)	
		16 PINS	
			UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance <sup>(1)</sup>	107.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance <sup>(2)</sup>	41.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance <sup>(3)</sup>	43.6	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter <sup>(4)</sup>	1.1	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter <sup>(5)</sup>	43.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance <sup>(6)</sup>	N/A	°C/W

- (1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (2) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (4) The junction-to-top characterization parameter,  $\Psi_{JT}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
- (5) The junction-to-board characterization parameter,  $\Psi_{JB}$ , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining  $\theta_{JA}$ , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

## 6.5 Electrical Characteristics (3 V ≤ V<sub>CC</sub> ≤ 3.6 V)

All minimum/maximum specifications are at T<sub>A</sub> = -40/85°C, V<sub>CC</sub> = 3.0 V/3.6 V, unless otherwise noted. Typical specifications are at T<sub>A</sub> = 25°C, V<sub>CC</sub> = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Power</b>						
I <sub>CC</sub>	Supply Current	OEn = L, DEVICE_ENABLE = 1		45	70	μA
I <sub>OFF_I2C</sub>	Device Shutdown Current	OEn = L, DEVICE_ENABLE = 0		17	30	μA
I <sub>OFF_OEN</sub>	Device Shutdown Current	OEn = 3.6 V		0.05	3.5	μA
	Device Shutdown Current	OEn = 1.4 V		4	12	μA
<b>SELO, SEL1</b>						
V <sub>IH</sub>	Input-high voltage		1.4			V
V <sub>IL</sub>	Input-low voltage				0.4	V
I <sub>IH</sub>	Input-high current	V <sub>IN</sub> = V <sub>CC</sub>			2.5	μA
I <sub>IL</sub>	Input-low current	V <sub>IN</sub> = 0 V			1	μA
R <sub>PD</sub>	Pull-down resistor		1.6	3.0	5.8	MΩ
<b>FLIP</b>						
V <sub>IH</sub>	Input-high voltage		1.4			V
V <sub>IL</sub>	Input-low voltage				0.4	V
I <sub>IH</sub>	Input-high current	V <sub>IN</sub> = V <sub>CC</sub>			2.5	μA
I <sub>IL</sub>	Input-low current	V <sub>IN</sub> = 0 V			1	μA
R <sub>PD</sub>	Pull-down resistor		1.6	3	5.8	MΩ
<b>OEn</b>						
V <sub>IH</sub>	Input-high voltage		1.4			V
V <sub>IL</sub>	Input-low voltage				0.4	V
I <sub>IH</sub>	Input-high current	V <sub>IN</sub> = V <sub>CC</sub>			0.6	μA
I <sub>IL</sub>	Input-low current	V <sub>IN</sub> = 0 V			6	μA
R <sub>PU</sub>	Pull-up resistor		0.6	1.1	2.5	MΩ
<b>I2C_EN</b>						
V <sub>IH</sub>	Input-high voltage		0.85			V <sub>CC</sub>

**Electrical Characteristics (3 V ≤ V<sub>CC</sub> ≤ 3.6 V) (continued)**

All minimum/maximum specifications are at T<sub>A</sub> = -40/85°C, V<sub>CC</sub> = 3.0 V/3.6 V, unless otherwise noted. Typical specifications are at T<sub>A</sub> = 25°C, V<sub>CC</sub> = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>IMH</sub>	Upper bound of mid-level input voltage. Higher input may be interpreted as logic HIGH.		0.6			V <sub>CC</sub>
V <sub>IML</sub>	Lower bound of mid-level input voltage. Lower input may be interpreted as logic LOW.				0.4	V <sub>CC</sub>
V <sub>IL</sub>	Input-low voltage				0.15	V <sub>CC</sub>
I <sub>IH</sub>	Input-high current				2.5	μA
I <sub>IM</sub>	Mid-level input current				1.2	μA
I <sub>IL</sub>	Input-low current				1	μA
R <sub>PD</sub>	Pull-down resistor		1.6	3.0	5.8	MΩ
<b>I<sup>2</sup>C Control Pins SCL, SDA</b>						
V <sub>IH_I2C</sub>	High-level input voltage	I <sup>2</sup> C mode	1.3		V <sub>I2C</sub>	V
V <sub>IL_I2C</sub>	Low-level input voltage	I <sup>2</sup> C mode	0		0.5	V
V <sub>OL_I2C</sub>	Low-level output voltage	I <sup>2</sup> C mode; I <sub>OL_I2C</sub> = 3 mA	0		0.4	V
I <sub>OL_I2C</sub>	Low-level output current	I <sup>2</sup> C mode; V <sub>OL_I2C</sub> = 0.4 V	6			mA
I <sub>I_I2C</sub>	Input current on SDA pin	0.1*V <sub>I2C</sub> < Input voltage < 3.6 V	-5		5	μA
C <sub>I_I2C</sub>	Input capacitance		0.5		10	pF
C <sub>(I2C_FM_BUS)</sub>	I <sup>2</sup> C bus capacitance for FM (400 kHz)				150	pF
R <sub>(EXT_I2C_FM)</sub>	External pull up resistors on both SDA and SCL for FM (400 kHz)	C <sub>(I2C_FM_BUS)</sub> = 150 pF	620	1500	2200	Ω
<b>SBU1, SBU2</b>						
C <sub>SBU_HS</sub>	Single-ended capacitance at 500MHz looking into SBU pin	V <sub>IN</sub> = 0 V, outputs open, high-speed path enabled	4	11	13	pF
C <sub>SBU_AU_DIO</sub>	Single-ended capacitance at 500MHz looking into SBU pin	V <sub>IN</sub> = 0 V, outputs open, audio path enabled; T <sub>A</sub> = 25°C; V <sub>CC</sub> = 3.3 V	8	10	14	pF
C <sub>SBU_OFF</sub>	Single-ended capacitance at 500MHz looking into SBU pin	V <sub>IN</sub> = 0 V, outputs open, OEn=H; T <sub>A</sub> = 25°C; V <sub>CC</sub> = 3.3 V	11	14	17	pF
R <sub>PD</sub>	Pull-down resistor		0.8	1.6	3.3	MΩ
<b>LnA, LnB, LnC: HIGH-SPEED PATH</b>						
V <sub>I_HS</sub>	Single-ended HS input voltage		-0.3		3.6	V
C <sub>HS_ON</sub>	Single-ended capacitance at 500 MHz looking into HS pins	V <sub>IN</sub> = 0 V, outputs open, high-speed path enabled		8.5	10.5	pF
C <sub>HS_AUDI_O</sub>	Single-ended capacitance at 500 MHz looking into HS pins	V <sub>IN</sub> = 0 V, outputs open, audio path enabled; T <sub>A</sub> = 25°C; V <sub>CC</sub> = 3.3 V		1.7	2	pF
C <sub>HS_OFF</sub>	Single-ended capacitance at 500 MHz looking into HS pins	V <sub>IN</sub> = 0 V, outputs open, OEn=H; T <sub>A</sub> = 25°C; V <sub>CC</sub> = 3.3 V		1.7	2	pF
R <sub>ON_HS</sub>	ON resistance	V <sub>IN</sub> = 0 V, I <sub>O</sub> = -40 mA		4.9	7.1	Ω
ΔR <sub>ON_HS</sub>	ON resistance match between pairs of the same channel	V <sub>IN</sub> ≤ 0 V, I <sub>O</sub> = -40 mA			0.5	Ω
R <sub>ON_FLAT_HS</sub>	ON resistance flatness (R <sub>ON_HS(MAX)</sub> - R <sub>ON_HS(MIN)</sub> )	0 V ≤ V <sub>IN</sub> ≤ 3.6 V, I <sub>O</sub> = -40 mA		1.35		Ω
BW <sub>HS</sub>	-3-dB bandwidth	R <sub>L</sub> = 50 Ω, V <sub>IN</sub> = 0 V, MIC_GND1 pin open, MIC_GND1 pin open; T <sub>A</sub> = 25°C; V <sub>CC</sub> = 3.3 V	460	510	550	MHz
R <sub>J_HS</sub>	Additive random jitter	R <sub>L</sub> = 50 Ω, 10 kHz to 20 MHz offset, f = 100 MHz; T <sub>A</sub> = 25°C; V <sub>CC</sub> = 3.3 V		0.012		ps-RMS
<b>MIC_GND1, MIC_GND2: AUDIO PATH</b>						
V <sub>I_MIC</sub>	MIC input voltage		-0.3		3.6	V

## Electrical Characteristics (3 V ≤ V<sub>CC</sub> ≤ 3.6 V) (continued)

All minimum/maximum specifications are at T<sub>A</sub> = -40/85°C, V<sub>CC</sub> = 3.0 V/3.6 V, unless otherwise noted. Typical specifications are at T<sub>A</sub> = 25°C, V<sub>CC</sub> = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C <sub>AUDIO_ON</sub>	Single-ended capacitance at 500MHz looking into the MIC_GND pins	V <sub>IN</sub> = 0 V, outputs open, audio path enabled; T <sub>A</sub> = 25°C; V <sub>CC</sub> = 3.3 V		9.5	12	pF
C <sub>AUDIO_HS</sub>	Single-ended capacitance at 500MHz looking into the MIC_GND pins	V <sub>IN</sub> = 0 V, outputs open, high-speed path enabled; T <sub>A</sub> = 25°C; V <sub>CC</sub> = 3.3 V		11.5	16	pF
C <sub>AUDIO_OFF</sub>	Single-ended capacitance at 500MHz looking into the MIC_GND pins	V <sub>IN</sub> = 0 V, outputs open, OEn=H; T <sub>A</sub> = 25°C; V <sub>CC</sub> = 3.3 V		12.5	14.5	pF
R <sub>ON_AUDIO</sub>	ON resistance for AUDIO path	V <sub>IN</sub> = 0 V, I <sub>O</sub> = -75 mA		50	80	mΩ
BW <sub>AUDIO</sub>	-3-dB bandwidth	R <sub>L</sub> = 50 Ω, V <sub>IN</sub> = 0 V; T <sub>A</sub> = 25°C; V <sub>CC</sub> = 3.3 V	580	630	700	MHz
PSR <sub>217</sub>	Power supply rejection	R <sub>L</sub> = 50 Ω, V <sub>IN</sub> = 3.3 V ± 200 mV <sub>PP</sub> , f = 217 Hz		-105	-100	dB
PSR <sub>1K</sub>		R <sub>L</sub> = 50 Ω, V <sub>IN</sub> = 3.3 V ± 200 mV <sub>PP</sub> , f = 1 kHz		-96	-92	dB
PSR <sub>20K</sub>		R <sub>L</sub> = 50 Ω, V <sub>IN</sub> = 3.3 V ± 200 mV <sub>PP</sub> , f = 20 kHz		-85	-81	dB
THD <sub>200_MIC</sub>	Total harmonic distortion	R <sub>S</sub> =600Ω, R <sub>L</sub> =600Ω, V <sub>IN</sub> =1.8V±200mV <sub>PP</sub> , f=20Hz~20kHz; T <sub>A</sub> = 25°C; V <sub>CC</sub> = 3.3 V		0.006		%
THD <sub>500_MIC</sub>	Total harmonic distortion	R <sub>S</sub> =600Ω, R <sub>L</sub> =600Ω, V <sub>IN</sub> =1.8V±500mV <sub>PP</sub> , f=20Hz~20kHz; T <sub>A</sub> = 25°C; V <sub>CC</sub> = 3.3 V		0.003		%
X <sub>TALK_MICGND</sub>	Crosstalk between MIC and AGND	V <sub>IN</sub> = 200 mV <sub>PP</sub> , f = 20 Hz – 20 kHz, R <sub>L</sub> = 50 Ω; T <sub>A</sub> = 25°C;		-110	-90	dB
ISO <sub>OFF_MICGND</sub>	OFF isolation	V <sub>IN</sub> = 200 mV <sub>PP</sub> , f = 20 Hz – 20 kHz, R <sub>L</sub> = 50 Ω; T <sub>A</sub> = 25°C;		-73	-67	dB

## 6.6 Electrical Characteristics (2.4 V ≤ V<sub>CC</sub> ≤ 5.5 V)

All minimum/maximum specifications are at T<sub>A</sub> = -40/85°C, V<sub>CC</sub> = 2.4 V/5.5 V, unless otherwise noted. Typical specifications are at T<sub>A</sub> = 25°C, V<sub>CC</sub> = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Power</b>						
I <sub>CC</sub>	Supply Current	OEn = L, DEVICE_ENABLE = 1		45	75	μA
I <sub>OFF_I2C</sub>	Device Shutdown Current	OEn = L, DEVICE_ENABLE = 0		17	40	μA
I <sub>OFF_OEN</sub>	Device Shutdown Current	OEn = 3.6 V		0.05	5.5	μA
	Device Shutdown Current	OEn = 1.4 V		4	80	μA
<b>SELO, SEL1</b>						
V <sub>IH</sub>	Input-high voltage		1.4			V
V <sub>IL</sub>	Input-low voltage				0.4	V
I <sub>IH</sub>	Input-high current	V <sub>IN</sub> = V <sub>CC</sub>			3.5	μA
I <sub>IL</sub>	Input-low current	V <sub>IN</sub> = 0 V			1	μA
R <sub>PD</sub>	Pull-down resistor		1.6	3.0	5.8	MΩ
<b>FLIP</b>						
V <sub>IH</sub>	Input-high voltage		1.4			V
V <sub>IL</sub>	Input-low voltage				0.4	V
I <sub>IH</sub>	Input-high current	V <sub>IN</sub> = V <sub>CC</sub>			3.5	μA
I <sub>IL</sub>	Input-low current	V <sub>IN</sub> = 0 V			1	μA
R <sub>PD</sub>	Pull-down resistor		1.6	3.0	5.8	MΩ
<b>OEn</b>						
V <sub>IH</sub>	Input-high voltage		1.5			V

**Electrical Characteristics (2.4 V ≤ V<sub>CC</sub> ≤ 5.5 V) (continued)**

All minimum/maximum specifications are at T<sub>A</sub> = -40/85°C, V<sub>CC</sub> = 2.4 V/5.5 V, unless otherwise noted. Typical specifications are at T<sub>A</sub> = 25°C, V<sub>CC</sub> = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>IL</sub>	Input-low voltage				0.4	V
I <sub>IH</sub>	Input-high current	V <sub>IN</sub> =V <sub>CC</sub>			1	μA
I <sub>IL</sub>	Input-low current	V <sub>IN</sub> =0 V			8	μA
R <sub>PU</sub>	Pull-up resistor		0.6	1.1	2.5	MΩ
<b>I2C_EN</b>						
V <sub>IH</sub>	Input-high voltage		0.9			V <sub>CC</sub>
V <sub>IMH</sub>	Upper bound of mid-level input voltage. Higher input may be interpreted as logic HIGH.		0.58			V <sub>CC</sub>
V <sub>IML</sub>	Lower bound of mid-level input voltage. Lower input may be interpreted as logic LOW.				0.42	V <sub>CC</sub>
V <sub>IL</sub>	Input-low voltage				0.14	V <sub>CC</sub>
I <sub>IH</sub>	Input-high current				3.5	μA
I <sub>IM</sub>	Mid-level input current				1.6	μA
I <sub>IL</sub>	Input-low current				1	μA
R <sub>PD</sub>	Pull-down resistor		1.6	3.0	5.8	MΩ
<b>I<sup>2</sup>C Control Pins SCL, SDA</b>						
V <sub>IH_I2C</sub>	High-level input voltage	I <sup>2</sup> C mode	1.3		V <sub>I2C</sub>	V
V <sub>IL_I2C</sub>	Low-level input voltage	I <sup>2</sup> C mode	0		0.5	V
V <sub>OL_I2C</sub>	Low-level output voltage	I <sup>2</sup> C mode; I <sub>OL_I2C</sub> = 3 mA	0		0.4	V
I <sub>OL_I2C</sub>	Low-level output current	I <sup>2</sup> C mode; V <sub>OL_I2C</sub> = 0.4 V	4			mA
I <sub>I_I2C</sub>	Input current on SDA pin	0.1*V <sub>I2C</sub> < Input voltage < 3.6 V	-5		5	μA
C <sub>I_I2C</sub>	Input capacitance		0.5		10	pF
C <sub>(I2C_FM_BUS)</sub>	I <sup>2</sup> C bus capacitance for FM (400 kHz)				150	pF
R <sub>(EXT_I2C_FM)</sub>	External pull up resistors on both SDA and SCL for FM (400 kHz)	C <sub>(I2C_FM_BUS)</sub> = 150 pF	620	1500	2200	Ω
<b>SBU1, SBU2</b>						
C <sub>SBU_HS</sub>	Single-ended capacitance at 500MHz looking into SBU pin	V <sub>IN</sub> = 0 V, outputs open, high-speed path enabled	4	11	13	pF
C <sub>SBU_AU_DIO</sub>	Single-ended capacitance at 500MHz looking into SBU pin	V <sub>IN</sub> = 0 V, outputs open, audio path enabled; T <sub>A</sub> = 25°C; V <sub>CC</sub> = 3.3 V	8	10	14	pF
C <sub>SBU_OFF</sub>	Single-ended capacitance at 500MHz looking into SBU pin	V <sub>IN</sub> = 0 V, outputs open, OEn=H; T <sub>A</sub> = 25°C; V <sub>CC</sub> = 3.3 V	11	14	17	pF
R <sub>PD</sub>	Pull-down resistor		0.8	1.6	3.3	MΩ
<b>LnA, LnB, LnC: HIGH-SPEED PATH</b>						
V <sub>I_HS</sub>	Single-ended HS input voltage		-0.3		3.6	V
C <sub>HS_ON</sub>	Single-ended capacitance at 500 MHz looking into HS pins	V <sub>IN</sub> = 0 V, outputs open, high-speed path enabled		8.5	10.5	pF
C <sub>HS_AUDI_O</sub>	Single-ended capacitance at 500 MHz looking into HS pins	V <sub>IN</sub> = 0 V, outputs open, audio path enabled; T <sub>A</sub> = 25°C; V <sub>CC</sub> = 3.3 V		1.7	2	pF
C <sub>HS_OFF</sub>	Single-ended capacitance at 500 MHz looking into HS pins	V <sub>IN</sub> = 0 V, outputs open, OEn=H; T <sub>A</sub> = 25°C; V <sub>CC</sub> = 3.3 V		1.7	2	pF
R <sub>ON_HS</sub>	ON resistance	V <sub>IN</sub> = 0 V, I <sub>O</sub> = -40 mA		4.9	7.5	Ω
ΔR <sub>ON_HS</sub>	ON resistance match between pairs of the same channel	V <sub>IN</sub> ≤ 0 V, I <sub>O</sub> = -40 mA			0.65	Ω
R <sub>ON_FLAT_HS</sub>	ON resistance flatness (R <sub>ON_HS(MAX)</sub> - R <sub>ON_HS(MIN)</sub> )	0 V ≤ V <sub>IN</sub> ≤ 3.6 V, I <sub>O</sub> = -40 mA		1.35		Ω



## Electrical Characteristics (2.4 V ≤ V<sub>CC</sub> ≤ 5.5 V) (continued)

All minimum/maximum specifications are at T<sub>A</sub> = -40/85°C, V<sub>CC</sub> = 2.4 V/5.5 V, unless otherwise noted. Typical specifications are at T<sub>A</sub> = 25°C, V<sub>CC</sub> = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BW <sub>HS</sub>	-3-dB bandwidth	R <sub>L</sub> = 50 Ω, V <sub>IN</sub> = 0 V; T <sub>A</sub> = 25°C; V <sub>CC</sub> = 3.3 V	450	510	670	MHz
RJ <sub>HS</sub>	Additive random jitter	R <sub>L</sub> = 50 Ω, 10 kHz to 20 MHz offset, f = 100 MHz; T <sub>A</sub> = 25°C; V <sub>CC</sub> = 3.3 V		0.012		ps-RMS
<b>MIC_GND1, MIC_GND2: AUDIO PATH</b>						
V <sub>I_MIC</sub>	MIC input voltage		-0.3		3.6	V
C <sub>AUDIO_ON</sub>	Single-ended capacitance at 500MHz looking into the MIC_GND pins	V <sub>IN</sub> = 0 V, outputs open, audio path enabled; T <sub>A</sub> = 25°C; V <sub>CC</sub> = 3.3 V		9.5	12	pF
C <sub>AUDIO_HS</sub>	Single-ended capacitance at 500MHz looking into the MIC_GND pins	V <sub>IN</sub> = 0 V, outputs open, high-speed path enabled; T <sub>A</sub> = 25°C; V <sub>CC</sub> = 3.3 V		11.5	16	pF
C <sub>AUDIO_OFF</sub>	Single-ended capacitance at 500MHz looking into the MIC_GND pins	V <sub>IN</sub> = 0 V, outputs open, OEN=H; T <sub>A</sub> = 25°C; V <sub>CC</sub> = 3.3 V		12.5	14.5	pF
R <sub>ON_AUDIO</sub>	ON resistance for AUDIO path	V <sub>IN</sub> = 0 V, I <sub>O</sub> = -75 mA		50	80	mΩ
BW <sub>AUDIO</sub>	-3-dB bandwidth	R <sub>L</sub> = 50 Ω, V <sub>IN</sub> = 0 V; T <sub>A</sub> = 25°C; V <sub>CC</sub> = 3.3 V	580	630	720	MHz
PSR <sub>217</sub>	Power supply rejection	R <sub>L</sub> = 50 Ω, V <sub>IN</sub> = 3.3 V ± 200 mV <sub>PP</sub> , f = 217 Hz		-105	-96	dB
PSR <sub>1K</sub>		R <sub>L</sub> = 50 Ω, V <sub>IN</sub> = 3.3 V ± 200 mV <sub>PP</sub> , f = 1 kHz		-96	-90	dB
PSR <sub>20K</sub>		R <sub>L</sub> = 50 Ω, V <sub>IN</sub> = 3.3 V ± 200 mV <sub>PP</sub> , f = 20 kHz		-85	-81	dB
THD <sub>200_MIC</sub>	Total harmonic distortion	R <sub>S</sub> =600Ω, R <sub>L</sub> =600Ω, V <sub>IN</sub> =1.8V±200mV <sub>PP</sub> , f=20Hz~20kHz; T <sub>A</sub> = 25°C; V <sub>CC</sub> = 3.3 V		0.006		%
THD <sub>500_MIC</sub>	Total harmonic distortion	R <sub>S</sub> =600Ω, R <sub>L</sub> =600Ω, V <sub>IN</sub> =1.8V±500mV <sub>PP</sub> , f=20Hz~20kHz; T <sub>A</sub> = 25°C; V <sub>CC</sub> = 3.3 V		0.003		%
X <sub>TALK_MICGND</sub>	Crosstalk between MIC and AGND	V <sub>IN</sub> = 200 mV <sub>PP</sub> , f = 20 Hz – 20 kHz, R <sub>L</sub> = 50 Ω; T <sub>A</sub> = 25°C;		-110	-90	dB
ISO <sub>OFF_MICGND</sub>	OFF isolation	V <sub>IN</sub> = 200 mV <sub>PP</sub> , f = 20 Hz – 20 kHz, R <sub>L</sub> = 50 Ω; T <sub>A</sub> = 25°C;		-73	-67	dB

## 6.7 Switching Characteristics (2.4 V ≤ V<sub>CC</sub> ≤ 5.5 V)

All minimum/maximum specifications are at T<sub>A</sub> = -40/85°C, V<sub>CC</sub> = 2.4 V/5.5 V, unless otherwise noted. Typical specifications are at T<sub>A</sub> = 25°C, V<sub>CC</sub> = 3.3 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>I2C</b>						
f <sub>SCL</sub>	I2C clock frequency				400	kHz
t <sub>BUF</sub>	Bus free time between START and STOP conditions		1.3			μs
t <sub>HDSTA</sub>	Hold time after repeated START condition. After this period, the first clock pulse is generated		0.6			μs
t <sub>LOW</sub>	Low period of the I2C clock		1.3			μs
t <sub>HIGH</sub>	High period of the I2C clock		0.6			μs
t <sub>SUSTA</sub>	Setup time for a repeated START condition		0.6			μs
t <sub>HDDAT</sub>	Data hold time		0			μs
t <sub>SUDAT</sub>	Data setup time		150			ns
t <sub>R</sub>	Rise time of both SDA and SCL signals				300	ns

## Switching Characteristics (2.4 V ≤ V<sub>CC</sub> ≤ 5.5 V) (continued)

All minimum/maximum specifications are at T<sub>A</sub> = -40/85°C, V<sub>CC</sub> = 2.4 V/5.5 V, unless otherwise noted. Typical specifications are at T<sub>A</sub> = 25°C, V<sub>CC</sub> = 3.3 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>F</sub>	Fall time of both SDA and SCL signals	20 × (V <sub>I2C</sub> /5.5 V)		300	ns
t <sub>SUSTO</sub>	Setup time for STOP condition	0.6			μs

## 6.8 Timing Requirements (3 V ≤ V<sub>CC</sub> ≤ 3.6 V)

All minimum/maximum specifications are at T<sub>A</sub> = -40/85°C, V<sub>CC</sub> = 3.0 V/3.6 V, unless otherwise noted. Typical specifications are at T<sub>A</sub> = 25°C, V<sub>CC</sub> = 3.3 V, unless otherwise noted.

	TEST CONDITIONS	MIN	NOM	MAX	UNIT
t <sub>ON_MICG</sub> ND	Switch ON time for MIC/AGND path V <sub>PU</sub> =1.8V, R <sub>PU</sub> =2100Ω, C <sub>L</sub> =50pF			10	μs
t <sub>OFF_MICG</sub> ND	Switch OFF time for MIC/AGND path V <sub>PU</sub> =1.8V, R <sub>PU</sub> =2100Ω, C <sub>L</sub> =50pF			5	μs
t <sub>ON_HS</sub>	Switch ON time for high-speed path R <sub>S</sub> =50Ω, R <sub>L</sub> =50Ω			1.1	μs
t <sub>OFF_HS</sub>	Switch OFF time for high-speed path R <sub>S</sub> =50Ω, R <sub>L</sub> =50Ω			725	ns
t <sub>BBM</sub>	Break before make off time for MIC/AGND path V <sub>PU</sub> =1.8V, R <sub>PU</sub> =2100Ω, R <sub>L</sub> =50Ω, C <sub>L</sub> =50pF	1300			ns
t <sub>FLIP</sub>	Response time for the FLIP pin R <sub>S</sub> =50Ω, R <sub>L</sub> =50Ω			1	μs
t <sub>DEV_ENA</sub> BLE	Device enable time from OEn = L to device ready OEn=L			350	μs
t <sub>DEV_DISA</sub> BLE	Device disable time from OEn = H to device shutdown OEn=H			175	ns
t <sub>D_PG</sub>	V <sub>CC</sub> (MIN) to Internal Power Good asserted high (Refer to <a href="#">Figure 1</a> ) OEn=L			250	μs
t <sub>CFG_DB</sub>	Debounce time for SEL[1:0] and I2C_EN configuration pins (Refer to <a href="#">Figure 1</a> ) OEn=L	150			ns
t <sub>VCC_RAM</sub> P	V <sub>CC</sub> power supply (0 – 100%) ramp time requirement (Refer to <a href="#">Figure 1</a> )	0.1		100	ms

## 6.9 Timing Requirements (2.4 V ≤ V<sub>CC</sub> ≤ 5.5 V)

All minimum/maximum specifications are at T<sub>A</sub> = -40/85°C, V<sub>CC</sub> = 2.4 V/5.5 V, unless otherwise noted. Typical specifications are at T<sub>A</sub> = 25°C, V<sub>CC</sub> = 3.3 V, unless otherwise noted.

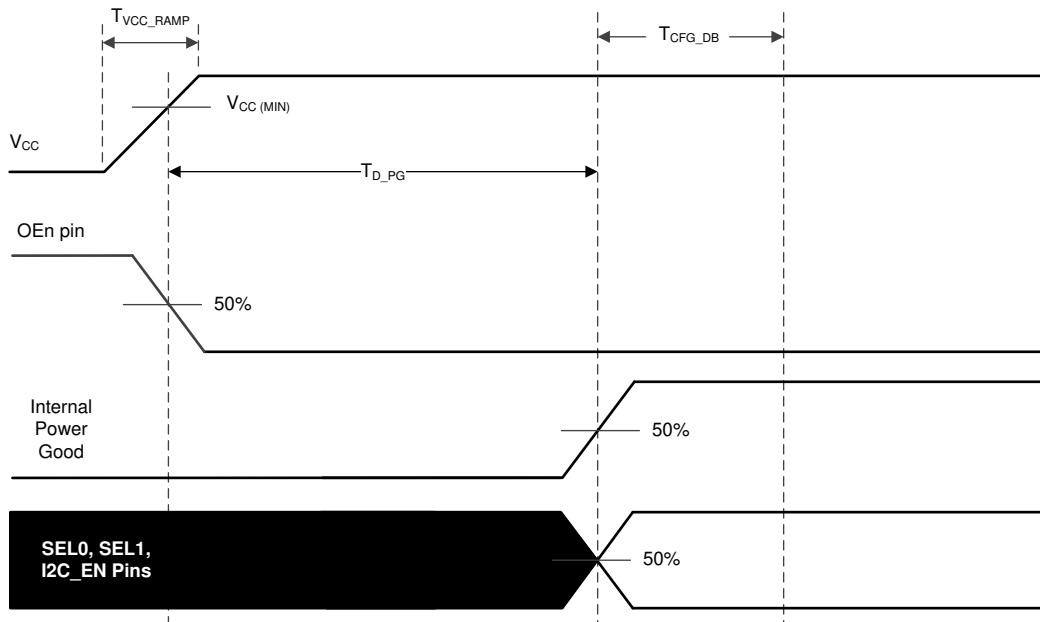
	TEST CONDITIONS	MIN	NOM	MAX	UNIT
t <sub>ON_MICG</sub> ND	Switch ON time for MIC/AGND path V <sub>PU</sub> =1.8V, R <sub>PU</sub> =2100Ω, C <sub>L</sub> =50pF			12	μs
t <sub>OFF_MICG</sub> ND	Switch OFF time for MIC/AGND path V <sub>PU</sub> =1.8V, R <sub>PU</sub> =2100Ω, C <sub>L</sub> =50pF			6	μs
t <sub>ON_HS</sub>	Switch ON time for high-speed path R <sub>S</sub> =50Ω, R <sub>L</sub> =50Ω			1.2	μs
t <sub>OFF_HS</sub>	Switch OFF time for high-speed path R <sub>S</sub> =50Ω, R <sub>L</sub> =50Ω			780	ns
t <sub>BBM</sub>	Break before make off time for MIC/AGND path V <sub>PU</sub> =1.8V, R <sub>PU</sub> =2100Ω, R <sub>L</sub> =50Ω, C <sub>L</sub> =50pF	1300			ns
t <sub>FLIP</sub>	Response time for the FLIP pin R <sub>S</sub> =50Ω, R <sub>L</sub> =50Ω			1.1	μs
t <sub>DEV_ENA</sub> BLE	Device enable time from OEn = L to device ready OEn=L			450	μs

**Timing Requirements (2.4 V ≤ V<sub>CC</sub> ≤ 5.5 V) (continued)**

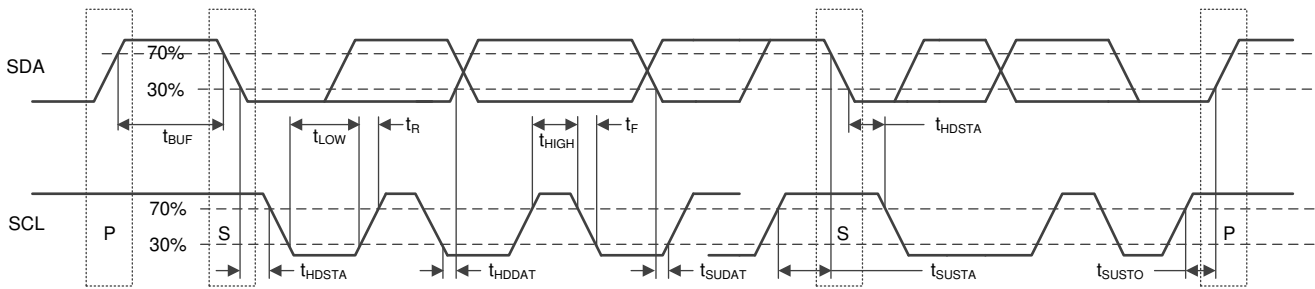
All minimum/maximum specifications are at T<sub>A</sub> = -40/85°C, V<sub>CC</sub> = 2.4 V/5.5 V, unless otherwise noted. Typical specifications are at T<sub>A</sub> = 25°C, V<sub>CC</sub> = 3.3 V, unless otherwise noted.

		TEST CONDITIONS	MIN	NOM	MAX	UNIT
t <sub>DEV_DISABLE</sub>	Device disable time from OEn = H to device shutdown	OEn=H			200	ns
t <sub>D_PG</sub>	V <sub>CC (MIN)</sub> to Internal Power Good asserted high (Refer to <a href="#">图 1</a> )	OEn=L			250	μs
t <sub>CFG_DB</sub>	Debounce time for SEL[1:0] and I2C_EN configuration pins (Refer to <a href="#">图 1</a> )	OEn=L	140			ns
t <sub>VCC_RAM_P</sub>	V <sub>CC</sub> power supply (0 – 100%) ramp time requirement (Refer to <a href="#">图 1</a> )		0.1		100	ms

### 6.10 Timing Diagrams



**图 1. Power-Up Timing**



**图 2. I<sup>2</sup>C Timing Diagram Definitions**

### 6.11 Typical Characteristics

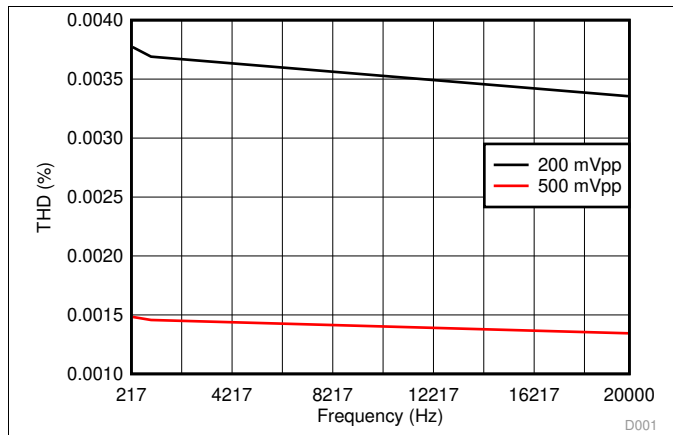


图 3. S3PX Total Harmonic Distortion

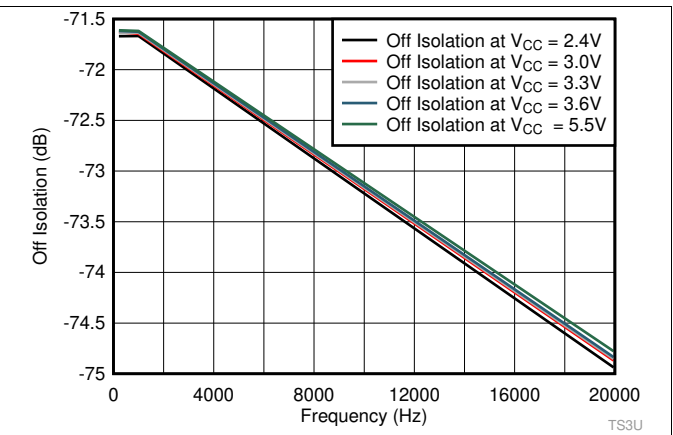


图 4. Off Isolation

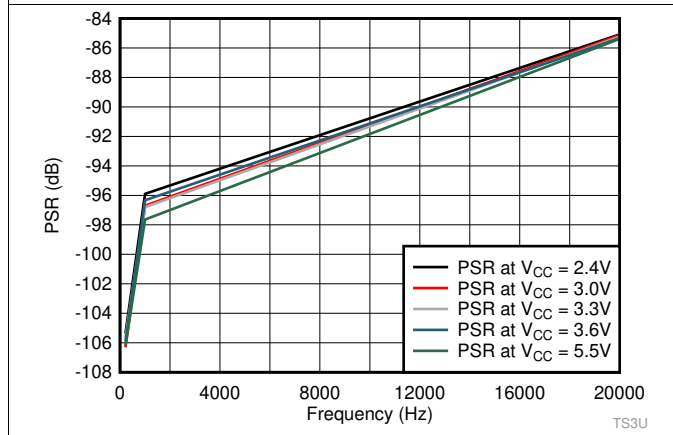


图 5. Power Supply Rejection

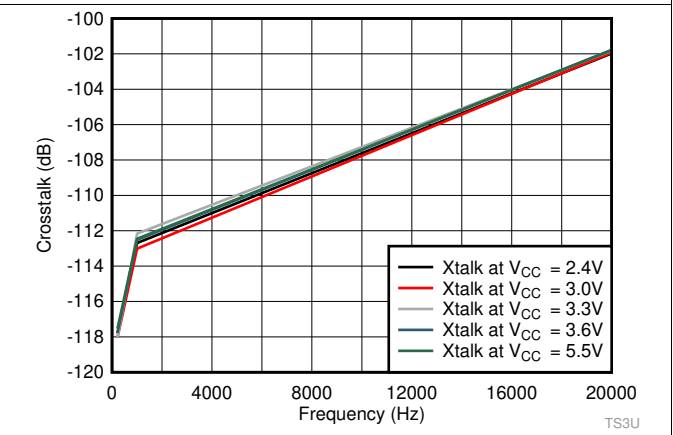
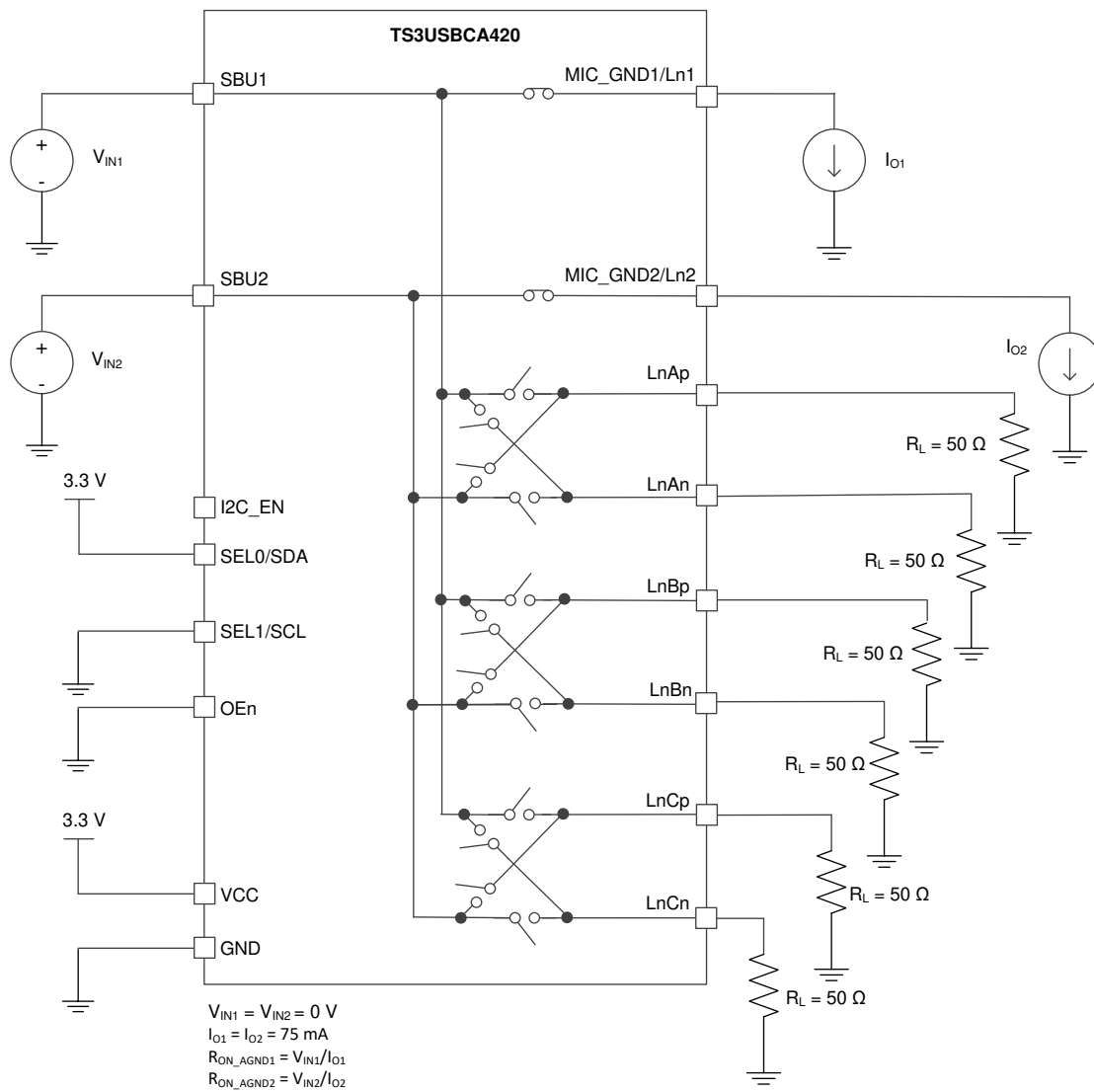


图 6. Crosstalk

## 7 Parameter Measurement Information



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图 7. ON-State Resistance for the Analog Audio GND ( $R_{ON\_AGND}$ )

Parameter Measurement Information (接下页)

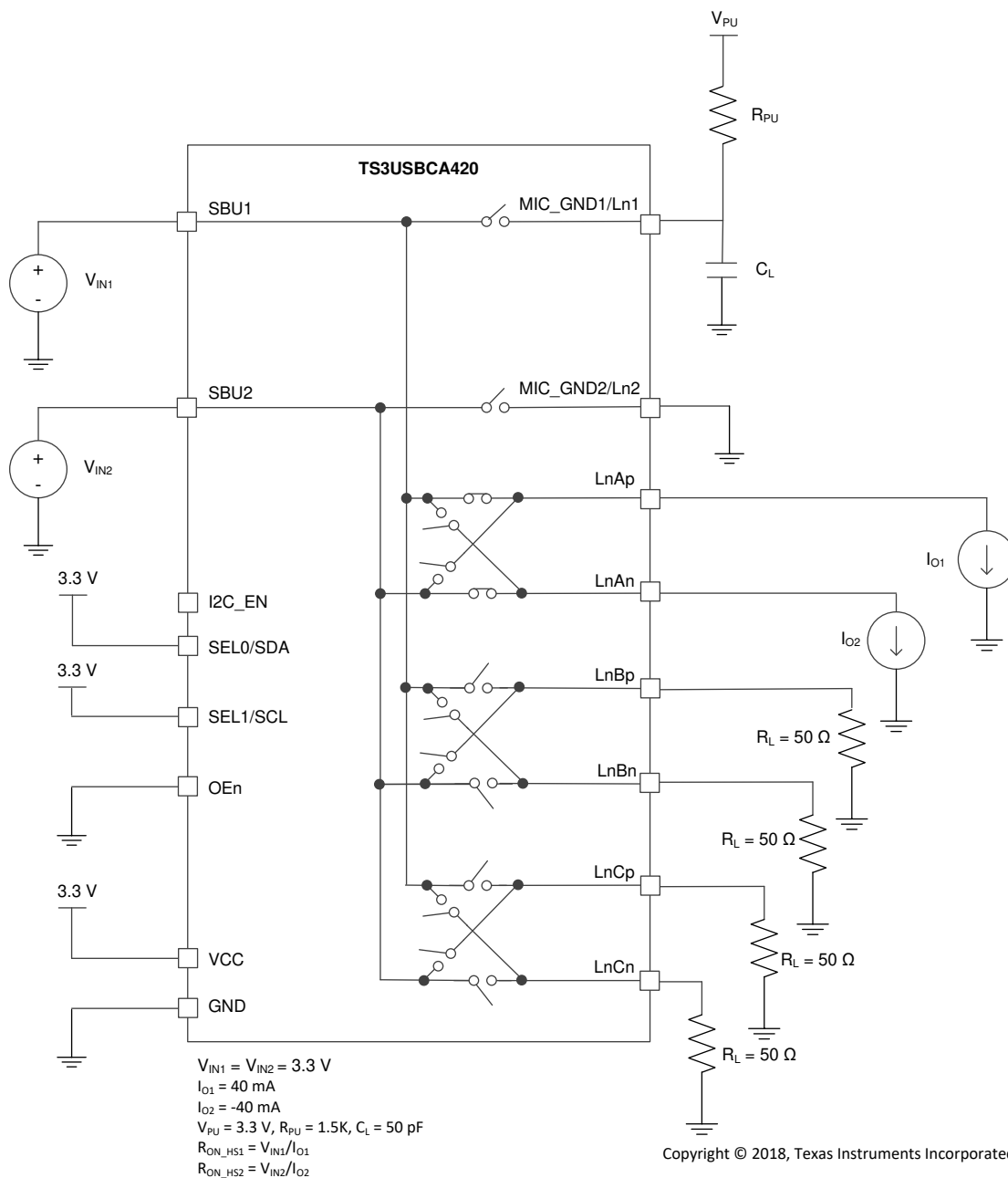


图 8. ON-State Resistance for High-Speed Data Paths ( $R_{ON\_HS}$ )

Parameter Measurement Information (接下页)

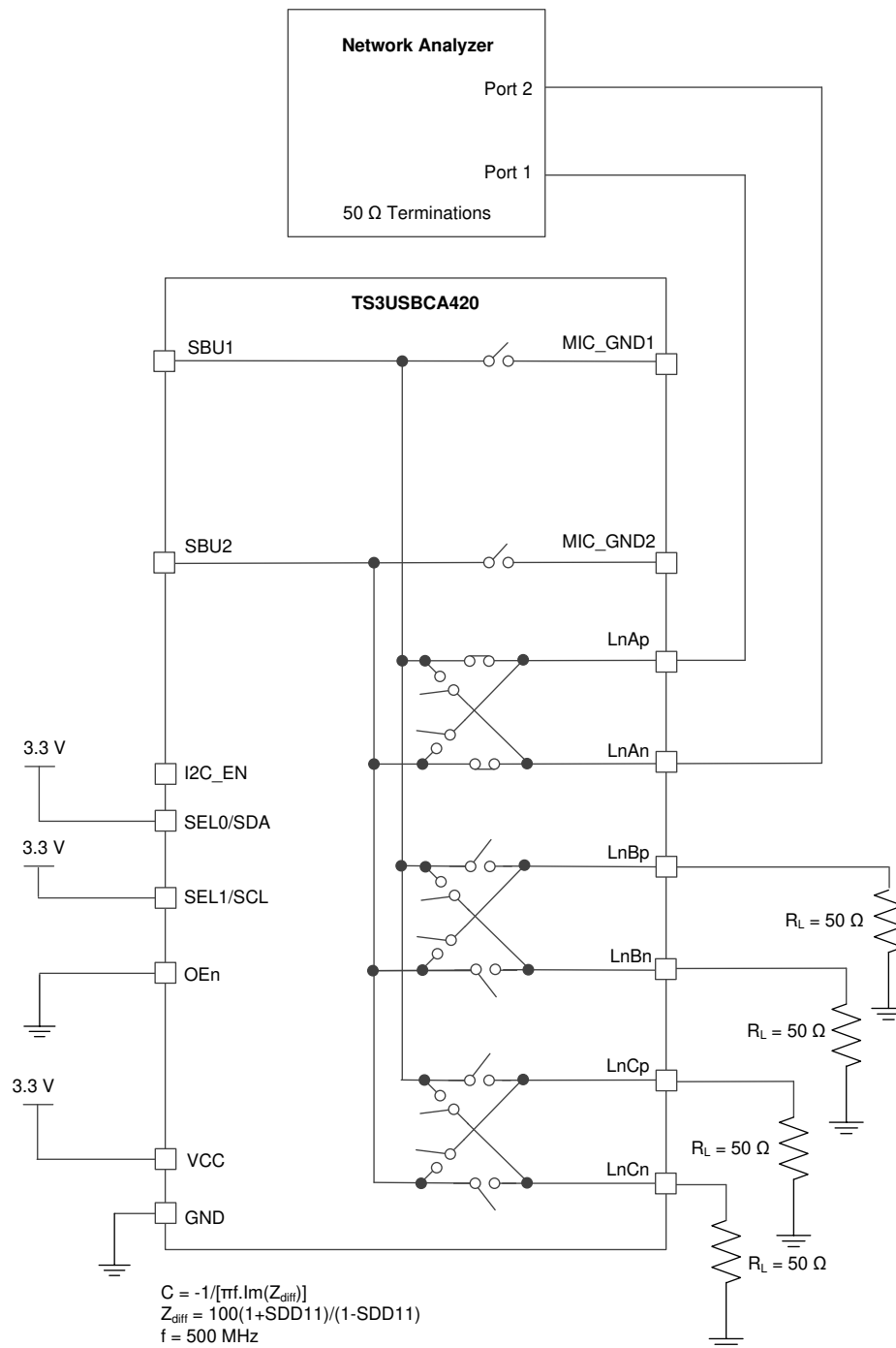


图 9. ON-State and OFF-State Output Capacitance for High-Speed Data Paths ( $C_{ON\_HS}$ ,  $C_{OFF\_HS}$ )



Parameter Measurement Information (接下页)

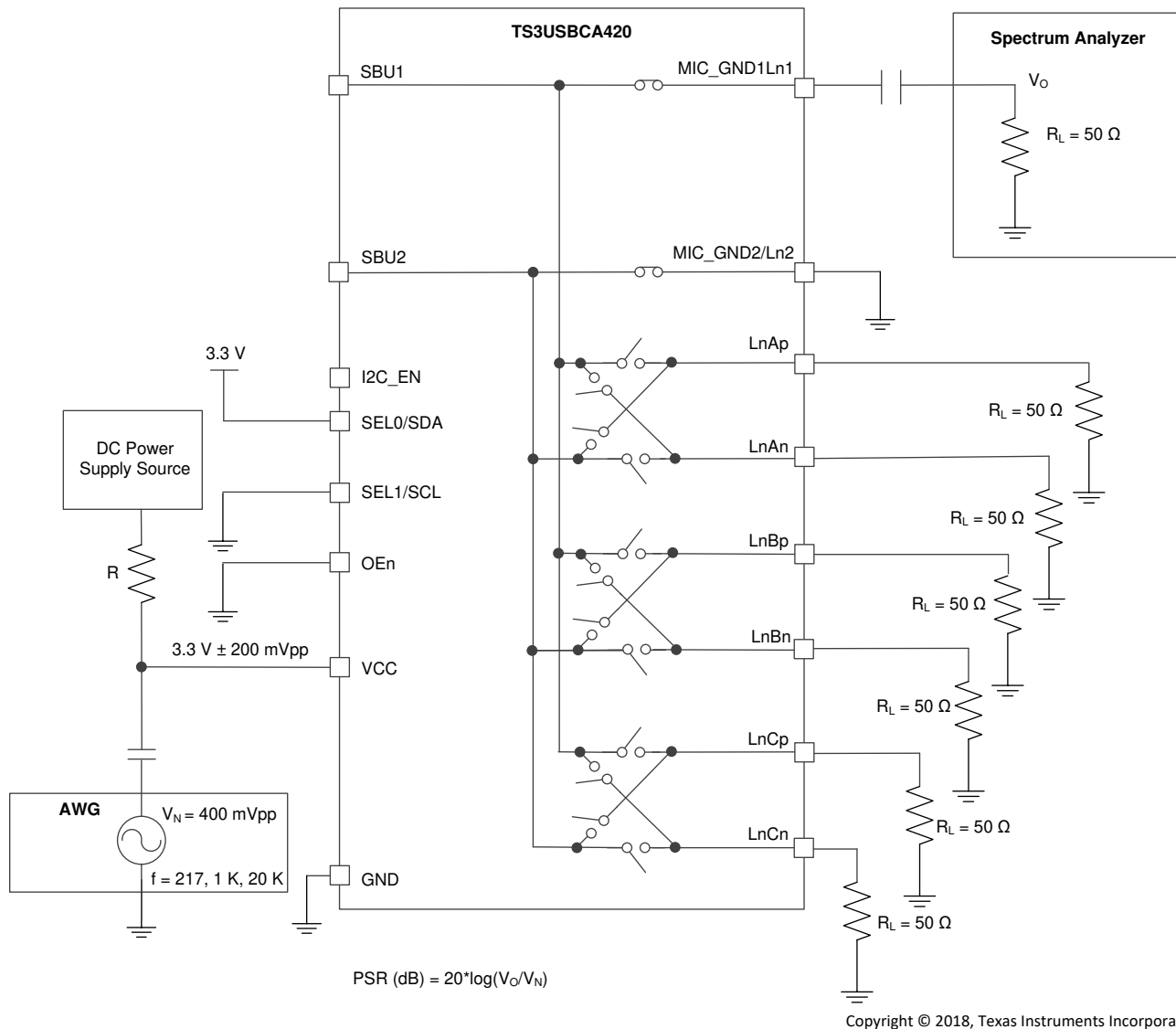
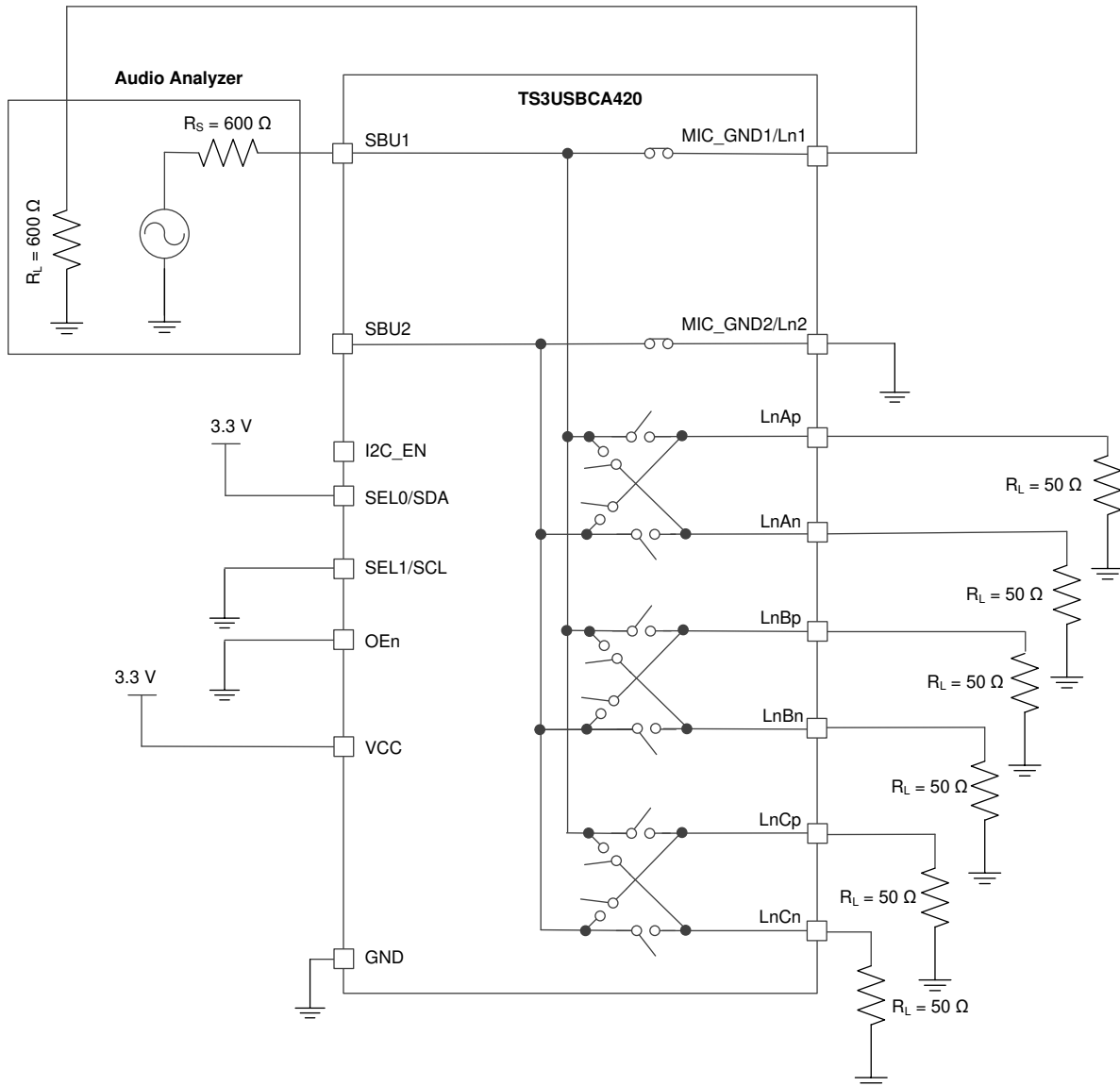


图 10. Power Supply Rejection (PSR)

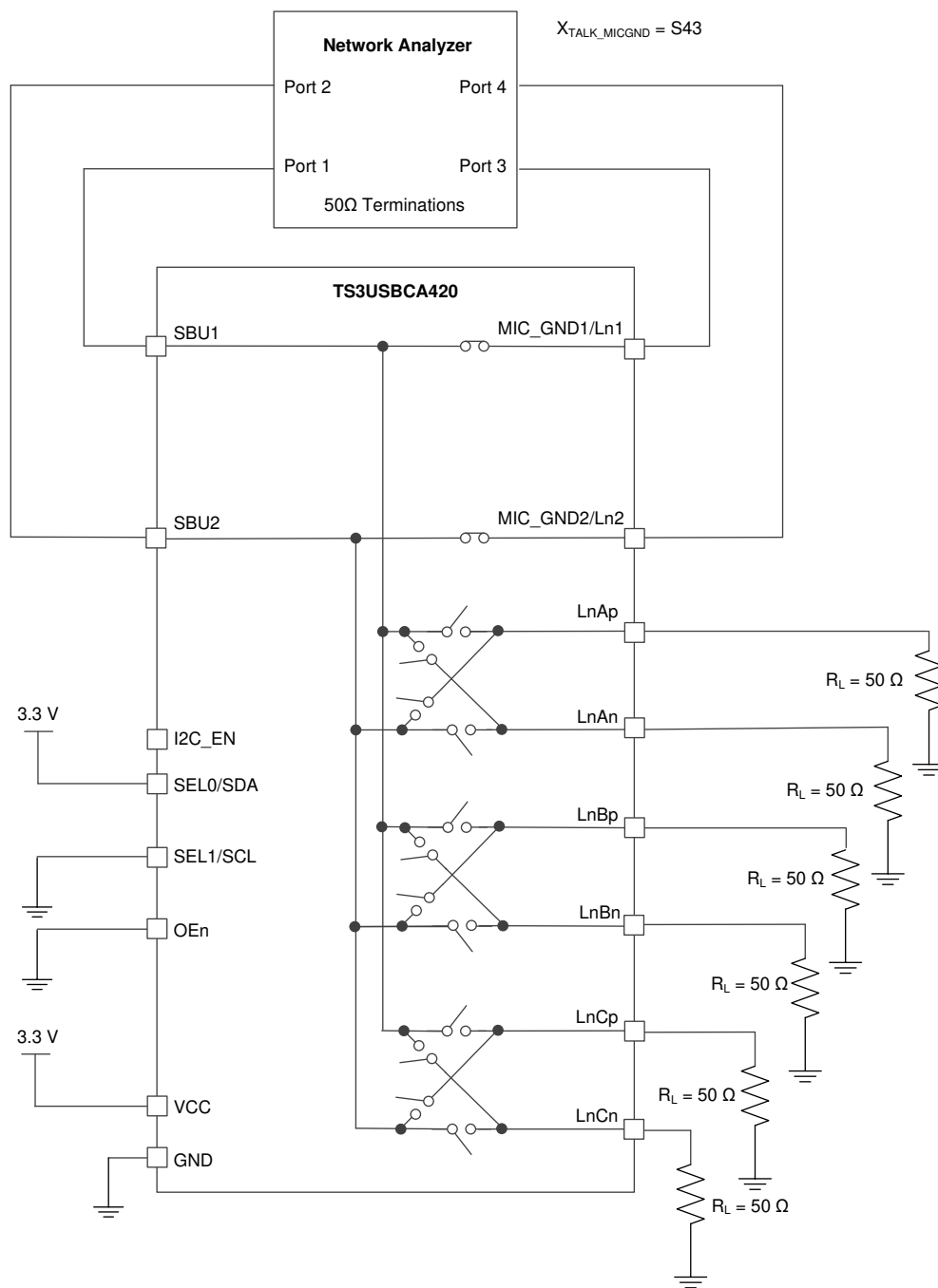
Parameter Measurement Information (接下页)



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图 11. Total Harmonic Distortion (THD)

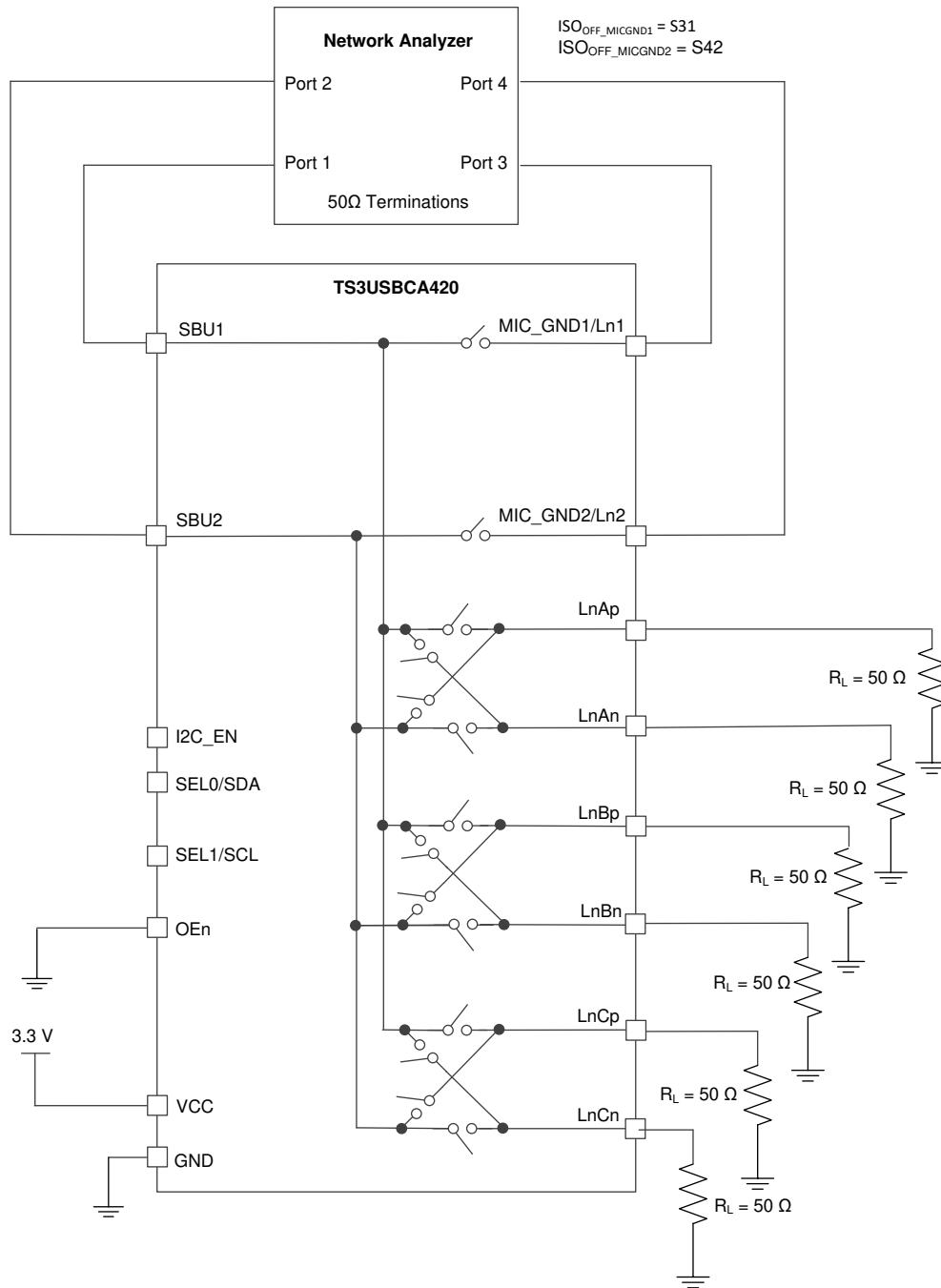
Parameter Measurement Information (接下页)



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图 12. Crosstalk Between MIC and AGND (XTALK<sub>MICGND</sub>)

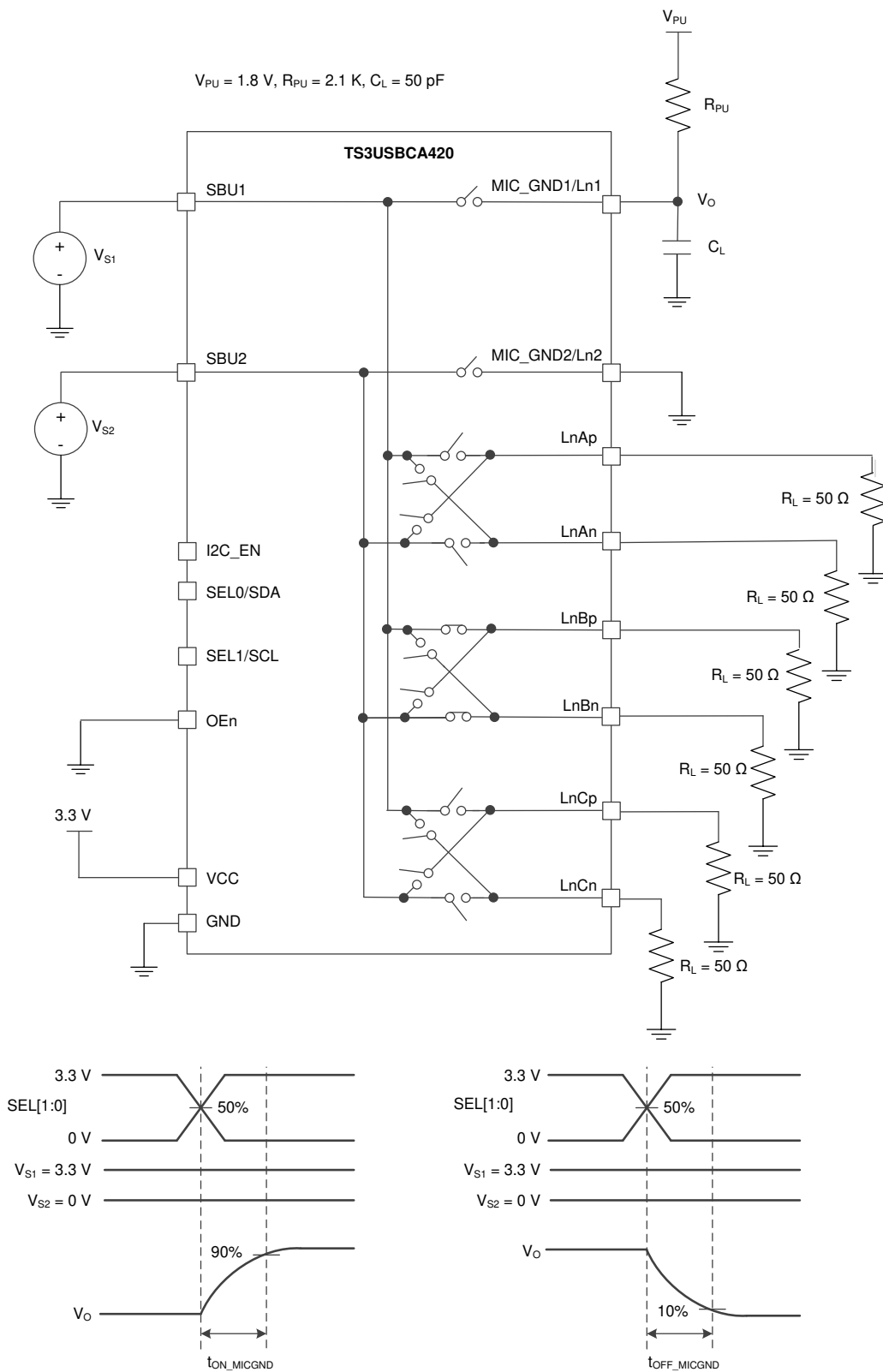
Parameter Measurement Information (接下页)



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图 13. OFF Isolation (ISO<sub>OFF\_MICGND</sub>)

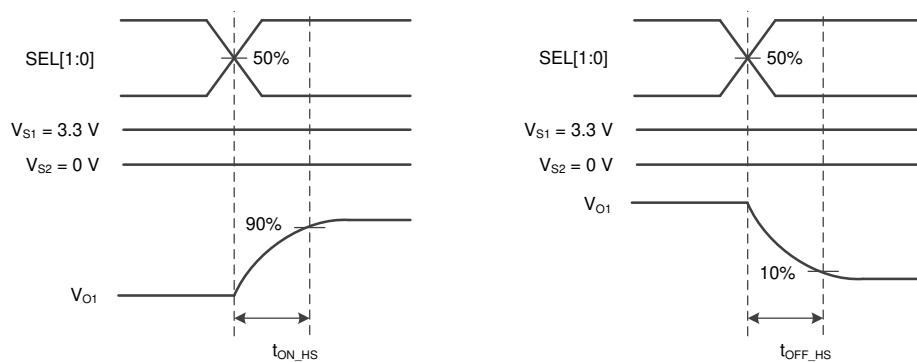
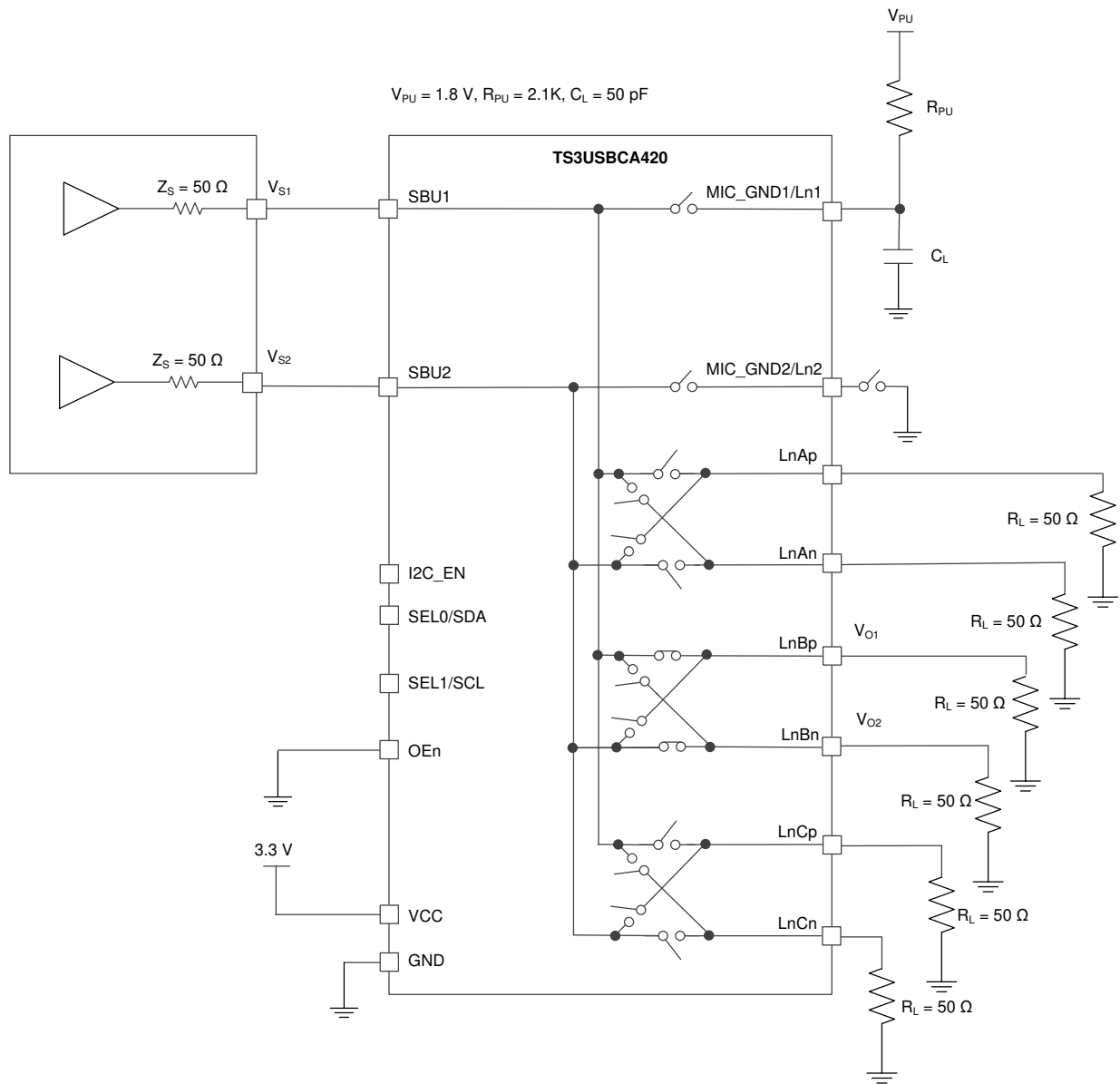
Parameter Measurement Information (接下页)



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图 14. Turn-ON time ( $t_{ON}$ ) and Turn-OFF time ( $t_{OFF}$ ) for MIC and AGND

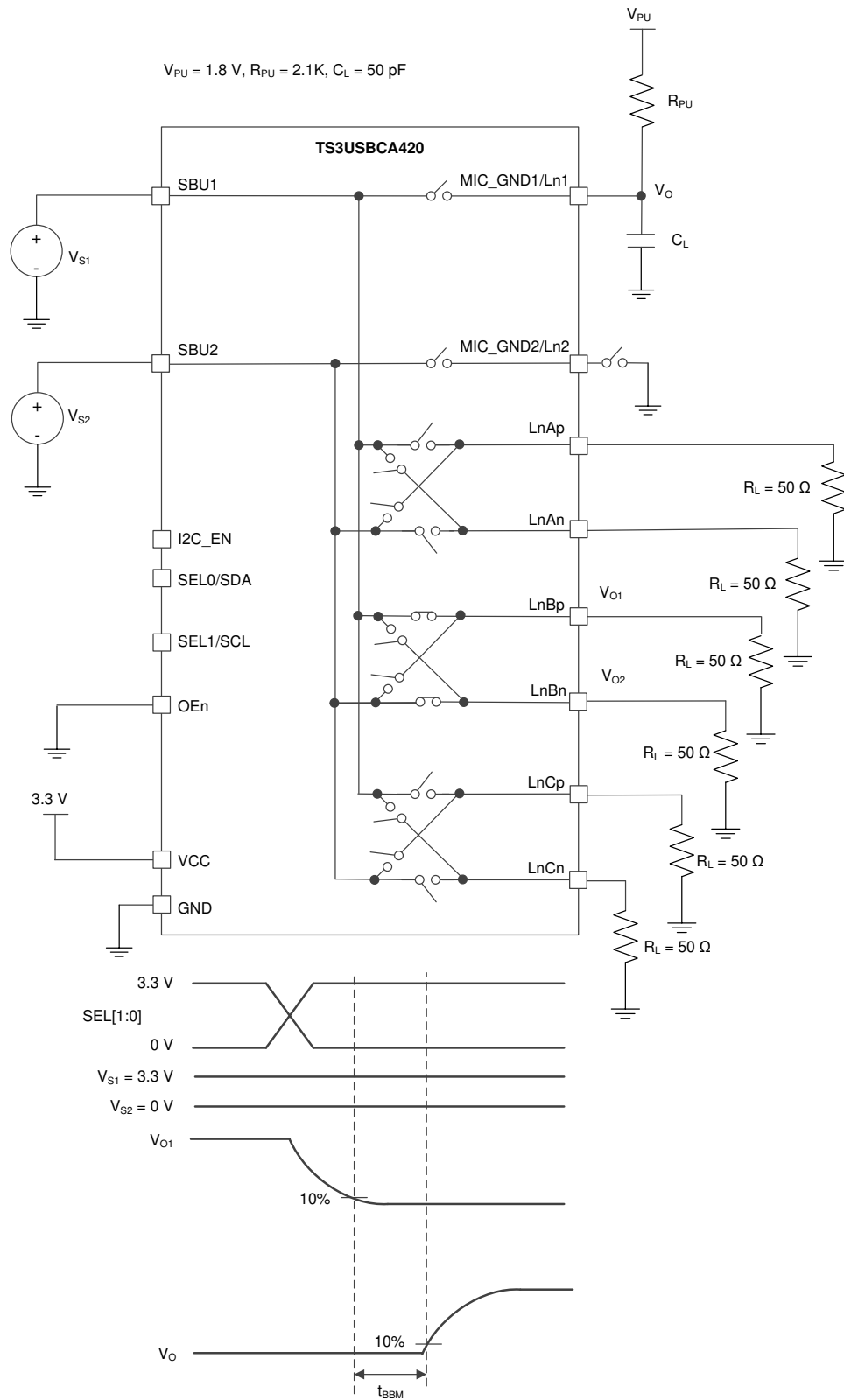
Parameter Measurement Information (接下页)



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图 15. Turn-ON time ( $t_{ON}$ ) and Turn-OFF time ( $t_{OFF}$ ) for High-Speed Data Paths

Parameter Measurement Information (接下页)



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图 16. Break-Before-Make Time ( $t_{BBM}$ )

## 8 Detailed Description

### 8.1 Overview

The TS3USBCA4 is a passive 4:1 (TS3USBCA420) and 3:1 (TS3USBCA410) MUX. It supports differential or single-ended signals on the SBU1/SBU2 terminals of a USB Type-C connected to different interfaces. The signals can be DisplayPort auxiliary (AUX), analog audio MIC and AGND, PCIe differential clock, or any other supported generic differential or single-ended signals.

The audio path features ultra-low ON-state resistance ( $R_{ON}$ ), low crosstalk and excellent total harmonic distortion (THD). The break-before-make feature prevents signal distortion during signal transfer from one channel to another. The high-speed paths support bandwidth as high as 500 MHz to provide adequate support for DisplayPort AUX, PCIe clock, and other similar signals. Together with low power consumption, these features make this device suitable for portable audio applications.

The TS3USBCA4 supports operation from a wide  $V_{CC}$  range between 2.4 V and 5.5 V, which gives the system designer the flexibility of powering the device from various sources, such as a regulator, a single-cell battery, or VBUS. The TS3USBCA4 provides options for both commercial and industrial temperature ranges.

### 8.2 Functional Block Diagram

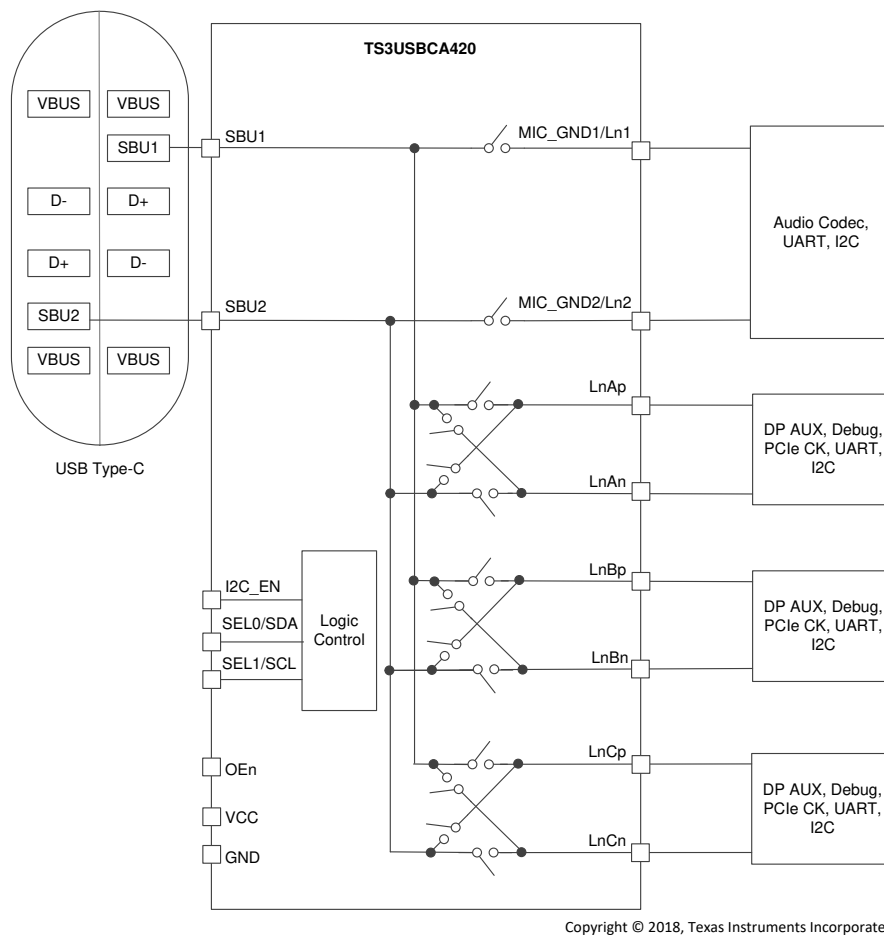


图 17. Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Analog Audio Path

The TS3USBCA4 supports analog audio switching between the SBU1 and SBU2 pins on one side of the switch. It supports the MIC\_GND1 and MIC\_GND2 pins on the other side of the switch. This audio path has an ultra-low ON resistance and low total harmonic distortion for better audio performance.

The MIC and AGND paths are identical by design, with both providing ultra-low  $R_{ON}$ . The audio path does not support flipping MIC and AGND. The audio codec should provide this function.

### 8.3.2 High-Speed Paths

The TS3USBCA4 supports three (TS3USBCA420) or two (TS3USBCA410) high-speed paths between the SBU1 and SBU2 pins on one side of the switch. The LnAp/LnAn, LnBp/LnBn or LnCp/LnCn pins on the other side of the switch. The high-speed paths are identical by design. All high-speed paths have a 500-MHz bandwidth, a low ON-state resistance, and low additive random jitter for signal integrity. For different USB Type-C plug orientations, the polarity of each high-speed lane can be flipped through the I<sup>2</sup>C interface in TS3USBCA420, or through either the I<sup>2</sup>C interface or pin control in TS3USBCA410.

### 8.3.3 3-level Input

The 3-level input pin I2C\_EN is used to enable the I<sup>2</sup>C interface and to choose between two I<sup>2</sup>C slave addresses to avoid address conflict. The settings for the three levels are shown in [表 1](#).

**表 1. 3-Level Control Pin Settings**

Level	I2C_EN Pin Settings	Configuration Mode
L	Tied directly to GND or left floating	Pin-configuration mode
M	Tied directly to $V_{CC}/2$	I <sup>2</sup> C-configuration mode with ADDR0
H	Tied directly to $V_{CC}$	I <sup>2</sup> C-configuration mode with ADDR1

## 8.4 Device Functional Modes

Switch selection and flipping can be controlled either through the I<sup>2</sup>C interface in I<sup>2</sup>C-configuration mode or through the control pins (SEL0, SEL1, and FLIP when applicable) in pin-configuration mode, according to 表 1. 表 2 and 表 3 show the configuration truth table for TS3USBCA420 and TS3USBCA410, respectively. Note in TS3USBCA420 the flipping capability is available only in I<sup>2</sup>C-configuration mode.

**表 2. TS3USBCA420 Switch Configuration Truth Table<sup>(1)</sup>**

{SWSEL[1:0], FLIPSEL} (I <sup>2</sup> C-Configuration Mode)	{SEL1, SEL0} (Pin-Configuration Mode)	Input Pin	Output Pin
000	LL	SBU1	LnBp
		SBU2	LnBn
001		SBU1	LnBn
		SBU2	LnBp
010	LH	SBU1	MIC_GND1/Ln1
		SBU2	MIC_GND2/Ln2
011		SBU1	MIC_GND1/Ln1
		SBU2	MIC_GND2/Ln2
100	HL	SBU1	LnCp
		SBU2	LnCn
101		SBU1	LnCp
		SBU2	LnCn
110	HH	SBU1	LnAp
		SBU2	LnAn
111		SBU1	LnAn
		SBU2	LnAp

(1) For normal operation, drive OEn low (and in I<sup>2</sup>C mode set DEVICE\_ENABLE = 1'b1). Driving the OEn pin high (or in I<sup>2</sup>C mode setting DEVICE\_ENABLE = 1'b0) disables the switch. Note: The ports which are not selected by the control lines are in high impedance state

**表 3. TS3USBCA410 Switch Configuration Truth Table<sup>(1)</sup>**

{SWSEL[1:0], FLIPSEL} (I <sup>2</sup> C-Configuration Mode)	{SEL1, SEL0, FLIP} (Pin-Configuration Mode)	Input Pin	Output Pin
000	LLL	SBU1	LnBp
		SBU2	LnBn
001	LLH	SBU1	LnBn
		SBU2	LnBp
010	LHL	SBU1	MIC_GND1/Ln1
		SBU2	MIC_GND2/Ln2
011	LHH	SBU1	MIC_GND1/Ln1
		SBU2	MIC_GND2/Ln2
100	HLL	SBU1	
		SBU2	
101	HLH	SBU1	
		SBU2	
110	HHL	SBU1	LnAp
		SBU2	LnAn
111	HHH	SBU1	LnAn
		SBU2	LnAp

(1) For normal operation, drive OEn low (and in I<sup>2</sup>C mode set DEVICE\_ENABLE = 1'b1). Driving the OEn pin high (or in I<sup>2</sup>C mode setting DEVICE\_ENABLE = 1'b0) disables the switch. Note: The ports which are not selected by the control lines are in high impedance state

In addition to switch control, the I<sup>2</sup>C-configuration mode also allows enabling and disabling the device through the *DEVICE\_ENABLE* register. [表 4](#) shows the details.

**表 4. TS3USBCA4 Enable/Disable Truth Table**

OEn	DEVICE_ENABLE	Device Behavior
L	0	Device is shut down with I <sub>OFF_I2C</sub> . On-chip bandgap and IO buffers are still on. I <sup>2</sup> C is functional.
L	1	Normal operation.
H	X	Device is under reset with I <sub>OFF_OEN</sub> . On-chip bandgap and IO buffers are off. I <sup>2</sup> C is not functional.

## 8.5 Programming

The TS3USBCA4 can be controlled using I<sup>2</sup>C. The SCL and SDA terminals are used for I<sup>2</sup>C clock and I<sup>2</sup>C data respectively.

**表 5. TS3USBCA4 I<sup>2</sup>C Slave Address**

ADDR	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (W/R)
ADDR0	1	0	1	1	1	0	0	0/1
ADDR1	1	0	1	1	1	0	1	0/1

The following procedure should be followed to write to TS3USBCA4 I<sup>2</sup>C registers:

1. The master initiates a write operation by generating a start condition (S), followed by the TS3USBCA4 7-bit address and a zero-value “W/R” bit to indicate a write cycle
2. The TS3USBCA4 acknowledges the address cycle.
3. The master presents the sub-address (I<sup>2</sup>C register within TS3USBCA4) to be written, consisting of one byte of data, MSB-first.
4. The TS3USBCA4 acknowledges the sub-address cycle.
5. The master presents the first byte of data to be written to the I<sup>2</sup>C register.
6. The TS3USBCA4 acknowledges the byte transfer.
7. The master may continue presenting additional bytes of data to be written, with each byte transfer completing with an acknowledge from the TS3USBCA4.
8. The master terminates the write operation by generating a stop condition (P).

The following procedure should be followed to read the TS3USBCA4 I<sup>2</sup>C registers:

1. The master initiates a read operation by generating a start condition (S), followed by the TS3USBCA4 7-bit address and a one-value “W/R” bit to indicate a read cycle
2. The TS3USBCA4 acknowledges the address cycle.
3. The TS3USBCA4 transmit the contents of the memory registers MSB-first starting at register 00h or last read sub-address+1. If a write to the I<sup>2</sup>C register occurred prior to the read, then the TS3USBCA4 shall start at the sub-address specified in the write.
4. The TS3USBCA4 shall wait for either an acknowledge (ACK) or a not-acknowledge (NACK) from the master after each byte transfer; the I<sup>2</sup>C master acknowledges reception of each data byte transfer.
5. If an ACK is received, the TS3USBCA4 transmits the next byte of data.
6. The master terminates the read operation by generating a stop condition (P).

The following procedure should be followed for setting a starting sub-address for I<sup>2</sup>C reads:

1. The master initiates a write operation by generating a start condition (S), followed by the TS3USBCA4 7-bit address and a zero-value “W/R” bit to indicate a write cycle.
2. The TS3USBCA4 acknowledges the address cycle.
3. The master presents the sub-address (I<sup>2</sup>C register within TS3USBCA4) to be written, consisting of one byte of data, MSB-first.
4. The TS3USBCA4 acknowledges the sub-address cycle.
5. The master terminates the write operation by generating a stop condition (P).

### 注

Upon reset, the TS3USBCA4 sub-address is always set to 0x00. The TS3USBCA4 increments the sub-address by one after each successful read or write transaction, so that the next read transaction that does not explicitly specify the sub-address will start from the next register.

## 8.6 Register Maps

### 8.6.1 TS3USBCA4 Registers

Table 6 lists the memory-mapped registers for the TS3USBCA4 registers. All register offset addresses not listed in Table 6 should be considered as reserved locations and the register contents should not be modified.

**Table 6. TS3USBCA4 Registers**

Offset	Acronym	Register Name	Section
9h	Revision_ID	Revision ID	<a href="#">Go</a>
Ah	General_1	Enable and FLIPSEL control	<a href="#">Go</a>
Bh	General_2	SWSEL control	<a href="#">Go</a>

Complex bit access types are encoded to fit into small table cells. Table 7 shows the codes that are used for access types in this section.

**Table 7. TS3USBCA4 Access Type Codes**

Access Type	Code	Description
<b>Read Type</b>		
R	R	Read
<b>Write Type</b>		
W	W	Write
<b>Reset or Default Value</b>		
-n		Value after reset or the default value

#### 8.6.1.1 Revision\_ID Register (Offset = 9h) [reset = 0h]

Revision\_ID is shown in Figure 18 and described in Table 8.

Return to [Summary Table](#).

**Figure 18. Revision\_ID Register**

7	6	5	4	3	2	1	0
RESERVED				REVISION_ID			
R-0h				R-0h			

**Table 8. Revision\_ID Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-4	RESERVED	R	0h	Reserved
3-0	REVISION_ID	R	0h	Silicon revision.

#### 8.6.1.2 General\_1 Register (Offset = Ah) [reset = 0h]

General\_1 is shown in Figure 19 and described in Table 9.

Return to [Summary Table](#).

**Figure 19. General\_1 Register**

7	6	5	4	3	2	1	0
RESERVED						DEVICE_ENAB LE	FLIPSEL
R-0h						R/W-0h	R/W-0h

**Table 9. General\_1 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	Reserved
1	DEVICE_ENABLE	R/W	0h	Controls the switch enable. 0h = Disabled 1h = Enabled
0	FLIPSEL	R/W	0h	Controls the USB-C orientation. 0h = Normal Orientation 1h = Flip orientation.

**8.6.1.3 General\_2 Register (Offset = Bh) [reset = 0h]**

 General\_2 is shown in [Figure 20](#) and described in [Table 10](#).

 Return to [Summary Table](#).

**Figure 20. General\_2 Register**

7	6	5	4	3	2	1	0
RESERVED						SWSEL	
R-0h						R/W-0h	

**Table 10. General\_2 Register Field Descriptions**

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0h	Reserved
1-0	SWSEL	R/W	0h	This field along with FLIPSEL controls the SBU switch connections. 0h = SBU to LnB 1h = SBU to MICGND 2h = SBU to LnC 3h = SBU to LnA

## 9 Application and Implementation

### 注

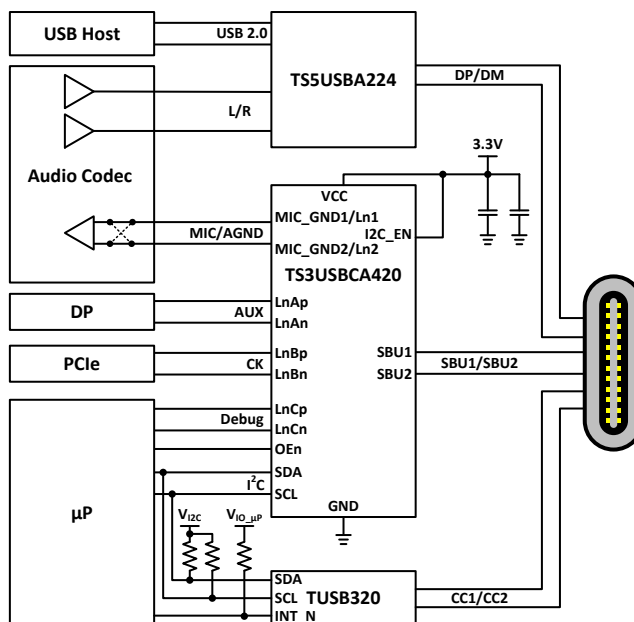
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The SBU1 and SBU2 pins of a USB type-C connector can be re-purposed in different applications. Examples include DisplayPort AUX, analog audio MIC and AGND, and debug signals. The TS3USBCA4 is controlled by a micro-processor (that is, an application processor in a smartphone) that routes SBU1 and SBU2 to the desired destination, such as a DisplayPort source or sink, an audio codec, or a processor. The TS3USBCA4 provides cross-switch capability for different USB type-C plug orientations.

### 9.2 Typical Application

图 21 shows the typical application of TS3USBCA420 in I<sup>2</sup>C-configuration mode from a 3.3-V supply. The I<sup>2</sup>C slave address is set to ADDR1. V<sub>IO\_UP</sub> is the supply for the micro-processor IOs.



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图 21. Application of TS3USBCA420 in I<sup>2</sup>C-Configuration Mode

图 22 shows the typical application of TS3USBCA420 in pin-configuration mode from VBUS. V<sub>IO\_UP</sub> is the supply for the micro-processor IOs.

Typical Application (接下页)

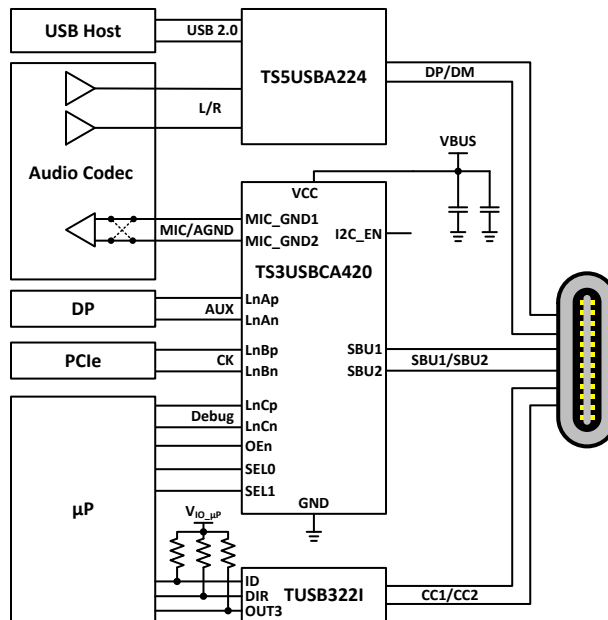
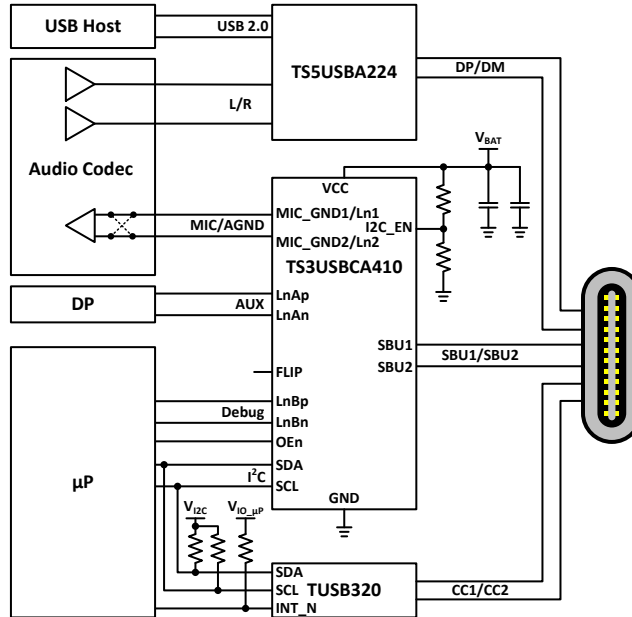


图 22. Application of TS3USBCA420 in Pin-Configuration Mode

图 21 shows the typical application of TS3USBCA410 in I<sup>2</sup>C-configuration mode from V<sub>BAT</sub>. The I<sup>2</sup>C slave address is set to ADDR0. V<sub>IO\_UP</sub> is the supply for the micro-processor IOs.



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图 23. Application of TS3USBCA410 in I<sup>2</sup>C-Configuration Mode

图 22 shows the typical application of TS3USBCA410 in pin-configuration mode from VBUS. V<sub>IO\_UP</sub> is the supply for the micro-processor IOs.



Typical Application (接下页)

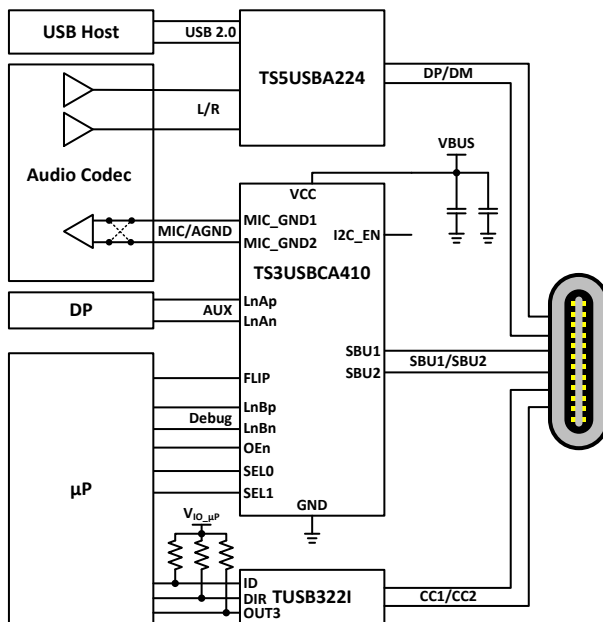


图 24. Application of TS3USBCA410 in Pin-Configuration Mode

9.2.1 Design Requirements

Design requirements of USB type-C and other relevant standards (DisplayPort, analog audio, etc.) must be followed.

9.2.2 Detailed Design Procedure

The design procedure starts with the choice of supply. TS3USBCA4 wide supply range from 2.4 V to 5.5 V gives the designer flexibility when selecting a supply. Examples include, but are not limited to, a single-cell battery, a 3.3-V regulator, or VBUS. The designer must account for the parametric variation of TS3USBCA4 with supply range, the supply range of other components in the system, the IO voltage levels of companion devices, and cost. For example, a regulated 3.3-V  $V_{CC}$  has the advantage of smaller variation of TS3USBCA4 performance compared to a single-cell battery between 2.7 V and 4.3 V. This regulator may add to the system cost and board area.

The next step in the design procedure is to choose between I<sup>2</sup>C- and pin-configuration mode. The I<sup>2</sup>C-configuration mode is preferred because it reduces the number of IOs needed from the micro-processor. Note that in TS3USBCA420 the flip functionality is only available in the I<sup>2</sup>C-configuration mode. The designer can choose from two I<sup>2</sup>C slave addresses through pin-strapping of I2C\_EN to avoid address conflict. The IOs of TS3USBCA4 have well-controlled  $V_{IH}$  and  $V_{IL}$  and are supposed to work with a wide range of IO voltage levels of the micro-processor. However, the designer needs to check the compatibility of the IOs between the micro-processor and TS3USBCA4, and insert level translators when necessary.

In I<sup>2</sup>C-configuration mode, when it is necessary to set I2C\_EN to the middle level to avoid slave address conflict, it is desirable to use as high a resistor value as possible for the resistor divider to minimize the static current through the resistor divider. However, the designer needs to take into account the resistor tolerance and the effect of the on-chip pull-down resistor to ensure a satisfactory voltage margin for  $V_{IM}$  of the I2C\_EN pin.

It should be noted that the bandwidth of the high-speed lanes is defined with the audio channel open. Due to the low  $R_{ON}$  of the audio channel, big parasitic capacitance exists between the audio output port and the SBU port. The load (capacitive and/or resistive) at the audio output port may significantly impact the bandwidth of the high-speed lanes. If bandwidth is importance, the audio channel is preferred. If certain high-speed signals have to go through the high-speed lanes, care should be taken to minimize the load at the audio output port, including the traces.

## Typical Application (接下页)

### 9.2.3 Application Curves

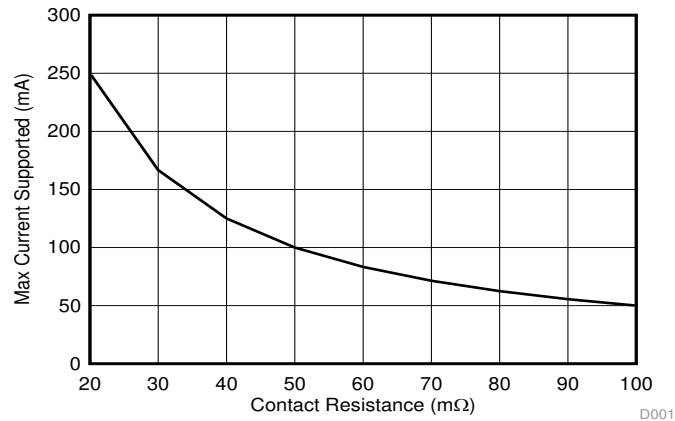


图 25. Max Current vs Contact Resistance

## 10 Power Supply Recommendations

The TS3USBCA4 is designed to operate from a  $V_{CC}$  range between 2.4 V and 5.5 V. The supply is recommended to be decoupled to ground via two de-coupling capacitors of 0.1  $\mu\text{F}$  and 1  $\mu\text{F}$  placed as close as possible to the TS3USBCA4. To ensure a POR trip during a power-down and power-on event the power supply should follow the minimum and maximum  $V_{CC}$  rise and fall times specified in the electrical specifications section.

## 11 Layout

### 11.1 Layout Guidelines

- The  $V_{CC}$  pin must have de-coupling capacitors placed as closely to the device as possible. Typically recommended capacitors are a 0.1- $\mu\text{F}$  and a 1- $\mu\text{F}$  capacitor.
- The total resistance from SBU1 and SBU2 pins of the type-C connector to the MIC\_GND1 and MIC\_GND2 pins of the audio codec should be kept low to avoid degrading the crosstalk performance.
- Route the I<sup>2</sup>C and digital signals away from the audio signals to prevent coupling onto the audio lines.

### 11.2 Layout Example

图 26 shows a layout example of TS3USBCA420.

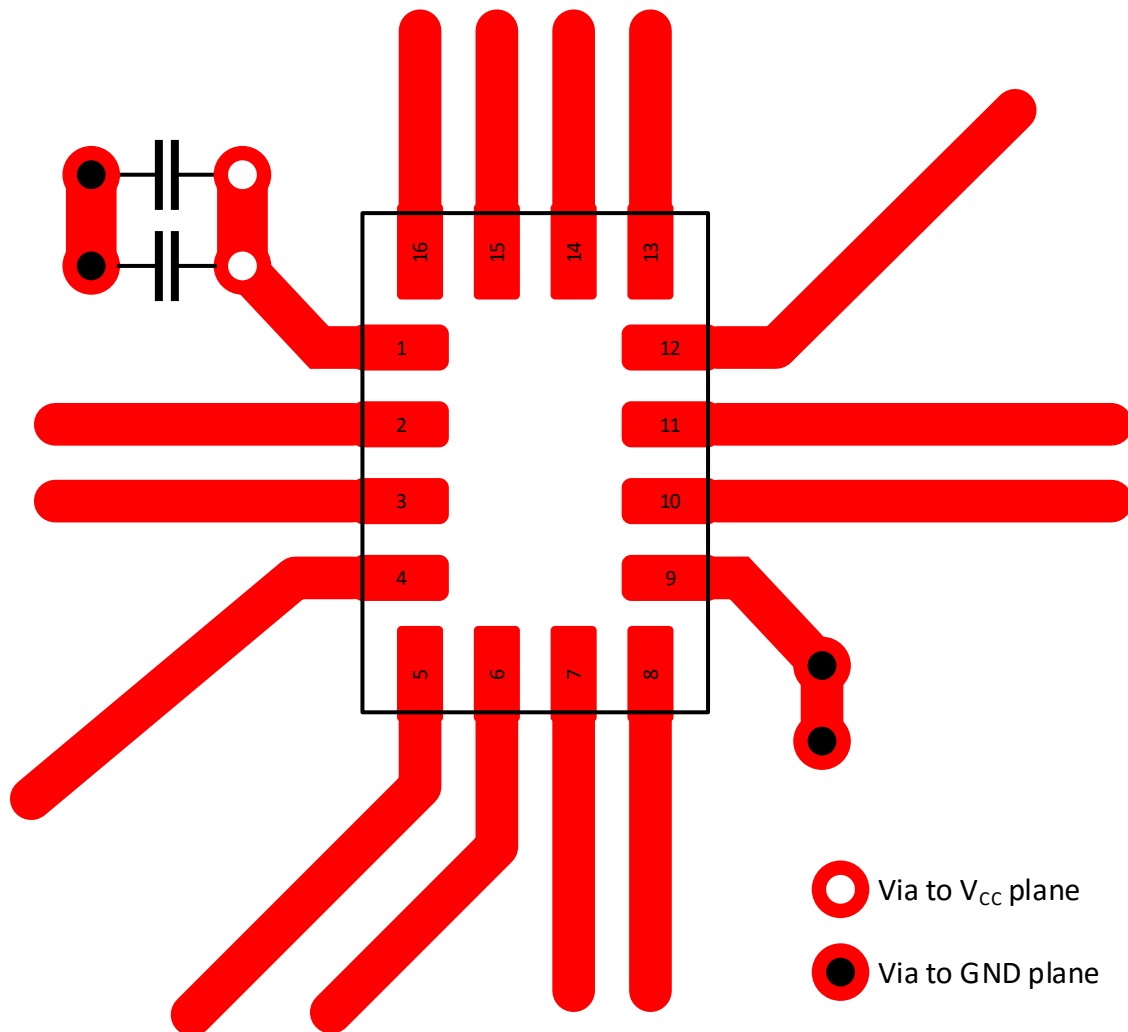


图 26. Layout Example

## 12 器件和文档支持

### 12.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。单击右上角的通知我进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 12.2 支持资源

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS3USBCA410IRSVR	ACTIVE	UQFN	RSV	16	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	410	Samples
TS3USBCA410IRSVT	ACTIVE	UQFN	RSV	16	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	410	Samples
TS3USBCA410RSVR	ACTIVE	UQFN	RSV	16	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	410	Samples
TS3USBCA410RSVT	ACTIVE	UQFN	RSV	16	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	410	Samples
TS3USBCA420IRSVR	ACTIVE	UQFN	RSV	16	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	420	Samples
TS3USBCA420IRSVT	ACTIVE	UQFN	RSV	16	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	420	Samples
TS3USBCA420RSVR	ACTIVE	UQFN	RSV	16	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	420	Samples
TS3USBCA420RSVT	ACTIVE	UQFN	RSV	16	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	0 to 70	420	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS3USBCA410IRSVR	UQFN	RSV	16	3000	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1
TS3USBCA410IRSVT	UQFN	RSV	16	250	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1
TS3USBCA410RSVR	UQFN	RSV	16	3000	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1
TS3USBCA410RSVT	UQFN	RSV	16	250	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1
TS3USBCA420IRSVR	UQFN	RSV	16	3000	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1
TS3USBCA420IRSVT	UQFN	RSV	16	250	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1
TS3USBCA420RSVR	UQFN	RSV	16	3000	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1
TS3USBCA420RSVT	UQFN	RSV	16	250	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS3USBCA410IRSVR	UQFN	RSV	16	3000	189.0	185.0	36.0
TS3USBCA410IRSVT	UQFN	RSV	16	250	189.0	185.0	36.0
TS3USBCA410RSVR	UQFN	RSV	16	3000	189.0	185.0	36.0
TS3USBCA410RSVT	UQFN	RSV	16	250	189.0	185.0	36.0
TS3USBCA420IRSVR	UQFN	RSV	16	3000	189.0	185.0	36.0
TS3USBCA420IRSVT	UQFN	RSV	16	250	189.0	185.0	36.0
TS3USBCA420RSVR	UQFN	RSV	16	3000	189.0	185.0	36.0
TS3USBCA420RSVT	UQFN	RSV	16	250	189.0	185.0	36.0



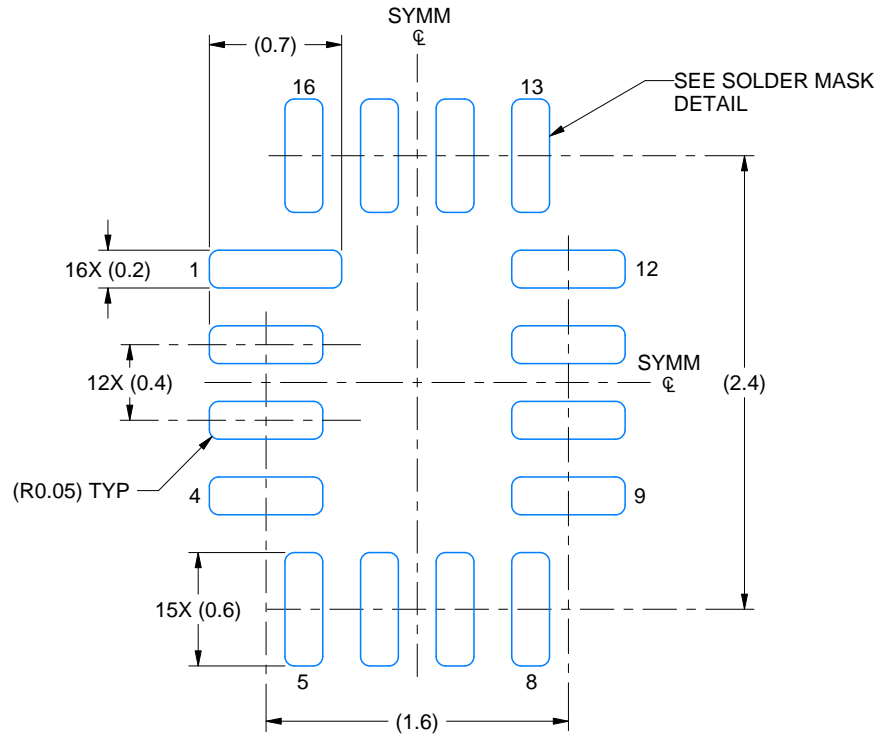


# EXAMPLE BOARD LAYOUT

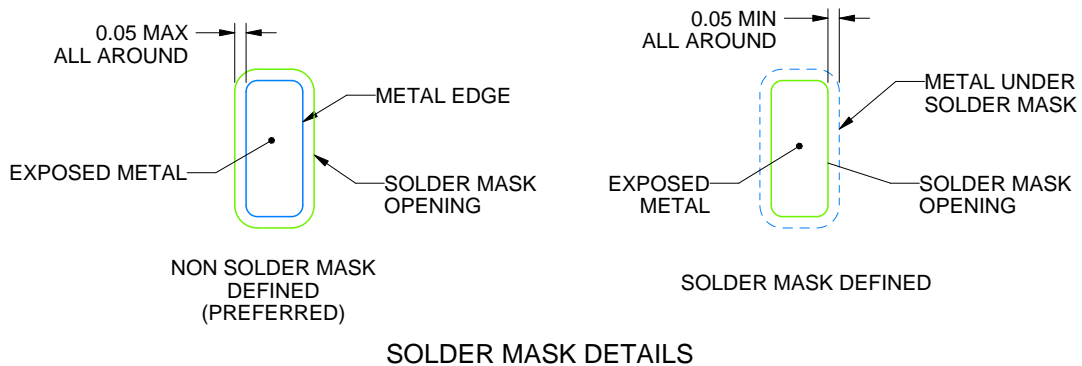
RSV0016A

UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 25X



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NOTES: (continued)

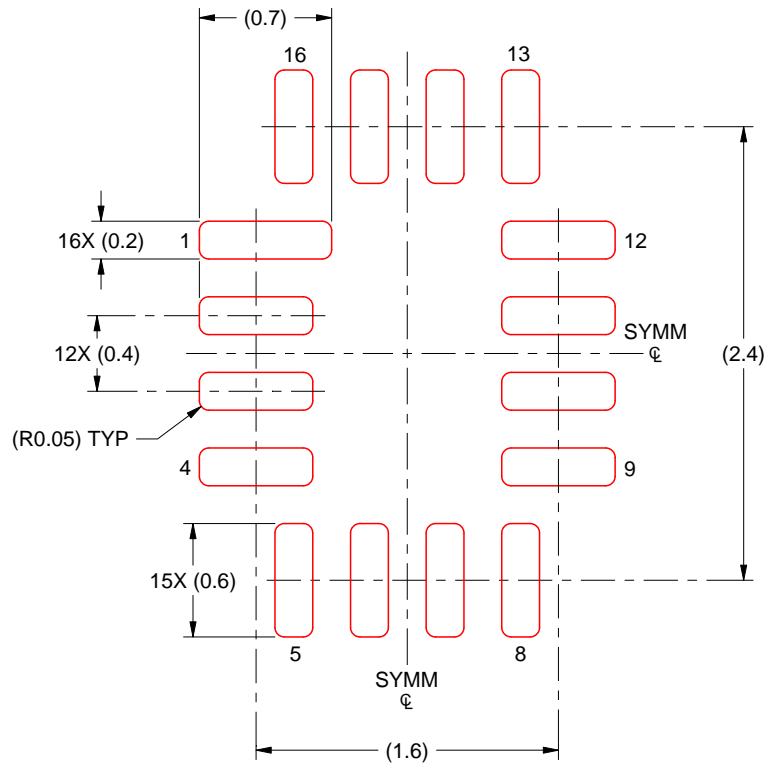
3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

RSV0016A

UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 25X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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