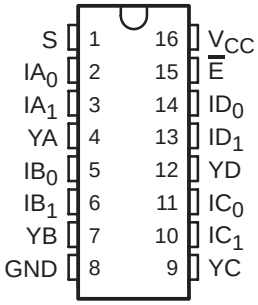
TS5L100
QUAD SPDT WIDE-BANDWIDTH LAN SWITCH WITH LOW ON-STATE RESISTANCE

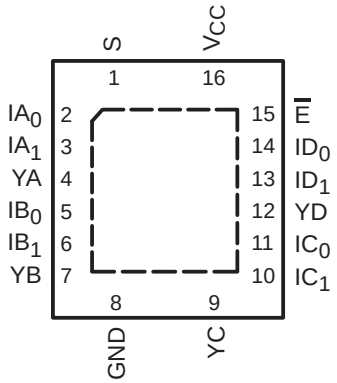
SCDS163A − MAY 2004 − REVISED MAY 2004

- **Wide Bandwidth (BW = 300 MHz Min)**
- **Low Differential Crosstalk (X_{TALK} = −60 dB Typ)**
- **Low Power Consumption (I_{CC} = 3 μA Max)**
- **Bidirectional Data Flow, With Near-Zero Propagation Delay**
- **Low ON-State Resistance (r_{on} = 3 Ω Typ)**
- **V_{CC} Operating Range From 6 V to 6.5 V**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Data and Control Inputs Provide Undershoot Clamp Diode**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **1000-V Charged-Device Model (C101)**
- **Suitable for Both 10 Base-T/100 Base-T Signaling**

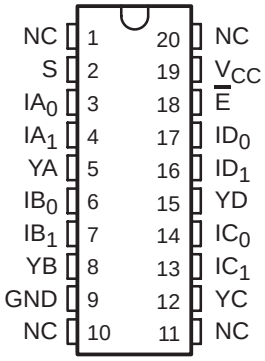
D OR DBQ PACKAGE
(TOP VIEW)



RGY PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)



NC − No internal connection

description/ordering information

The TI TS5L100 LAN switch is a 4-bit 1-of-2 multiplexer/demultiplexer with a single switch-enable ($\overline{E}$) input. When $\overline{E}$ is low, the switch is enabled and the I port is connected to the Y port. When $\overline{E}$ is high, the switch is disabled and the high-impedance state exists between the I and Y ports. The select (S) input controls the data path of the multiplexer/demultiplexer.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	QFN − RGY	Tape and reel	TS5L100RGYR	TG100
	SOIC − D	Tube	TS5L100D	TS5L100
		Tape and reel	TS5L100DR	
	SSOP (QSOP) − DBQ	Tape and reel	TS5L100DBQR	TG100
	TSSOP − PW	Tube	TS5L100PW	TG100
		Tape and reel	TS5L100PWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

description/ordering information (continued)

This device can be used to replace mechanical relays in LAN applications. This device has low r_{on}, wide bandwidth, and low differential crosstalk, making it suitable for 10 Base-T, 100 Base-T, and various other LAN applications.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down, $\overline{E}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

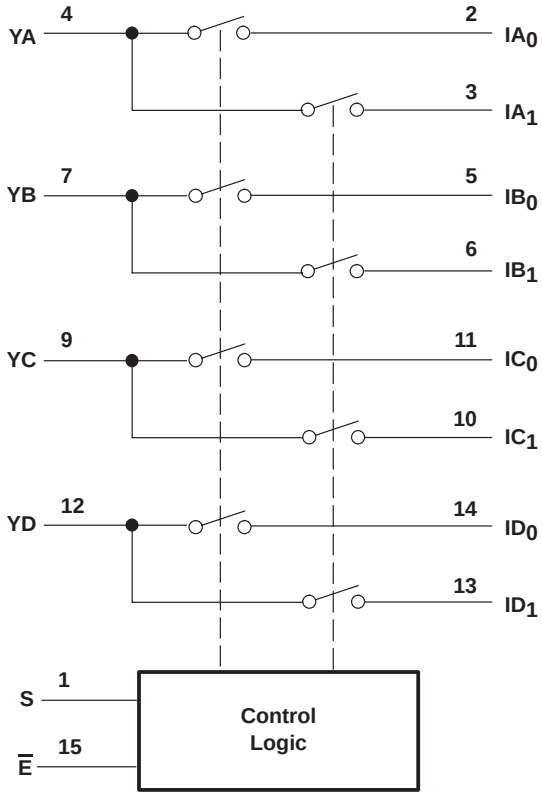
FUNCTION TABLE

INPUTS		INPUT/OUTPUT YX	FUNCTION
$\overline{E}$	S		
L	L	IX_0	$YX = IX_0$
L	H	IX_1	$YX = IX_1$
H	X	Z	Disconnect

PIN DESCRIPTIONS

PIN NAME	DESCRIPTION
IAn−IDn	Data I/Os
S	Select input
$\overline{E}$	Enable input
YA−YD	Data I/Os

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Control input voltage range, V_{IN} (see Notes 1 and 2) . . . . . −0.5 V to 7 V
Switch I/O voltage range, $V_{I/O}$ (see Notes 1, 2, and 3) . . . . . −0.5 V to 7 V
Control input clamp current, I_{IK} (V_{IN} < 0) . . . . . −50 mA
I/O port clamp current, $I_{I/OK}$ ($V_{I/O}$ < 0) . . . . . −50 mA
ON-state switch current, $I_{I/O}$ (see Note 4) . . . . . ±128 mA
Continuous current through V_{CC} or GND terminals . . . . . ±100 mA
Package thermal impedance, θ_{JA} (see Note 5): D package . . . . . 73°C/W
(see Note 5): DBQ package . . . . . 90°C/W
(see Note 5): PW package . . . . . 83°C/W
(see Note 6): RGY package . . . . . 39°C/W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages are with respect to ground, unless otherwise specified.
2. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. V_I and V_O are used to denote specific conditions for $V_{I/O}$.
4. I_I and I_O are used to denote specific conditions for $I_{I/O}$.
5. The package thermal impedance is calculated in accordance with JESD 51-7.
6. The package thermal impedance is calculated in accordance with JESD 51-5.

recommended operating conditions (see Note 7)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	6	6.5	V
V_{IH}	High-level control input voltage ($\overline{E}$, S)	2.5	6.5	V
V_{IL}	Low-level control input voltage ($\overline{E}$, S)	0	0.8	V
T_A	Operating free-air temperature	0	70	°C

NOTE 7: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range, V_{CC} = 6 V to 6.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	$\overline{E}$, S	V_{CC} = 6 V,	I_{IN} = −18 mA				−1.8	V
V_{hys}	$\overline{E}$, S					150		mV
V_O		V_I = 4.5 V,	$\overline{E}$ = low,	R_L = 100 Ω, see Figure 11	3.7	4.06		V
I_{IH}	$\overline{E}$, S	V_{CC} = 6.5 V,	V_{IN} = V_{CC}				±1	μA
I_{IL}	$\overline{E}$, S	V_{CC} = 6.5 V,	V_{IN} = GND				±1	μA
I_{OZ}‡		V_{CC} = 6.5 V,	V_O = 0 to 6.5 V, V_I = 0,	Switch OFF			±1	μA
I_{OS}§		V_{CC} = 6.5 V,	V_O = 0 to 0.5 V_{CC}, V_I = 0,	Switch ON	50			mA
I_{off}		V_{CC} = 0,	V_O = 0 to 6.5 V,	V_I = 0			1	μA
I_{CC}		V_{CC} = 6.5 V,	$I_{I/O}$ = 0,	Switch ON or OFF			3	μA
ΔI_{CC}	$\overline{E}$, S	V_{CC} = 6.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND			6	mA
I_{CCD}		V_{CC} = 6.5 V,	I and Y ports open,	V_{IN} input switching 50% duty cycle			0.35	mA/ MHz
C_{IN}	$\overline{E}$, S	f = 1 MHz				3.5		pF
C_{OFF}	I port	V_I = 0,	f = 1 MHz, Outputs open,	Switch OFF		4.5		pF
	Y port					6.5		
C_{ON}		V_I = 0,	f = 1 MHz, Outputs open,	Switch ON		14		pF
r_{on}	M1	V_I = 4.5 V,	Switch ON,	R_L = 100 Ω, see Figure 11	7.5	11.2	19	Ω
	M2				2	3	6	
Δr_{on}		V_I = 4.5 V,	Switch ON			1	2	Ω

V_I, V_O, I_I, and I_O refer to I/O pins. V_{IN} refers to the control inputs.
† All typical values are at V_{CC} = 6.2 V (unless otherwise noted), T_A = 25°C.
‡ For I/O ports, I_{OZ} includes the input leakage current.
§ The I_{OS} test is applicable to only one ON channel at a time. The duration of this test is less than one second.

switching characteristics over recommended operating free-air temperature range, V_{CC} = 6 V to 6.5 V, R_L = 100 Ω, C_L = 35 pF (unless otherwise noted) (see Figure 7)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{ON}	S	Y		7	ns
t_{OFF}	S	Y		4	ns

† All typical values are at V_{CC} = 6.2 V (unless otherwise noted), T_A = 25°C.

dynamic characteristics over recommended operating free-air temperature range, V_{CC} = 6 V to 6.5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
X_{TALK}(Diff)	R_L = 100 Ω,	f = 10 MHz, see Figure 12,	t_r = t_f = 2 ns	−40	−60		dB
X_{TALK}	R_L = 100 Ω,	f = 30 MHz, see Figure 9			−50		dB
O_{IRR}	R_L = 100 Ω,	f = 30 MHz, see Figure 10			−40		dB
BW	R_L = 100 Ω, see Figure 8				350		MHz

† All typical values are at V_{CC} = 6.2 V (unless otherwise noted), T_A = 25°C.

OPERATING CHARACTERISTICS

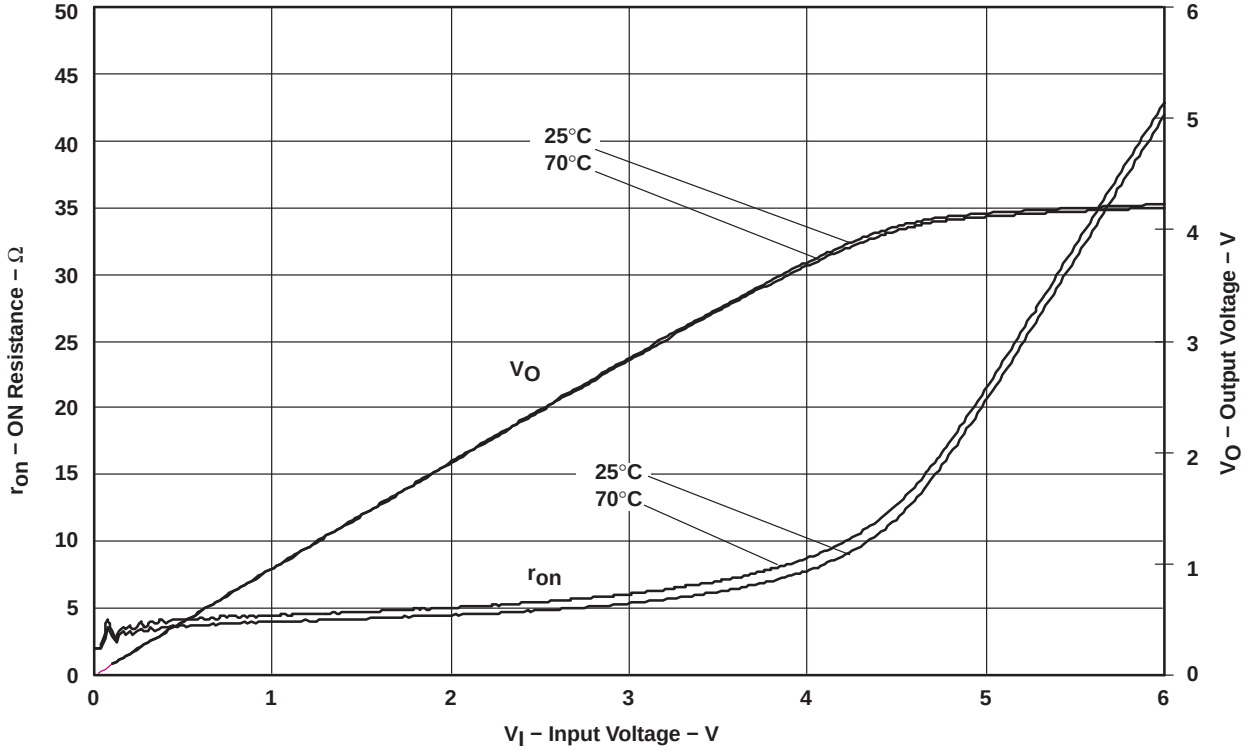


Figure 1. r_{on} and V_O vs V_I Over Temperature (V_{CC} = 6 V)

OPERATING CHARACTERISTICS

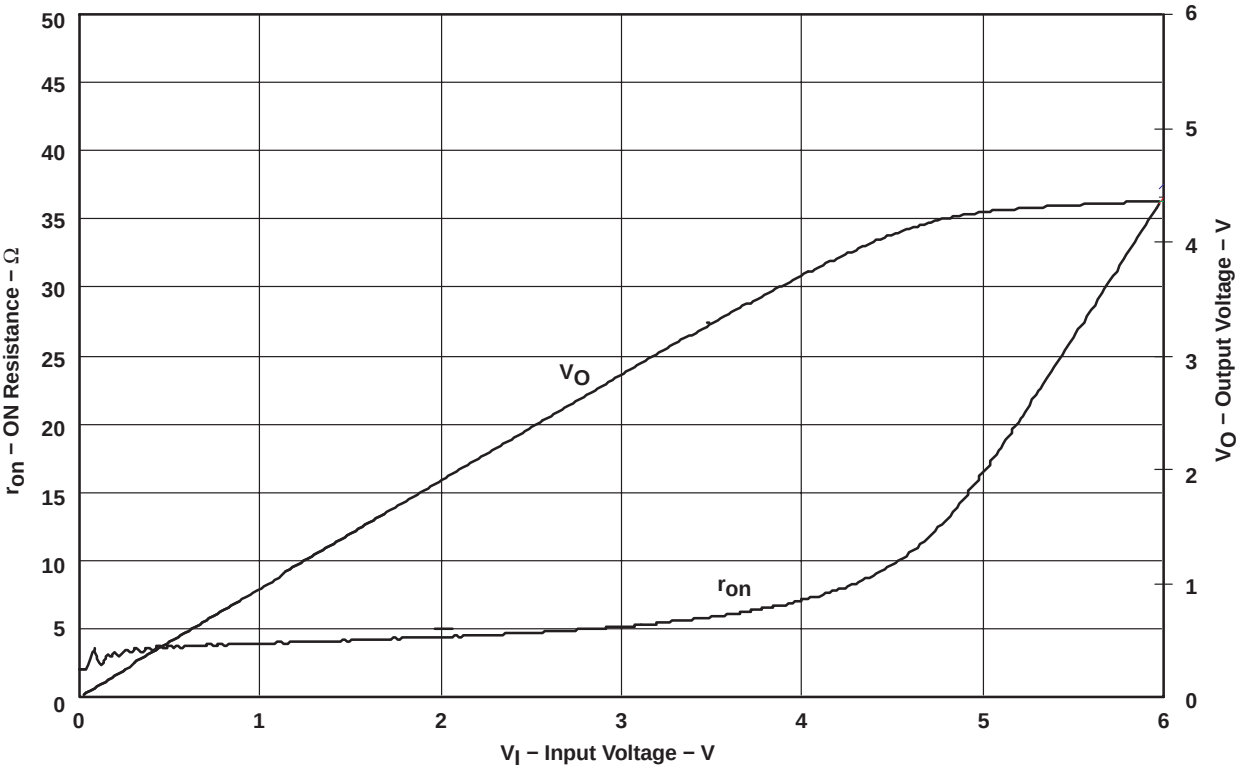
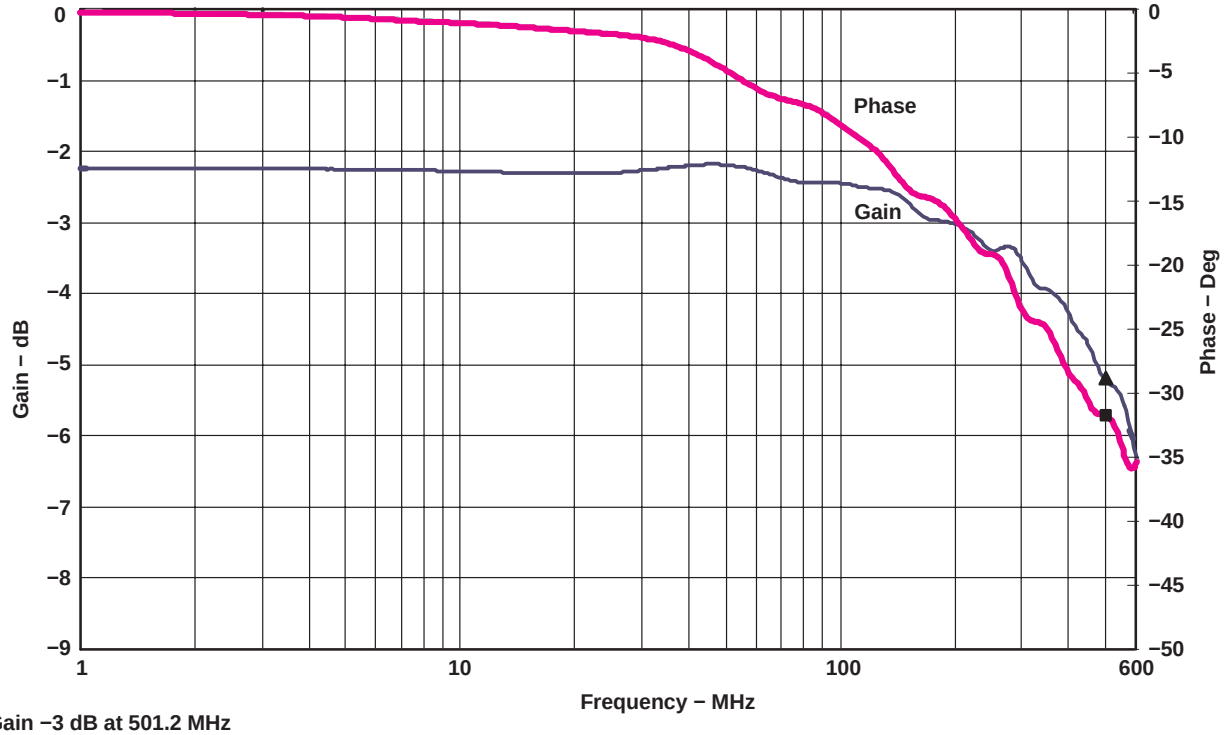


Figure 2. r_{on} and V_O vs V_I (V_{CC} = 6.2 V and T_A = 25°C)

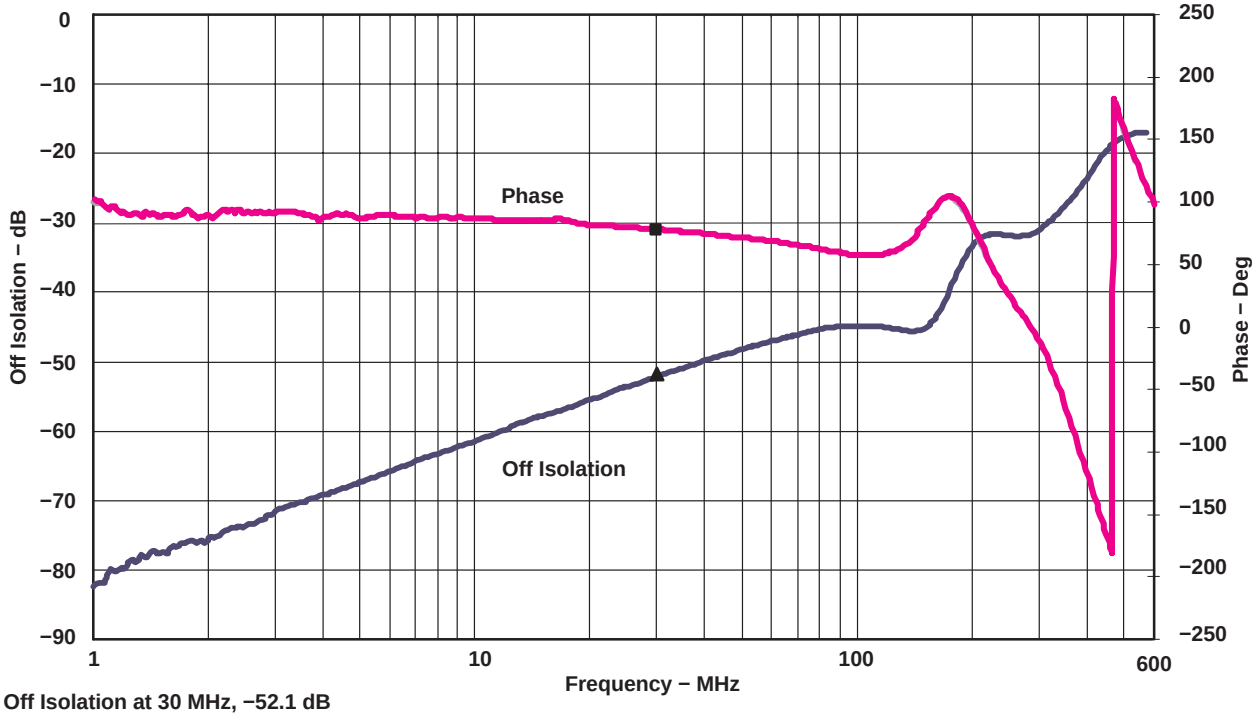
OPERATING CHARACTERISTICS



▲ Gain −3 dB at 501.2 MHz
■ Phase at −3-dB Frequency, −31.7 Degrees

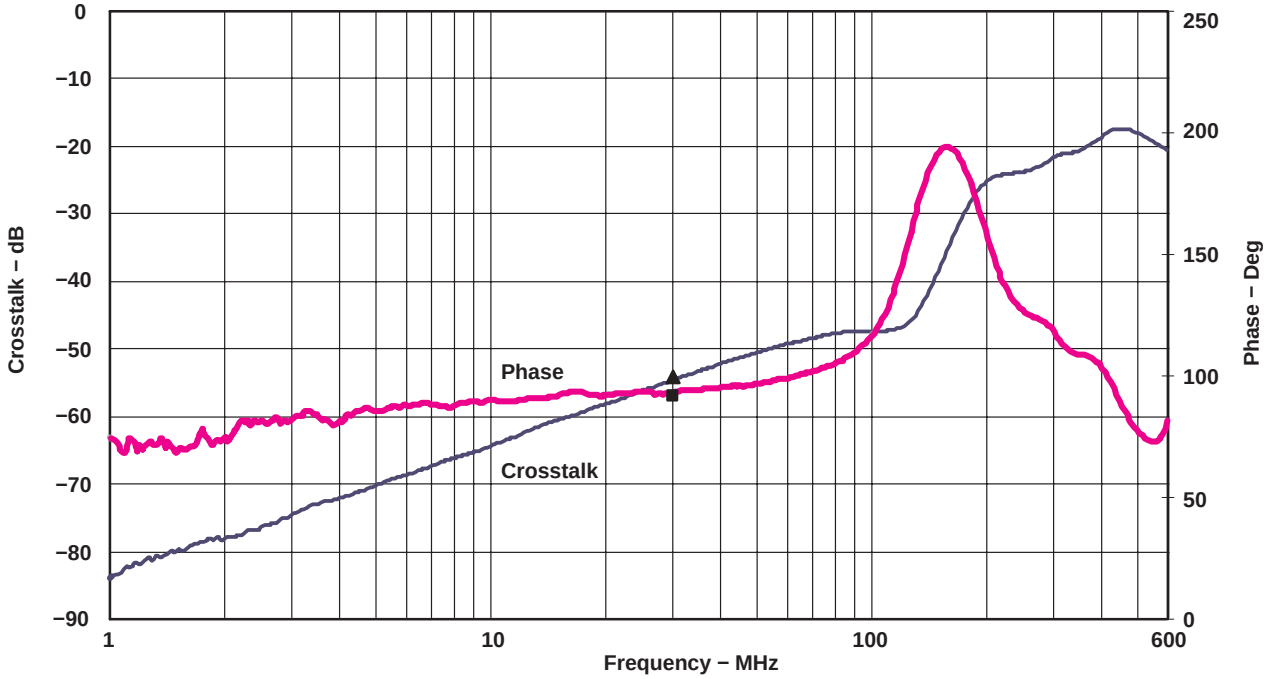
Figure 3. Gain/Phase vs Frequency

OPERATING CHARACTERISTICS



▲ Off Isolation at 30 MHz, −52.1 dB
■ Phase at 30 MHz, 77 Degrees

Figure 4. Off Isolation vs Frequency



▲ Crosstalk at 30 MHz, −54 dB
■ Phase at 30 MHz, 93.2 Degrees

Figure 5. Crosstalk vs Frequency

OPERATING CHARACTERISTICS

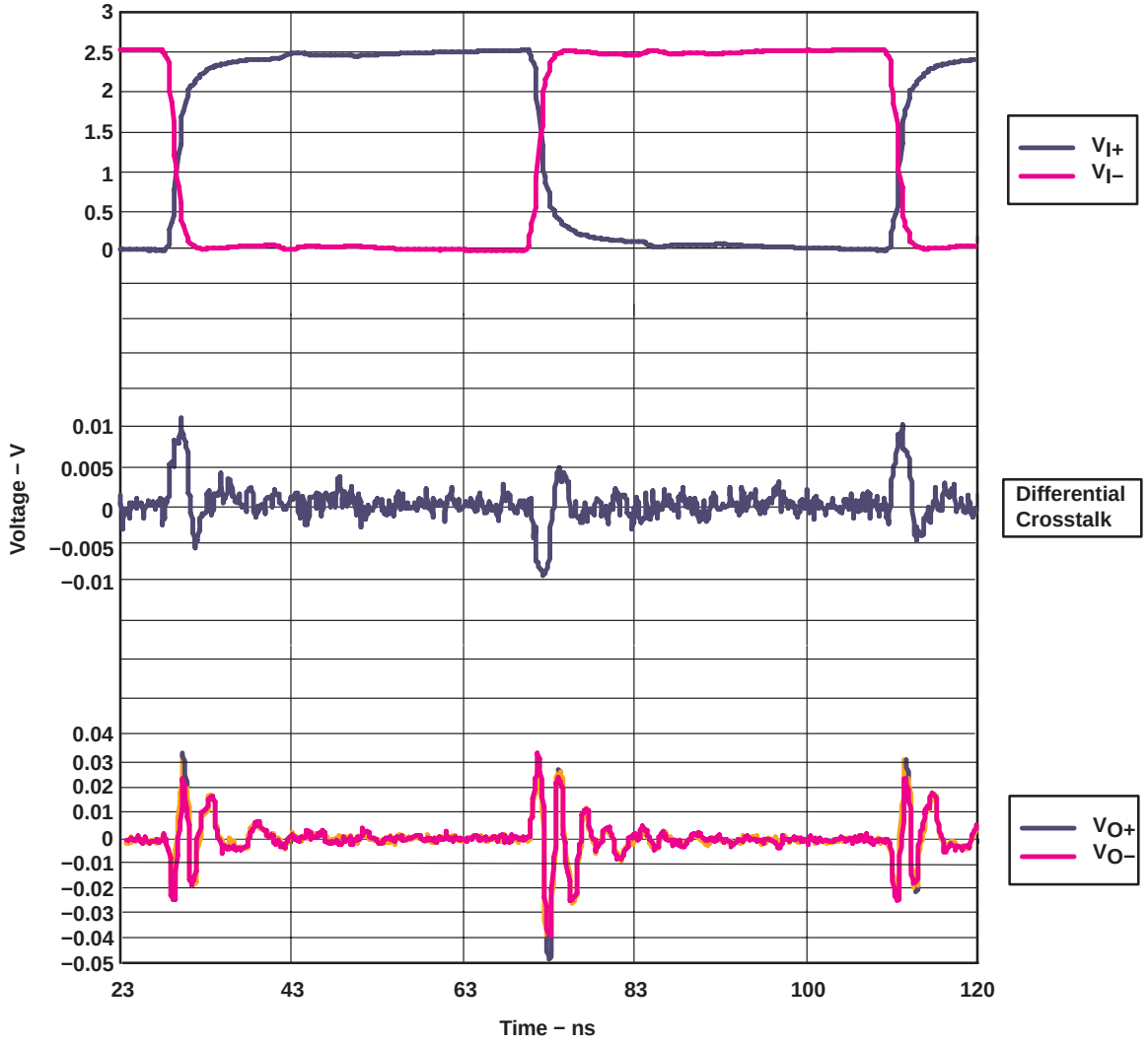
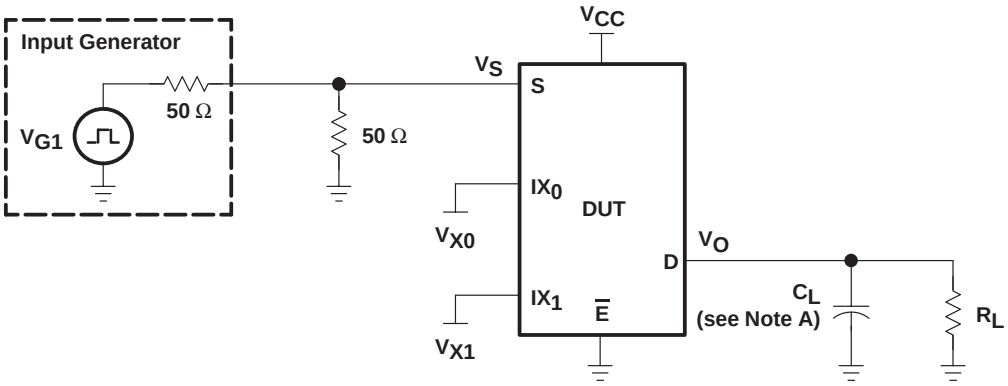
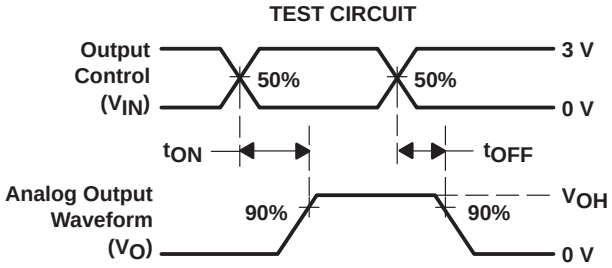


Figure 6. Differential Crosstalk

PARAMETER MEASUREMENT INFORMATION



TEST	V_{CC}	R_L	C_L	V_{X0}	V_{X1}
t_{ON}	6.2 V	100 Ω	35 pF	GND	4.5 V
	6.2 V	100 Ω	35 pF	4.5 V	GND
t_{OFF}	6.2 V	100 Ω	35 pF	GND	4.5 V
	6.2 V	100 Ω	35 pF	4.5 V	GND



NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
C. The outputs are measured one at a time, with one transition per measurement.

Figure 7. Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

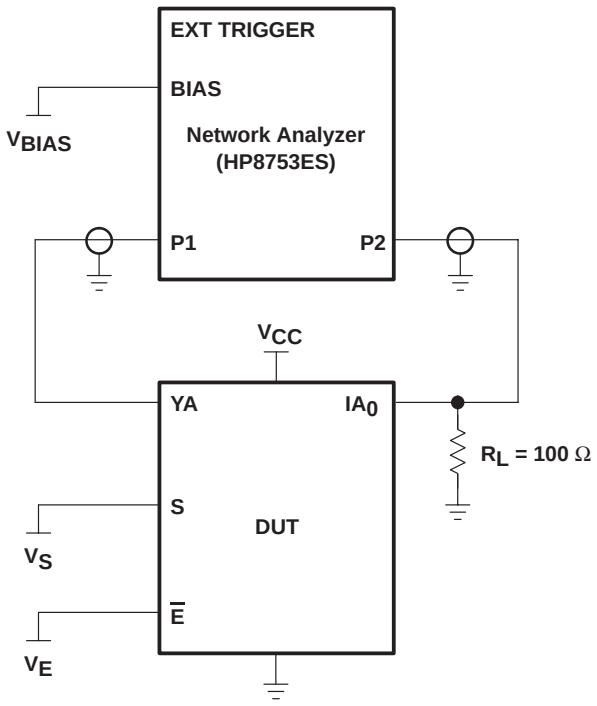


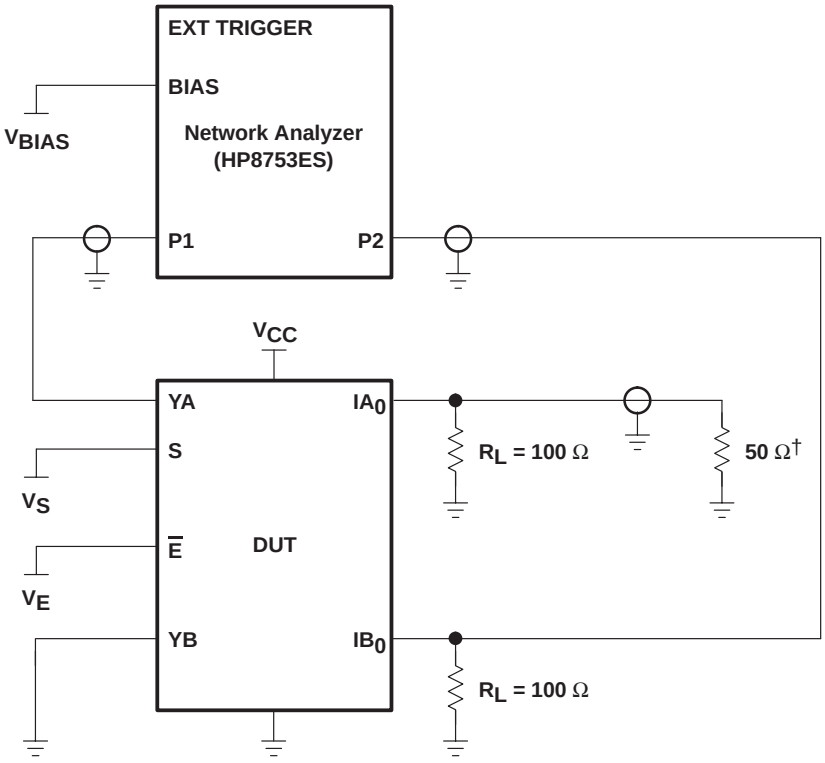
Figure 8. Test Circuit for Frequency Response (BW)

Frequency response is measured at the output of the ON channel. For example, when V_S = 0, V_E = 0, and YA is the input, the output is measured at IA_0. All unused analog I/O ports are left open.

HP8753ES setup

Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBM

PARAMETER MEASUREMENT INFORMATION



† A 50-Ω termination resistor is needed for the network analyzer.

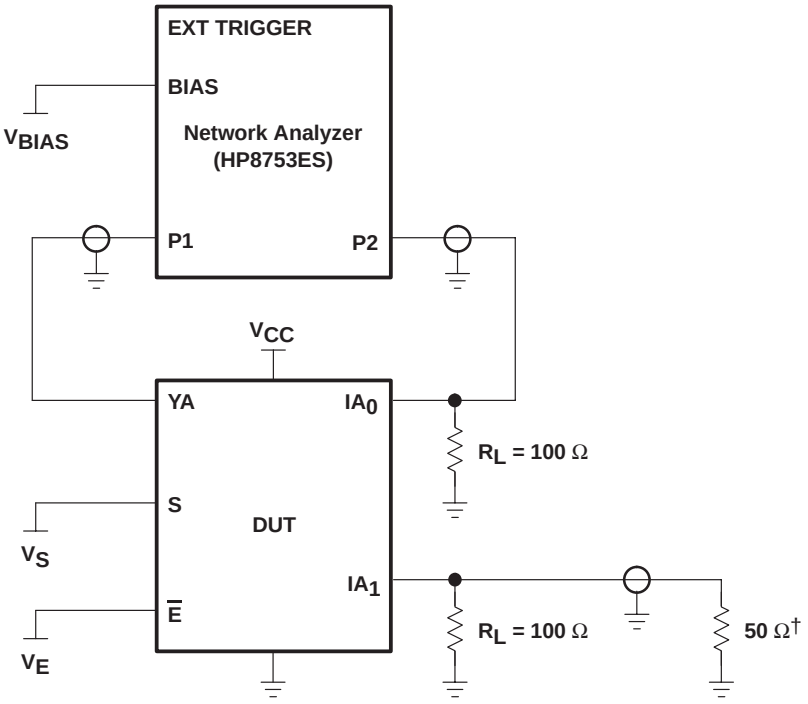
Figure 9. Test Circuit for Crosstalk (X_{TALK})

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when V_S = 0, V_E = 0, and YA is the input, the output is measured at IB_0. All unused analog input (Y) ports are connected to GND, and output (A) ports are connected to GND through 50-Ω pulldown resistors.

HP8753ES setup

Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBM

PARAMETER MEASUREMENT INFORMATION



† A 50-Ω termination resistor is needed for the network analyzer.

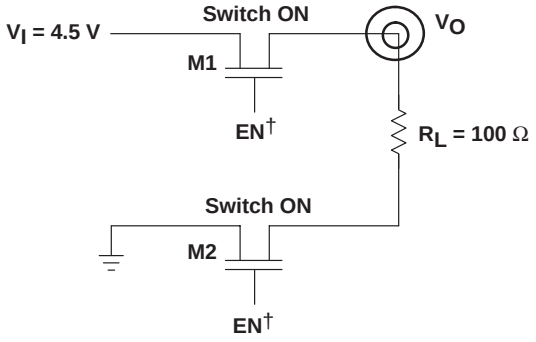
Figure 10. Test Circuit for Off Isolation (O_{IRR})

Off isolation is measured at the output of the OFF channel. For example, when $V_S = V_{CC}$, $V_E = 0$, and YA is the input, the output is measured at IA_0. All unused analog input (Y) ports are left open, and output (A) ports are connected to GND through 50-Ω pulldown resistors.

HP8753ES setup

Average = 4
RBW = 3 kHz
V_{BIAS} = 0.35 V
ST = 2 s
P1 = 0 dBM

PARAMETER MEASUREMENT INFORMATION



† EN is the internal enable signal applied to the switch.
NOTE A: r_{on} (M1) and r_{on} (M2) are calculated from the voltage drop and current across the two terminals of M1 and M2, respectively.

Figure 11. Test Circuit for V_O and r_{on}

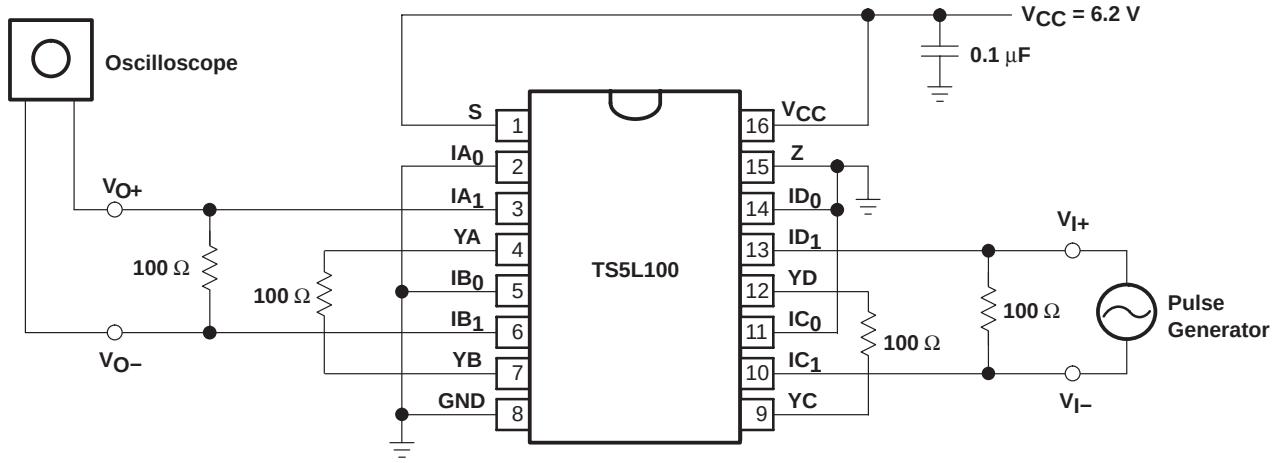


Figure 12. Differential Crosstalk Measurement

Differential crosstalk is a measure of coupling noise between a transmit and receive pair in the LAN application. Differential crosstalk depends on the edge rate, frequency, and load. This is calculated from the equation, X_{TALK}(Diff) db = 20 log V_O(Diff)/V_I(Diff), where V_O(Diff) is the differential output voltage and V_I(Diff) is the differential input voltage.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TS5L100D	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TS5L100	Samples
TS5L100DBQR	ACTIVE	SSOP	DBQ	16	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	TG100	Samples
TS5L100DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TS5L100	Samples
TS5L100PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TG100	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

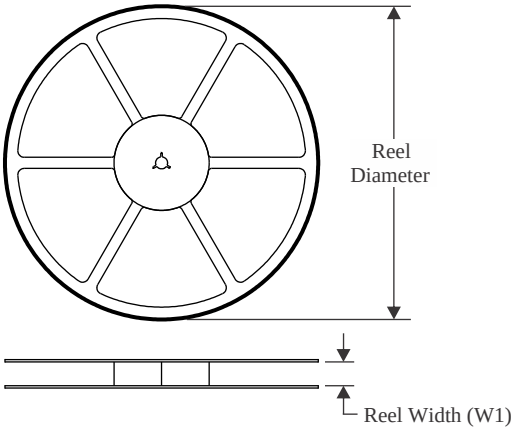
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

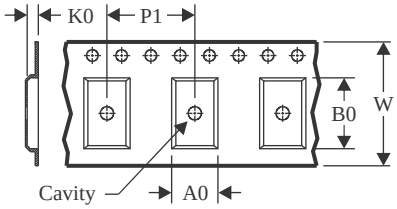
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

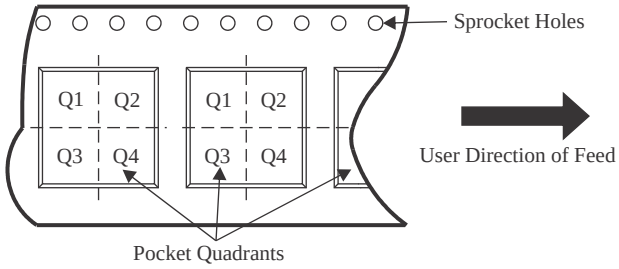


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

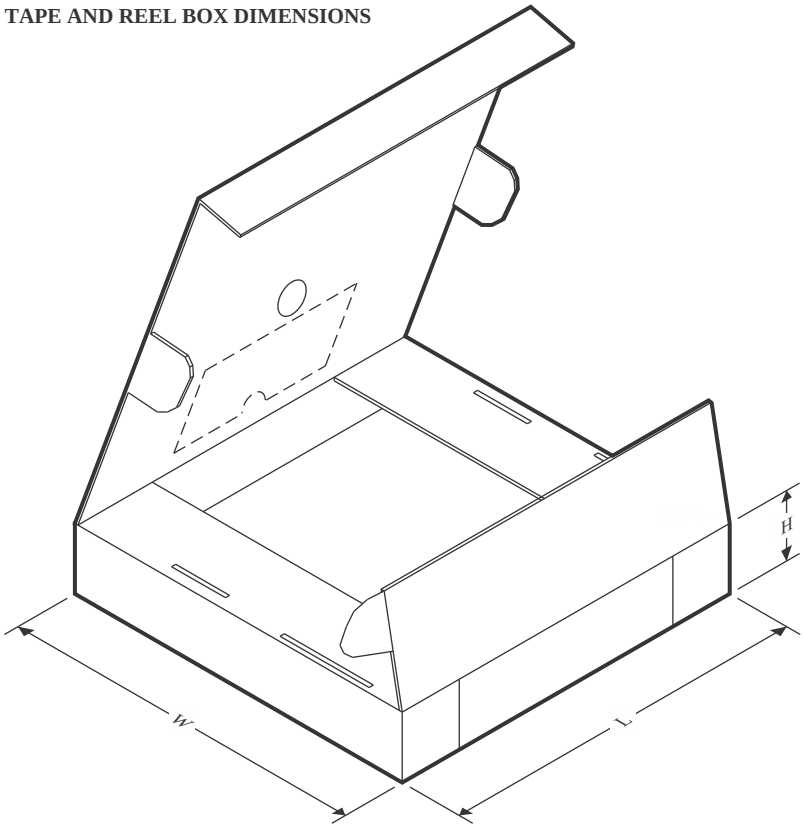
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS5L100DBQR	SSOP	DBQ	16	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
TS5L100DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TS5L100PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

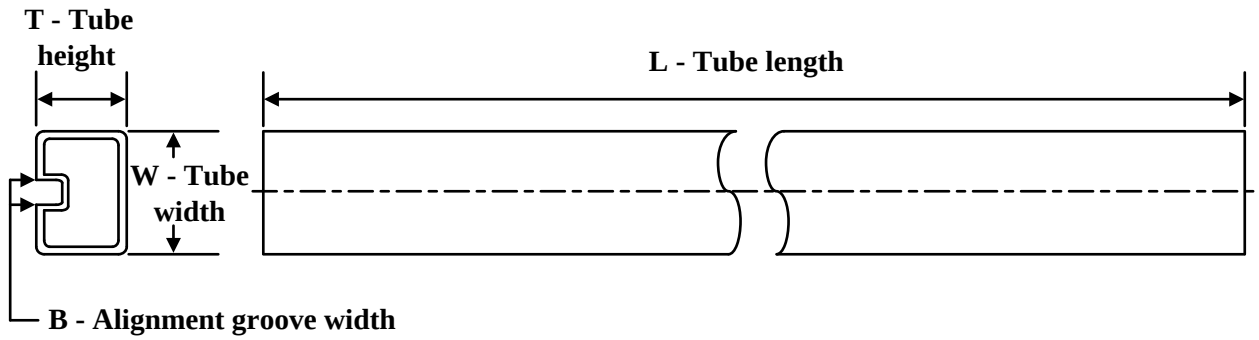
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

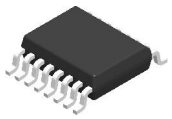
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TS5L100DBQR	SSOP	DBQ	16	2500	340.5	338.1	20.6
TS5L100DR	SOIC	D	16	2500	340.5	336.1	32.0
TS5L100PWR	TSSOP	PW	20	2000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TS5L100D	D	SOIC	16	40	507	8	3940	4.32

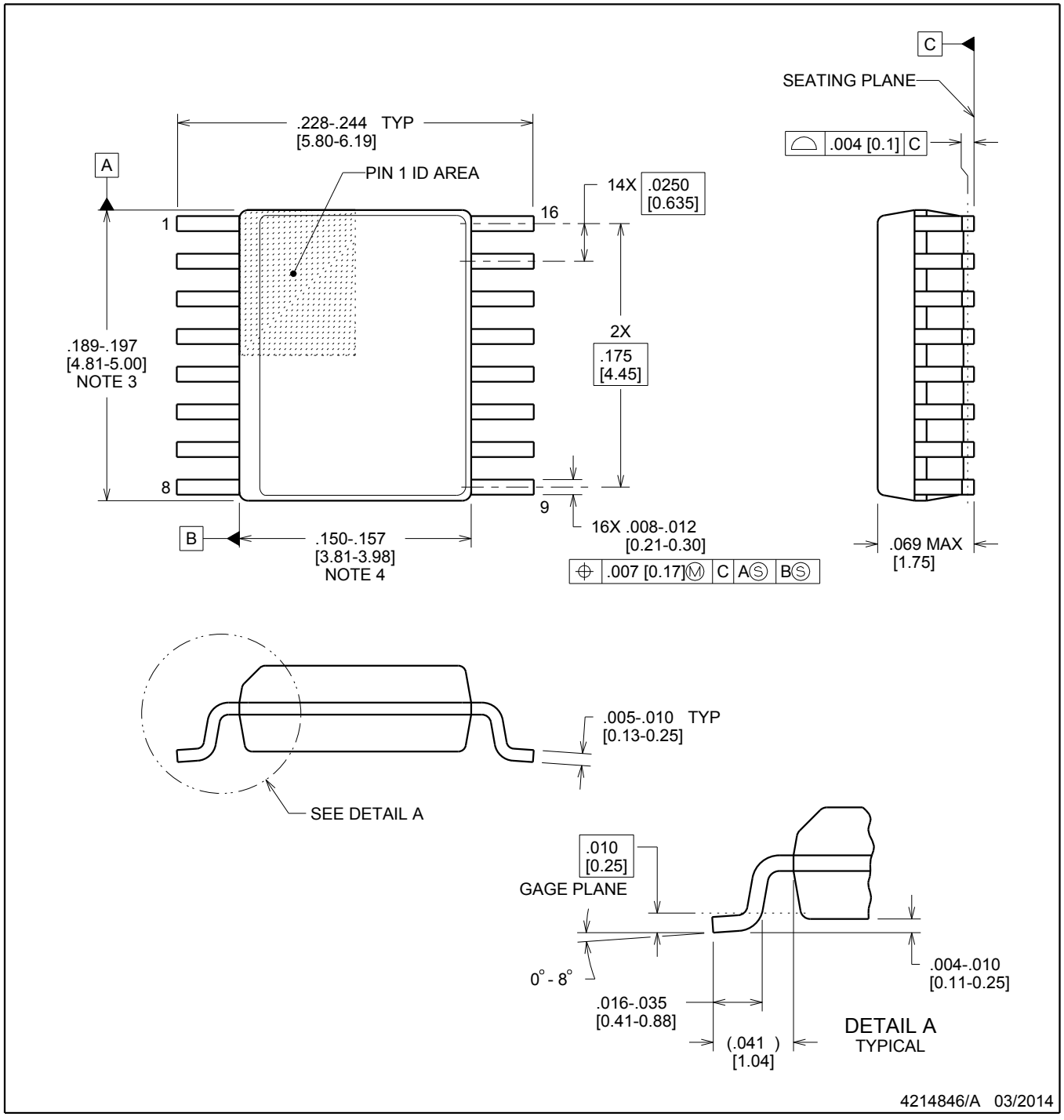


PACKAGE OUTLINE

DBQ0016A

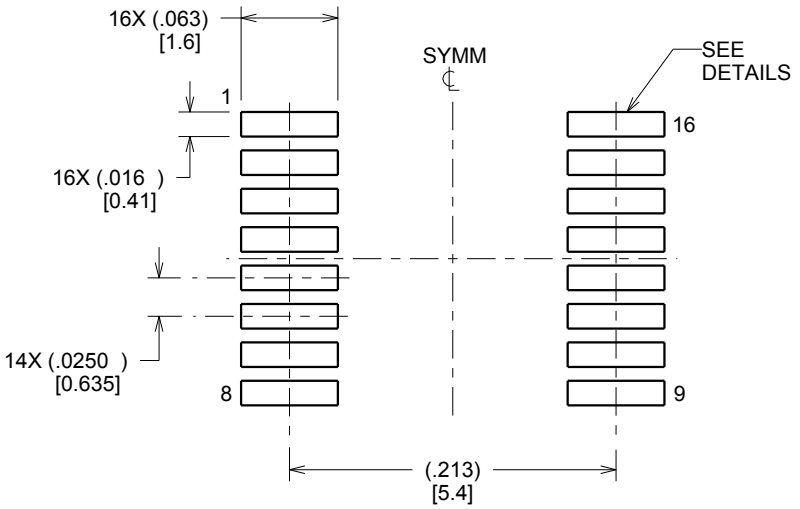
SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE

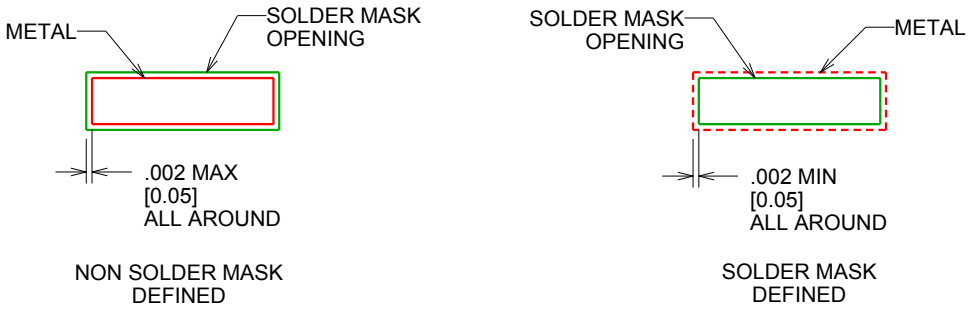


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 inch, per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MO-137, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4214846/A 03/2014

NOTES: (continued)

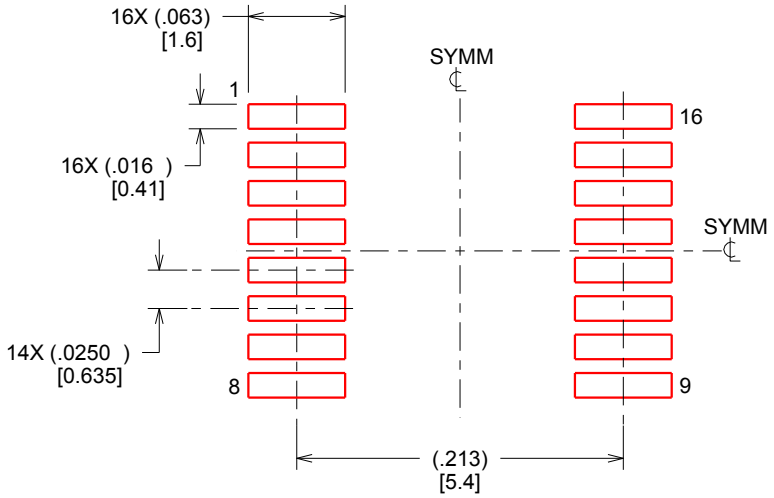
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBQ0016A

SSOP - 1.75 mm max height

SHRINK SMALL-OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.127 MM] THICK STENCIL
SCALE:8X

4214846/A 03/2014

NOTES: (continued)

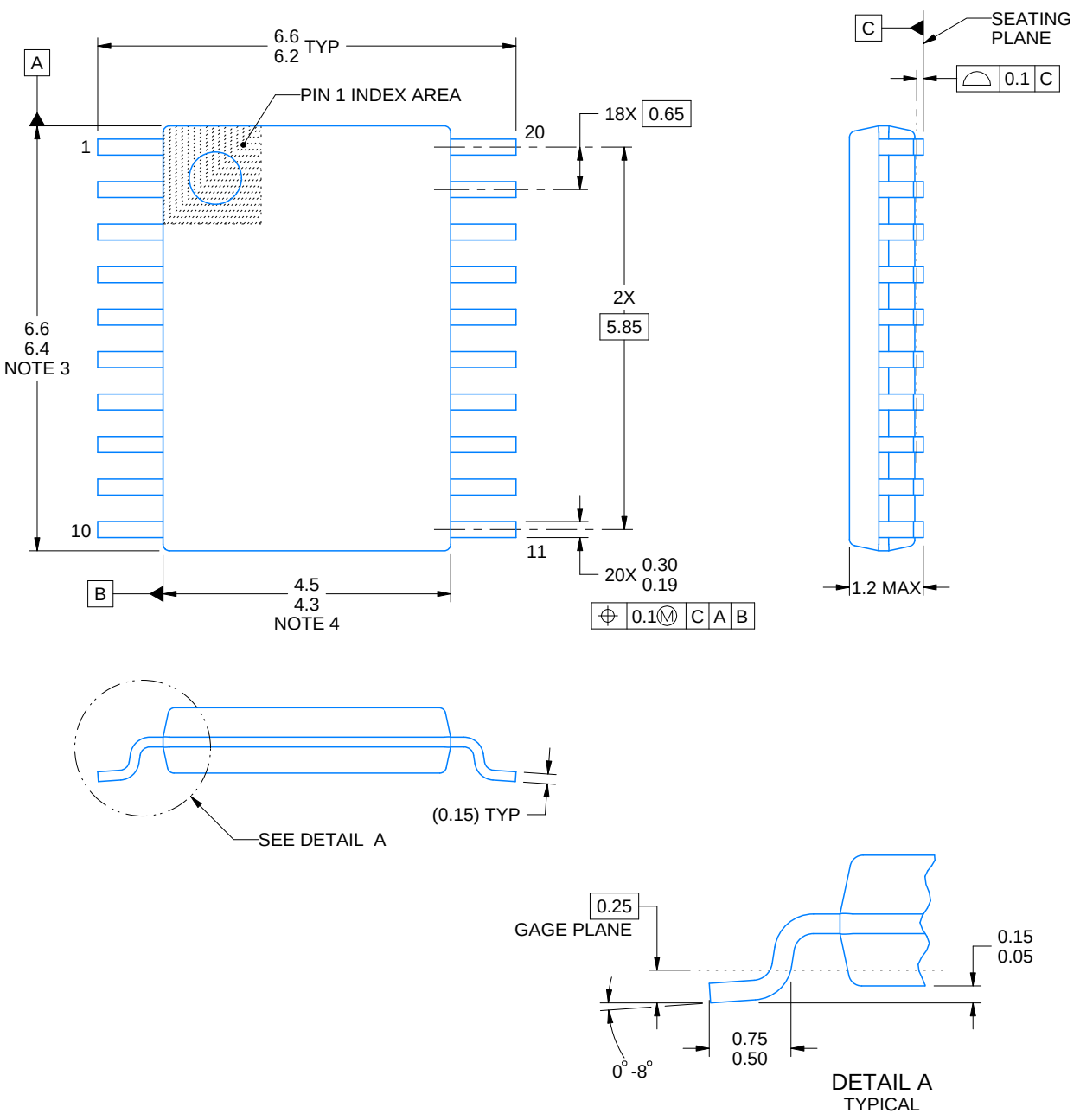
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

PW0020A

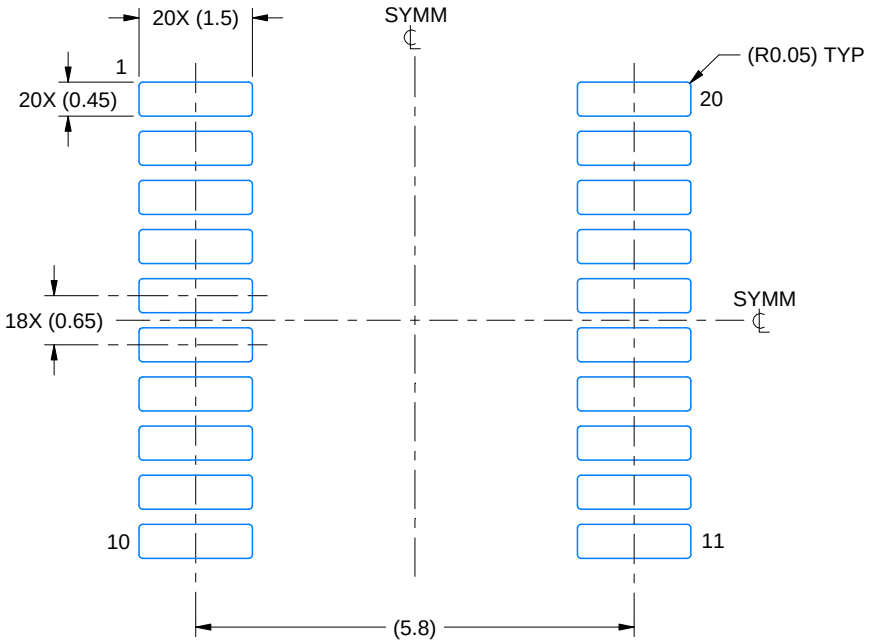
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



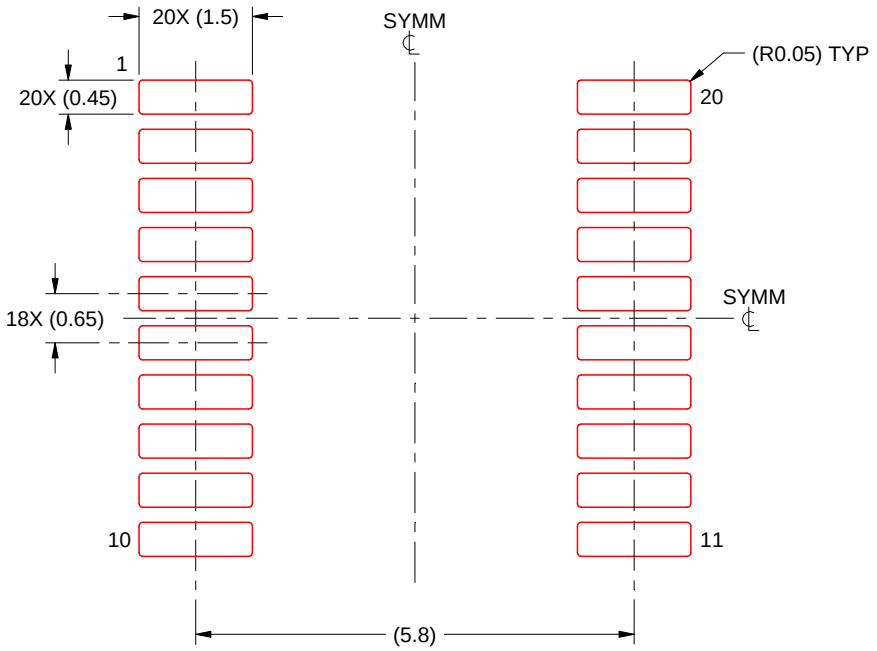
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



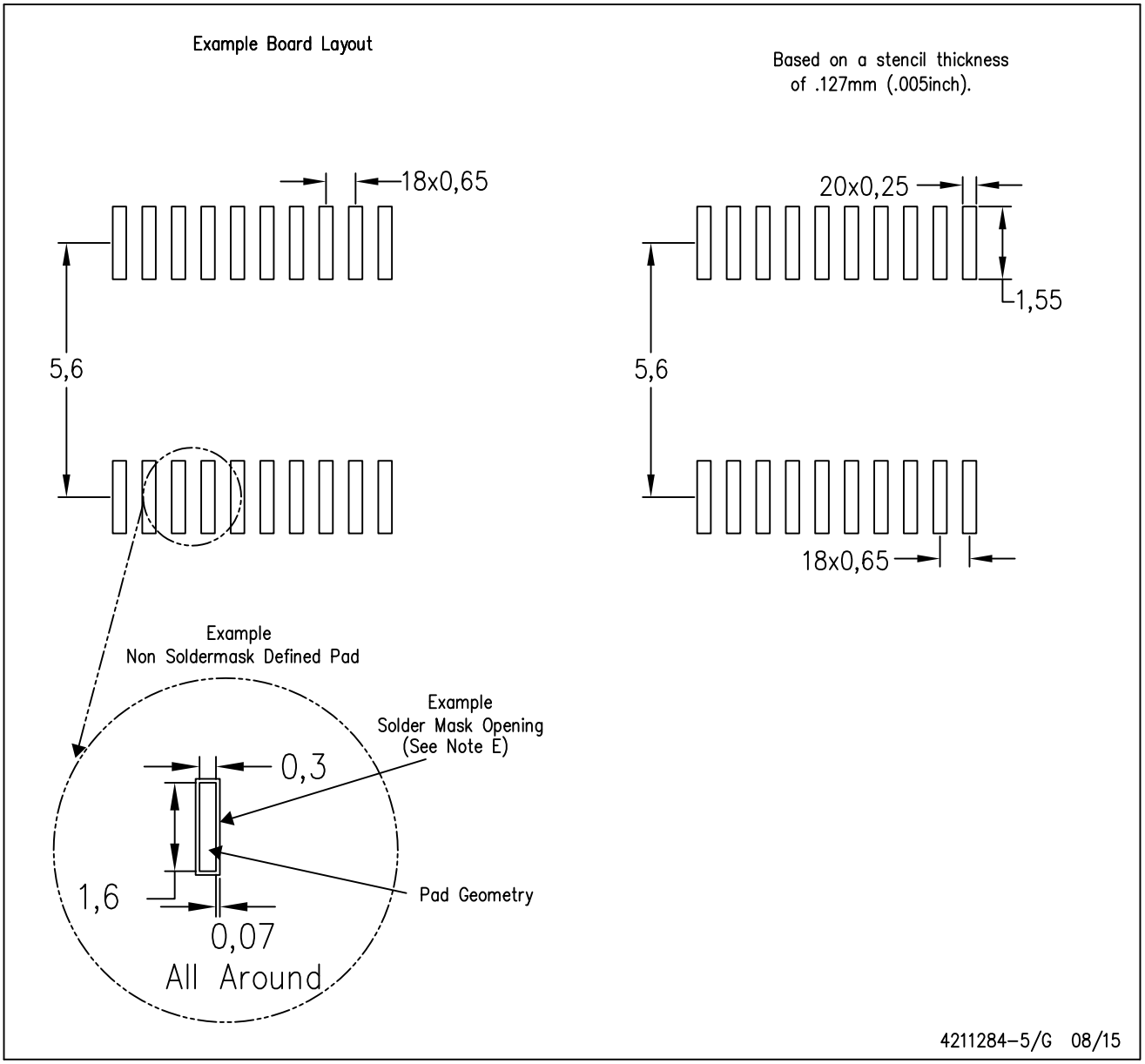
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

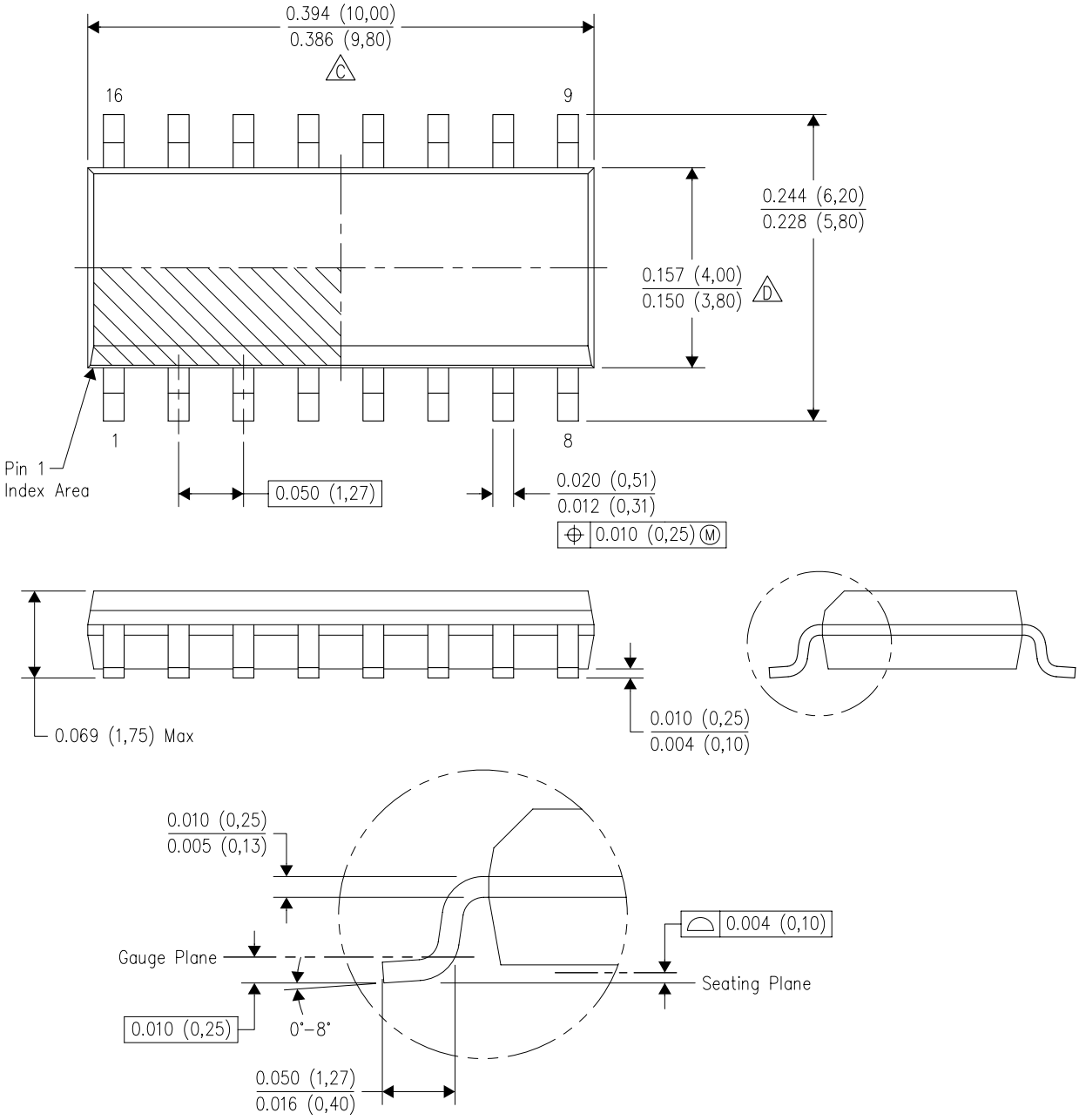
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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