Natural Interleaving™ 具有改进可闻噪声抗扰的转换模式功率因数校正 (PFC) 控制器

查询样品: UCC28061-Q1

特性

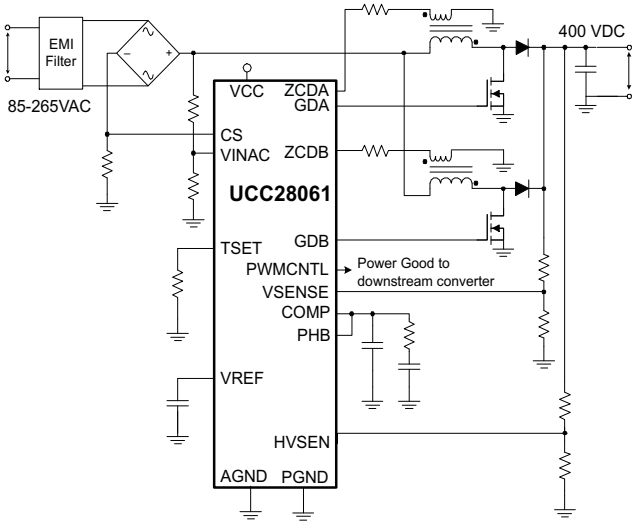
- 符合汽车应用要求
- 符合 **AEC-Q100** 标准的下列结果
  - 器件温度 **1** 级：**-40**℃ 至 **+125**℃ 的环境运行温度范围
  - 器件人体模型 **(HBM)** 静电放电 **(ESD)** 分类等级 **H2**
  - 器件充电器件模型 **(CDM) ESD** 分类等级 **C3B**
- 简便相位管理使得符合轻负载高效标准变得更加容易
- 双路故障安全过压保护 **(OVP)** 防止由电压感测故障引起的输出过压情况
- 无传感器电流整形简化了电路板设计并提升了效率
- 涌入安全电流限制：
  - 涌入期间防止金属氧化物半导体场效应晶体管 **(MOSFET)** 传导
  - 消除了输出整流器内的反向恢复事件

系统特性

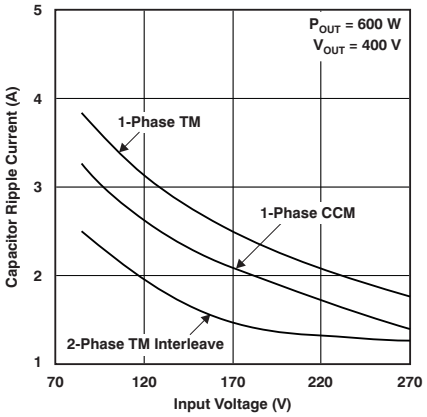
- 改进的可闻噪声性能
- 过压上的软启动
- 集成欠压保护
- 在传统、单相位持续传导模式 **(CCM)** 上提升的效率和设计灵活性
- 输入滤波器和输出电容器电流撤销：
  - 为了实现更高系统可靠性和更小大容量电容器而减少的电流纹波
  - 缩小的电磁干扰 **(EMI)** 滤波器尺寸
- 在无需扩展缓冲器电路的情况下可使用低成本二极管
- 改进的轻负载效率
- 改进的瞬态响应
- 完整的系统级保护
- **1A** 源电流 **/ 1.8A** 吸收电流栅极驱动器

应用范围

- **100W** 至 **800W** 电源
- 电动自行车
- 车载应用



典型应用电路



纹波电流衰减

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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内容

说明

针对对可闻噪声消除有要求的消费类应用，这个解决方案将转换模式的优势--使用低成本组件实现高效率--扩展至比之前的可能值更高的额定功率值。 通过使用一个 Natural Interleaving 技术，两个作为主信道运行的信道（也就是说，没有从信道）与同一频率同步。 这个方法从内部产生了强匹配、更快速的响应、并确保每个信道都运行在转换模式。

完整的系统级保护特有输入欠压保护、输出过压保护、开环路保护、过载保护、软启动、相位故障检测、和热关断功能。 附加的故障安全过压保护 (OVP) 特性防止到一个中间电压的短路，如果没有检测到此短路的话，有可能导致非常严重的器件故障。

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Table 1. ORDERING INFORMATION(1)

PART NUMBER	Package Marking	PACKAGE(2)	OPERATING TEMPERATURE RANGE, T_A
UCC28061QDRQ1	28061Q1	SOIC 16-Pin (D)	–40°C to +125°C

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) SOIC (D) package is available taped and reeled by adding ***R*** to the above part number. Reeled quantities for UCC28061-Q1DR are 2500 devices per reel.

ABSOLUTE MAXIMUM RATINGS(1)

All voltages are with respect to GND, –40°C < T_J = T_A < +125°C, and currents are positive into and negative out of the specified terminal, unless otherwise noted.

		UCC28061-Q1	UNIT
Input voltage range	VCC(2)	–0.5 to +21	V
	PWMCNTL	–0.5 to +20	
	COMP(3), CS, PHB, HVSEN(4), VINAC(4), VSENSE(4)	–0.5 to +7	
	ZCDA, ZCDB	–0.5 to +4	
Continuous input current	VCC	20	mA
Input current	PWMCNTL	10	
Input current range	ZCDA, ZCDB, VSENSE	–5 to +5	
Output current	VREF	–10	
Continuous gate current	GDA, GDB(5)	±25	
Junction temperature, T_J	Operating	–40 to +125	°C
	Storage	–65 to +150	
Lead temperature, T_{SOL}	Soldering, 10s	+260	
Electrostatic discharge (ESD) protection	Human body model (HBM) AEC-Q100 Classification Level H2	2000	V
	Charged device model (CDM) AEC-Q100 Classification Level C3B	750	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those included under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods of time may affect device reliability.
(2) Voltage on VCC is internally clamped. VCC may exceed the absolute maximum input voltage if the source is current limited below the absolute maximum continuous VCC input current level.
(3) In normal use, COMP is connected to capacitors and resistors and is internally limited in voltage swing.
(4) In normal use, VINAC, VSENSE, and HVSEN are connected to resistors and are internally limited in voltage swing. Although not recommended for extended use, VINAC, VSENSE, and HVSEN can survive input currents as high as ±10 mA from high voltage sources.
(5) No GDA or GDB current limiting is required when driving a power MOSFET gate. However, a small series resistor may be required to damp ringing due to stray inductance. See Figure 12 and Figure 13 for details.

THERMAL INFORMATION

THERMAL METRIC(1)		UCC28061-Q1 D (16 PIN)	UNITS
θ_{JA}	Junction-to-ambient thermal resistance	91.6	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	52.1	
θ_{JB}	Junction-to-board thermal resistance	48.6	
ψ_{JT}	Junction-to-top characterization parameter	14.9	
ψ_{JB}	Junction-to-board characterization parameter	48.3	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	

(1) 有关传统和新的热度量的更多信息，请参阅 *IC 封装热度量* 应用报告 SPRA953。

RECOMMENDED OPERATING CONDITIONS

All voltages are with respect to GND, –40°C < T_J = T_A < +125°C, and currents are positive into and negative out of the specified terminal, unless otherwise noted.

	MIN	MAX	UNIT
VCC input voltage from a low-impedance source	14	21	V
VCC input current from a high-impedance source	8	18	mA
VREF load current	0	–2	
VINAC Input voltage	0	6	V
ZCDA, ZCDB series resistor	20	80	kΩ
TSET resistor to program PWM on-time	66.5	400	

RECOMMENDED OPERATING CONDITIONS (continued)

All voltages are with respect to GND, –40°C < T_J = T_A < +125°C, and currents are positive into and negative out of the specified terminal, unless otherwise noted.

	MIN	MAX	UNIT
HVSEN input voltage	0.8	4.5	V
PWMCNTL pull-up resistor to VREF	1	10	kΩ

ELECTRICAL CHARACTERISTICS

At VCC = 16 V, AGND = PGND = 0 V, VINAC = 3 V, VSENSE = 6 V, HVSEN = 3 V, PHB = 5 V, R_{TSET} = 133 kΩ; all voltages are with respect to GND, all outputs unloaded, –40°C < T_J = T_A < +125°C, and currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCC BIAS SUPPLY						
$VCC_{(shunt)}$	VCC shunt voltage (1)	I_{VCC} = 10 mA	22	24	26	V
$I_{VCC(stby)}$	VCC current, disabled	VSENSE = 0 V		100	200	µA
$I_{VCC(on)}$	VCC current, enabled	VSENSE = 6 V		5	8	mA
UNDERVOLTAGE LOCKOUT (UVLO)						
$VCC_{(on)}$	VCC turn-on threshold		11.5	12.6	13.5	V
$VCC_{(off)}$	VCC turn-off threshold		9.5	10.35	11.5	
	UVLO Hysteresis		1.85	2.25	2.65	
REFERENCE						
V_{REF}	VREF output voltage, no load	I_{VREF} = 0 mA	5.82	6.00	6.18	V
	VREF change with load	0 mA ≤ I_{VREF} ≤ –2 mA		1	6	mV
	VREF change with VCC	12 V ≤ VCC ≤ 20 V		1	10	
ERROR AMPLIFIER						
	VSENSE input regulation voltage	T_A = +25°C	5.85	6.00	6.15	V
	VSENSE input regulation voltage		5.82	6.00	6.18	
	VSENSE input bias current	In regulation	125	300	800	nA
	COMP high voltage, clamped	VSENSE = 5.8 V	4.70	4.95	5.10	V
	COMP low voltage, saturated	VSENSE = 6.2 V		0.03	0.125	
g_m	VSENSE to COMP transconductance	COMP = 3 V, 5.94 V < VSENSE < 6.06 V	75	96	110	µS
	COMP source current, overdriven	VSENSE = 5 V, COMP = 3 V	–120	–160	–190	µA
	COMP sink current	VSENSE = 6.2 V, COMP = 3 V	7	20	32	
	VSENSE threshold for COMP offset enable, down from V_{REF}	Voltage below V_{REF}	135	185	235	mV
V_{OVP}	VSENSE over-voltage threshold, rising		6.25	6.45	6.7	V
	VSENSE over-voltage hysteresis		0.1	0.2	0.4	
	VSENSE enable threshold, rising		1.15	1.25	1.35	
	VSENSE enable hysteresis		0.02	0.05	0.2	
OUTPUT MONITORING						
$V_{PWMCNTL}$	HVSEN threshold to PWMCNTL	HVSEN rising	2.35	2.50	2.65	V
	HVSEN input bias current, high	HVSEN = 3 V	–0.5		0.5	µA
	HVSEN input bias current, low	HVSEN = 2 V	28	36	41	
	HVSEN rising threshold to over-voltage fault		4.64	4.87	5.1	V
	HVSEN falling threshold to over-voltage fault		4.45	4.67	4.80	
	Phase Fail filter time to PWMCNTL high	PHB = 5 V, ZCDA switching, ZCDB = 0.5 V	8	12	20	ms
	PWMCNTL leakage current high	HVSEN = 2 V, PWMCNTL = 15 V	–1		1	µA
	PWMCNTL output voltage low	HVSENS = 3 V, IPWMCNTL = 5 mA		0.2	0.5	V

(1) Excessive VCC input voltage and current will damage the device. This clamp does not protect the device from an unregulated supply. If an unregulated supply is used, a Fixed Positive Voltage Regulator such as the UA78L15A is recommended. See the Absolute Maximum Ratings table for the limits on VCC voltage and current.

ELECTRICAL CHARACTERISTICS (continued)

At VCC = 16 V, AGND = PGND = 0 V, VINAC = 3 V, VSENSE = 6 V, HVSEN = 3 V, PHB = 5 V, R_{TSET} = 133 kΩ; all voltages are with respect to GND, all outputs unloaded, –40°C < T_J = T_A < +125°C, and currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GATE DRIVE(2)						
	GDA, GDB output voltage high	I_{GDA}, I_{GDB} = –100 mA	11.5	13	15	V
	GDA, GDB output voltage high, clamped	VCC = 20 V, I_{GDA}, I_{GDB} = –5 mA	12	13.5	15	
	GDA, GDB output voltage high, low VCC	VCC = 12 V, I_{GDA}, I_{GDB} = –5 mA	10	10.5	11.5	
	GDA, GDB on-resistance high	I_{GDA}, I_{GDB} = –100 mA		8	14	Ω
	GDA, GDB output voltage low	I_{GDA}, I_{GDB} = 100 mA		0.15	0.3	V
	GDA, GDB on-resistance low	I_{GDA}, I_{GDB} = 100 mA		2	3	Ω
	Rise time	1 V to 9 V, C_{LOAD} = 1 nF		18	30	ns
	Fall time	9 V to 1 V, C_{LOAD} = 1 nF		12	25	
	GDA, GDB output voltage UV	I_{GDA}, I_{GDB} = 2.5 mA		1.6	2	V
ZERO CURRENT DETECTOR						
	ZCDA, ZCDB voltage threshold, falling		0.8	1.0	1.2	V
	ZCDA, ZCDB voltage threshold, rising		1.5	1.68	1.88	
	ZCDA, ZCDB clamp, high	I_{ZCDA} = +2 mA, I_{ZCDB} = +2 mA	2.6	3.0	3.4	
	ZCDA, ZCDB input bias current	ZCDA = 1.4 V, ZCDB = 1.4 V	–0.5		0.5	µA
	ZCDA, ZCDB clamp, low	I_{ZCDA} = –2 mA, I_{ZCDB} = –2 mA	–0.4	–0.2	0	V
	ZCDA, ZCDB delay to GDA, GDB outputs(2)	Respective gate drive output rising 10% from zero crossing input falling to 1 V		45	100	ns
CURRENT SENSE						
	CS input bias current	At rising threshold		–150	–250	µA
	CS current limit rising threshold		–0.18	–0.20	–0.22	V
	CS current limit falling threshold		–0.005	–0.015	–0.029	
	CS current limit response time(2)	From CS exceeding threshold –0.05 V to GDx dropping 10%		60	100	ns
MAINS INPUT						
	VINAC input bias current	VINAC = 2 V	–0.5		0.5	µA
BROWNOUT						
	VINAC brownout threshold	VINAC falling	1.34	1.39	1.44	V
	VINAC brownout current	VINAC = 1 V	5	7	9	µA
	VINAC brownout filter time	VINAC fails to exceed the brownout threshold for the brownout filter time	340	440	540	ms

(2) Refer to Figure 12, Figure 13, Figure 14, and Figure 15 in the Typical Characteristics for typical gate drive waveforms.

ELECTRICAL CHARACTERISTICS (continued)

At VCC = 16 V, AGND = PGND = 0 V, VINAC = 3 V, VSENSE = 6 V, HVSEN = 3 V, PHB = 5 V, R_{TSET} = 133 kΩ; all voltages are with respect to GND, all outputs unloaded, –40°C < T_J = T_A < +125°C, and currents are positive into and negative out of the specified terminal, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PULSE-WIDTH MODULATOR						
K_{TL}	On-time factor, phases A and B	VINAC = 3.2 V, VSENSE = 5.8 V(3)	3.6	4.0	4.4	µs/V
K_{TLS}	On-time factor, single-phase, A	VINAC = 3.2 V, VSENSE = 5.8 V, PHB = 0 V(3)	7.2	8	8.9	µs/V
	Phase B to phase A on-time matching	VSENSE = 5.8 V, VINAC = 3.2 V	–6%		6%	
	Zero-crossing distortion correction additional on time	COMP = 0.25 V, VINAC = 1 V	1.2	2	2.7	µs
		COMP = 0.25 V, VINAC = 0.1 V	12.6	20	29	µs
	PHB threshold falling, to single-phase operation	To GDB output shutdown VINAC = 1.5 V	0.7	0.8	0.9	V
	PHB threshold rising, to two-phase operation	To GDB output running VINAC = 1.5 V	0.9	1.0	1.1	V
$T_{(min)}$	Minimum switching period	R_{TSET} = 133 kΩ(3)	1.7	2.2	2.5	µs
	PWM restart time	ZCDA = ZCDB = 2 V(4)	165	200	265	µs
THERMAL SHUTDOWN						
	Thermal shutdown temperature	T_J, temperature rising(5)		+160		°C
	Thermal restart temperature	T_J, temperature falling(5)		+140		°C

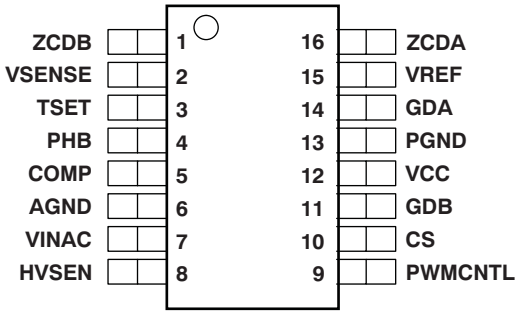
(3) Gate drive on-time is proportional to V_{COMP} – 125 mV. The on-time proportionality factor, K_T, is different in two-phase and single-phase modes. The on-time factor, K_T, scales linearly with the value of R_{TSET}. The minimum switching period is proportional to R_{TSET}.

(4) An output on-time is generated at both GDA and GDB if both ZCDA and ZCDB negative-going edges are not detected for the restart time. In single-phase mode, the restart time applies for the ZCDA input and the GDA output.

(5) Thermal shutdown occurs at temperatures higher than the normal operating range. Device performance above the normal operating temperature is not specified or assured.

DEVICE INFORMATION

UCC28061-Q1D
SOIC 16-Pin (D)
Top View



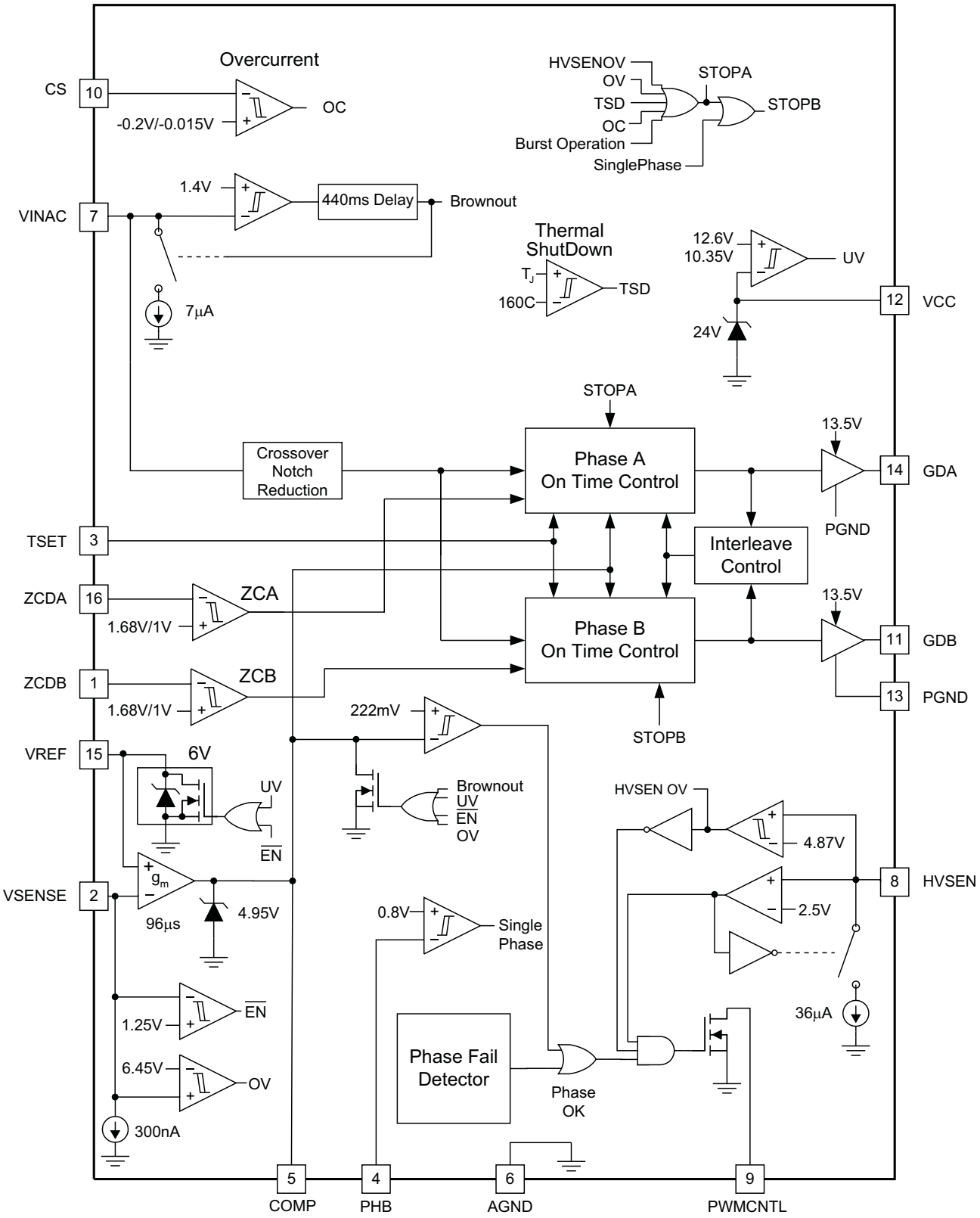
TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
NAME	NO.	I/O	
AGND	6	—	**Analog ground:** Connect analog signal bypass capacitors, compensation components, and analog signal returns to this pin. Connect the analog and power grounds at a single point to isolate high-current noise signals of the power components from interference with the low-current analog circuits.
COMP	5	O	**Error amplifier output:** The error amplifier is a transconductance amplifier, so this output is a high-impedance current source. Connect voltage regulation loop compensation components from this pin to AGND. The on-time seen at the gate drive outputs is proportional to the voltage at this pin minus an offset of approximately 125 mV. During soft-start events (undervoltage, brownout, disable or output over voltage), COMP is pulled low. Normal operation only resumes after the soft-start event clears and COMP has been discharged below 0.5 V, making sure that the circuit restarts with a low COMP voltage and a short on-time. Do not connect COMP to a low-impedance source that would interfere with COMP falling below 0.5 V.
CS	10	I	**Current sense input:** Connect the current sense resistor and the negative terminal of the diode bridge to this pin. Connect the return of the current sense resistor to the AGND pin with a separate trace. As input current increases, the voltage on CS goes more negative. This cycle-by-cycle over-current protection limits input current by turning off both gate driver (GDx) outputs when CS is more negative than the CS rising threshold (approximately –200 mV). The GD outputs remain low until CS falls to the CS falling threshold (approximately –15 mV). Current sense is blanked for approximately 100 ns following the falling edge of either GD output. This blanking filters noise that occurs when current switches from a power FET to a boost diode. In most cases, no additional current sense filtering is required. If filtering is required, the filter series resistance must be under 100 Ω to maintain accuracy. To prevent excessive negative voltage on the CS pin during inrush conditions, connect the current sensing resistor to the CS pin through a low value external resistor.
GDA	14	O	**Channel A and channel B gate drive output:** Connect these pins to the gate of the power FET for each phase through the shortest connection practical. If it is necessary to use a trace longer than 0.5 inch (12.6 mm) for this connection, some ringing may occur due to trace series inductance. This ringing can be reduced by adding a 5-Ω to 10-Ω resistor in series with GDA and GDB.
GDB	11	O	
HVSEN	8	I	**High voltage output sense:** The UCC28061-Q1 incorporates FailSafe OVP so that any single failure does not allow the output to boost above safe levels. Output over-voltage is monitored by both VSENSE and HVSEN and shuts down the PWM if either pin exceeds the appropriate over-voltage threshold. Using two pins to monitor for over-voltage provides redundant protection and fault tolerance. HVSEN can also be used to enable a downstream power converter when the voltage on HVSEN is within the operating region. Select the HVSEN divider ratio for the desired over-voltage and power-good thresholds. Select the HVSEN divider impedance for the desired power-good hysteresis. During operation, HVSEN must never fall below 0.8 V. Dropping HVSEN below 0.8 V puts the UCC28061-Q1 into a special test mode, used only for factory testing. A bypass capacitor from HVSEN to AGND is recommended to filter noise and prevent false over-voltage shutdown.
PGND	13	—	**Power ground for the integrated circuit:** Connect this pin to AGND through a separate short trace to isolate gate driver noise from analog signals.
PHB	4	I	**Phase B enable:** This pin turns on/off channel B of the boost converter. The commanded on-time for channel A is immediately doubled when channel B is disabled, which helps to keep COMP voltage constant during the phase management transient. The PHB thresholds change with line range for the best efficiency when PHB is connected to COMP. PHB can also be driven by external logic signals to allow customized phase management. To disable phase management, connect the PHB pin to the VREF pin.

TERMINAL FUNCTIONS (continued)

TERMINAL			DESCRIPTION
NAME	NO.	I/O	
PWMCNTL	9	O	**PWM enable logic output:** This open-drain output goes low when HVSEN is within the HVSEN good region and the ZCDA and ZCDB inputs are switching correctly if operating in two-phase mode (see PHB Pin). Otherwise, PWMCNTL is high impedance.
TSET	3	I	**Timing set:** PWM on-time programming input. Connect a resistor from TSET to AGND to set the on-time versus COMP voltage and the minimum period at the gate drive outputs.
VCC	12	—	**Bias supply input:** Connect this pin to a controlled bias supply of between 14 V and 21 V. Also connect a 0.1-µF ceramic bypass capacitor from this pin to PGND with the shortest possible board trace. This supply powers all circuits in the device and must be capable of delivering 6 mA dc plus the transient power MOSFET gate charging current.
VINAC	7	I	**Input ac voltage sense:** For normal operation, connect this pin to a voltage divider across the rectified input power mains. When the voltage on VINAC remains below the brownout threshold for more than the brownout filter time, the device enters a brownout mode and both output drives are disabled. Select the input voltage divider ratio for the desired brownout threshold. Select the divider impedance for the desired brownout hysteresis.
VREF	15	O	**Voltage reference output:** Connect a 0.1-µF ceramic bypass capacitor from this pin to AGND. VREF turns off during VCC undervoltage and VSENSE disable to save supply current and increase efficiency. This 6 VDC reference can be used to bias other circuits requiring less than 2 mA of total supply current.
VSENSE	2	I	**Output dc voltage sense:** Connect this pin to a voltage divider across the output of the power converter. The error amplifier reference voltage is 6 V. Select the output voltage divider ratio for the desired output voltage. Connect the ground side of this divider to ground through a separate short trace for best output regulation accuracy and noise immunity. VSENSE can be pulled low by an open-drain logic output or 6-V logic output in series with a low-leakage diode to disable the outputs and reduce VCC current. If VSENSE is disconnected, open-loop protection provides an internal current source to pull VSENSE low, turning off the gate drivers.
ZCDA	16	I	**Zero current detection inputs:** These inputs expect to see a negative edge when the inductor current in the respective phases go to zero. The inputs are clamped at 0 V and 3 V. Signals should be coupled through a series resistor that limits the clamping current to less than ±3 mA. Connect these pins through a current limiting resistor to the zero crossing detection windings of the appropriate boost inductor. The inductor winding must be connected so that this voltage drops when inductor current decays to zero. When the inductor current drops to zero, the ZCD input must drop below the falling threshold, approximately 1 V, to cause the gate drive output to rise. When the power MOSFET turns off, the ZCD input must rise above the rising threshold, approximately 1.7 V, to arm the logic for another falling ZCD edge.
ZCDB	1	I	

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

At VCC = 16 V, AGND = PGND = 0 V, VINAC = 3 V, VSENSE = 6 V, HVSEN = 3 V, PHB = 5 V, R_{TSET} = 133 kΩ; all voltages are with respect to GND, all outputs unloaded, $T_J = T_A$ = +25°C, and currents are positive into and negative out of the specified terminal, unless otherwise noted.

BIAS SUPPLY CURRENT vs BIAS SUPPLY VOLTAGE

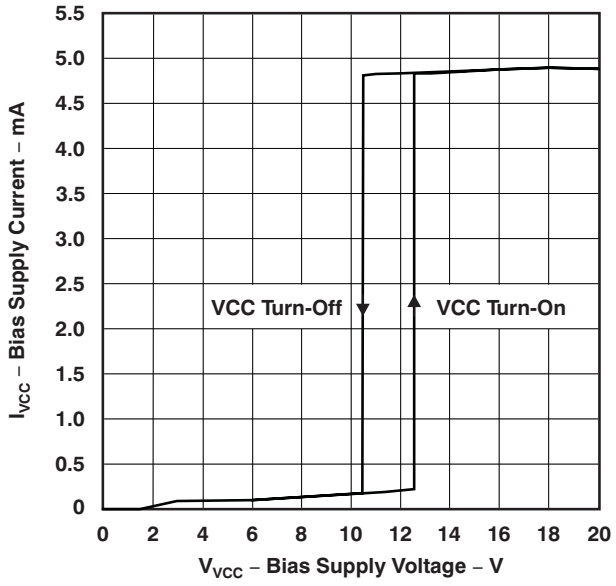


Figure 1.

BIAS SUPPLY CURRENT vs TEMPERATURE

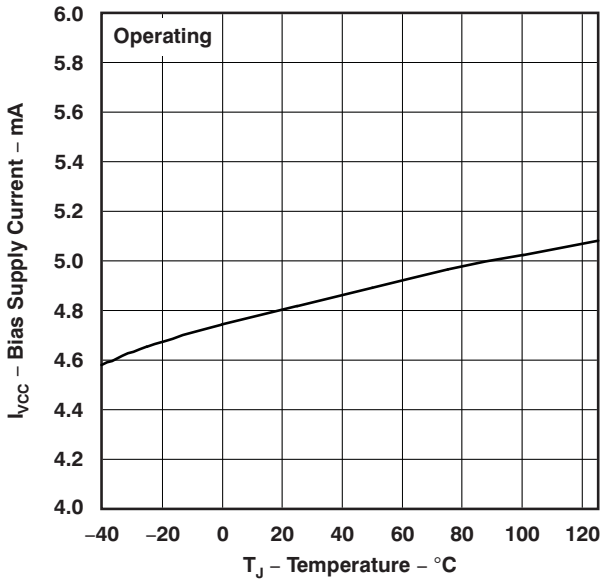


Figure 2.

BIAS SUPPLY CURRENT vs TEMPERATURE

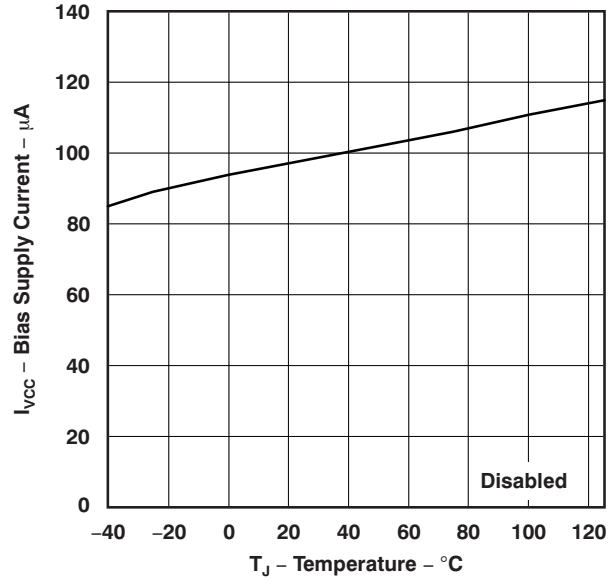


Figure 3.

ERROR AMPLIFIER TRANSFER FUNCTION

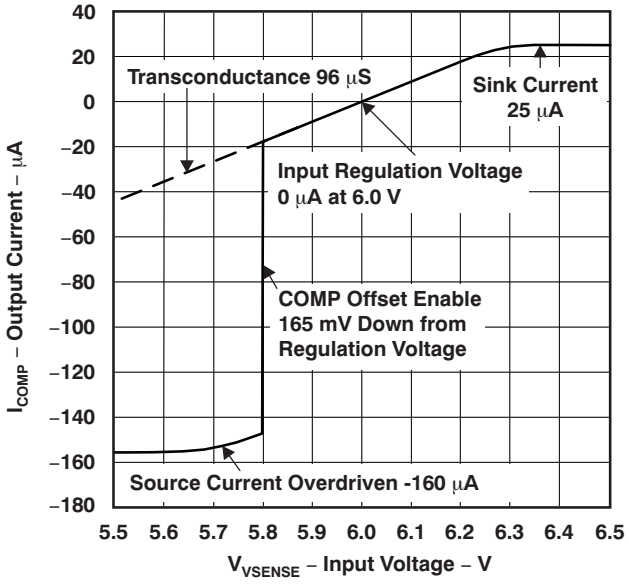


Figure 4.

TYPICAL CHARACTERISTICS (continued)

At VCC = 16 V, AGND = PGND = 0 V, VINAC = 3 V, VSENSE = 6 V, HVSEN = 3 V, PHB = 5 V, R_{TSET} = 133 kΩ; all voltages are with respect to GND, all outputs unloaded, $T_J = T_A$ = +25°C, and currents are positive into and negative out of the specified terminal, unless otherwise noted.

ERROR AMPLIFIER TRANSCONDUCTANCE vs TEMPERATURE

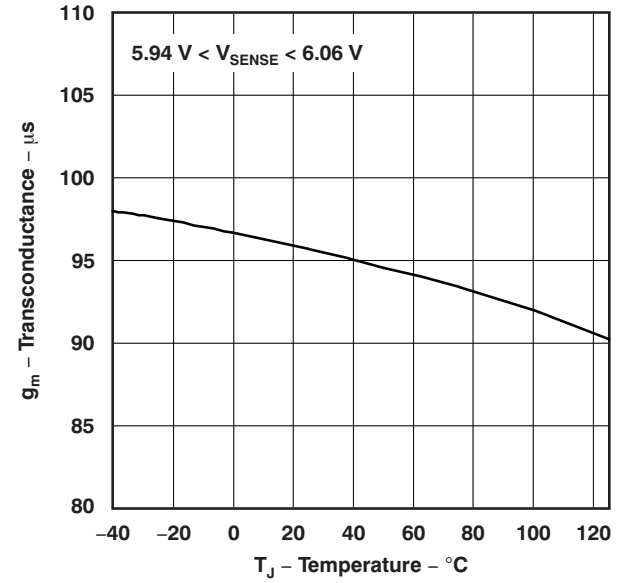


Figure 5.

ERROR AMPLIFIER OUTPUT CURRENT vs OUTPUT VOLTAGE

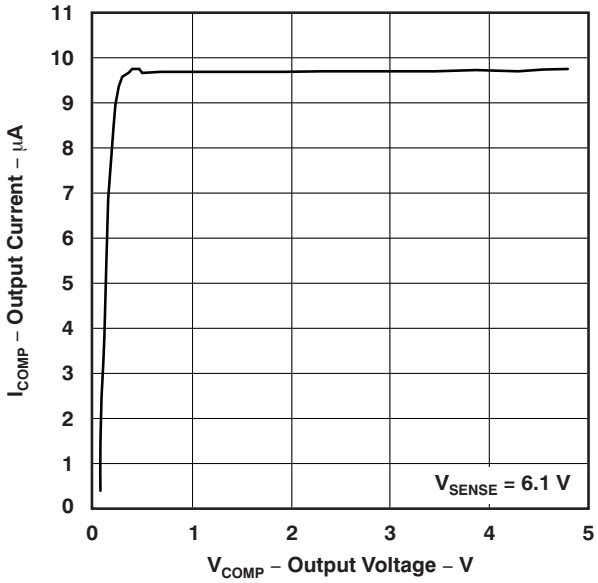


Figure 6.

ERROR AMPLIFIER INPUT BIAS CURRENT vs INPUT VOLTAGE

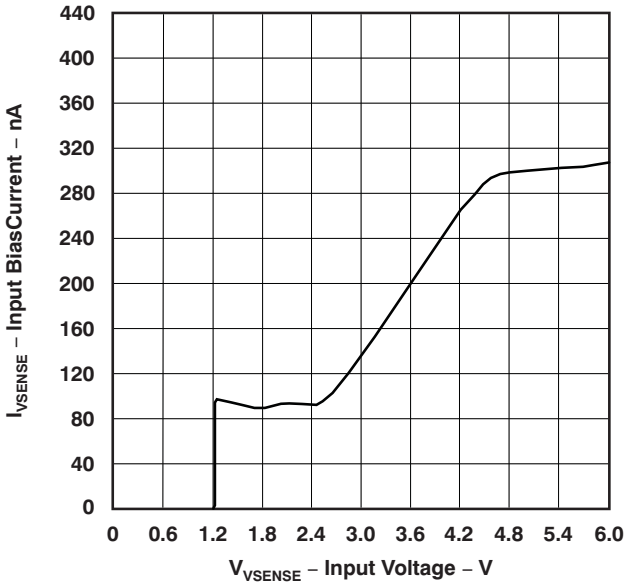


Figure 7.

CURRENT SENSE INPUT BIAS CURRENT vs TEMPERATURE

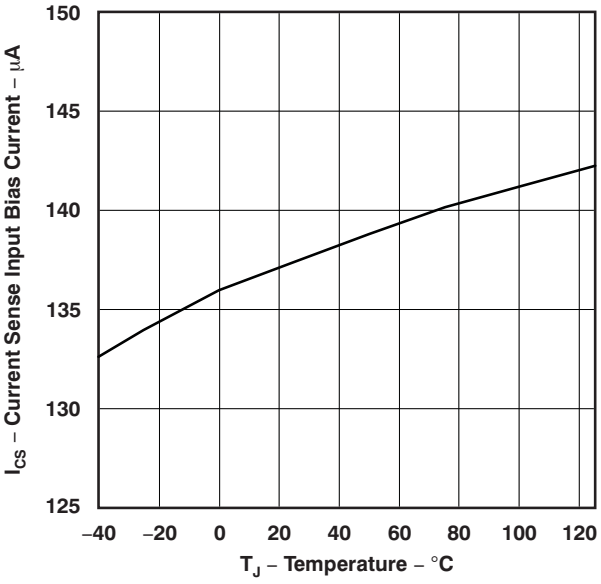


Figure 8.

TYPICAL CHARACTERISTICS (continued)

At VCC = 16 V, AGND = PGND = 0 V, VINAC = 3 V, VSENSE = 6 V, HVSEN = 3 V, PHB = 5 V, R_{TSET} = 133 kΩ; all voltages are with respect to GND, all outputs unloaded, $T_J = T_A$ = +25°C, and currents are positive into and negative out of the specified terminal, unless otherwise noted.

ZERO CURRENT DETECT CLAMP CURRENT vs HIGH INPUT VOLTAGE

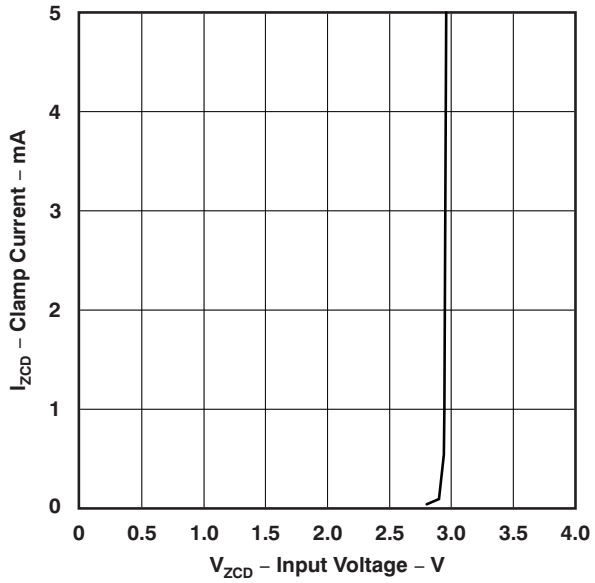


Figure 9.

ZERO CURRENT DETECT CLAMP CURRENT vs LOW INPUT VOLTAGE

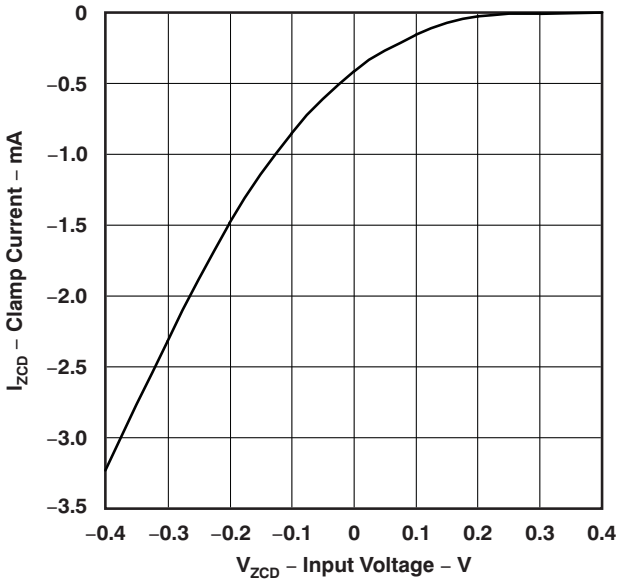


Figure 10.

BROWNOUT FILTER DELAY TIME vs TEMPERATURE

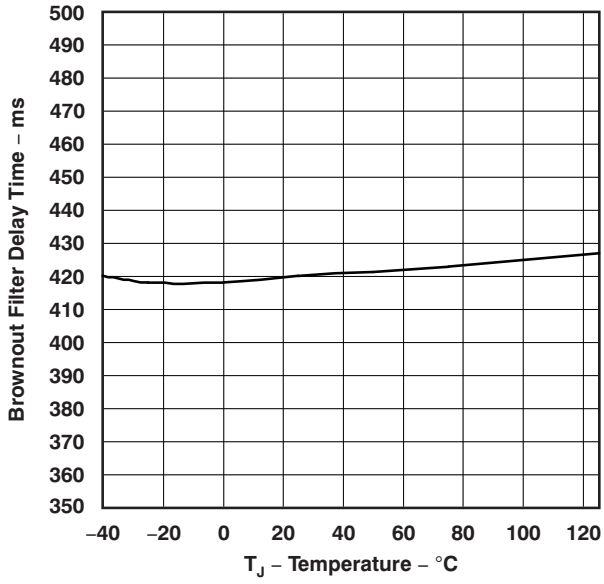


Figure 11.

GATE DRIVE RISING vs TIME

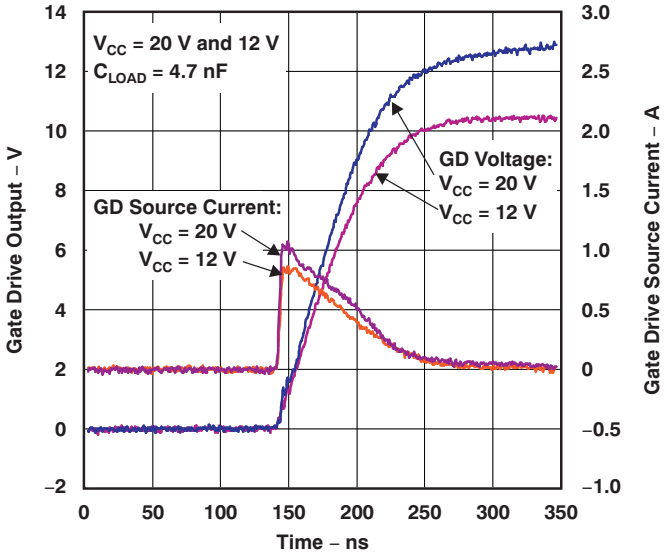


Figure 12.

TYPICAL CHARACTERISTICS (continued)

At VCC = 16 V, AGND = PGND = 0 V, VINAC = 3 V, VSENSE = 6 V, HVSEN = 3 V, PHB = 5 V, R_{TSET} = 133 kΩ; all voltages are with respect to GND, all outputs unloaded, $T_J = T_A$ = +25°C, and currents are positive into and negative out of the specified terminal, unless otherwise noted.

GATE DRIVE FALLING vs TIME

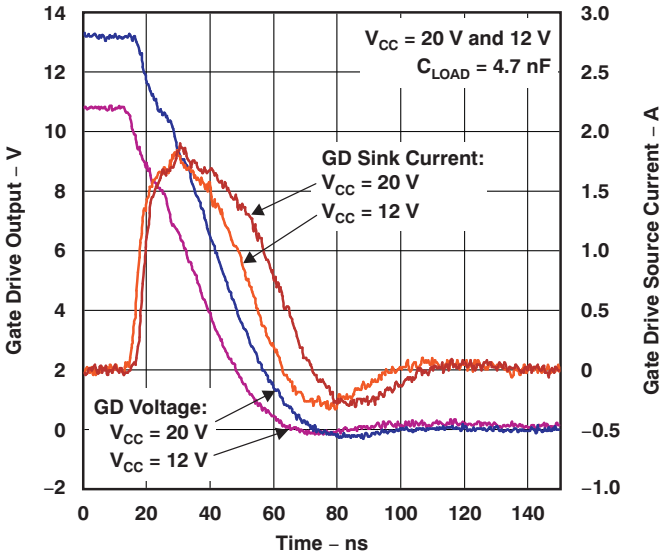


Figure 13.

GATE DRIVE RISING vs TIME AND DELAY FROM ZCD INPUT

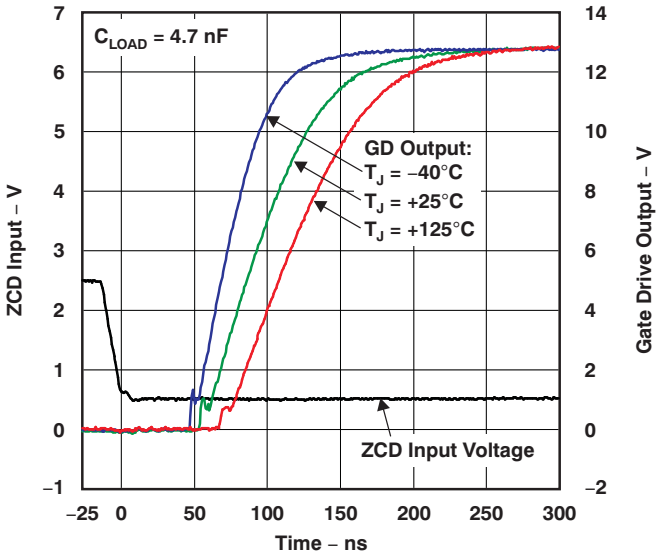


Figure 14.

GATE DRIVE FALLING vs TIME AND DELAY FROM CS INPUT

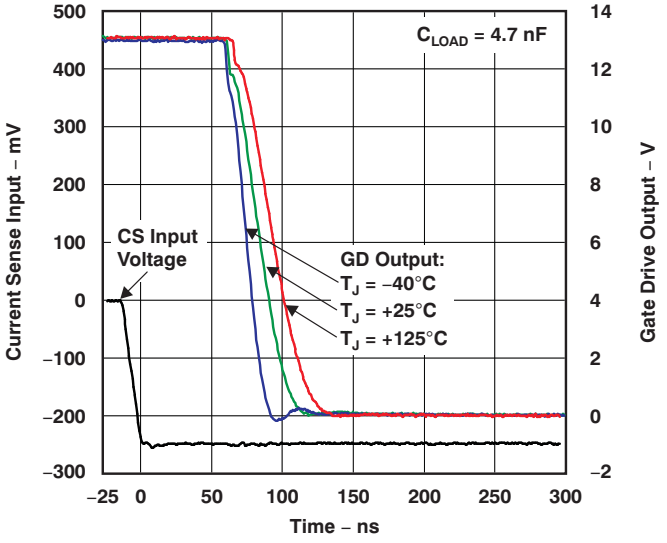


Figure 15.

GATE DRIVE OUTPUT HIGH vs VCC

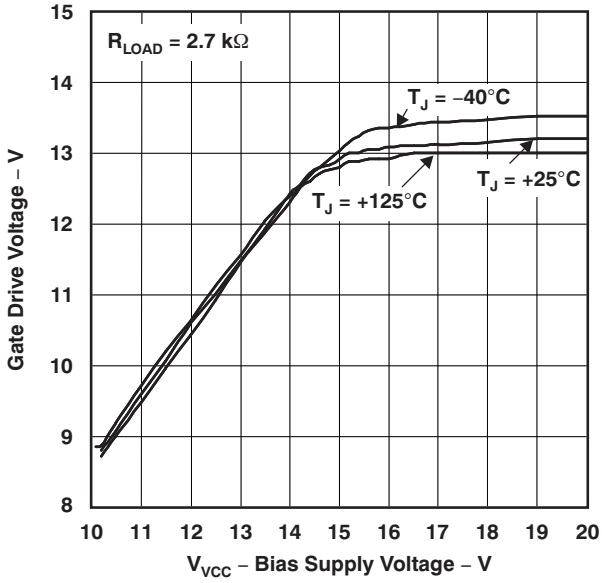


Figure 16.

TYPICAL CHARACTERISTICS (continued)

At VCC = 16 V, AGND = PGND = 0 V, VINAC = 3 V, VSENSE = 6 V, HVSEN = 3 V, PHB = 5 V, R_{TSET} = 133 kΩ; all voltages are with respect to GND, all outputs unloaded, $T_J = T_A$ = +25°C, and currents are positive into and negative out of the specified terminal, unless otherwise noted.

GATE DRIVE OUTPUT IN UVLO vs SINK CURRENT

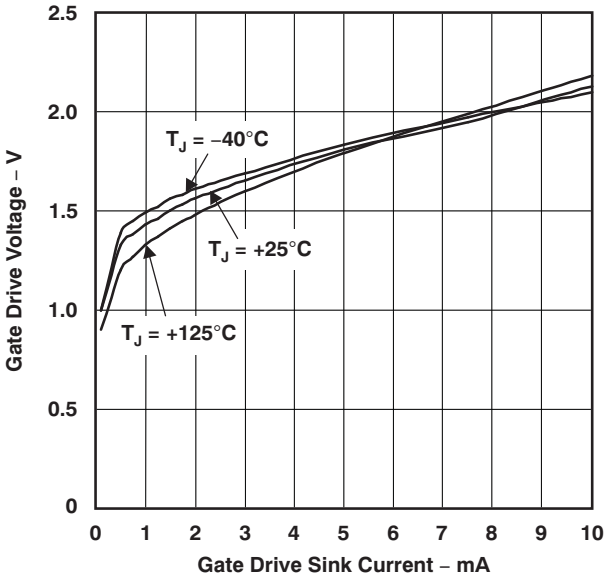


Figure 17.

GATE DRIVE HIGH VOLTAGE vs TEMPERATURE

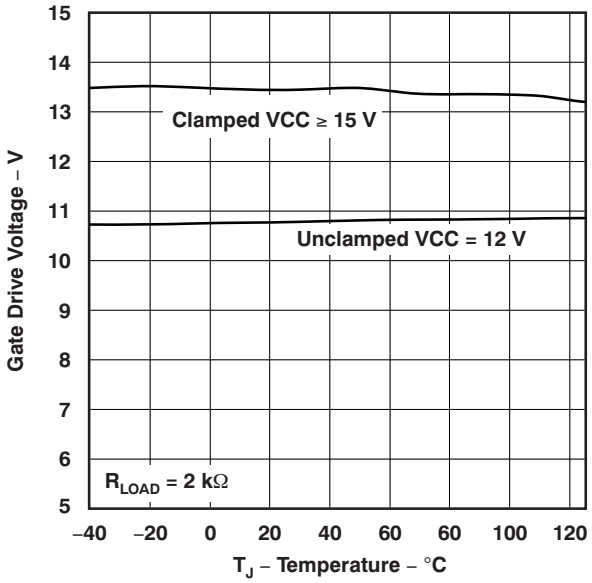


Figure 18.

ON-TIME FACTOR vs TIME SETTING RESISTOR

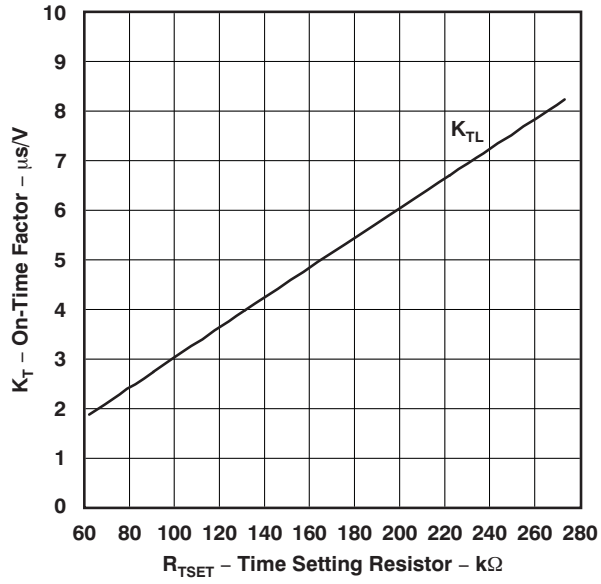


Figure 19.

ON-TIME FACTOR PHASE A AND B vs TEMPERATURE

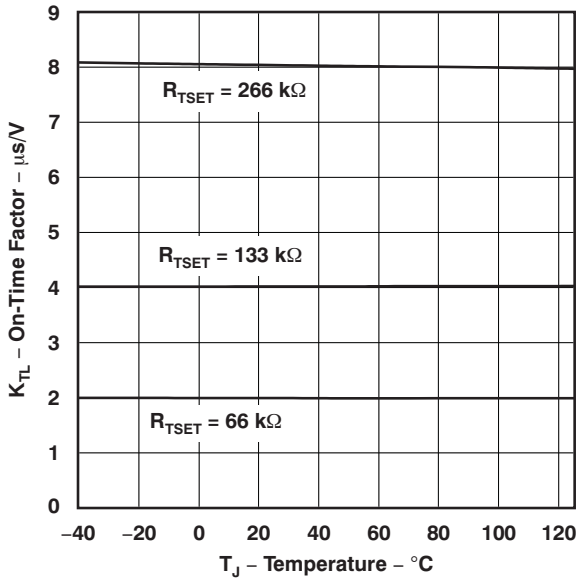


Figure 20.

TYPICAL CHARACTERISTICS (continued)

At VCC = 16 V, AGND = PGND = 0 V, VINAC = 3 V, VSENSE = 6 V, HVSEN = 3 V, PHB = 5 V, R_{TSET} = 133 kΩ; all voltages are with respect to GND, all outputs unloaded, $T_J = T_A$ = +25°C, and currents are positive into and negative out of the specified terminal, unless otherwise noted.

ON-TIME FACTOR vs PHASE SHIFT

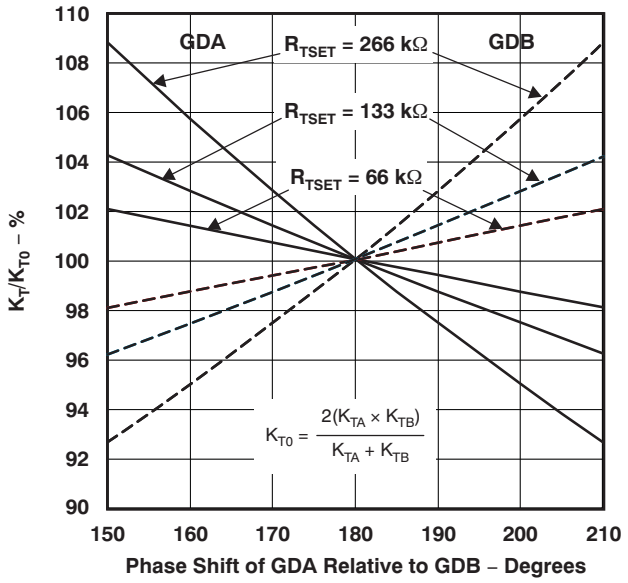


Figure 21.

PWM RESTART TIME vs TEMPERATURE

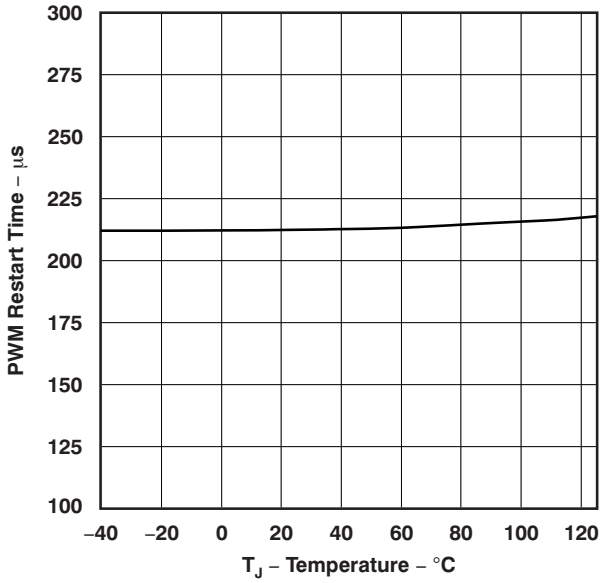


Figure 22.

ADDITIONAL ON-TIME vs VINAC ZERO-CROSSING DISTORTION CORRECTION

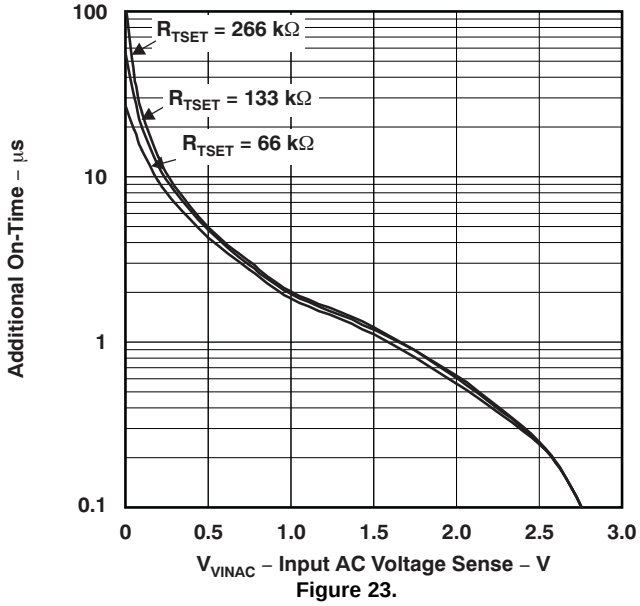


Figure 23.

APPLICATION INFORMATION

Theory of Operation

The UCC28061-Q1 contains the control circuits for two boost pulse-width modulation (PWM) power converters. The boost PWM power converters ramp current in the boost inductors for a time period proportional to the voltage on the error amplifier output. Each power converter then turns off the power MOSFET until current in the boost inductor decays to 0, as sensed on the zero current detection inputs (ZCDA and ZCDB). Once the inductor current decays to 0, the power converter starts another cycle. This on/off cycling produces a triangle wave of current, with peak current set by the on-time and power mains input voltage, as shown in Equation 1.

$$I_{PEAK}(t) = \frac{VINAC(t) \times T_{ON}}{L} \quad (1)$$

The average line current is exactly equal to half of the peak line current, as shown in Equation 2.

$$I_{AVG}(t) = \frac{VINAC(t) \times T_{ON}}{2 \times L} \quad (2)$$

With T_{ON} and L being essentially constant during an ac line period, the resulting triangular current waveform during each switching cycle has an average value proportional to the instantaneous value of the rectified ac line voltage. This architecture results in a resistive input impedance characteristic at the line frequency and a near-unity power factor.

The outputs of the two PWMs operate 180° out-of-phase so that power-line ripple current for the two PWMs is greatly reduced from the ripple current of each individual PWM. This design reduces ripple current at the input and output, allowing the reduction in size and cost of input and output filters.

Optimal phase balance occurs if the individual power stages and the on-times are well-matched. Mismatches in inductor values do not affect the phase relationship.

On-Time Control, Maximum Frequency Limiting, and Restart Timer

Gate drive on-time varies with the error amplifier output voltage by a factor called K_T, as shown in Equation 3.

$$T_{ON} = K_T (V_{COMP} - 125\ mV) \quad (3)$$

Where:

V_{COMP} is the output of the error amplifier, and 125 mV is a modulator offset.

To provide smooth transition between two-phase and single-phase operation, K_T increases by a factor of two in single-phase mode:

- $K_{TLS} = 2 \times K_{TL}$; active in single-phase operation

The clamped maximum output of the error amplifier is limited to 4.95 V. This value, less the 125 mV modulator offset, limits on-time to Equation 4.

$$T_{ON(max)} = K_T \times 4.825\ V \quad (4)$$

This on-time limit sets the maximum power that can be delivered by the converter at a given input voltage level.

The switching frequency of each phase is limited by minimum period timers. If the current decays to 0 before the minimum period timer elapses, turn-on is delayed, resulting in discontinuous phase current.

The restart timer ensures starting under all circumstances by restarting both phases if either phase ZCD input has not transitioned high-to-low for approximately 200 µs. To prevent the circuit from operating in continuous conduction mode (CCM), the restart time does not trigger turn-on until both phase currents return to 0.

The on-time factors (K_{TH}, K_{THS}, K_{TL}, K_{TLS}) and the minimum switching period T_{MIN} are proportional to the time setting resistor R_{TSET}, the resistor from the TSET pin to ground, and they can be calculated by Equation 5 through Equation 6:

$$K_{TL} = \frac{R_{TSET}}{133\ k\Omega} \times 4.0\ \frac{\mu s}{V} \quad (5)$$

$$T_{MIN} = \frac{R_{TSET}}{133\ k\Omega} \times 2.2\mu s;\ \text{Minimum Switching Period} \quad (6)$$

The proper value of R_{TSET} results in the clamped maximum on-time, $T_{ON(max)}$, required by the converter operating at the minimum input line and maximum load.

Natural Interleaving

Under normal operating conditions, the UCC28061-Q1 regulates the relative phasing of the channel A and channel B inductor currents to be very close to 180°, minimizing the ripple currents seen at the line source and output capacitor. The phase control function differentially modulates the on-times of the A and B channels based on the phase and frequency relationship. This natural interleaving method allows the converter to achieve 180° phase shift and transition mode operation for both phases without the requirements on boost inductor tolerance. As a result, the current sharing of the A and B channels are proportional to the inductor tolerance. The best current sharing is achieved when both inductors are exactly the same value.

Phase Management

At light load, it can improve efficiency to shut down one phase. Although conduction losses increase in one-phase operation, switching losses decrease. At certain power levels, the reduction of switching losses is greater than the increase in conduction losses. Turning off one phase at light load is especially valuable for meeting light-load efficient standards.

To operate in two-phase (normal) mode, pull PHB high or connect PHB to VREF. To operate in one-phase mode, connect PHB to ground.

Zero Crossing Detection and Valley Switching

In transition-mode PFC circuits, the MOSFET turns on when the boost inductor current crosses 0. Because of the resonance between the boost inductor and the parasitic capacitor at the MOSFET drain node, part of the energy stored in the MOSFET junction capacitor can be recovered, reducing switching losses. Furthermore, when the rectified input voltage is less than half of the output voltage, all the energy stored in the MOSFET junction capacitor can be recovered and zero-voltage switching (ZVS) can be realized. By adding an appropriate delay, the MOSFET can be turned on at the valley of its resonating drain voltage (valley switching). In this way, the energy recovery can be maximized and switching loss is minimized.

The RC time constant is generally derived empirically, but a good starting point is a value equal to 25% of the resonant period of the drain circuit. The delay can be realized by a simple RC filter, as shown in Figure 24. Because the ZCD pin is internally clamped, a more accurate delay can also be realized by using Figure 25.

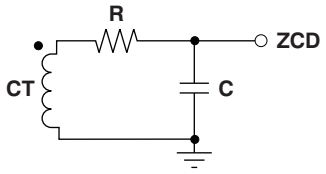


Figure 24. Simple RC Delay Circuit

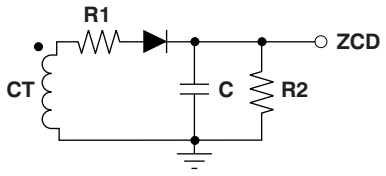


Figure 25. More Accurate Time Delay Circuit

Brownout Protection

As the power line RMS voltage decreases, RMS input current increases to maintain the output voltage constant for a specific load. Brownout protection prevents the RMS input current from exceeding a safe operating level. Power line RMS voltage is sensed at VINAC. When the voltage applied to VINAC fails to exceed the brownout threshold for the brownout filter time, a brownout condition is detected and both gate drive outputs immediately pull low. During brownout, COMP is actively pulled low. Gate drive outputs remain low until the voltage on VINAC rises above the brownout threshold. After a brownout, the power stage soft-starts as COMP rises.

The brownout detection threshold and its hysteresis are set by the voltage divider ratio and resistor values. Brownout protection is based on VINAC peak voltage; the threshold and hysteresis are also based on line peak voltage. The peak VINAC voltage can be easily translated into RMS value. Suggested resistor values for the voltage divider are 3 MΩ ±1% from the rectified input voltage to VINAC and 46.4 kΩ ±1% from VINAC to ground. These resistors set the typical thresholds for RMS line voltages, as shown in Table 2.

Table 2. Brownout Thresholds

THRESHOLD	BROWNOUT (RMS)
Falling	65 V
Rising	79.8 V

Failsafe OVP—Output Over-Voltage Protection

FailSafe OVP prevents any single failure from allowing the output to boost above safe levels. Redundant paths for output voltage sensing provide additional protection against output over-voltage. Over-voltage protection is implemented through two independent paths: VSENSE and HVSEN. The converter shuts down if either input senses an over-voltage condition. The output voltage can still maintain a safe level with either loop failure. The device is re-enabled when both sense inputs fall back into the normal range. At that time, the gate drive outputs resume switching under PWM control. Output over-voltage does not cause soft-start and the COMP pin is not discharged during an output over-voltage event.

Over-Current Protection

Under certain conditions (such as inrush, brownout recovery, and output overload), the PFC power stage sees large currents. It is critical that the power devices be protected from switching during these conditions.

The conventional current sensing method uses a shunt resistor in series with the MOSFET source to sense the converter current, resulting in multiple ground points and high power dissipation. Furthermore, since no current information is available when the MOSFETs are off, the source resistor current sensing method requires repeated turn-ons of the MOSFETs during over-current conditions. As a result, the converter may temporarily operate in continuous current mode (CCM) and experience failures induced by excessive reverse recovery currents in the boost diode.

The UCC28061-Q1 uses a single resistor to continuously sense the total inductor (input) current. This way, turn-on of the MOSFETs is completely avoided when the inductor currents are excessive. The drive to the MOSFETs is inhibited until total inductor current drops to near zero, precluding reverse recovery induced failures (these failures are most likely to occur when the ac line recovers from a brownout condition).

Following an over-current condition, both MOSFETs are turned on in phase when the input current drops to near 0. Because two phase currents are temporarily operating in phase, set the over-current protection threshold to more than twice of each phase maximum current ripple value in order to allow a return to normal operation after an over-current event.

Phase Fail Protection

The UCC28061-Q1 detects failure of one phase by monitoring the sequence of ZCD pulses. During normal two-phase operation, if one ZCD input remains idle for longer than approximately 14 ms while the other ZCD input switches normally, PWMCNTL goes high, indicating that the power stage is not operating correctly. During normal single-phase operation, phase failure is not monitored. On the UCC28061-Q1, phase failure is not monitored if COMP is below approximately 222 mV.

Distortion Reduction

Because of the resonance between the capacitance present across the drain-source of the switching MOSFET and the boost inductor, conventional transition mode power factor correction circuits may not be able to absorb power from the input line when the input voltage is around 0 V. This limitation results in waveform distortion and increased harmonic distortion. To reduce line current distortion to the lowest possible level, the UCC28061-Q1 increases switching MOSFET on-time when input voltage is around 0 V to increase the power absorption and compensate for this effect.

Improved Error Amplifier

The voltage error amplifier is a transconductance amplifier. Voltage loop compensation is connected from the error amplifier output, COMP, to analog ground, AGND. The recommended compensation network is shown in Figure 26.

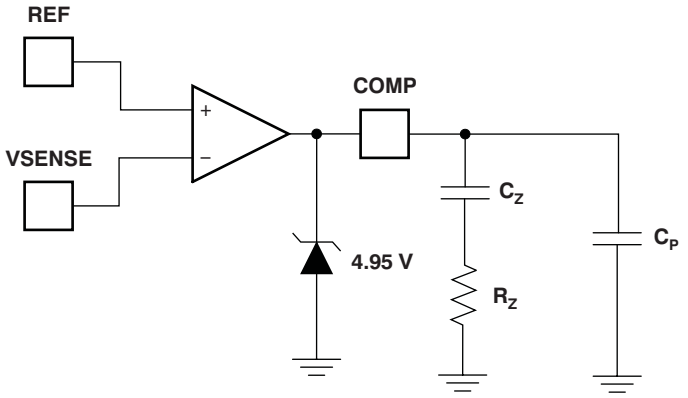


Figure 26. Typical Error Amplifier Compensation

To improve the transient response, the error amplifier output current is increased by 100 µA when the error amp input is below 5.8 V, as shown in Figure 27. This increase allows faster charging of the compensation components following sudden load current increases (also refer to Figure 4 in the Typical Characteristics).

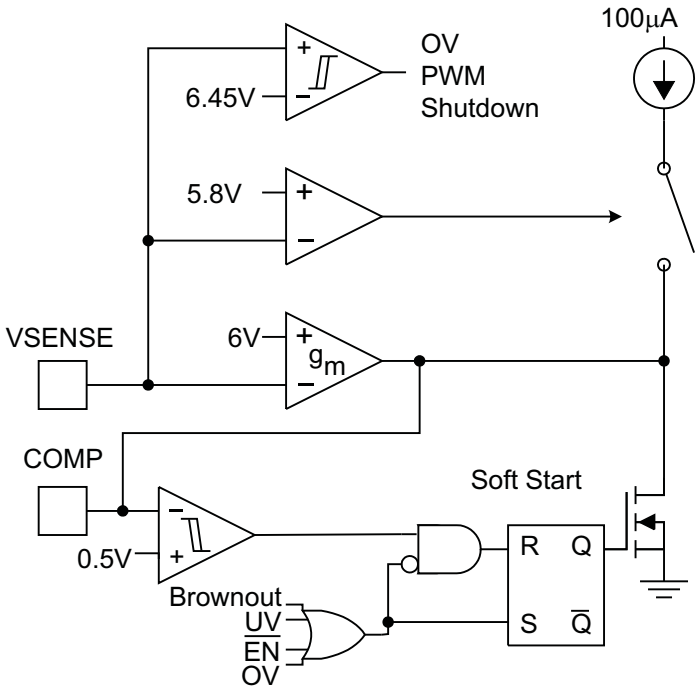


Figure 27. Error Amplifier Block Diagram Showing Speed-Up and Latched Soft-Start

The UCC28061-Q1 asserts soft start when output over-voltage is detected, pulling COMP to ground. This improves response to a change from heavy load to light load.

Open-Loop Protection

If the feedback loop is disconnected from the device, a current source internal to the UCC28061-Q1 pulls the VSENSE pin voltage towards ground. When VSENSE falls below 1.20 V, the device is disabled. When disabled, supply current decreases, and both gate drive outputs and COMP are actively pulled low. The device is re-enabled when VSENSE rises above 1.25 V. At that time, the gate drive outputs begin switching under PWM control.

The device can be externally disabled by grounding the VSENSE pin with an open-drain or open-collector driver. When disabled, device supply current drops and COMP is actively pulled low. When VSENSE is released, the device soft-starts. This disable method forces the device into standby mode and minimizes its power consumption. This feature is particularly useful when standby power is a key design aspect.

If the feedback loop is disconnected from ground, the VSENSE voltage goes high. When VSENSE rises above the over-voltage protection threshold, both gate drive outputs go low, and COMP is actively pulled low. The device is re-enabled when VSENSE falls back into range. At that time, the gate drive outputs begin switching under PWM control. The VSENSE pin is internally clamped to protect the device from damage under this condition.

Soft-Start

The PWM gradually ramps from zero on-time to normal on-time as the compensation capacitor from COMP to AGND charges from a low level to the final value. This process implements a soft-start, with a time constant set by the output current of the error amplifier and the value of the compensation capacitors. In the event of a brownout, logic disable, or VCC undervoltage fault, COMP is actively pulled low so the PWM soft-starts after this event is cleared. The UCC28061-Q1 also asserts soft start when output over-voltage is detected. Even if a fault event happens very briefly, soft-start fully discharges the compensation components before resuming operation, ensuring soft-starting. See Figure 27 for details.

Light-Load Operation

As load current decreases, the error amplifier commands less input current by lowering the COMP voltage. If PHB (normally connected to COMP) falls below 0.8 V at low input line (or 1.1 V at high input line), channel B stops switching and channel A on-time doubles to compensate. If COMP falls below 150 mV, channel A also stops switching and the loop enters a hysteretic control mode. The PWM skips cycles to maintain regulation.

Instead of skipping cycles, the UCC28061-Q1 allows on-time reduction smoothly to zero as load decreases. However, maximum switching frequency is limited, so at very light load, discountinuous operation is possible.

Command for the Downstream Converter

In the UCC28061-Q1, the PWMCNTL pin is used to coordinate the PFC stage with a downstream converter. Through the HVSEN pin, the output voltage is sensed. When the output voltage is within the desired range, the PWMCNTL pin is pulled to ground internally and can be used to enable a downstream converter. The enable threshold and hysteresis can be adjusted independently through the voltage divider ratio and resistor values. The HVSEN pin is also used for the FailSafe over-voltage protection. When designing the voltage divider, make sure this FailSafe over-voltage protection level is set above normal operating levels.

VCC Undervoltage Protection

VCC must rise above the undervoltage threshold for the PWM to begin functioning. If VCC drops below the threshold during operation, both gate drive outputs and COMP are actively pulled low. VCC must rise above the threshold for PWM function to restart.

VCC

VCC is connected to a bias supply of between 13 V and 21 V. When powered from a poorly-regulated supply, an external zener diode is recommended to prevent excessive current into VCC.

DESIGN EXAMPLE

An example of the UCC28061-Q1 PFC controller in a two-phase transition mode interleaved PFC pre-regulator is shown in Figure 28.

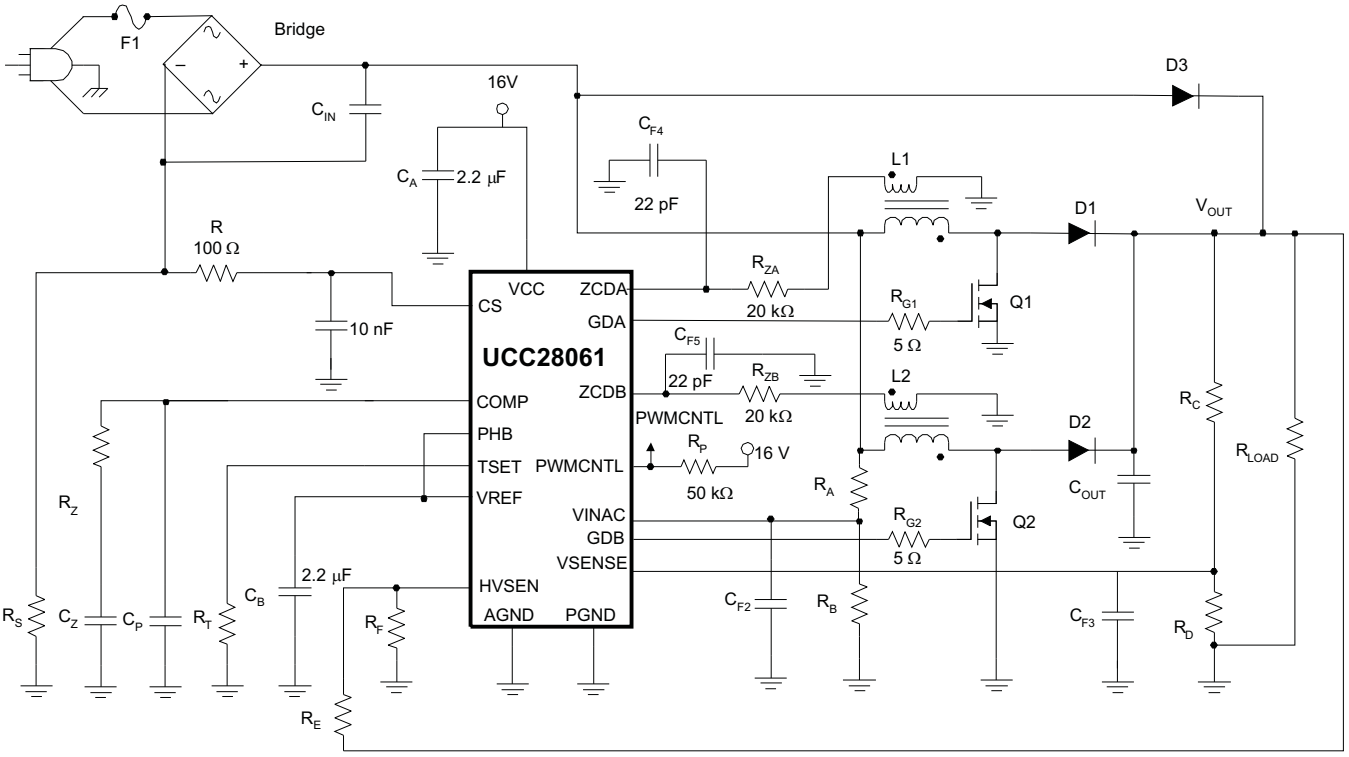


Figure 28. Typical Transition Mode Interleaved PFC Pre-Regulator

Design Goals

The specifications for this design were chosen based on the power requirements of a 300-W LCD TV. These specifications are shown in Table 3.

Table 3. Design Specifications

PARAMETER		MIN	TYP	MAX	UNIT
V_{IN}	RMS input voltage	85 (V_{IN_MIN})		265 (V_{IN_MAX})	V_{RMS}
V_{OUT}	Output voltage		390		V
f_{LINE}	Line frequency	47		63	Hz
PF	Power factor at maximum load	0.90			
P_{OUT}				300	W
η	Full load efficiency	0.92			
f_{MIN}	Minimum switching frequency	45			kHz

Recommended PCB Device Layout

Interleaved transition-mode PFC system architecture dramatically reduces input and output ripple current, allowing the circuit to use smaller and less expensive filters. To maximize the benefits of interleaving, the input and output filter capacitors should be located after the two phase currents are combined together. Similar to other power management devices, when laying out the printed circuit board (PCB) it is important to use star grounding techniques and keep filter capacitors as close to device ground as possible. To minimize the interference caused by capacitive coupling from the boost inductor, the device should be located at least 1 in (25.4 mm) away from the boost inductor. It is also recommended that the device not be placed underneath magnetic elements. Because of the precise timing requirement, the timing setting resistor R_T should be put as close as possible to the TSET pin and returned to the analog ground. See Figure 29 for a recommended component layout and placement.

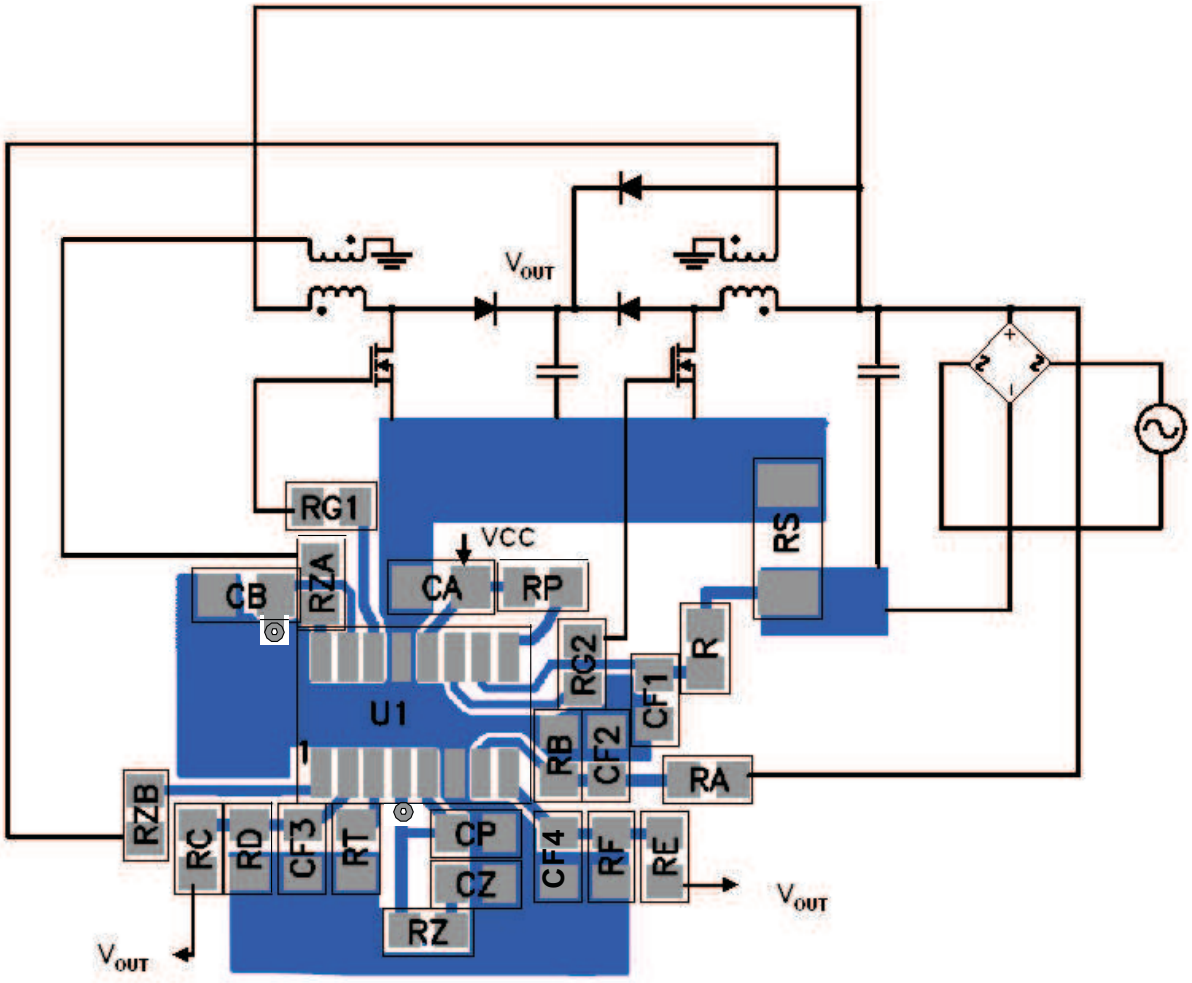


Figure 29. Recommended PCB Layout

NOTE

PHB and VREF Pins are connected by a Jumper on the back of the board.

Inductor Selection

The boost inductor is selected based on the inductor ripple current requirements at the peak of low line. Selecting the inductor requires calculating the boost converter duty cycle at the peak of low line ($D_{PEAK\_LOW\_LINE}$), as shown in Equation 7.

$$D_{PEAK\_LOW\_LINE} = \frac{V_{OUT} - V_{IN\_MIN}\sqrt{2}}{V_{OUT}} = \frac{390\ V - 85\ V\sqrt{2}}{390\ V} \approx 0.69 \quad (7)$$

The minimum switching frequency of the converter (f_{MIN}) under low line conditions occurs at the peak of low line and is set between 25 kHz and 50 kHz to avoid audible noise. For this design example, f_{MIN} was set to 45 kHz:

$$L1 = L2 = \frac{\eta \times V_{IN\_MIN}^{2} \times D_{PEAK\_LOW\_LINE}}{P_{OUT} \times f_{MIN}} = \frac{0.92(85\ V)^{2}\ 0.69}{300\ W \times 45\ kHz} \approx 340\ \mu H \quad (8)$$

The inductor for this design would have a peak current (I_{LPEAK}) of 5.4 A, as shown in Equation 9, and an RMS current (I_{LRMS}) of 2.2 A, as shown in Equation 10.

$$I_{LPEAK} = \frac{P_{OUT}\sqrt{2}}{V_{IN\_MIN} \times \eta} = \frac{300\ W\sqrt{2}}{85\ V \times 0.92} \approx 5.4\ A \quad (9)$$

$$I_{LRMS} = \frac{I_{LPEAK}}{\sqrt{6}} = \frac{5.4\ A}{\sqrt{6}} \approx 2.2\ A \quad (10)$$

This converter uses constant on-time (T_{ON}) and zero-current switching (ZCS) to set up the converter timing. Auxiliary windings off of L1 and L2 detect when the inductor currents are 0. Selecting the turns ratio in Equation 11 ensures that there is at least 2 V at the peak of high line to reset the ZCD comparator after every switching cycle.

The turns-ratio of each auxiliary winding is:

$$\frac{N_P}{N_S} = \frac{V_{OUT} - V_{IN\_MAX}\sqrt{2}}{2\ V} = \frac{390\ V - 265\ V\sqrt{2}}{2\ V} \approx 8 \quad (11)$$

ZCD Resistor Selection (R_{ZA}, R_{ZB})

The minimum value of the ZCD resistors is selected based on the internal zener clamp maximum current rating of 3 mA, as shown in Equation 12.

$$R_{ZA} = R_{ZB} \geq \frac{V_{OUT}\,N_S}{N_P \times 3\ mA} = \frac{390\ V}{8 \times 3\ mA} \approx 16.3\ k\Omega \quad (12)$$

In this design the ZCD resistors were set to 20 kΩ, as shown in Equation 13.

$$R_{ZA} = R_{ZB} = 20\ k\Omega \quad (13)$$

HVSENSE

The HVSENSE pin programs the PWMCNTL output of the UCC28061-Q1. The PWMCNTL open-drain output can be used to disable a downstream converter while the PFC output capacitor is charging. PWMCNTL starts in high impedance and pulls to ground when the HVSENSE increases above 2.5 V. Setting the point where PWMCNTL becomes active requires a voltage divider from the boost voltage to the HVSEN pin to ground. Equation 14 to Equation 18 show how to set the PWMCNTL pin to activate when the output voltage is within 90% of its nominal value.

$$V_{OUT\_OK} = V_{OUT} \times 0.90 \approx 351 \text{ V} \tag{14}$$

Resistor R_E sets up the high side of the voltage divider and programs the hysteresis of the PWMCNTL signal. For this example, R_E was selected to provide 108 V of hysteresis, as shown in Equation 15.

$$R_E = \frac{\text{Hysteresis}}{36\ \mu\text{A}} = \frac{108\ \text{V}}{36\ \mu\text{A}} = 3\ \text{M}\Omega \tag{15}$$

Resistor R_F is used to program the PWMCNTL active threshold, as shown in Equation 16.

$$R_F = \left(\frac{2.5\ \text{V}}{\frac{V_{OUT\_OK} - 2.5\ \text{V}}{R_E} - 36\ \mu\text{A}} \right) = \frac{2.5\ \text{V}}{\frac{351\ \text{V} - 2.5\ \text{V}}{3\ \text{M}\Omega} - 36\ \mu\text{A}} = 31.185\ \text{k}\Omega \approx 31.6\ \text{k}\Omega \tag{16}$$

This PWMCNTRL output remains active until a minimum output voltage (V_{OUT_MIN}) is reached, as shown in Equation 17.

$$V_{OUT\_MIN} = \frac{2.5\ \text{V}\ (R_E + R_F)}{R_F} = \frac{2.5\ \text{V}\ (3\ \text{M}\Omega + 31.6\ \text{k}\Omega)}{31.6\ \text{k}\Omega} \approx 240\ \text{V} \tag{17}$$

According to the resistor value, the FailSafe OVP threshold should be set according to Equation 18:

$$V_{OV\_FAILSAFE} = \frac{4.87\ \text{V}\ (R_E + R_F)}{R_F} = \frac{4.87\ \text{V}\ (3\ \text{M}\Omega + 31.6\ \text{k}\Omega)}{31.6\ \text{k}\Omega} \approx 467\ \text{V} \tag{18}$$

Output Capacitor Selection

The output capacitor (C_{OUT}) is selected based on holdup requirements as shown in Equation 19.

$$C_{OUT} \geq \frac{2\frac{P_{OUT}}{\eta}\frac{1}{f_{LINE}}}{V_{OUT}^{2} - (V_{OUT\_MIN})^{2}} = \frac{2\frac{300\ W}{0.92}\frac{1}{47\ Hz}}{(390\ V)^{2} - (240\ V)^{2}} \approx 147\ \mu F \tag{19}$$

Two 100-µF capacitors were used in parallel for the output capacitor:

$$C_{OUT} = 200\ \mu F \tag{20}$$

For this size capacitor, the output voltage ripple (V_{RIPPLE}) is approximately 11 V, as shown in Equation 21:

$$V_{RIPPLE} = \frac{2 \times P_{OUT}}{\eta}\frac{1}{V_{OUT} \times 4\pi \times f_{LINE} \times C_{OUT}} = \frac{2 \times 300W}{0.92 \times 390V \times 4\pi \times 47Hz \times 200\,\mu F} \approx 14V \tag{21}$$

In addition to hold-up requirements, a capacitor must be selected so that it can withstand the low-frequency RMS current ($I_{COUT\_100\ Hz}$) and the high-frequency RMS current (I_{COUT_HF}); see Equation 22 to Equation 24. High-voltage electrolytic capacitors generally have both a low- and a high-frequency RMS current rating on the product data sheets.

$$I_{COUT\_100Hz} = \frac{P_{OUT}}{V_{OUT} \times \eta \times \sqrt{2}} = \frac{300\ W}{390\ V \times 0.92 \times \sqrt{2}} = 0.591\ A \tag{22}$$

$$I_{COUT\_HF} = \sqrt{\left(\frac{P_{OUT}\ 2\sqrt{2}}{2 \times \eta \times V_{IN\_MIN}}\sqrt{\frac{4\sqrt{2}\ V_{IN\_MIN}}{9\pi\ V_{OUT}}}\right)^{2} - (I_{COUT\_100\ Hz})^{2}} \tag{23}$$

$$I_{COUT\_HF} = \sqrt{\left(\frac{300\ W \times 2\sqrt{2}}{2 \times 0.92 \times 85\ V}\sqrt{\frac{4\sqrt{2} \times 85\ V}{9\pi \times 390\ V}}\right)^{2} - (0.591\ A)^{2}} \approx 0.966\ A \tag{24}$$

Selecting an R_S for Peak Current Limiting

The UCC28061-Q1 peak limit comparator senses the total input current and is used to protect the MOSFETs during inrush and over-load conditions. For reliability, the peak current limit (I_{PEAK}) threshold in this design is set for 120% of the nominal inrush current that is observed during power-up, as shown in Equation 25.

$$I_{PEAK} = \frac{2P_{OUT}\sqrt{2}\,(1.2)}{\eta \times V_{IN\_MIN}} = \frac{2 \times 300\ W\sqrt{2} \times 1.2}{0.92 \times 85\ V} \approx 13\ A \tag{25}$$

A standard 15-mΩ metal-film current-sense resistor is used for current sensing, as shown in Equation 26. The estimated power loss of the current sense resistor (P_{RS}) is less than 0.25 W during normal operation, as shown in Equation 27.

$$R_S = \frac{200\ mV}{I_{PEAK}} = \frac{200\ mV}{13\ A} \approx 15\ m\Omega \tag{26}$$

$$P_{RS} = \left(\frac{P_{OUT}}{V_{IN\_MIN} \times \eta}\right)^2 R_S = \left(\frac{300\ W}{85\ V \times 0.92}\right)^2 \times 15\ m\Omega \approx 0.22\ W \tag{27}$$

The most critical parameter in selecting a current-sense resistor is the surge rating. The resistor needs to withstand a short-circuit current larger than the current required to open the fuse (F1). I^2t (ampere squared seconds) is a measure of thermal energy resulting from current flow required to melt the fuse, where I^2t is equal to RMS current squared times the duration of the current flow in seconds. A 4-A fuse with an I^2t of 14 A^2s was chosen to protect the design from a short-circuit condition. To ensure the current-sense resistors have a high enough surge protection, a 15-MΩ, 500-mW, metal-strip resistor was chosen for the design. The resistor has a 2.5-W surge rating for 5 seconds. This result translates into 833 A^2s and has a high enough I^2t rating to survive a short-circuit before the fuse opens, as described in Equation 28.

$$I^2t = \frac{2.5\ W}{0.015\ \Omega} \times 5\ s = 833\ A^2s \tag{28}$$

Power Semiconductor Selection (Q1, Q2, D1, D2):

The selection of Q1, Q2, D1, and D2 are based on the power requirements of the design. Application note SLUU138, *UCC38050 100-W Critical Conduction Power Factor Corrected (PFC) Pre-Regulator*, explains how to select power semiconductor components for transition-mode PFC pre-regulators.

The MOSFET maximum-pulsed drain current (Q1, Q2) is shown in Equation 29:

$$I_{DM} \geq I_{PEAK} = 13\ A \tag{29}$$

The MOSFET RMS current calculation (Q1, Q2) is shown in Equation 30:

$$I_{DS} = \frac{I_{PEAK}}{2}\sqrt{\frac{1}{6} - \frac{4\sqrt{2}\,V_{IN\_MIN}}{9\pi \times V_{OUT}}} = \frac{13\ A}{2}\sqrt{\frac{1}{6} - \frac{4\sqrt{2} \times 85\ V}{9\pi \times 390\ V}} \approx 2.3\ A \tag{30}$$

To meet the power requirements of the design, IRFB11N50A 500-V MOSFETs were chosen for Q1 and Q2.

The boost diode RMS current (D1, D2) is shown in Equation 31:

$$I_D = \frac{I_{PEAK}}{2}\sqrt{\frac{4\sqrt{2}\,V_{IN\_MIN}}{9\pi \times V_{OUT}}} = \frac{13\ A}{2}\sqrt{\frac{4\sqrt{2} \times 85\ V}{9\pi \times 390\ V}} \approx 1.4\ A \tag{31}$$

To meet the power requirements of the design, MURS306T3 600-V diodes from On Semiconductor were chosen for the design for D1 and D2.

Brownout Protection

Resistor R_A and R_B are selected to activate brownout protection at 75% of the specified minimum operated input voltage. Resistor R_A programs the brownout hysteresis comparator, which was selected to provide 21 V of hysteresis. R_A and R_B are shown in Equation 32 and Equation 33.

In this design example, brownout becomes active when the input drops below 64 V_{RMS} and deactivates when the input reaches 79 V_{RMS}.

$$R_A = \frac{\text{Hysteresis}}{7\ \mu A} = \frac{21\ V}{7\ \mu A} \approx 3\ M\Omega \tag{32}$$

$$R_B = \frac{1.4\ V \times R_A}{V_{IN\_MIN} \times 0.75\sqrt{2} - 1.4\ V} = \frac{1.4\ V \times 3\ M\Omega}{85\ V \times 0.75\sqrt{2} - 1.4\ V} \approx 47\ k\Omega \tag{33}$$

Converter Timing

Select the timing resistor, R_{TSET}, for the correct on-time (T_{ON}) based on K_{TL}, as shown in Equation 34. To ensure proper operation, the timing must be set based on the highest boost inductance ($L1_{MAX}$). In this design example, the boost inductor could be as high as 390 µH, based on line and load conditions, as shown in Equation 35.

$$f_{MIN} = \frac{\eta \times (V_{IN\_MIN})^2 \left(1 - \frac{V_{IN\_MIN} \times \sqrt{2}}{V_{OUT}}\right)}{P_{OUT} \times L1_{MAX}} = \frac{0.92 \times (85\ V)^2 \left(1 - \frac{85\ V \times \sqrt{2}}{390\ V}\right)}{300\ W \times 390\ \mu H} = 39.2\ kHz \tag{34}$$

$$R_{TSET} = \frac{133\ k\Omega \left(1 - \frac{V_{IN\_MIN} \times \sqrt{2}}{V_{OUT}}\right)}{4.85\ V \times 4\ \mu s \times f_{MIN}} = \frac{133\ k\Omega \left(1 - \frac{85\ V \times \sqrt{2}}{390\ V}\right)}{4.85\ V \times 4\ \mu s \times 39.2\ kHz} \approx 121\ k\Omega \tag{35}$$

This result sets the maximum frequency clamp (f_{MAX}), as shown in Equation 36, which improves efficiency at light load.

$$f_{MAX} = \frac{133\ k\Omega}{2\ \mu s \times R_T} = \frac{133\ k\Omega}{2\ \mu s \times 121\ k\Omega} \approx 550\ kHz \tag{36}$$

Programming V_{OUT}

Resistor R_C is selected to minimize error because of VSENSE input bias current and minimize loading on the power line when the PFC is disabled. Construct resistor R_C from two or more resistors in series to meet high-voltage requirements. R_C was also selected to be of a similar value of R_A and R_E to simplify the bill of materials and reduce design costs.

Based on the resistor values shown in Equation 37 to Equation 39, the primary output over-voltage protection threshold should be as shown in Equation 40:

$$R_C = 3\ M\Omega \tag{37}$$

$$V_{REF} = 6\ V \tag{38}$$

$$R_D = \frac{V_{REF} \times R_C}{(V_{OUT} - V_{REF})} = \frac{6\ V \times 3\ M\Omega}{(390\ V - 6V)} \approx 47\ k\Omega \tag{39}$$

$$V_{OVP} = 6.45\ V\frac{R_C + R_D}{R_D} = 6.45\ V\frac{3\ M\Omega + 47\ k\Omega}{47\ k\Omega} = 418\ V \tag{40}$$

Loop Compensation

Resistor R_Z is sized to attenuate low-frequency ripple to less than 2% of the voltage amplifier output range. This value ensures good power factor and low input current harmonic distortion.

The transconductance amplifier gain is shown in Equation 41:

$$g_m = 96\ \mu S \tag{41}$$

The voltage divider feedback gain is shown in Equation 42 and Equation 43:

$$H = \frac{V_{REF}}{V_{OUT}} = \frac{6\ V}{390\ V} \approx 0.015 \tag{42}$$

$$R_Z = \frac{100\ mV}{V_{RIPPLE} \times H \times g_m} = \frac{100\ mV}{11\ V \times 0.015 \times 96\ \mu S} = 6.313\ k\Omega \approx 6.34\ k\Omega \tag{43}$$

C_Z is then set to add 45° of phase margin at 1/5th of the switching frequency, as shown in Equation 44:

$$C_Z = \frac{1}{2\pi \times \frac{f_{LINE}}{5} \times R_Z} = \frac{1}{2\pi \times \frac{47\ Hz}{5} \times 6.34\ k\Omega} = 2.67\ \mu F \tag{44}$$

C_P is sized to attenuate high-frequency noise, as shown in Equation 45:

$$C_P = \frac{1}{2\pi \times \frac{f_{MIN}}{2} \times R_Z} = \frac{1}{2\pi \times \frac{45\ kHz}{2} \times 6.34\ k\Omega} = 1.12\ nF \tag{45}$$

The standard values of Equation 46 and Equation 47 should be chosen for C_Z and C_P.

$$C_Z = 2.2\ \mu F \tag{46}$$

$$C_P = 1\ nF \tag{47}$$

ADDITIONAL REFERENCES

Related Parts

Table 4 lists several TI parts that have characteristics similar to the UCC28061-Q1.

Table 4. Related Parts

DEVICE	DESCRIPTION
UCC28051	PFC controller for low to medium power applications
UCC28019	8-pin continuous conduction mode (CCM) PFC controller
UCC28060	Natural Interleaving™ Dual-Phase Transition-Mode PFC Controller

References

These references, design tools, and links to additional references, including design software, may be found at www.power.ti.com:

- Evaluation Module, *UCC28060EVM 300W interleaved PFC Pre-regulator*, SLUU280 from Texas Instruments
- Application Note, *UCC38050 100-W Critical Conduction Power Factor Corrected (PFC) Pre-regulator*, SLUU138 from Texas Instruments

Package Outline and Recommended PCB Footprint

The mechanical packages at the end of this data sheet outline the mechanical dimensions of the 16-pin D (SOIC) package and provide recommendations for PCB layout.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC28061QDRQ1	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	28061Q1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

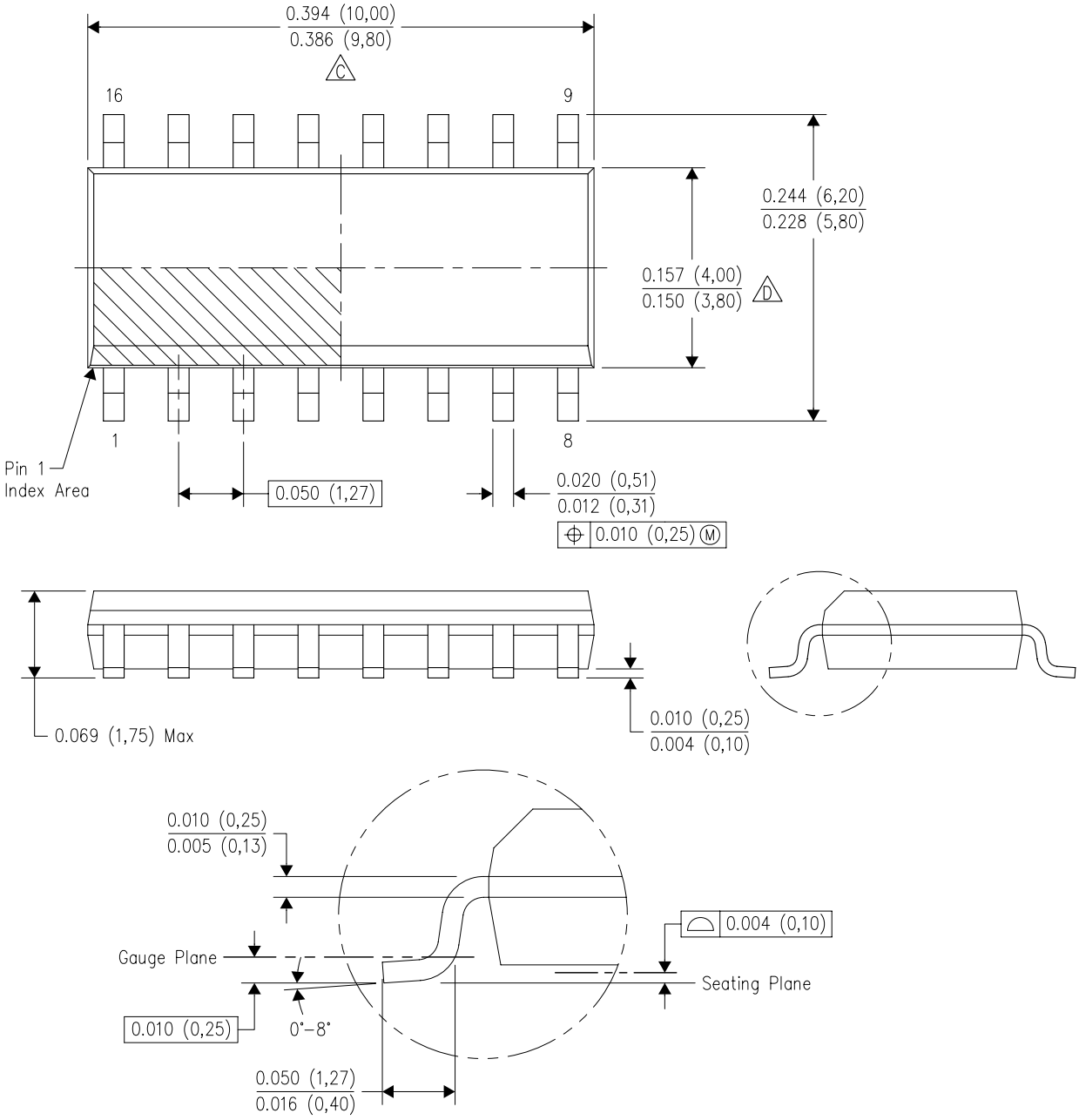
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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