

UCD8220-Q1 数控推挽式模拟脉宽调制 (PWM) 控制器

1 特性

- 具有符合 AEC-Q100 的下列结果：器件从预览变为生产
 - 器件温度 1 级：-40°C 至 125°C 的环境运行温度范围
 - 器件人体模型 (HBM) 静电放电 (ESD) 分类等级 2
 - 器件组件充电模式 (CDM) ESD 分类等级 C4B
- 用于使用 μC 或者 TMS320™ 数字信号处理器 (DSP) 系列的数控电源
- 带有逐周期电流限制的电压或者峰值电流模式控制
- 来自数字控制器的时钟输入设定运行频率和最大占空比
- 模拟 PWM 比较器
- 2MHz 开关频率
- 110V 输入启动电路和热关断 (UCD8620)
- 内部可编程斜率补偿
- 3.3V, 10mA 线性稳压器
- DSP/ μC 兼容输入
- 双 $\pm 4\text{A}$ TrueDrive™ 集成电路高电流驱动器
- 由 2.2nF 电容实现的 10ns 典型上升和下降时间
- 25ns 输入到输出传播延迟
- 25ns 电流感测到输出传播延迟
- 可编程电流限制阈值
- 数字输出电流限制标志
- 4.5V 至 15.5V 电源电压范围

2 应用

- 混合动力汽车/电动汽车 (HEV/EV) 和动力总成
- 数控开关模式电源
- 推挽、半桥、或全桥转换器
- 电池充电器

3 说明

UCD8220-Q1 模拟脉宽调制器 (PWM) 器件适用于采用微控制器或者 TMS320 DSP 系列的数控电源。

UCS8220-Q1 器件是一款配有推挽驱动逻辑的双端 PWM 控制器。

使用 UCD8220-Q1 的系统使用传统模拟方法闭合 PWM 反馈环路，但是 UCD8220-Q1 控制器也包括用于解释一个时域数字连续脉冲信号的电路。这个连续脉冲信号包含用于控制电源操作的运行频率和最大占空比限制。该器件的电路简化了具有高电平控制特性的转换器的实现方式，无需在离散时域中闭合控制环路，因而不会造成额外的复杂性或可能的 PWM 分辨率限制。

UCD8220-Q1 器件可配置为峰值电流模式或电压模式控制。此器件提供了可编程电流限制功能和一个可由主机控制器加以监控的数字输出电流限制标志，用于设定限流操作。为了实现快速开关速度，输出级采用 TrueDrive 输出电路架构，此架构传送 $\pm 4\text{A}$ 的额定电流进入 MOSFET 的栅极。最后，该器件还包括一个 3.3V、10mA 的线性稳压器，该稳压器能够为数字控制器供电或用作系统中的一个基准。

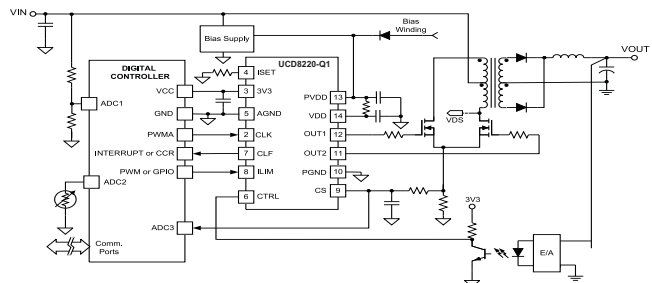
UCD8220-Q1 控制器与 UCD9K 数字电源控制器，DSP，微控制器，或者 ASIC 的 3.3V 标准 I/O 端口兼容并封装在 PowerPAD™ 集成电路散热薄型小尺寸封装 (HTSSOP) 内。

器件信息(1)

器件型号	封装	封装尺寸 (标称值)
UCD8220-Q1	HTSSOP (16)	5.00mm x 4.40mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

UCD8220-Q1 典型简化推挽转换器应用电路原理图



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (July 2014) to Revision C

Page

<ul style="list-style-type: none"> • 已添加 向数据表中添加了以下部分：器件功能模式、应用信息、设计要求、应用曲线、电源建议和布局示例 1 • Changed the <i>Handling Ratings</i> table to <i>ESD ratings</i> and moved the storage temperature into the <i>Absolute Maximum Ratings</i> table 4 	<p>1</p> <p>4</p>
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Changes from Revision A (June 2012) to Revision B

Page

<ul style="list-style-type: none"> • 更新了数据表格式以满足新的 TI 数据表标准 1 • Deleted VIN (input to internal start-up circuitry) from the <i>Pin Functions</i> table 3 • 已添加 the <i>Clearing the Current-Limit Flag (CLF)</i> section 17 	<p>1</p> <p>3</p> <p>17</p>
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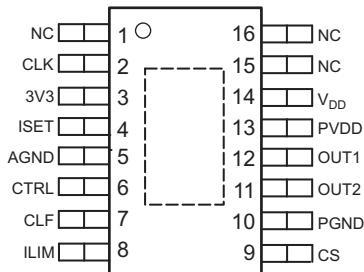
Changes from Original (June 2012) to Revision A

Page

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5 Pin Configuration and Functions

PWP Package
16-Pin HTSSOP With PowerPAD
Top View



NC – No internal connection

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
3V3	3	O	Regulated 3.3-V rail. The onboard linear voltage regulator is capable of sourcing up to 10 mA of current. Place a 0.22- μ F ceramic capacitor from this pin to analog ground.
AGND	5	—	Analog ground return
CLF	7	O	Current-limit flag. When the CS level is greater than the ILIM voltage minus 25 mV, the output driver is forced low and the current-limit flag (CLF) is set high. The CLF signal is latched high until the device receives the next rising edge on the CLK pin. This signal is also used for the start-up handshaking between the digital controller and the analog controller
CLK	2	I	Clock. Input pulse train contains operating frequency and maximum duty cycle limit. This pin is a high impedance digital input capable of accepting 3.3-V logic level signals up to 2 MHz. An internal Schmitt trigger comparator isolates the internal circuitry from any external noise.
CS	9	I	Current sense pin. A fast current-limit comparator connected to the CS pin is used to protect the power stage by implementing cycle-by-cycle current limiting.
CTRL	6	I	Input for the error feedback voltage from the external error amplifier. This input is multiplied by 0.5 and routed to the negative input of the PWM comparator
ILIM	8	I	Current-limit threshold set pin. The current-limit threshold can be set to any value between 0.25 V and 1 V. The default value while open is 0.5 V.
ISET	4	I	Pin for programming the current used to set the amount of slope compensation in peak current-mode control or to set the internal capacitor charging in voltage-mode control.
NC	1	—	No connection.
	15		
	16		
OUT1	12	O	The high-current TrueDrive integrated circuit driver output.
OUT2	11	O	The high-current TrueDrive integrated circuit driver output.
PGND	10	—	Power ground return. This pin should be connected close to the source of the power MOSFET.
PVDD	13	—	Supply pin provides power for the output drivers. This pin is not connected internally to the V_{DD} supply rail. The bypass capacitor for this pin should be returned to PGND.
V_{DD}	14	I	Supply input pin to power the control circuitry. Bypass the pin with a capacitor with a value of at least 4.7 μ F, returned to AGND.

6 Specifications

6.1 Absolute Maximum Ratings⁽¹⁾⁽²⁾

		MIN	MAX	UNIT
Supply voltage, V_{DD}			16	V
Supply current, I_{DD}	Quiescent		20	mA
	Switching, $T_A = 25^\circ\text{C}$, $T_J = 125^\circ\text{C}$, $V_{DD} = 12\text{ V}$		200	
Output gate-drive voltage, V_O	OUTx	-1	PVDD	V
Output gate-drive sink current, $I_{O(\text{sink})}$	OUTx		4	A
Output gate-drive source current, $I_{O(\text{source})}$	OUTx	-4		
Analog input	ISET, CS, CTRL, ILIM	-0.3	3.6	V
Digital I/Os	CLK, CLF	-0.3	3.6	
Continuous total power dissipation		See Thermal Information		
Operating junction temperature range, T_J		-55	150	$^\circ\text{C}$
Lead temperature (Soldering, 10 sec)			300	$^\circ\text{C}$
Storage temperature, T_{stg}		-65	150	$^\circ\text{C}$

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal.

6.2 ESD Ratings

			VALUE	UNIT	
V_{ESD}	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾	± 2000	V	
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 8, 9, and 16)		± 750
			Other pins		± 500

- (1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{DD}	Supply voltage, PVDD	4.5	15.5	V

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		PWP (HTSSOP)	UNIT
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.1	$^\circ\text{C}/\text{W}$
$R_{\theta JC(\text{top})}$	Junction-to-case (top) thermal resistance	29.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	24.2	
Ψ_{JT}	Junction-to-top characterization parameter	1	
Ψ_{JB}	Junction-to-board characterization parameter	24	
$R_{\theta JC(\text{bot})}$	Junction-to-case (bottom) thermal resistance	1.8	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

$V_{DD} = 12\text{ V}$, 4.7- μF capacitor from V_{DD} to AGND, 1 μF from PVDD to PGND, 0.22- μF capacitor from 3V3 to AGND, $T_A = T_J = -40^\circ\text{C}$ to 125°C , (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY SECTION						
Supply current, OFF		$V_{DD} = 4.2\text{ V}$		300	500	μA
Supply current, ON		Outputs not switching, CLK = low	1.6		3	mA
LOW VOLTAGE UNDERVOLTAGE LOCKOUT						
V_{DD} UVLO ON			4.25	4.5	4.75	V
V_{DD} UVLO OFF			4.05	4.25	4.45	V
V_{DD} UVLO hysteresis			150	250	350	mV
REFERENCE / EXTERNAL BIAS SUPPLY						
3V3 initial set point		$T_A = 25^\circ\text{C}$, $I_{LOAD} = 0$	3.267	3.3	3.333	V
3V3 set point over temperature			3.234	3.3	3.366	V
3V3 load regulation		$I_{LOAD} = 1\text{ mA}$ to 10 mA , $V_{DD} = 5\text{ V}$		1	6.6	mV
3V3 line regulation		$V_{DD} = 4.75\text{ V}$ to 12 V , $I_{LOAD} = 10\text{ mA}$		1	6.6	mV
Short circuit current		$V_{DD} = 4.75$ to 12 V	9	20	35	mA
3V3 OK threshold, ON		3.3 V rising	2.9	3.0	3.1	V
3V3 OK threshold, OFF		3.3 V falling	2.7	2.8	2.9	V
CLOCK INPUT (CLK)						
VIT+	HIGH, positive-going input threshold voltage		1.65		2.08	V
VIT-	LOW negative-going input threshold voltage		1.16		1.5	V
(VIT+) – (VIT-)	Input voltage hysteresis		0.6		0.8	V
Frequency		OUTX = 1 MHz			2	MHz
SLOPE COMPENSATION (ISET)						
ISET Voltage		V_{ISET} , 3V3 = 3.3 V, $\pm 2\%$	1.78	1.84	1.90	V
m	V_{SLOPE} (I-Mode)	$R_{ISET} = 6.19\text{ k}\Omega$ to AGND, CS = 0.25 V, CTRL = 2.5 V	1.48	2.12	2.76	V/ μs
		$R_{ISET} = 100\text{ k}\Omega$ to AGND, CS = 0.25 V, CTRL = 2.5 V	0.099	0.142	0.185	
		$R_{ISET} = 499\text{ k}\Omega$ to AGND, CS = 0.25 V, CTRL = 2.5 V	0.019	0.028	0.037	
m	V_{SLOPE} (V-Mode)	$R_{ISET} = 4.99\text{ k}\Omega$ to 3V3, CTRL = 2.5 V	1.44	2.06	2.68	V/ μs
		$R_{ISET} = 100\text{ k}\Omega$ to 3V3, CTRL = 2.5 V	0.068	0.114	0.148	
		$R_{ISET} = 402\text{ k}\Omega$ to 3v3, CTRL = 2.5 V	0.016	0.027	0.035	
ISET resistor range		Current mode control; R_{ISET} connected to AGND	6.19		499	k Ω
ISET resistor range		Voltage mode control; R_{ISET} connected to 3V3	4.99		402	k Ω
ISET current range		Voltage mode control with Feed-Forward; R_{ISET} connected to VIN	3.7		300	μA
PWM						
PWM offset at CTRL input		3V3 = 3.3 V $\pm 2\%$	0.45	0.51	0.6	V
CTRL buffer gain ⁽¹⁾		Gain from CTRL to PWM comparator input		0.5		V/V

(1) Specified by design. Not 100% tested in production.

Electrical Characteristics (接下页)

$V_{DD} = 12\text{ V}$, 4.7- μF capacitor from V_{DD} to AGND, 1 μF from PVDD to PGND, 0.22- μF capacitor from 3V3 to AGND, $T_A = T_J = -40^\circ\text{C}$ to 125°C , (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMIT (ILIM)					
ILIM internal current limit threshold	ILIM = OPEN	0.466	0.5	0.536	V
ILIM maximum current limit threshold	ILIM = 3.3 V	0.975	1.025	1.075	V
ILIM current limit threshold	ILIM = 0.75 V	0.700	0.725	0.750	V
ILIM minimum current limit threshold	ILIM = 0.25 V	0.2	0.23	0.25	V
CLF output high level	CS > ILIM, $I_{LOAD} = -7\text{ mA}$	2.64			V
CLF output low level	CS \leq ILIM, $I_{LOAD} = 7\text{ mA}$			0.66	V
CURRENT SENSE COMPARATOR					
Bias voltage	Includes CS comp offset	5	25	50	mV
Input bias current			-1		μA
CURRENT SENSE DISCHARGE TRANSISTOR					
Discharge resistance	CLK = low, resistance from CS to AGND	10	35	75	Ω
OUTPUT DRIVERS					
Source current ⁽¹⁾	$V_{DD} = 12\text{ V}$, CLK = high, OUTx = 5 V		4		A
Sink current ⁽¹⁾	$V_{DD} = 12\text{ V}$, CLK = low, OUTx = 5 V		4		A
Source current ⁽¹⁾	$V_{DD} = 4.75\text{ V}$, CLK = high, OUTx = 0		2		A
Sink current ⁽¹⁾	$V_{DD} = 4.75\text{ V}$, CLK = low, OUTx = 4.75 V		3		A
Output with $V_{DD} < UVLO$	$V_{DD} = 1.0\text{ V}$, $I_{SINK} = 10\text{ mA}$		0.8	1.2	V

6.6 Timing Requirements

$V_{DD} = 12\text{ V}$, 4.7- μF capacitor from V_{DD} to AGND, 1 μF from PVDD to PGND, 0.22- μF capacitor from 3V3 to AGND, $T_A = T_J = -40^\circ\text{C}$ to 125°C , (unless otherwise noted).

		MIN	NOM	MAX	UNIT	
CLOCK INPUT (CLK)						
Minimum allowable off time ⁽¹⁾				20	ns	
CURRENT LIMIT (ILIM)						
Propagation delay from CLK to CLF	CLK rising to CLF falling after a current limit event		15	25	ns	
CURRENT SENSE COMPARATOR						
Propagation delay from CS to OUTx	ILIM = 0.5 V, measured on OUTx, CS = threshold + 60 mV		25	40	ns	
Propagation delay from CS to CLF	ILIM = 0.5 V, measured on CLF, CS = threshold + 60 mV		25	50		
OUTPUT DRIVERS						
t_R	Rise time	$C_{LOAD} = 2.2\text{ nF}$, $V_{DD} = 12\text{ V}$, See 图 1		10	20	ns
t_F	Fall time	$C_{LOAD} = 2.2\text{ nF}$, $V_{DD} = 12\text{ V}$, See 图 1		10	15	
t_{D1}	Propagation delay from CLK to OUTx, CLK rising	$C_{LOAD} = \text{open}$, $V_{DD} = 12\text{ V}$, See 图 1		25	35	ns
t_{D2}	Propagation delay from CLK to OUTx, CLK falling	$C_{LOAD} = \text{open}$, $V_{DD} = 12\text{ V}$, See 图 1		25	35	

(1) Specified by design. Not 100% tested in production.

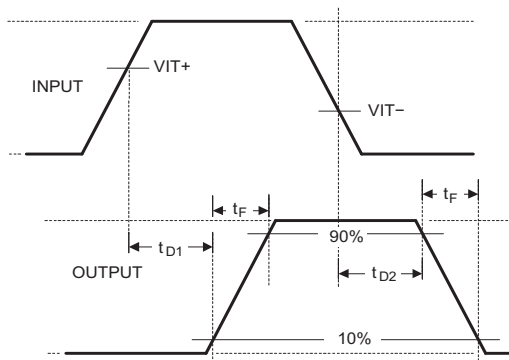


图 1. Timing Diagram

6.7 Typical Characteristics

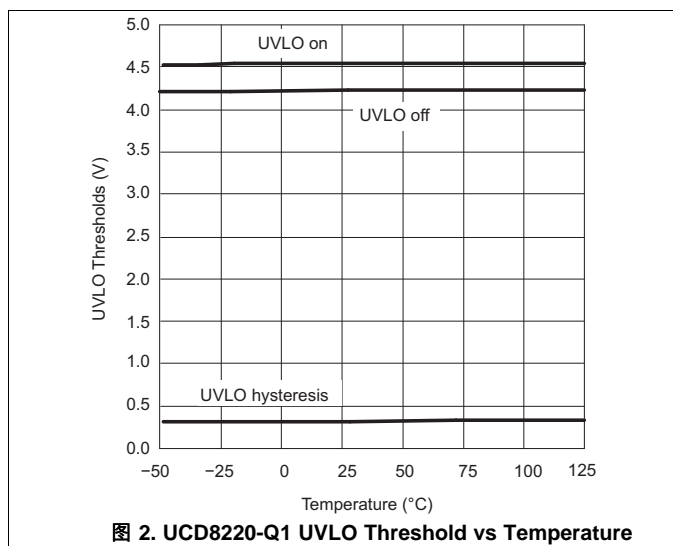


图 2. UCD8220-Q1 UVLO Threshold vs Temperature

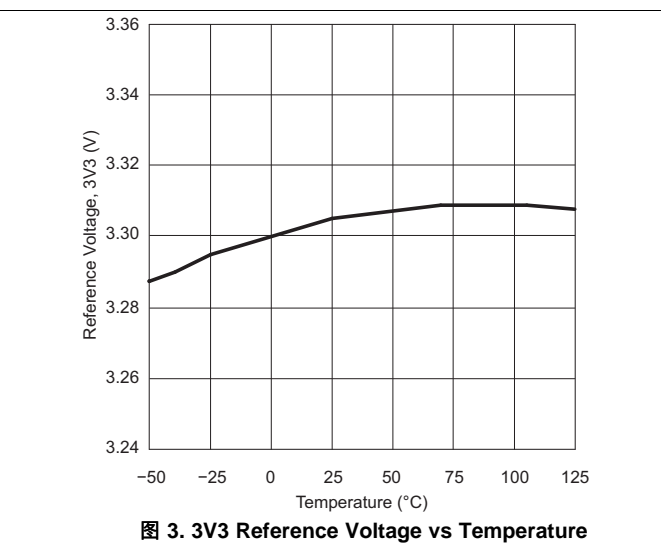


图 3. 3V3 Reference Voltage vs Temperature

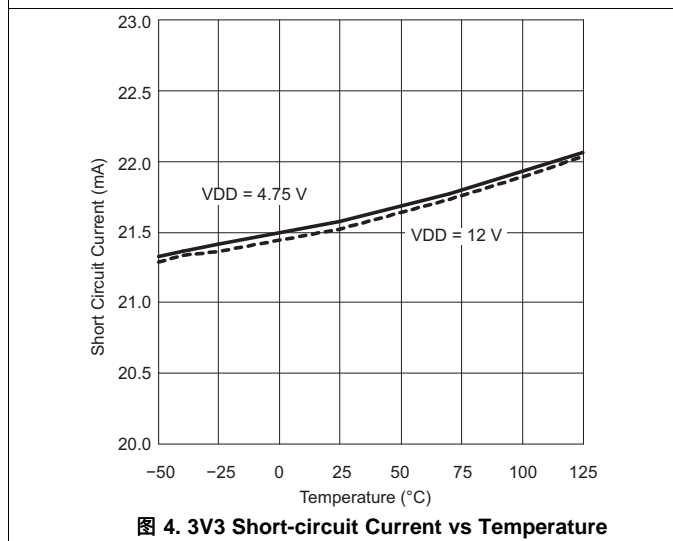


图 4. 3V3 Short-circuit Current vs Temperature

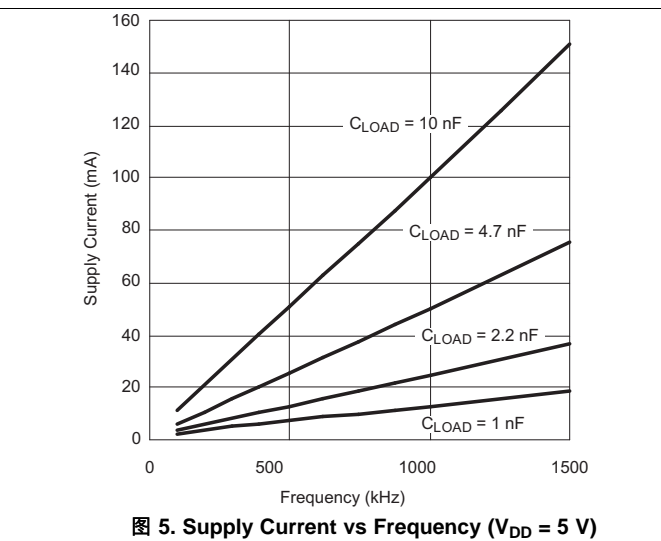


图 5. Supply Current vs Frequency (V_{DD} = 5 V)

Typical Characteristics (接下页)

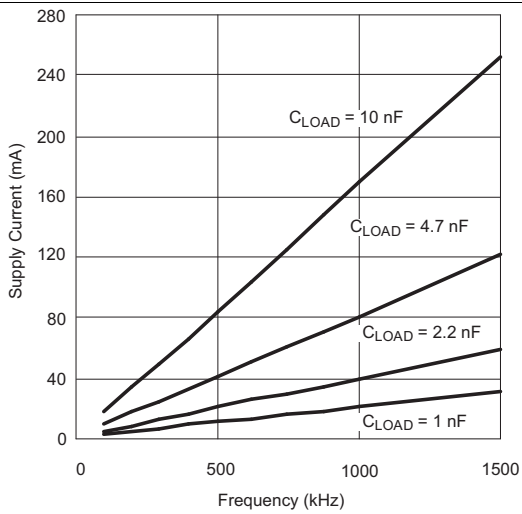


图 6. Supply Current vs Frequency ($V_{DD} = 8\text{ V}$)

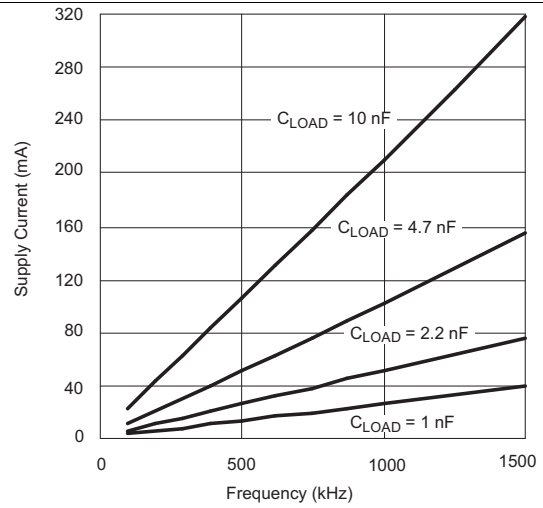


图 7. Supply Current vs Frequency ($V_{DD} = 10\text{ V}$)

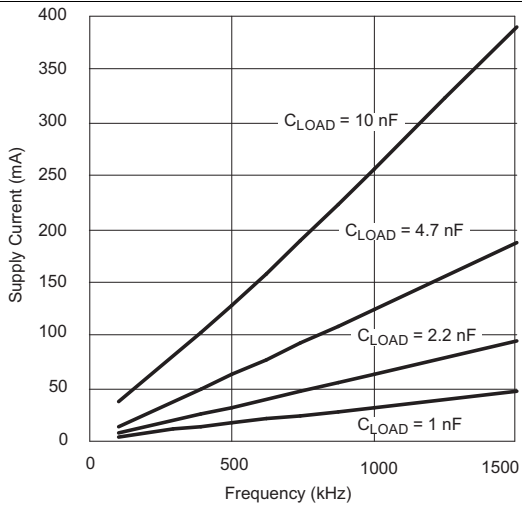


图 8. Supply Current vs Frequency ($V_{DD} = 12\text{ V}$)

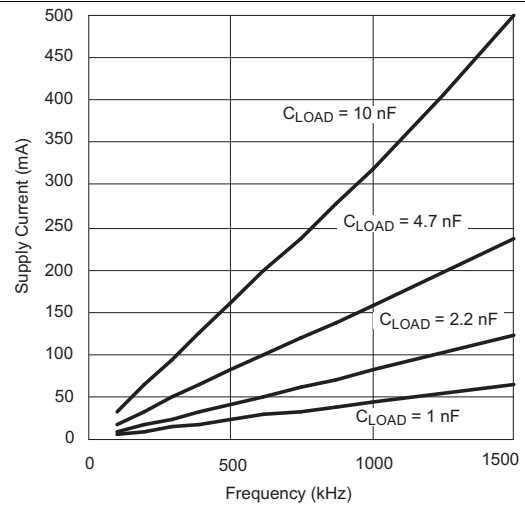


图 9. Supply Current vs Frequency ($V_{DD} = 15\text{ V}$)

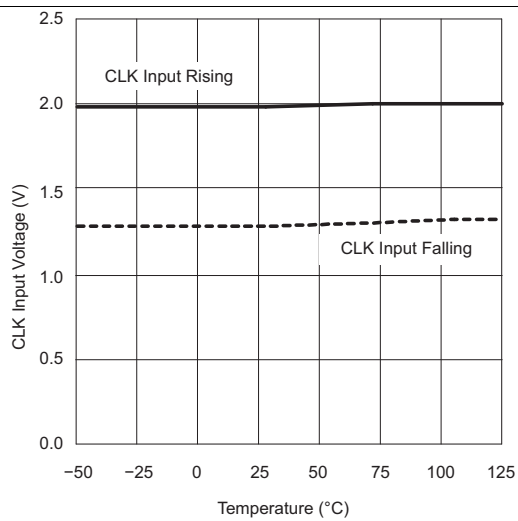


图 10. CLK Input Threshold vs Temperature

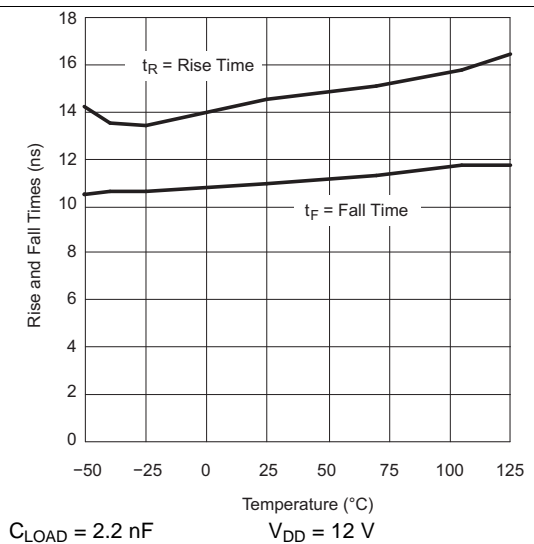


图 11. Output Rise Time and Fall Time vs Temperature

Typical Characteristics (接下页)

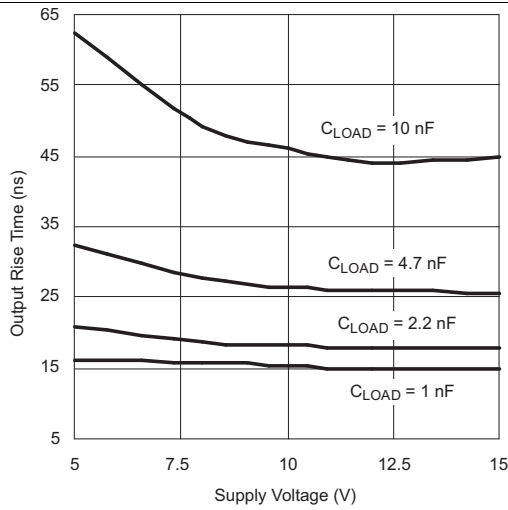


图 12. Output Rise Time vs Supply Voltage

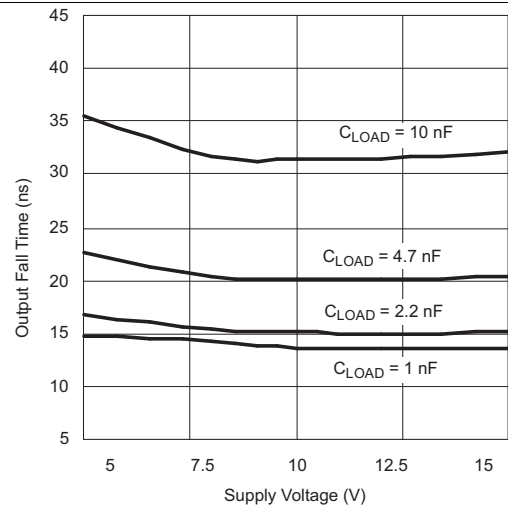


图 13. Output Fall Time vs Supply Voltage

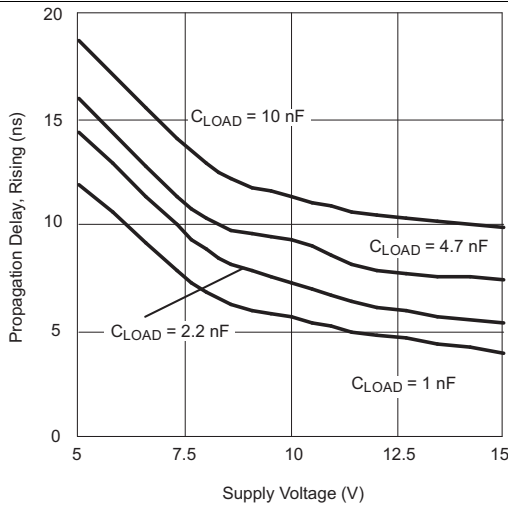


图 14. CLK to OUTx Propagation Delay Rising vs Supply Voltage

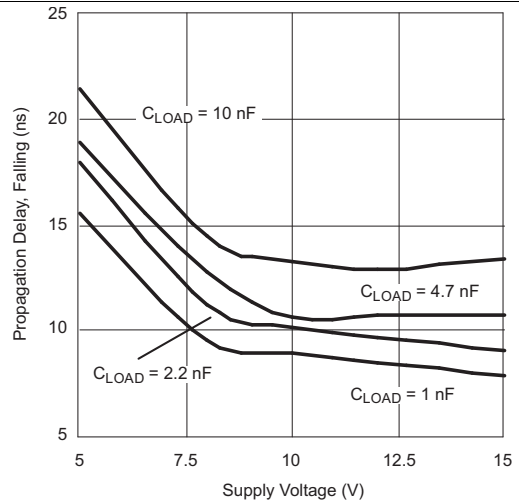


图 15. CLK to OUTx Propagation Delay Falling vs Supply Current

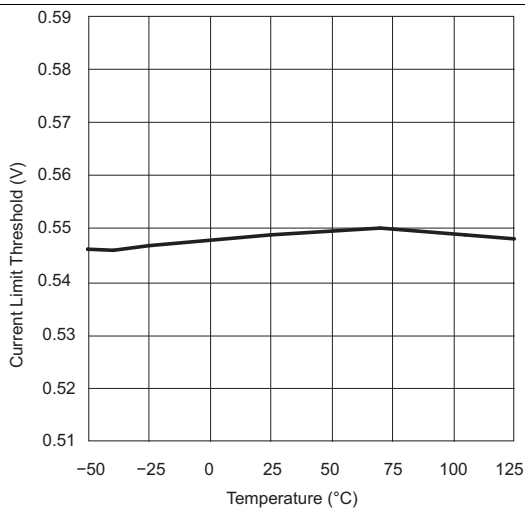


图 16. Default Current Limit Threshold vs Temperature

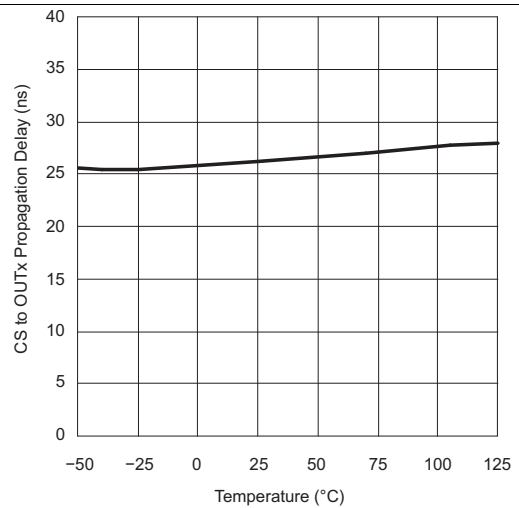


图 17. CS to OUTx Propagation Delay vs Temperature

Typical Characteristics (接下页)

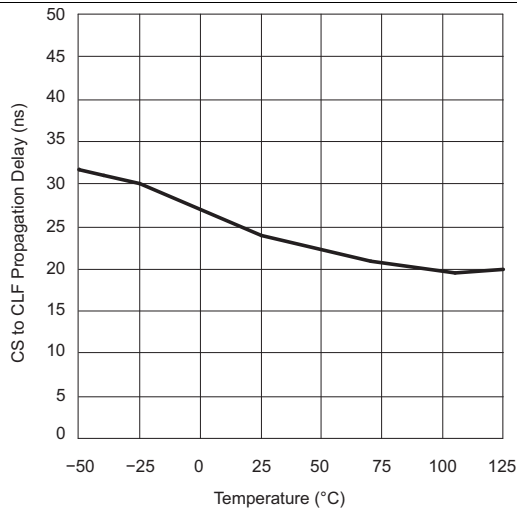


图 18. CS to CLF Propagation Delay vs Temperature

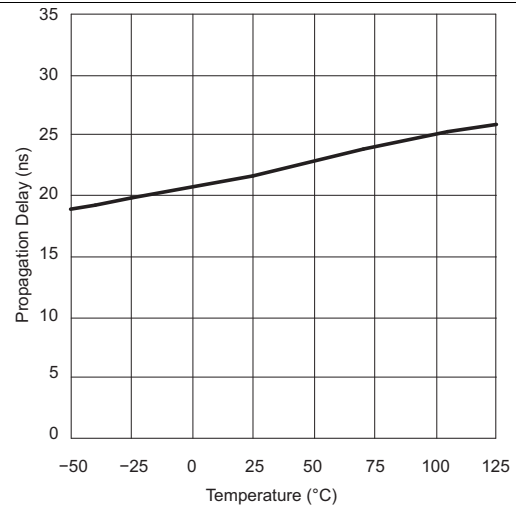
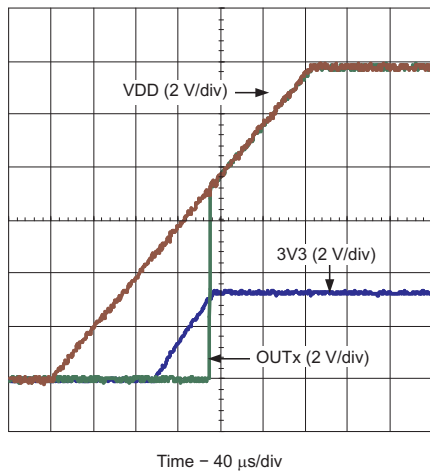
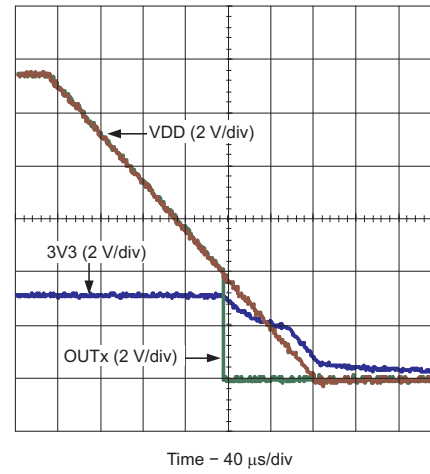


图 19. CLK to OUT Propagation Delay vs Temperature



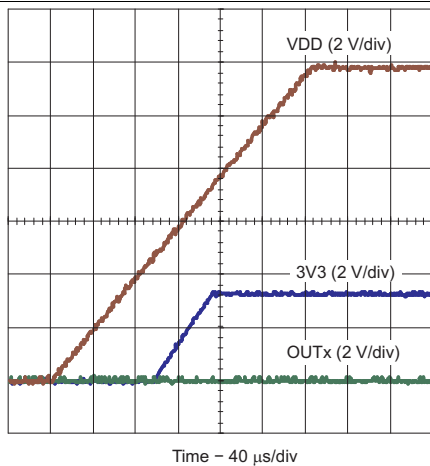
CLK = CTRL = 3V3

图 20. Start-Up Behavior at $V_{DD} = 12\text{ V}$



CLK = CTRL = 3V3

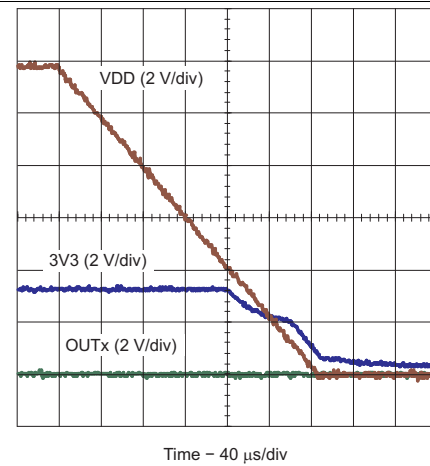
图 21. Shut-Down Behavior at $V_{DD} = 12\text{ V}$



CLK = AGND

CTRL = 3V3

图 22. Start-Up Behavior at $V_{DD} = 12\text{ V}$

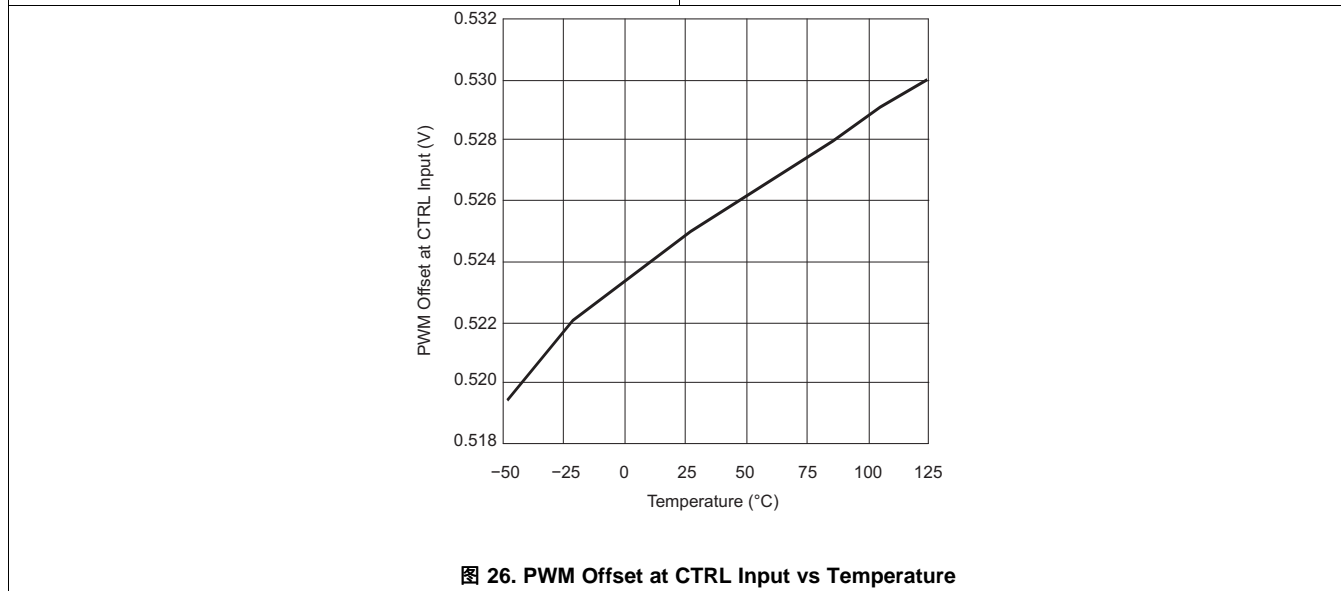
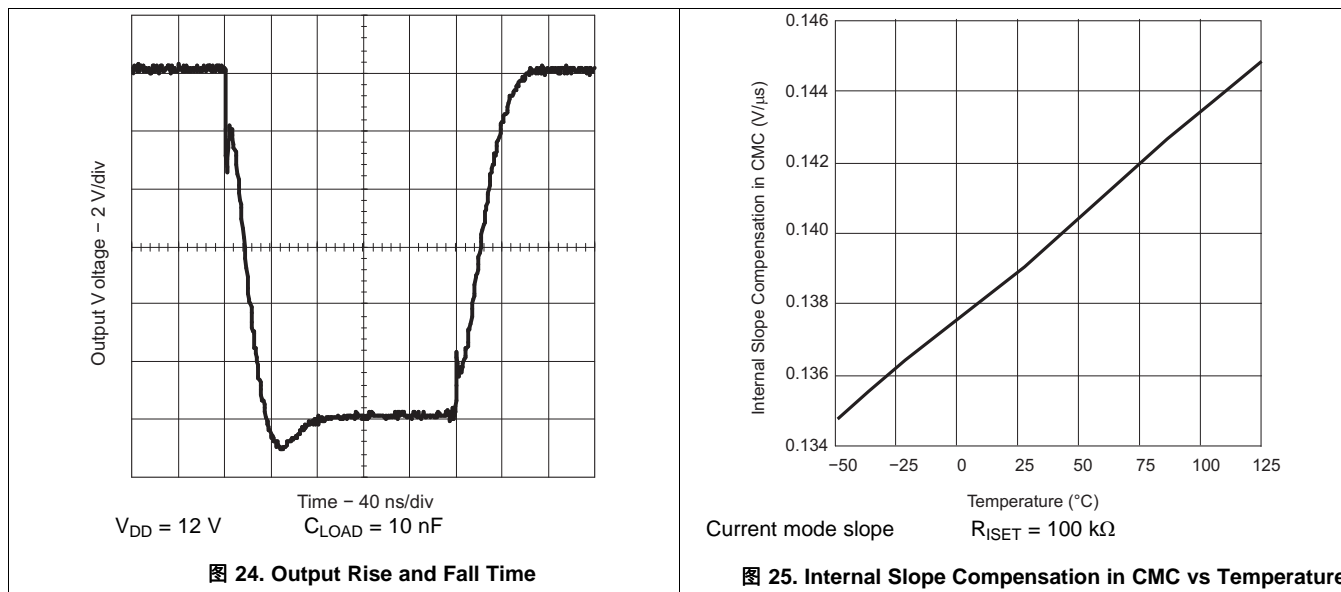


CLK = AGND

CTRL = 3V3

图 23. Shut-Down Behavior at $V_{DD} = 12\text{ V}$

Typical Characteristics (接下页)



7 Detailed Description

7.1 Overview

The UCD8220-Q1 device is a digitally managed analog PWM controller that is configured with push-pull drive logic.

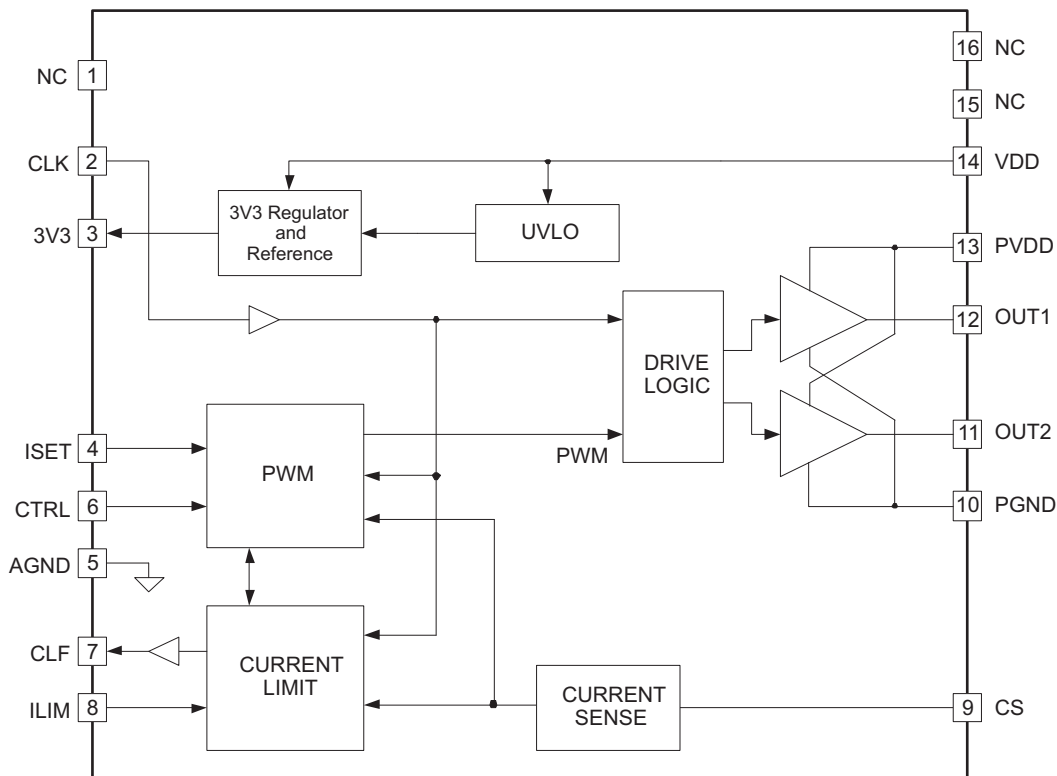
In systems using the UCD8220-Q1 device, the PWM feedback loop is closed using the traditional analog methods. However, the UCD8220-Q1 includes circuitry to interpret a time-domain digital pulse train from a digital controller. The pulse train contains the operating frequency and maximum duty-cycle limit and therefore controls the power supply operation. The device circuitry eases the implementation of a converter with high-level control features without the added complexity or digital PWM-resolution limitations encountered when closing the voltage control-loop in the discrete time domain.

The UCD8220-Q1 device can be configured for either peak current-mode or voltage-mode control. The device provides a programmable current-limit function and a digital output current limit flag which can be monitored by the host controller. For fast switching speeds, the output stages use the TrueDrive output-circuit architecture, which delivers rated current of ± 4 -A into the gate of a MOSFET during the Miller plateau region of the switching transition. Finally the device also includes a 3.3-V, 10-mA linear regulator to provide power for the digital controller.

The UCD8220-Q1 device includes circuitry and features to ease implementing a converter that is managed by a microcontroller or a digital signal processor. Digitally managed power supplies provide software programmability and monitoring capability of the operation of the power supply, including:

- Switching frequency
- Synchronization
- D_{MAX}
- $V \times S$ clamp
- Input UVLO start and stop voltage
- Input OVP start and stop voltage
- Soft-start profile
- Current-limit operation
- Shutdown
- Temperature shutdown

7.2 Functional Block Diagram



7.3 Feature Description

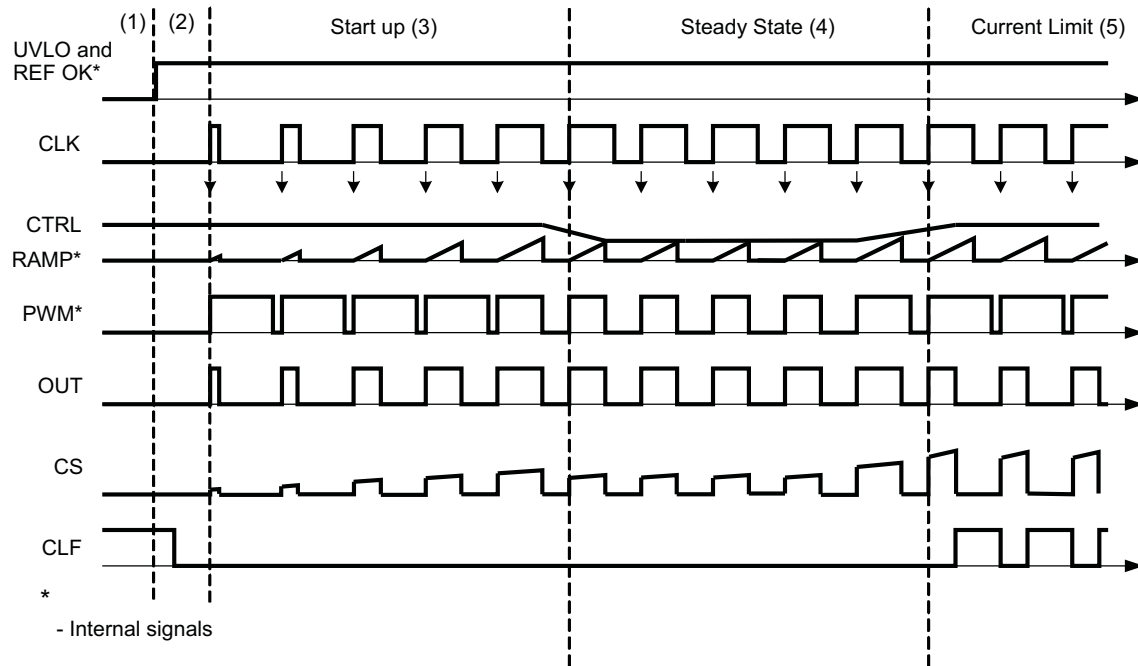
7.3.1 CLK Input Time-Domain Digital Pulse Train

While the loop is closed in the analog domain, the UCD8220-Q1 device is managed by a time-domain digital pulse train from a digital controller. The pulse train, shown as CLK in Figure 27, contains the operating frequency and maximum duty-cycle limit and therefore controls the power supply operation as previously listed. The pulse train uses a Texas Instruments communication protocol which is a proprietary communication system that provides control of the power supply operation through software programming. The rising edge of the CLK signal represents the switching frequency. Figure 27 depicts the operation of the UCD8220-Q1 device in one of five modes. At the time when the internal signal *REF OK* is low, the UCD8220-Q1 device is not ready to accept CLK inputs. When the *REF OK* signal goes high, then the device is ready to process inputs. While the CLK input is low, the outputs are disabled and the CLK signal is used as an enable input. When the digital controller completes the initialization routine and verifies that all voltages are within operating range, then the controller begins the soft-start procedure by slowly ramping up the duty cycle of the CLK signal, while maintaining the desired switching frequency. The CLK duty cycle continues to increase until it reaches steady-state where the analog control loop takes over and regulates the output voltage to the desired set point. During steady state, the duty cycle of the CLK pulse can be set using a volt-second product calculation to protect the primary of the power transformer from saturation during transients.

When the power supply detects an overcurrent event, it enters the current-limit mode where the outputs are quickly turned off and the CLF signal is set high to notify the digital controller that the last power pulse was truncated. This technique is beneficial because it allows the digital controller to decide how to handle this overcurrent event while providing some protection to the other components being supplied by this device.

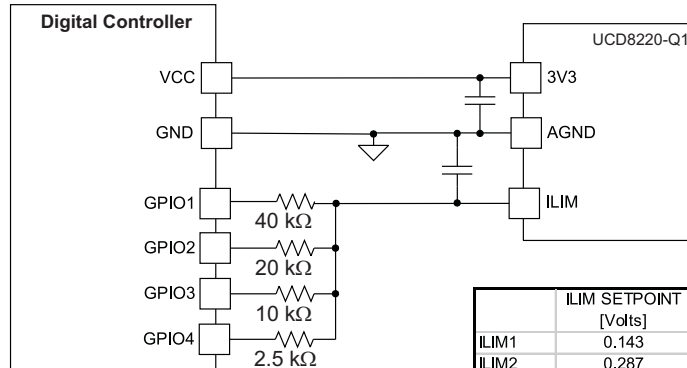
Feature Description (接下页)

The software is now in charge of the response to overcurrent events. In typical analog designs, the power supply response to overcurrent is hardwired in the silicon. With this method, the user can configure the response differently for different applications. For example, the software can be configured to latch-off the power supply in response the first overcurrent event, or to allow a fixed number of current-limit events, so that the supply is capable of starting up into a capacitive load. The user can also configure the supply to enter into *hiccup* mode immediately or after a certain number of current-limit events. As described later in this data sheet, the current limit threshold can be varied in time to create unique current limit profiles. For example, the current limit set point can be set high for a predefined number of cycles to blow a manual fuse, and can be reduced down to protect the system in the event of a faulty fuse.


图 27. Timing and Circuit Operation Diagram

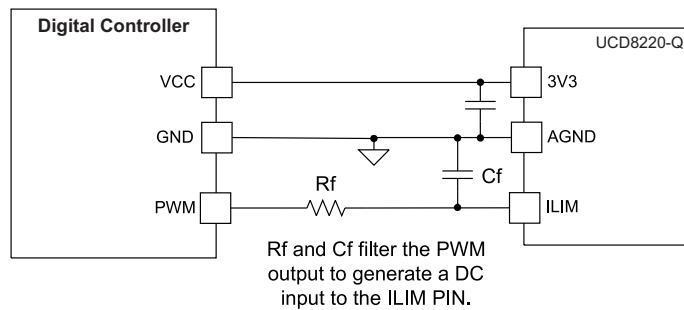
7.3.2 Current Sensing and Protection

a) GPIO outputs

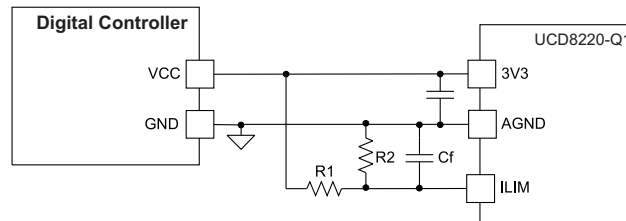


	ILIM SETPOINT [Volts]	GPIO3	GPIO2	GPIO1	GPIO4
ILIM1	0.143	0	0	1	0
ILIM2	0.287	0	1	0	0
ILIM3	0.43	0	1	1	0
ILIM0	0.5	OPEN	OPEN	OPEN	OPEN
ILIM4	0.574	1	0	0	0
ILIM5	0.717	1	0	1	0
ILIM6	0.861	1	1	0	0
ILIM7	1.004	1	1	1	0

b) PWM output



c) Resistor divider



d) Internal set point

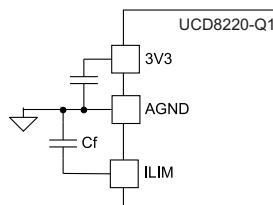


图 28. ILIM Settings

7.3.3 Handshaking

The UCD8220-Q1 device has a built-in handshaking feature to facilitate efficient start-up of the digitally managed power supply. At start-up the CLF flag is held high until all the internal and external supply voltages of the UCD8220-Q1 device is within its operating range. When the supply voltages are within acceptable limits, the CLF flag goes low and the device processes the CLK signals. The digital controller should monitor the CFL flag at start-up and wait for the CLF flag to go low before sending CLK pulses to the UCD8220-Q1 device.

7.3.4 Driver Output

The high-current output stage of the UCD8220-Q1 device is capable of supplying ± 4 -A peak current pulses and swings to both the PVDD and PGND pins.

The drive output uses the TI's TrueDrive output-circuit architecture, which delivers rated current into the gate of a MOSFET when it is most needed, during the Miller plateau region of the switching transition providing efficiency gains.

The TrueDrive integrated circuit consists of pullup and pulldown circuits with bipolar and MOSFET transistors in parallel. The peak output current rating is the combined current from the bipolar and MOSFET transistors. This hybrid output stage also allows efficient current sourcing at low supply voltages.

7.3.5 Source and Sink Capabilities During Miller Plateau

Large power MOSFETs present a large load to the control circuitry. Proper drive is required for efficient, reliable operation. The UCD8220-Q1 driver has been optimized to provide maximum drive to a power MOSFET during the Miller plateau region of the switching transition. This interval occurs while the drain voltage is swinging between the voltage levels dictated by the power topology, requiring the charging or discharging of the drain-gate capacitance with current supplied or removed by the driver device. See (5) in the [相关文档](#) section.

7.3.6 Drive Current and Power Requirements

The UCD8220-Q1 device contains drivers that can deliver high current into a MOSFET gate for a period of several hundred nanoseconds. High-peak current is required to turn on a MOSFET. To turn off a MOSFET, the driver is required to sink a similar amount of current to ground. This cycle repeats at the operating frequency of the power device.

For additional information on the current required to drive a power MOSFET and other capacitive-input switching devices, see (5) in the [相关文档](#) section.

When a driver device is tested with a discrete, capacitive load, calculating the power that is required from the bias supply is fairly simple. Use [公式 1](#) to calculate the energy that must be transferred from the bias supply to charge the capacitor.

$$E = \frac{1}{2} \times CV^2$$

where

- C is the load capacitor
 - V is the bias voltage feeding the driver
- (1)

An equal amount of energy is transferred to ground when the capacitor is discharged. This transfer of energy results in a power loss which is calculated with [公式 2](#).

$$P = CV^2 \times f$$

where

- f is the switching frequency
- (2)

This power is dissipated in the resistive elements of the circuit. Thus, with no external resistor between the driver and gate, this power is dissipated inside the driver. Half of the total power is dissipated when the capacitor is charged, and the other half is dissipated when the capacitor is discharged.

Use 公式 3 to calculate the power loss with the following values: $V_{DD} = 12\text{ V}$, $C_{LOAD} = 2.2\text{ nF}$, and $f = 300\text{ kHz}$.

$$P = 2.2\text{ nF} \times 12^2 \times 300\text{ kHz} = 0.095\text{ W} \quad (3)$$

Use 公式 4 to calculate the current with a 12-V supply.

$$I = \frac{P}{V} = \frac{0.095\text{ W}}{12\text{ V}} = 7.9\text{ mA} \quad (4)$$

7.3.7 Clearing the Current-Limit Flag (CLF)

In the UCD8220-Q1 design, the CLF signal is cleared by the comparator (compares the voltage between the CS and ILIM pins) output. However, the comparator output is enabled by the OUTx pin. Therefore, the CLF signal does not clear (go low) unless one or both OUTx pins are on, which enables the comparator output. Pulling the CTRL pin high turns the OUTx pin on which is why the CLF flag only clears when CTRL is high (greater than 0.45 to 0.6 V). Therefore, anything that turns on the OUTs pins enables the comparator, and if V_{CS} is less than V_{ILIM} , the comparator output clears the CLF signal. The CLF signal goes low during the next rising edge on the CLK pin after these conditions are met.

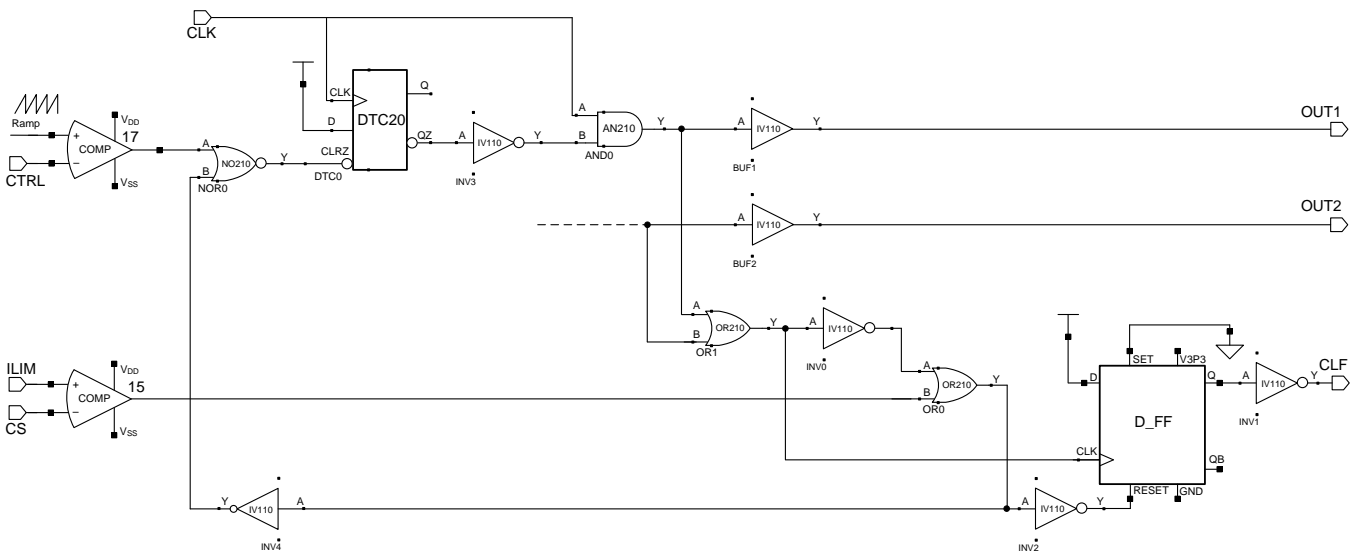


图 29. Logic Circuit for CLF

7.4 Device Functional Modes

The device has no additional functional modes.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The UCD8220-Q1 device can be configured for either peak current mode or voltage mode control. The device can be used to implement a variety of applications such as push-pull, half-bridge, or full-bridge converter.

8.2 Typical Application

Using the UCD8220-Q1 device in an application, a high degree of digital control can be achieved because the device integrates the PWM, logic, error amplifier, current limit, and drivers. In addition, the on-chip regulator provides power to the microcontroller. An example application is using the device in half-bridge power topology.

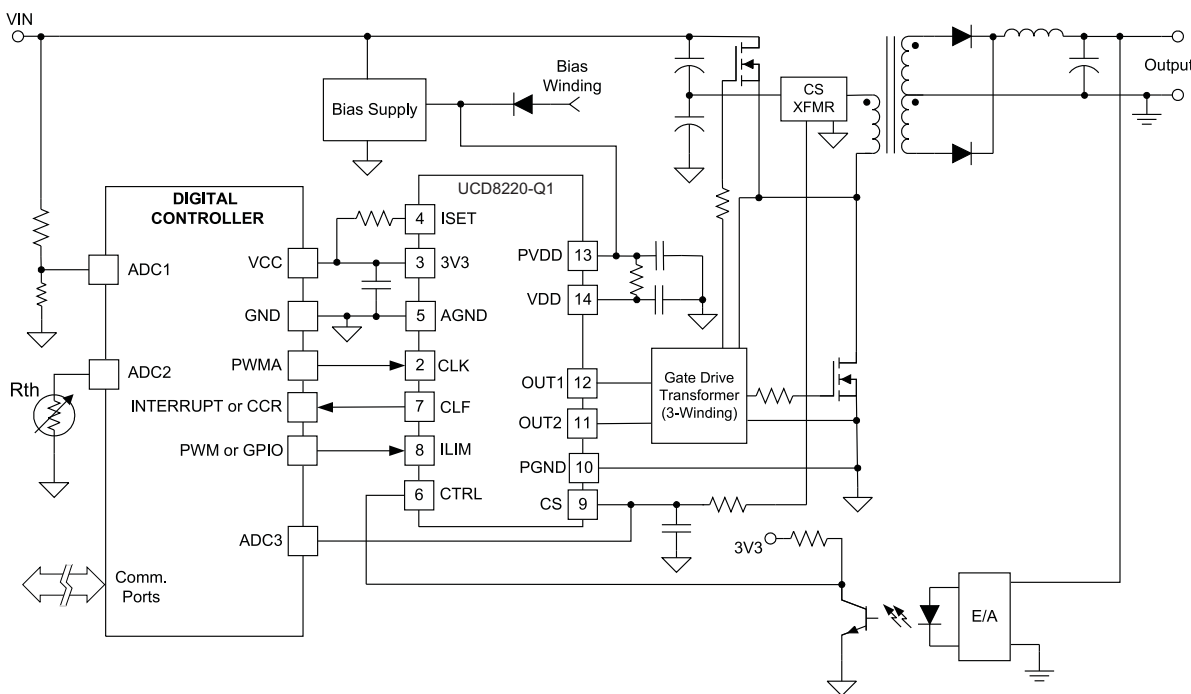


图 30. UCD8220-Q1 Typical Simplified Half-Bridge Converter Application Schematic

8.2.1 Design Requirements

When designing a half-bridge system, the key requirement is determining which functions should remain in the digital domain rather than the analog domain. The design shown in 图 30 allows for a high degree of control over various blocks such as PWM, logic, error amplifier, current limit, and drivers. The UCD8220-Q1 closes the control loop for the power supply and provides the loop compensation. During operation, the UCD8220-Q1 monitors current and terminates the switching cycle safely if the value exceeds the current limit. By performing this task in the UCD8220-Q1, the device assists in real-time and full-time safety. The UCD8220-Q1 device provides notification of overcurrent events to the microcontroller. The notification of overcurrent events to the microcontroller allows the microcontroller to have a more complex response strategy. The firmware can, for example, direct the system to tolerate a finite number of current events, go to soft-stop, or shut down.

Typical Application (接下页)

8.2.2 Detailed Design Procedure

Current limit is set through a simple resistor divider at the ISET pin. In the case of an overcurrent limit, the UCD8220-Q1 device sets the current flag (CF) pin high and the device is turned off by the host controller if the current limit exceeds a certain number of cycles. Depending upon the control method, the ISET resistor can be selected as previously mentioned.

8.2.2.1 Selecting the ISET Resistor for Voltage Mode Control

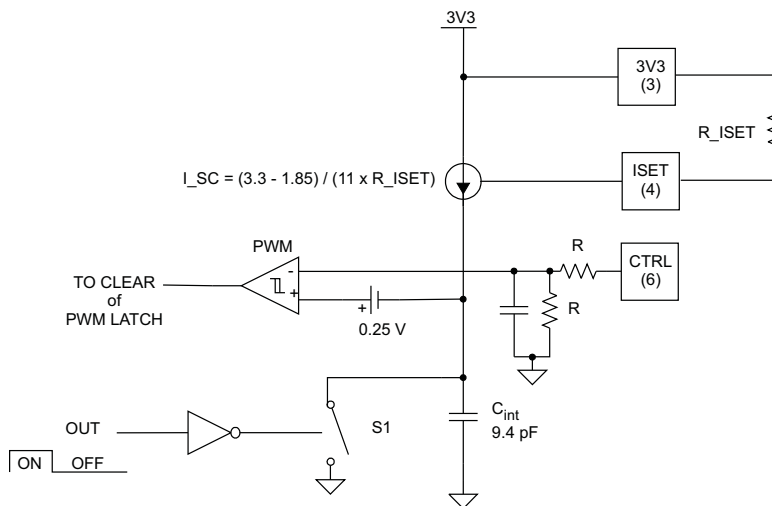


图 31. UCD8220-Q1 Configured in Voltage Mode Control With an Internal Timing Capacitor

When the ISET resistor is configured as shown in 图 31 with the ISET resistor connected between the ISET pin and the 3V3 pin, the device is set up for voltage mode control. For purposes of voltage loop compensation the, voltage ramp is 1.4 V from the valley to the peak. Use 公式 5 to calculate the proper resistance for a desired clock frequency.

$$R_{ISET} = \frac{(3.3 - 1.85) \times 10^{12}}{11 \times 1.4 \times f_{clk} \times 9.4} \Omega$$

where

- fclk = desired clock frequency in Hz (5)

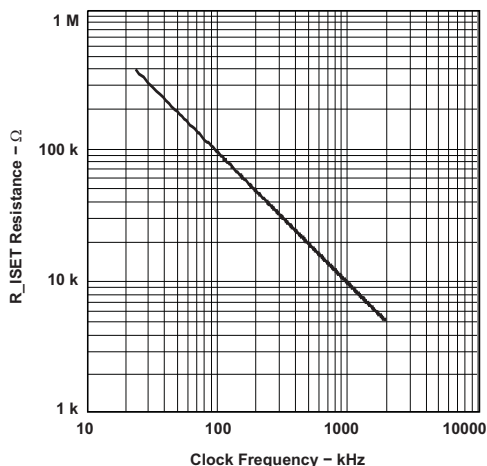


图 32. ISET Resistance Versus Clock Frequency

Typical Application (接下页)

图 32 显示了用于所需时钟频率的电阻的标称值。例如，1000 kHz 的时钟频率将需要 10 kΩ 的 ISET 电阻。UCD8220-Q1 器件具有两个由推挽逻辑控制的输出，因此输出纹波频率等于时钟频率，且每个输出开关在时钟频率的一半处切换。

8.2.2.2 Selecting the ISET Resistor for Voltage Mode Control with Voltage Feed Forward

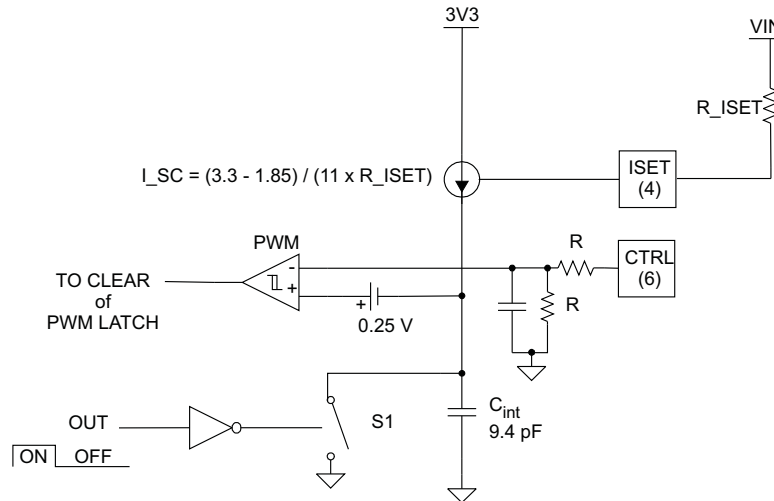


图 33. UCD8220-Q1 配置在电压模式控制带电压前馈

当 ISET 电阻器如图 33 所示配置，将 ISET 电阻器连接在 ISET 引脚和输入电压，VIN 之间，该器件配置为电压模式控制带电压前馈。对于电压环路补偿的目的，电压斜坡为 $1.4 \text{ V} \times \text{VIN} / \text{VIN}_{\text{max}}$ 从谷到峰。使用公式 6 来计算所需的电阻器，用于所需的时钟频率和输入电压范围。

$$R_{\text{ISET}} = \frac{(\text{Vin}_{\text{max}} - 1.85) \times 10^{12}}{11 \times 1.4 \times \text{fclk} \times 9.4} \Omega$$

where

- fclk = Desired Clock Frequency in Hz (6)

For a general discussion of the benefits of voltage mode control with voltage feed forward, see (5) in the 相关文档 section.

Typical Application (接下页)

8.2.2.3 Selecting the ISET Resistor for Peak Current Mode Control with Internal Slope Compensation

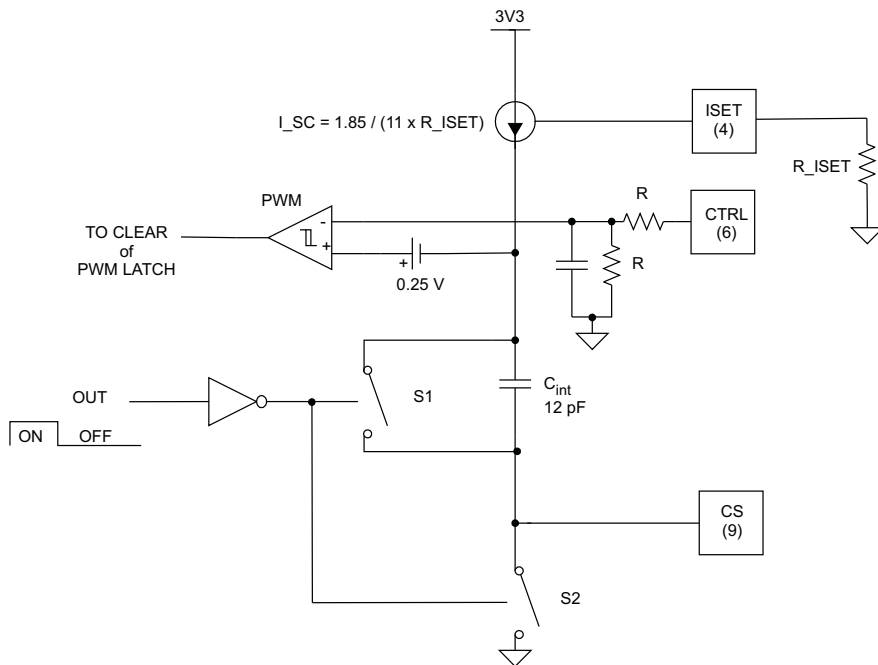


图 34. UCD8220-Q1 Configured in Peak Current Control with Internal Slope Compensation

When the ISET resistor is configured as shown in 图 34 with the ISET resistor connected between the ISET pin and the AGND pin, the device is configured for peak current-mode control with internal slope compensation. The voltage at the ISET pin is 1.85 V so the internal slope compensation current, I_{SC} , being fed into the internal slope compensation capacitor is equal to $1.85 / (11 \times R_{ISET})$. Use 公式 7 to calculate the voltage slope at the PWM comparator input which is generated by this current.

$$SLOPE = \frac{1.85 \times 10^6}{11 \times R_{ISET} \times 12} \text{ V}/\mu\text{s} \tag{7}$$

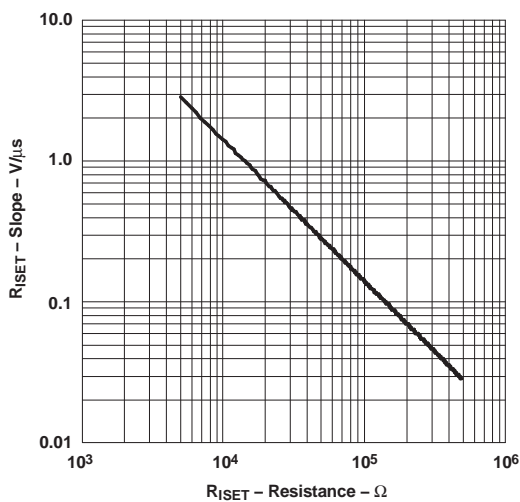
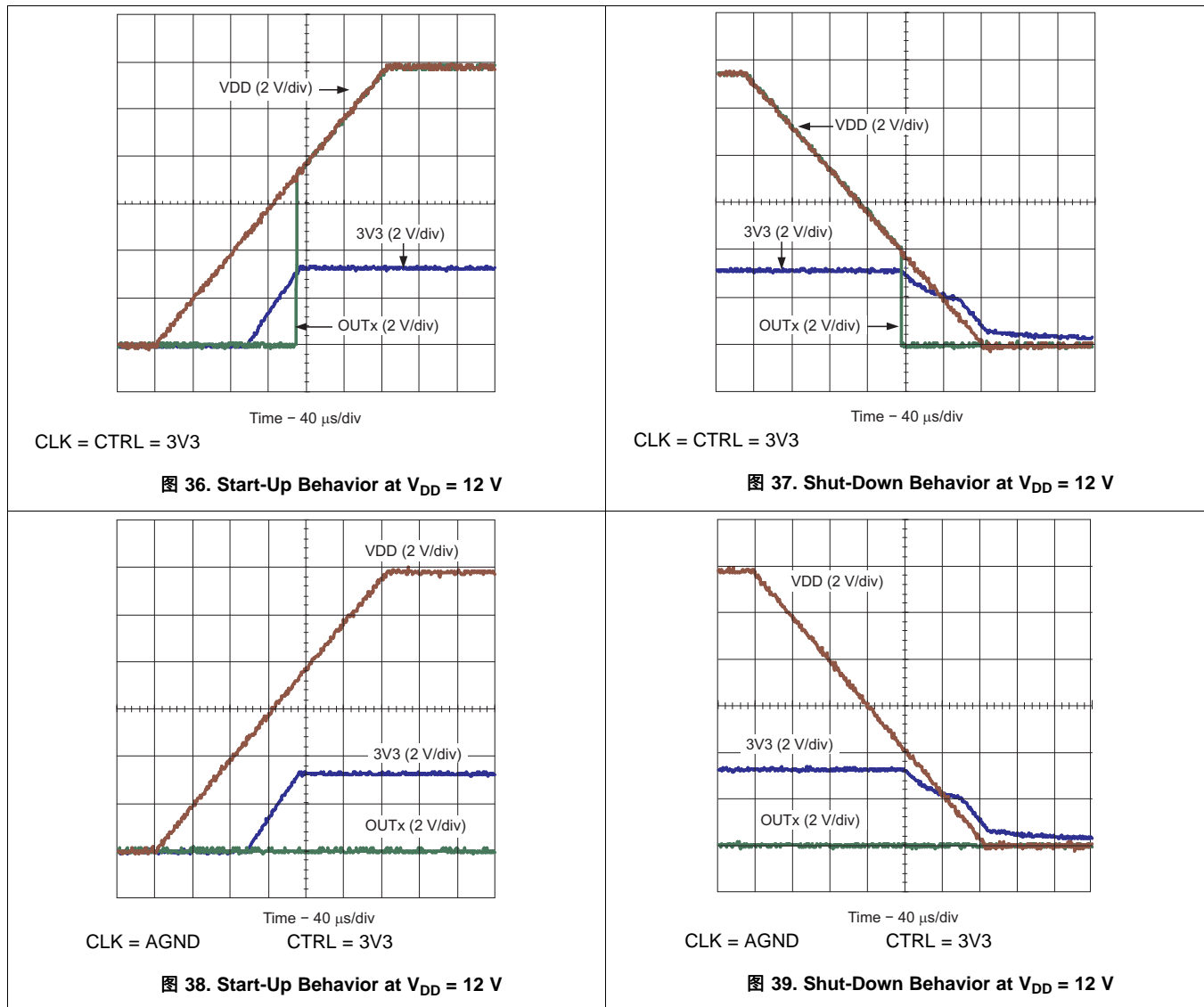


图 35. Slope vs R_ISET Resistance

Typical Application (接下页)

The amount of slope compensation required depends on the design of the power stage and the output specifications. A general rule is to add an up-slope equal to the down slope of the output inductor. Refer to (1) and (8) in the [相关文档](#) section for a more detailed discussion regarding slope compensation in peak current mode controlled power stages.

8.2.3 Application Curves



9 Power Supply Recommendations

The UCD8220-Q1 device operates from an input supply voltage range from 4.5 V to 15.5 V. Ensure that the power supply rail is clean and uses high quality ceramic decoupling capacitors.

10 Layout

10.1 Layout Guidelines

In a MOSFET driver operating at high frequency, minimizing stray inductance to minimize overshoot, undershoot, and ringing is critical. The low output impedance of the drivers produces waveforms with high di/dt which tends to induce ringing in the parasitic inductances. Connecting the driver device close to the MOSFETs is advantageous. To reduce ringing, minimize the trace inductance from OUT 1 and OUT 2 to the MOSFET input. Connecting the PGND and AGND pins to the PowerPAD integrated circuit package with a thin trace is recommended. Ensuring that the voltage potential between these two pins does not exceed 0.3 V is critical. The use of schottky diodes on the outputs to the PGND and PVDD is recommended when driving gate transformers. See (3) in the [相关文档](#) section for a description of proper pad layout for the PowerPAD integrated circuit package.

10.2 Layout Example

- Minimize these traces
- Ground trace

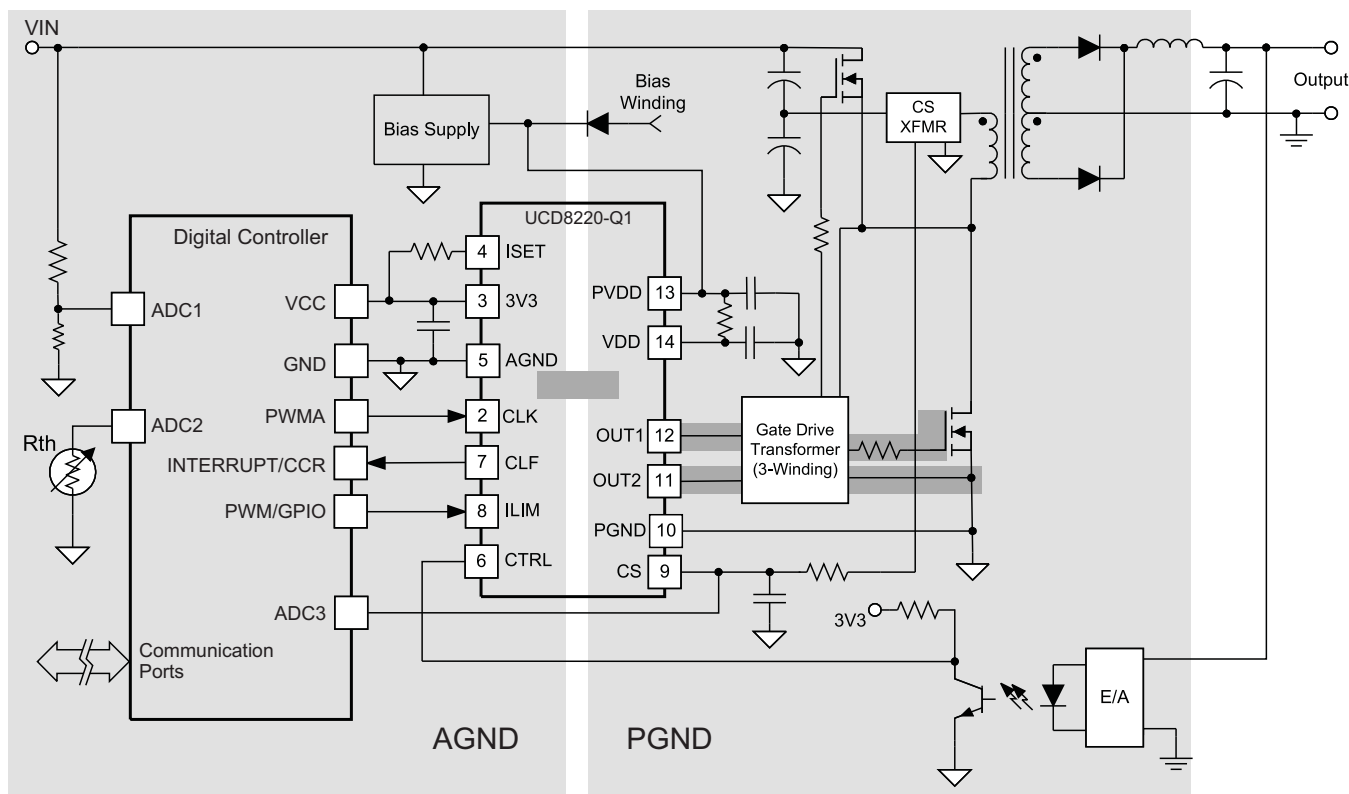


图 40. UCD8220-Q1 Layout Example

10.3 Thermal Considerations

The useful range of a driver is greatly affected by the drive power requirements of the load and the thermal characteristics of the device package. In order for a power driver to be useful over a particular temperature range the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The UCD8220-Q1 device is available in the PowerPAD integrated circuit package, HTSSOP, to cover a range of application requirements. The package has an exposed pad to enhance thermal conductivity from the semiconductor junction.

As shown in (4) in the [相关文档](#) section, the PowerPAD integrated circuit packages offer a leadframe die pad that is exposed at the base of the package. This pad is soldered to the copper on the PC board (PCB) directly underneath the device package, reducing the $R_{\theta JA}$ down to 37.47°C/W. The PC board must be designed with thermal lands and thermal vias to complete the heat removal subsystem, as discussed in (3) in the [相关文档](#) section.

Note that the PowerPAD integrated circuit package is not directly connected to any leads of the package. However, the PowerPAD is electrically and thermally connected to the substrate which is the ground of the device. The PowerPAD integrated circuit package should be connected to the quiet ground of the circuit.

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档：

- (1) 《电流模式转换器的建模、分析和补偿》，[SLUA101](#)
- (2) 《MSP430F1232、MSP430x11x2、MSP430x12x2 混合信号微控制器》，[SLAS361](#)
- (3) 《PowerPAD 速成》，[SLMA004](#)
- (4) 《PowerPAD 耐热增强型封装》，[SLMA002](#)
- (5) SEM-300 电源研讨会主题 2，《闭合反馈环路》，[SLUP068](#)
- (6) SEM-1400 电源研讨会主题 2：《高速 MOSFET 栅极驱动电路设计 and 应用指南》，[SLUP133](#)
- (7) SEM-1600 电源主题研讨会主题 6：《数字电源控制实用简介》，[SLUP224](#)
- (8) 《电流模式电源的实际问题》，[SLUA110](#)

11.2 商标

TMS320, TrueDrive, PowerPAD are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCD8220QPWPRQ1	ACTIVE	HTSSOP	PWP	16	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	UC8220Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCD8220QPWPRQ1	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

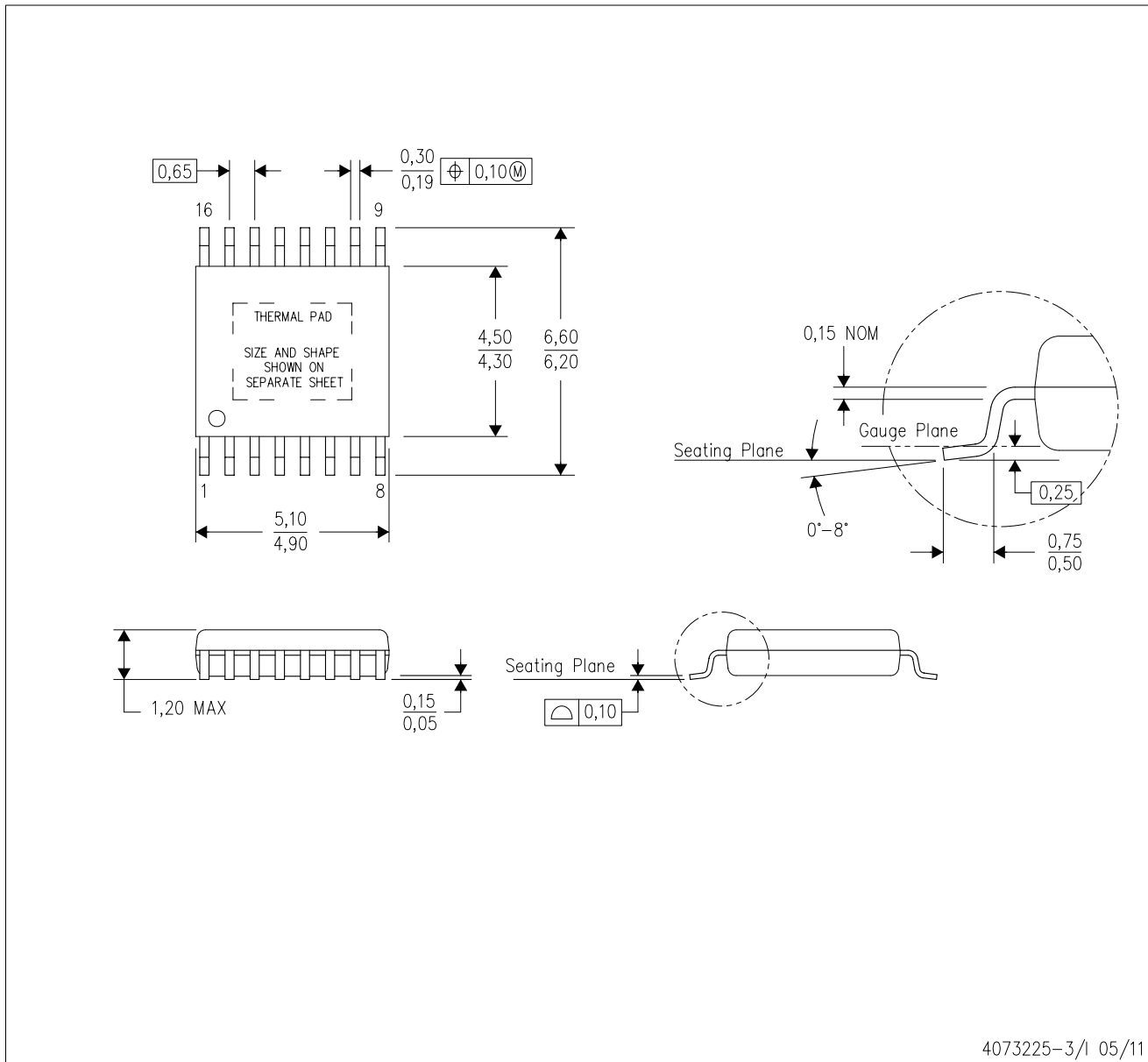
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCD8220QPWPRQ1	HTSSOP	PWP	16	2000	350.0	350.0	43.0



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

PWP (R-PDSO-G16)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

THERMAL PAD MECHANICAL DATA

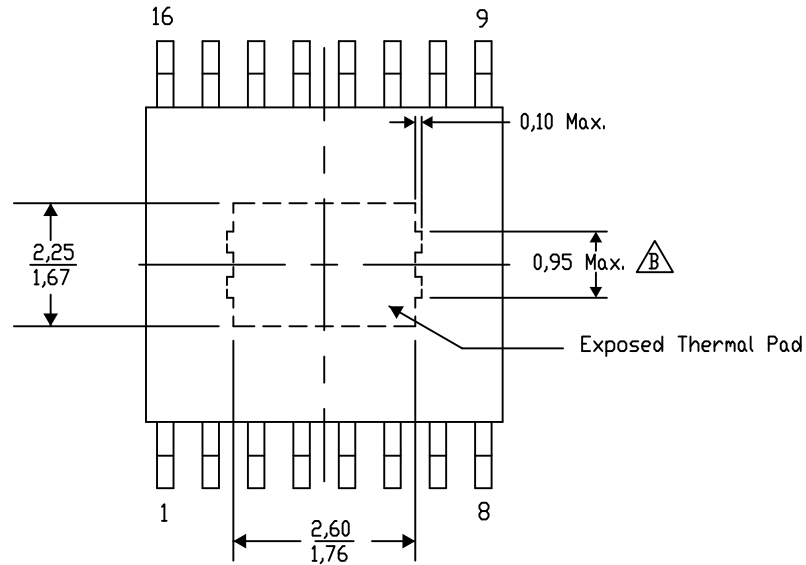
PWP (R-PDSO-G16) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332-12/AO 01/16

NOTE: A. All linear dimensions are in millimeters

$\triangle B$ Exposed tie strap features may not be present.

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PWP0016J



PACKAGE OUTLINE

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4223595/A 03/2017

NOTES:

PowerPAD is a trademark of Texas Instruments.

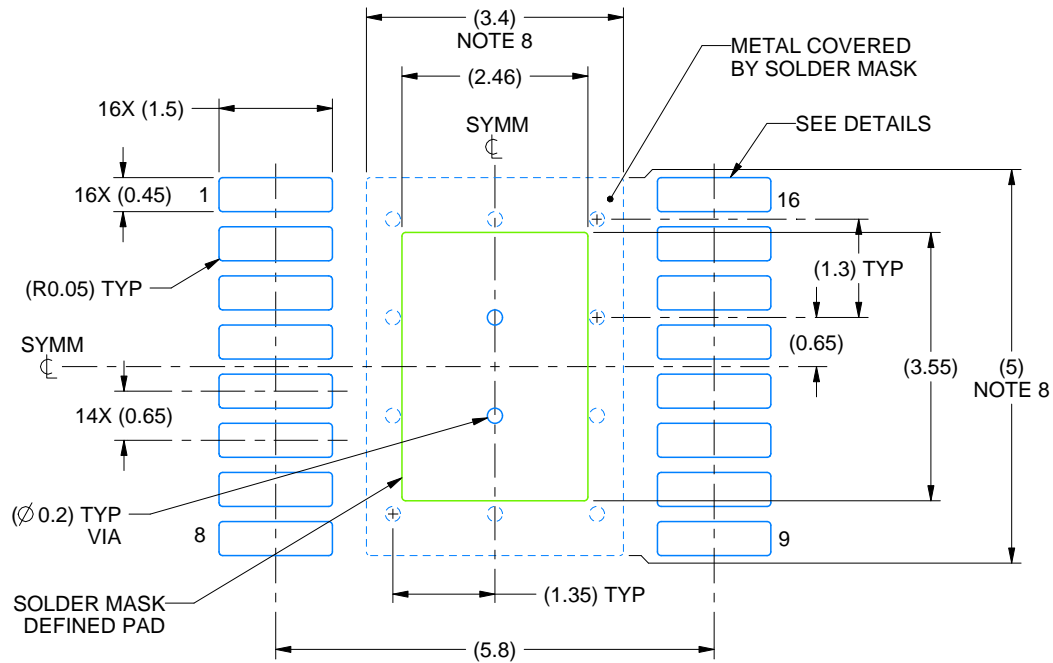
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

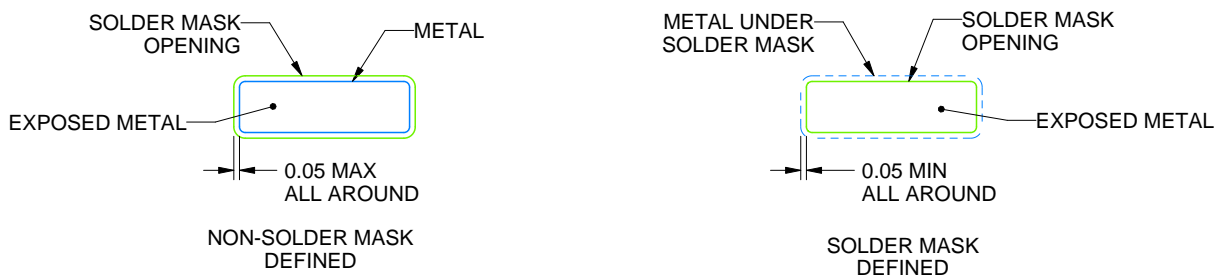
PWP0016J

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4223595/A 03/2017

NOTES: (continued)

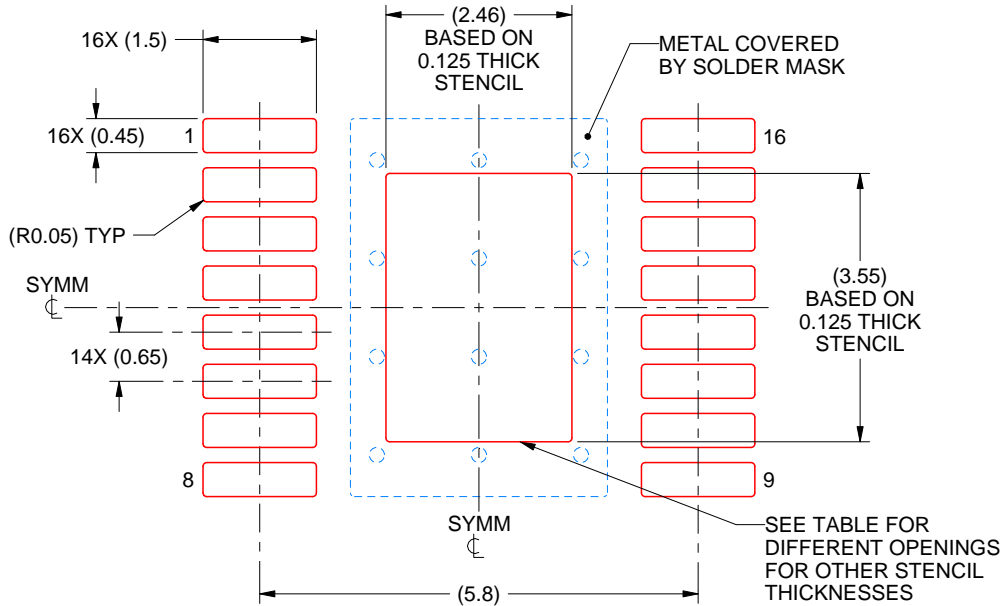
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
8. Size of metal pad may vary due to creepage requirement.
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

PWP0016J

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL
 SCALE: 10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.75 X 3.97
0.125	2.46 X 3.55 (SHOWN)
0.15	2.25 X 3.24
0.175	2.08 X 3.00

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NOTES: (continued)

- 10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
- 11. Board assembly site may have different recommendations for stencil design.

重要声明和免责声明

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